Appendix A

Analysis of Switching Elements

A.1 Analysis of Input Rate and Output Rate of Switching Elements

This section precisely induces the output rate of each switching element in the original, the 2-dilated and the hybrid dilated banyan networks. Through this section, the input rate of each input port is described by a and b for any banyan switching elements, or a, b, c and d for any 2-dilated banyan switching elements. The output rate of all output ports is p. When a switching element has input and/or output bypass links, its input and/or output rate is q and/or r.

A.1.1 Input Rate and Output Rate of Banyan Switching Elements

In this subsection, the output rates of banyan switching elements are obtained. First, the banyan switching element Type 2 in Fig. A.1 is considered.

For the above model, the following two cases exist.

Case 1: No cell arrives at the input bypass link.

- When no cell arrives at any input port, the probability of this case is $(1-q)(1-a)(1-b)$. No cell is sent to the output ports and the output bypass link. Then, the output rates of this case are:

  output port:

$$(1-q)(1-a)(1-b) \times 0 = 0,$$

  output bypass link:

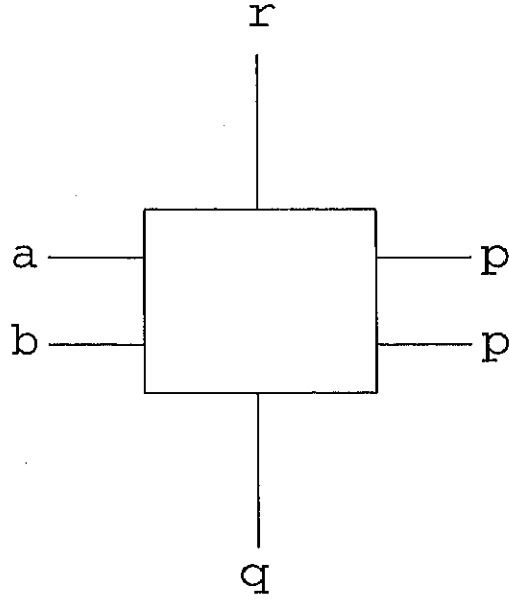$$(1-q)(1-a)(1-b) \times 0 = 0.$$

Figure A.1: Banyan switching element Type 2.

- When there is an arriving cell at one of the two input ports, the probability of this case is $(1 - q)(a(1 - b) + b(1 - a))$. No cell is blocked and the output probability of each output port is $\frac{1}{2}$. Then, the output rates of this case are:

output port:

$$(1 - q)(a(1 - b) + b(1 - a)) \times \frac{1}{2},$$

output bypass link:

$$(1 - q)(a(1 - b) + b(1 - a)) \times 0 = 0.$$

- When there are arriving cells at both of the input ports, the probability of this case is $(1 - q) \times a \times b$. The probability of cell blocking is $\frac{1}{2}$ and the output probability of each output port is $\frac{3}{4}$. Then, the output rates of this case are:

output port:

$$(1 - q) \times a \times b \times \frac{3}{4},$$

output bypass link:

$$(1 - q) \times a \times b \times \frac{1}{2}.$$

Case 2: A cell arrives at the input bypass link.

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- When no cell arrives at both of input ports, the probability of this case is $q \times (1-a)(1-b)$. No cell are blocked and the probability of each output port is $\frac{1}{2}$. Then, the output rates of this case are:

output port:

$$q \times (1-a)(1-b) \times \frac{1}{2},$$

output bypass link:

$$q \times (1-a)(1-b) \times 0 = 0.$$

- When there is an arriving cell at one of the input ports, the probability of this case is $q(a(1-b)+b(1-a))$. The probability of cell blocking is $\frac{1}{2}$ and the output probability of each output port is $\frac{3}{4}$. Then, the output rates of this case are:

output port:

$$q(a(1-b)+b(1-a)) \times \frac{3}{4},$$

output bypass link:

$$q(a(1-b)+b(1-a)) \times \frac{1}{2}.$$

- When there are arriving cells at both of the input ports, the probability of this case is $q \times a \times b$. More than one cell must be blocked and the output probability of each output port is $\frac{7}{8}$. Then, the output rates of this case are:

output port:

$$q \times a \times b \times \frac{7}{8},$$

output bypass link:

$$q \times a \times b \times 1.$$

From the above results, the total output rate p of each output port is:

$$p = \frac{1}{2}a + \frac{1}{2}b - \frac{1}{4}ab + \frac{1}{2}q - \frac{1}{4}aq - \frac{1}{4}bq + \frac{1}{8}abq, \qquad (A.1)$$

and the total output rate r of the bypass link is:

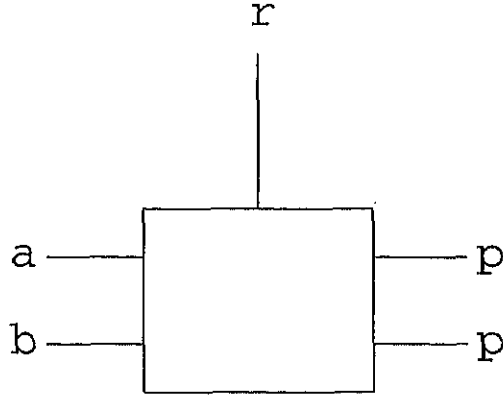$$r = \frac{1}{2}ab + \frac{1}{2}aq + \frac{1}{2}bq - \frac{1}{2}abq. \qquad (A.2)$$

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Figure A.2: Banyan switching element Type 1.

For the banyan switching element Type 1 is shown in Fig. A.2, there is no cell from the bypass input link. Thus, the output rates are inferred from (A.1) and (A.2) whose $q = 0$, as follows:

$$p = \frac{1}{2}a + \frac{1}{2}b - \frac{1}{4}ab, \qquad (A.3)$$
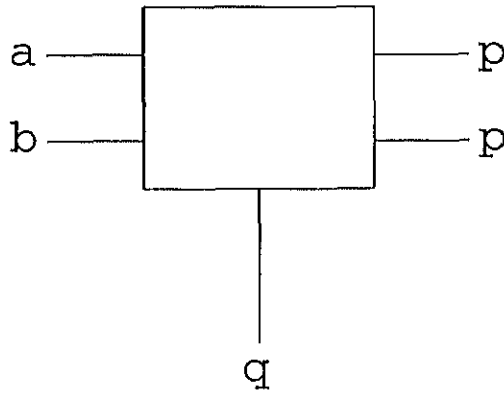
$$r = \frac{1}{2}ab. \qquad (A.4)$$

Figure A.3: Banyan switching element Type 3.

For the banyan switching element Type 3 is shown in Fig. A.3, p is same as (A.1), but there is no bypass output link. The output rate p is described in the following again.

$$p = \frac{1}{2}a + \frac{1}{2}b - \frac{1}{4}ab + \frac{1}{2}q - \frac{1}{4}aq - \frac{1}{4}bq + \frac{1}{8}abq. \qquad (A.5)$$
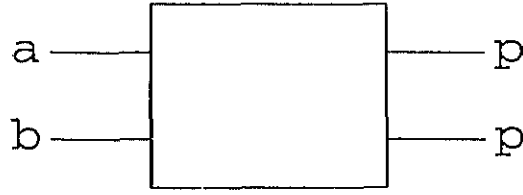
Figure A.4: Banyan switching element Type 4.

For the banyan switching element Type 4 is shown in Fig. A.4, p is equal to (A.3), but there is no bypass output link. The output rate p is described in the following again.

$$p = \frac{1}{2}a + \frac{1}{2}b - \frac{1}{4}ab. \tag{A.6}$$

For the original banyan network, all input rates of each input port is same, i.e., $a = b$. Then the output rate p[29] is:

$$p = 1 - (1 - \frac{a}{2})^2. \tag{A.7}$$

A.1.2 Input Rate and Output Rate of 2-Dilated Banyan Switching Elements

This subsection infers the output rates of 2-dilated banyan switching elements. As in the previous subsection, the 2-dilated banyan switching element Type 2 in Fig. A.5 is considered.
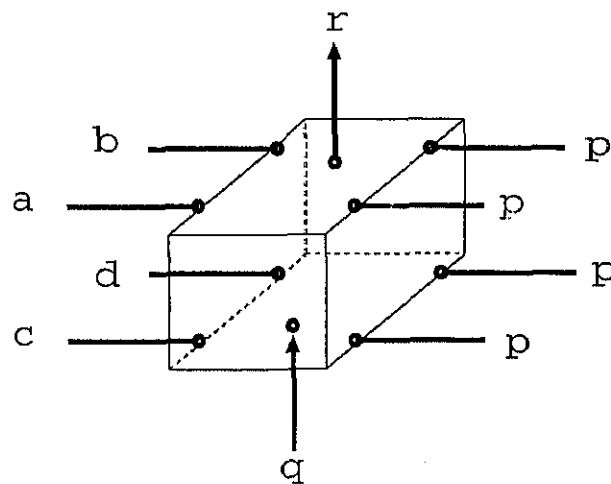

Figure A.5: 2-dilated banyan switching element Type 2.

For the above model, the following cases exist.

Case 1: No cell arrives at the input bypass link.

- When no cell arrive at any input ports, the probability of this case is $(1-a)(1-b)(1-c)(1-d)(1-q)$. No cell is sent to the output ports and the output bypass link. Then, the output rates of this case are:

output port:

$$(1-a)(1-b)(1-c)(1-d)(1-q) \times 0 = 0,$$

output bypass link:

$$(1-a)(1-b)(1-c)(1-d)(1-q) \times 0 = 0.$$

- When there is an arriving cell at one of four input ports, the probability of this case is $[a(1-b)(1-c)(1-d) \times (1-q)] + [b(1-a)(1-c)(1-d) \times (1-q)] + [c(1-a)(1-b)(1-d) \times (1-q)] + [d(1-a)(1-b)(1-c) \times (1-q)]$. No cell is blocked and the output probability of each output port is $\frac{1}{4}$. Then, the output rates of this case are:

output port:

$$a(1-b)(1-c)(1-d) \times (1-q) \times \frac{1}{4} + b(1-a)(1-c)(1-d) \times (1-q) \times \frac{1}{4}$$
$$+c(1-a)(1-b)(1-d) \times (1-q) \times \frac{1}{4} + d(1-a)(1-b)(1-c) \times (1-q) \times \frac{1}{4},$$

output bypass link:

$$[a(1-b)(1-c)(1-d) \times (1-q)] \times 0 + [b(1-a)(1-c)(1-d) \times (1-q)] \times 0$$
$$+[c(1-a)(1-b)(1-d) \times (1-q)] \times 0 + [d(1-a)(1-b)(1-c) \times (1-q)] \times 0 = 0.$$

- When there are arriving cells at two of the four input ports, the probability of this case is $[ab(1-c)(1-d) \times (1-q)] + [ac(1-b)(1-d) \times (1-q)] + [ad(1-b)(1-c) \times (1-q)] + [bc(1-a)(1-d) \times (1-q)] + [bd(1-a)(1-c) \times (1-q)] + [cd(1-b)(1-a) \times (1-q)]$. No cell is blocked and the output probability of each output port is $\frac{1}{2}$. Then, the output rates of this case are:

output port:

$$ab(1-c)(1-d) \times (1-q) \times \frac{1}{2} + ac(1-b)(1-d) \times (1-q) \times \frac{1}{2}$$
$$+ad(1-b)(1-c) \times (1-q) \times \frac{1}{2} + bc(1-a)(1-d) \times (1-q) \times \frac{1}{2}$$
$$+bd(1-a)(1-c) \times (1-q) \times \frac{1}{2} + cd(1-b)(1-a) \times (1-q) \times \frac{1}{2},$$

output bypass link:

$$ab(1-c)(1-d) \times (1-q) \times 0 + ac(1-b)(1-d) \times (1-q) \times 0$$

$$+ad(1-b)(1-c) \times (1-q) \times 0 + bc(1-a)(1-d) \times (1-q) \times 0$$

$$+bd(1-a)(1-c) \times (1-q) \times 0 + cd(1-b)(1-a) \times (1-q) \times 0 = 0.$$

- When there are arriving cells at three of the four input ports, the probability of this case is $[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times (1-q)$. The probability of cell blocking is $\frac{1}{4}$ and the output probability of each output port is $\frac{44}{64}$. Then, the output rates of this case are:

output port:

$$[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times (1-q) \times \frac{44}{64},$$

output bypass link:

$$[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times (1-q) \times \frac{1}{4}.$$

- When there are arriving cells at all of the four input ports, the probability of this case is $abcd \times (1-q)$. The probability of cell blocking is $\frac{10}{16}$ and the output probability of each output port is $\frac{208}{256}$. Then, the output rates of this case are:

output port:

$$abcd \times (1-q) \times \frac{208}{256},$$

output bypass link:

$$abcd \times (1-q) \times \frac{10}{16}.$$

Case 2: A cell arrives at the input bypass link.

- When no cell arrives at any input ports, the probability of this case is $(1-a)(1-b)(1-c)(1-d) \times q$. No cell is blocked and the output probability of each output port is $\frac{1}{4}$. Then, the output rates of this case are:

output port:

$$(1-a)(1-b)(1-c)(1-d) \times q \times \frac{1}{4},$$

output bypass link:

$$(1-a)(1-b)(1-c)(1-d) \times q \times 0 = 0.$$

- When there is an arriving cell at one of four input ports, the probability of this case is $[a(1-b)(1-c)(1-d) \times q] + [b(1-a)(1-c)(1-d) \times q] + [c(1-a)(1-b)(1-d) \times q] + [d(1-a)(1-b)(1-c) \times q]$. No cell is blocked and the output probability of each output port is $\frac{1}{2}$. Then, the output rates of this case are:

output port:

$$[a(1-b)(1-c)(1-d) \times q] \times \frac{1}{2} + [b(1-a)(1-c)(1-d) \times q] \times \frac{1}{2}$$
$$+[c(1-a)(1-b)(1-d) \times q] \times \frac{1}{2} + [d(1-a)(1-b)(1-c) \times q] \times \frac{1}{2},$$

output bypass link:

$$[a(1-b)(1-c)(1-d) \times q] \times 0 + [b(1-a)(1-c)(1-d) \times q] \times 0$$
$$+[c(1-a)(1-b)(1-d) \times q] \times 0 + [d(1-a)(1-b)(1-c) \times q] \times 0 = 0.$$

- When there are arriving cells at two of the four input ports, the probability of this case is $[ab(1-c)(1-d) \times q] + [ac(1-b)(1-d) \times q] + [ad(1-b)(1-c) \times q] + [bc(1-a)(1-d) \times q] + [bd(1-a)(1-c) \times q] + [cd(1-b)(1-a) \times q]$. The probability of cell blocking is $\frac{1}{4}$ and the output probability of each output port is $\frac{44}{64}$. Then, the output rates of this case are:

output port:

$$ab(1-c)(1-d) \times q \times \frac{44}{64} + ac(1-b)(1-d) \times q \times \frac{44}{64} + ad(1-b)(1-c) \times q \times \frac{44}{64}$$
$$+bc(1-a)(1-d) \times q \times \frac{44}{64} + bd(1-a)(1-c) \times q \times \frac{44}{64} + cd(1-b)(1-a) \times q \times \frac{44}{64},$$

output bypass link:

$$ab(1-c)(1-d) \times q \times \frac{1}{4} + ac(1-b)(1-d) \times q \times \frac{1}{4} + ad(1-b)(1-c) \times q \times \frac{1}{4}$$
$$+bc(1-a)(1-d) \times q \times \frac{1}{4} + bd(1-a)(1-c) \times q \times \frac{1}{4} + cd(1-b)(1-a) \times q \times \frac{1}{4}.$$

- When there are arriving cells at three of the four input ports, the probability of this case is $[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times q$. The probability of cell blocking is $\frac{10}{16}$ and the output probability of each output port is $\frac{208}{256}$. Then, the output rates of this case are:

output port:

$$[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times q \times \frac{208}{256},$$

output bypass link:

$$[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times q \times \frac{10}{16}.$$

- When there are arriving cells at all of the four input ports, the probability of this case is $abcd \times q$. More than one cell must be blocked and the output probability of each output port is $\frac{912}{1024}$. Then, the output rates of this case are:

output port:

$$abcd \times q \times \frac{912}{1024},$$

output bypass link:

$$abcd \times q \times 1.$$

From the above results, the total output rate p of each output port is:

$$
\begin{aligned}
p = \ & \frac{1}{4}a + \frac{1}{4}b + \frac{1}{4}c + \frac{1}{4}d - \frac{1}{16}abc - \frac{1}{16}abd - \frac{1}{16}acd \\
& - \frac{1}{16}bcd + \frac{1}{16}abcd + \frac{1}{4}q - \frac{1}{16}abq - \frac{1}{16}acq \\
& - \frac{1}{16}adq - \frac{1}{16}bcq - \frac{1}{16}cdq - \frac{1}{16}bdq + \frac{1}{16}abdq \\
& + \frac{1}{16}acdq + \frac{1}{16}bcdq + \frac{1}{16}abcq - \frac{3}{64}abcdq,
\end{aligned}
\tag{A.8}
$$

and the total output rate r of the bypass link is:

$$
\begin{aligned}
r = \ & \frac{1}{4}abc + \frac{1}{4}acd + \frac{1}{4}abd + \frac{1}{4}bcd - \frac{3}{8}abcd - \frac{3}{8}abcq \\
& - \frac{3}{8}acdq - \frac{3}{8}abdq - \frac{3}{8}bcdq + \frac{3}{8}abcdq + \frac{1}{4}abq \\
& + \frac{1}{4}acq + \frac{1}{4}adq + \frac{1}{4}bcq + \frac{1}{4}bdq + \frac{1}{4}cdq.
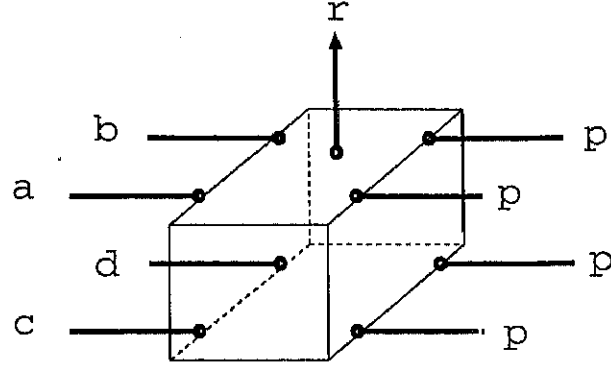\end{aligned}
\tag{A.9}
$$

Figure A.6: 2-dilated banyan switching element Type 1.

For the 2-dilated banyan switching element Type 1 is shown in Fig. A.6, there is no cell from the bypass input link. Thus, the output rates are inferred from (A.8) and (A.9) whose $q = 0$, as follows:

$$p = \frac{1}{4}a + \frac{1}{4}b + \frac{1}{4}c + \frac{1}{4}d - \frac{1}{16}abc - \frac{1}{16}abd - \frac{1}{16}acd - \frac{1}{16}bcd + \frac{1}{16}abcd, \qquad (A.10)$$

$$r = \frac{1}{4}abc + \frac{1}{4}acd + \frac{1}{4}abd + \frac{1}{4}bcd - \frac{3}{8}abcd. \qquad (A.11)$$
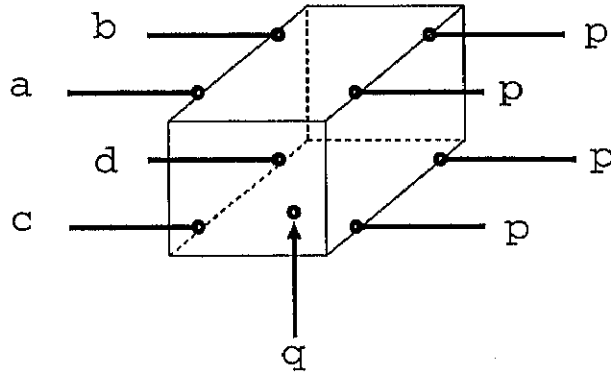

Figure A.7: 2-dilated banyan switching element Type 3.

For the 2-dilated banyan switching element Type 3 is shown in Fig. A.7, p is same as (A.7), but there is no bypass output link. The output rate p is described in the following.

$$p = \frac{1}{4}a + \frac{1}{4}b + \frac{1}{4}c + \frac{1}{4}d - \frac{1}{16}abc - \frac{1}{16}abd - \frac{1}{16}acd$$

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$$-\frac{1}{16}bcd + \frac{1}{16}abcd + \frac{1}{4}q - \frac{1}{16}abq - \frac{1}{16}acq$$

$$-\frac{1}{16}adq - \frac{1}{16}bcq - \frac{1}{16}cdq - \frac{1}{16}bdq + \frac{1}{16}abdq$$

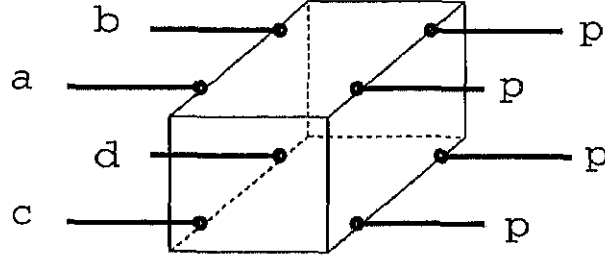$$+\frac{1}{16}acdq + \frac{1}{16}bcdq + \frac{1}{16}abcq - \frac{3}{64}abcdq. \qquad (A.12)$$

Figure A.8: 2-dilated banyan switching element Type 4.

For the 2-dilated banyan switching element Type 4 is shown in Fig. A.8, p is equal to (A.9), but there is no bypass output link. The output rate p is described in the following again.

$$p = \frac{1}{4}a + \frac{1}{4}b + \frac{1}{4}c + \frac{1}{4}d - \frac{1}{16}abc - \frac{1}{16}abd - \frac{1}{16}acd - \frac{1}{16}bcd + \frac{1}{16}abcd. \qquad (A.13)$$

For the original 2-dilated banyan network, all input rates of each input port is same, i.e., $a = b = c = d$. Then, the output rate p is:

$$p = a - \frac{1}{4}a^3 + \frac{1}{16}a^4. \qquad (A.14)$$

A.1.3 Input Rate and Output Rate of 4×2 Re-Arrangeable Output Switching Elements

This subsection infers the output rates of 4×2 re-arrangeable output switching elements. As in the previous subsection, the 4×2 re-arrangeable output switching element Type 2 in Fig. A.9 is considered.

For the above model, the following cases exist.

Case 1: No cell arrives at the input bypass link.

- When no cell arrives at any input ports, the probability of this case is $(1 - a)(1 - b)(1 - c)(1 - d)(1 - q)$. No cell is sent to the output ports and the output bypass link. Then, the output rates of this case are:
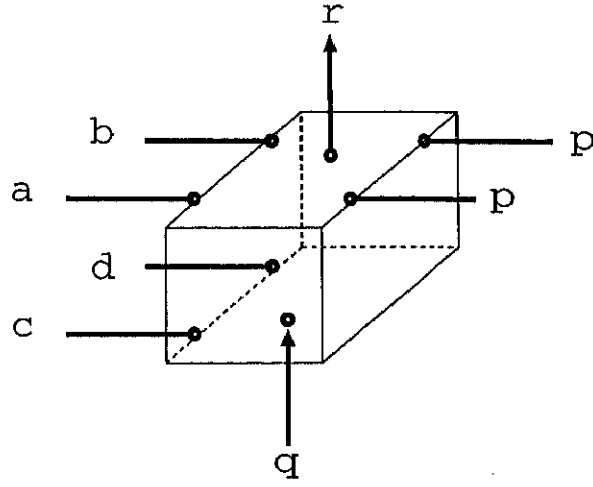
r

b ⟶ p

a ⟶

d ⟶ p

c ⟶

q

Figure A.9: 4 × 2 re-arrangeable output switching elements Type 2.

output port:

$$(1-a)(1-b)(1-c)(1-d)(1-q) \times 0 = 0,$$

output bypass link:

$$(1-a)(1-b)(1-c)(1-d)(1-q) \times 0 = 0.$$

- When there is an arriving cell at one of four input ports, the probability of this case is $[a(1-b)(1-c)(1-d) \times (1-q)] + [b(1-a)(1-c)(1-d) \times (1-q)] + [c(1-a)(1-b)(1-d) \times (1-q)] + [d(1-a)(1-b)(1-c) \times (1-q)]$. No cell is blocked and the output probability of each output port is $\frac{1}{2}$. Then, the output rates of this case are:

output port:

$$[a(1-b)(1-c)(1-d) \times (1-q)] \times \frac{1}{2} + [b(1-a)(1-c)(1-d) \times (1-q)] \times \frac{1}{2}$$
$$+[c(1-a)(1-b)(1-d) \times (1-q)] \times \frac{1}{2} + [d(1-a)(1-b)(1-c) \times (1-q)] \times \frac{1}{2},$$

output bypass link:

$$[a(1-b)(1-c)(1-d) \times (1-q)] \times 0 + [b(1-a)(1-c)(1-d) \times (1-q)] \times 0$$
$$+[c(1-a)(1-b)(1-d) \times (1-q)] \times 0 + [d(1-a)(1-b)(1-c) \times (1-q)] \times 0 = 0.$$

- When there are arriving cells at two of the four input ports, the probability of this case is $[ab(1-c)(1-d) \times (1-q)] + [ac(1-b)(1-d) \times (1-q)] + [ad(1-b)(1-c) \times (1-q)] +$

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$$[bc(1-a)(1-d) \times (1-q)] + [bd(1-a)(1-c) \times (1-q)] + [cd(1-b)(1-a) \times (1-q)].$$

The probability of cell blocking is $\frac{1}{2}$ and the output probability of each output port is $\frac{3}{4}$. Then, the output rates of this case are:

output port:

$$ab(1-c)(1-d) \times (1-q) \times \frac{3}{4} + ac(1-b)(1-d) \times (1-q) \times \frac{3}{4}$$
$$+ad(1-b)(1-c) \times (1-q) \times \frac{3}{4} + bc(1-a)(1-d) \times (1-q) \times \frac{3}{4}$$
$$+bd(1-a)(1-c) \times (1-q) \times \frac{3}{4} + cd(1-b)(1-a) \times (1-q) \times \frac{3}{4},$$

output bypass link:

$$ab(1-c)(1-d) \times (1-q) \times \frac{1}{2} + ac(1-b)(1-d) \times (1-q) \times \frac{1}{2}$$
$$+ad(1-b)(1-c) \times (1-q) \times \frac{1}{2} + bc(1-a)(1-d) \times (1-q) \times \frac{1}{2}$$
$$+bd(1-a)(1-c) \times (1-q) \times \frac{1}{2} + cd(1-b)(1-a) \times (1-q) \times \frac{1}{2}.$$

- When there are arriving cells at three of the four input ports, the probability of this case is $[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times (1-q)$. The probability of cell blocking is 1 and the output probability of each output port is $\frac{7}{8}$. Then, the output rates of this case are:

output port:

$$[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times (1-q) \times \frac{7}{8},$$

output bypass link:

$$[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times (1-q) \times 1.$$

- When there are arriving cells at all of the four input ports, the probability of this case is $abcd \times (1-q)$. The probability of cell blocking is 1 and the output probability of each output port is $\frac{15}{16}$. Then, the output rates of this case are:

output port:

$$abcd \times (1-q) \times \frac{15}{16},$$

output bypass link:

$$abcd \times (1-q) \times 1.$$

Case 2: A cell arrives at the input bypass link.

- When no cell arrives at any input ports, the probability of this case is $(1-a)(1-b)(1-c)(1-d) \times q$. No cell is blocked and the output probability of each output port is $\frac{1}{2}$. Then, the output rates of this case are:

output port:

$$(1-a)(1-b)(1-c)(1-d) \times q \times \frac{1}{2},$$

output bypass link:

$$(1-a)(1-b)(1-c)(1-d) \times q \times 0 = 0.$$

- When there is an arriving cell at one of four input ports, the probability of this case is $[a(1-b)(1-c)(1-d) \times q] + [b(1-a)(1-c)(1-d) \times q] + [c(1-a)(1-b)(1-d) \times q] + [d(1-a)(1-b)(1-c) \times q]$. The probability of cell blocking is $\frac{1}{2}$ and the output probability of each output port is $\frac{3}{4}$. Then, the output rates of this case are:

output port:

$$a(1-b)(1-c)(1-d) \times q \times \frac{3}{4} + b(1-a)(1-c)(1-d) \times q \times \frac{3}{4}$$
$$+c(1-a)(1-b)(1-d) \times q \times \frac{3}{4} + d(1-a)(1-b)(1-c) \times q \times \frac{3}{4},$$

output bypass link:

$$[a(1-b)(1-c)(1-d) \times q] \times \frac{1}{2} + [b(1-a)(1-c)(1-d) \times q] \times \frac{1}{2}$$
$$+[c(1-a)(1-b)(1-d) \times q] \times \frac{1}{2} + [d(1-a)(1-b)(1-c) \times q] \times \frac{1}{2}.$$

- When there are arriving cells at two of the four input ports, the probability of this case is $[ab(1-c)(1-d) \times q] + [ac(1-b)(1-d) \times q] + [ad(1-b)(1-c) \times q] + [bc(1-a)(1-d) \times q] + [bd(1-a)(1-c) \times q] + [cd(1-b)(1-a) \times q]$. More than one cell must be blocked and the output probability of each output port is $\frac{7}{8}$. Then, the output rates of this case are:

output port:

$$ab(1-c)(1-d) \times q \times \frac{7}{8} + ac(1-b)(1-d) \times q \times \frac{7}{8} + ad(1-b)(1-c) \times q \times \frac{7}{8}$$
$$+bc(1-a)(1-d) \times q \times \frac{7}{8} + bd(1-a)(1-c) \times q \times \frac{7}{8} + cd(1-b)(1-a) \times q \times \frac{7}{8},$$

output bypass link:

$$ab(1-c)(1-d) \times q \times 1 + ac(1-b)(1-d) \times q \times 1 + ad(1-b)(1-c) \times q \times 1$$
$$+ bc(1-a)(1-d) \times q \times 1 + bd(1-a)(1-c) \times q \times 1 + cd(1-b)(1-a) \times q \times 1.$$

- When there are arriving cells at three of the four input ports, the probability of this case is $[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times q$. More than one cell must be blocked and the output probability of each output port is $\frac{15}{16}$. Then, the output rates of this case are:

output rate:

$$[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times q \times \frac{15}{16},$$

output bypass link:

$$[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times q \times 1.$$

- When there are arriving cells at all of the four input ports, the probability of this case is $abcd \times q$. More than one cell must be blocked and the output probability of each output port is $\frac{31}{32}$. Then, the output rates of this case are:

output rate:

$$abcd \times q \times \frac{31}{32},$$

output bypass link:

$$abcd \times q \times 1.$$

From the above results, the total output rate p of each output port is:

$$
\begin{aligned}
p = \; & \frac{1}{2}a + \frac{1}{2}b + \frac{1}{2}c + \frac{1}{2}d - \frac{1}{4}ab - \frac{1}{4}ac - \frac{1}{4}bd \\
& - \frac{1}{4}ad - \frac{1}{4}bc - \frac{1}{4}cd + \frac{1}{8}abc + \frac{1}{8}abd \\
& + \frac{1}{8}acd + \frac{1}{8}bcd - \frac{1}{16}abcd \\
& + \frac{1}{2}q - \frac{1}{4}aq - \frac{1}{4}bq - \frac{1}{4}cq - \frac{1}{4}dq \\
& + \frac{1}{8}abq + \frac{1}{8}acq + \frac{1}{8}adq + \frac{1}{8}bcq + \frac{1}{8}bdq + \frac{1}{8}cdq \\
& - \frac{1}{16}abdq - \frac{1}{16}acdq - \frac{1}{16}bcdq - \frac{1}{16}abcq + \frac{1}{32}abcdq,
\end{aligned}
\tag{A.15}
$$

and the total output rate r of the bypass link is:

$$
\begin{aligned}
r &= \frac{1}{2}ab + \frac{1}{2}ac + \frac{1}{2}ad + \frac{1}{2}bc + \frac{1}{2}bd + \frac{1}{2}cd \\
&\quad -\frac{1}{2}abc - \frac{1}{2}abd - \frac{1}{2}acd - \frac{1}{2}bcd \\
&\quad +\frac{1}{2}aq + \frac{1}{2}bq + \frac{1}{2}cq + \frac{1}{2}dq - \frac{1}{2}abq \\
&\quad -\frac{1}{2}acq - \frac{1}{2}adq - \frac{1}{2}bcq - \frac{1}{2}bdq - \frac{1}{2}cdq + abcdq.
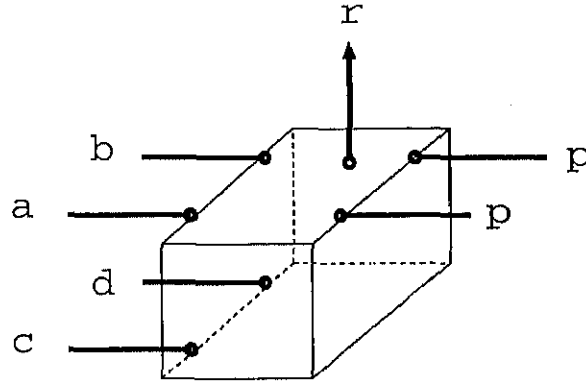\end{aligned}
\tag{A.16}
$$

Figure A.10: 4×2 re-arrangeable output switching element Type 1.

For the 4×2 re-arrangeable output switching element Type 1 is shown in Fig. A.10, there is no cell from the bypass link. Thus, the output rates are inferred from (A.15) and (A.16) whose $q = 0$, as follows:

$$
\begin{aligned}
p &= \frac{1}{2}a + \frac{1}{2}b + \frac{1}{2}c + \frac{1}{2}d - \frac{1}{4}ab - \frac{1}{4}ac - \frac{1}{4}bd \\
&\quad -\frac{1}{4}ad - \frac{1}{4}bc - \frac{1}{4}cd + \frac{1}{8}abc + \frac{1}{8}abd \\
&\quad +\frac{1}{8}acd + \frac{1}{8}bcd - \frac{1}{16}abcd,
\end{aligned}
\tag{A.17}
$$

$$
\begin{aligned}
r &= \frac{1}{2}ab + \frac{1}{2}ac + \frac{1}{2}ad + \frac{1}{2}bc + \frac{1}{2}bd + \frac{1}{2}cd \\
&\quad -\frac{1}{2}abc - \frac{1}{2}abd - \frac{1}{2}acd - \frac{1}{2}bcd.
\end{aligned}
\tag{A.18}
$$

For the 4×2 re-arrangeable output switching element Type 3 is shown in Fig. A.11, p is same as (A.15), but there is no bypass output link. The output rate p is described in the following.
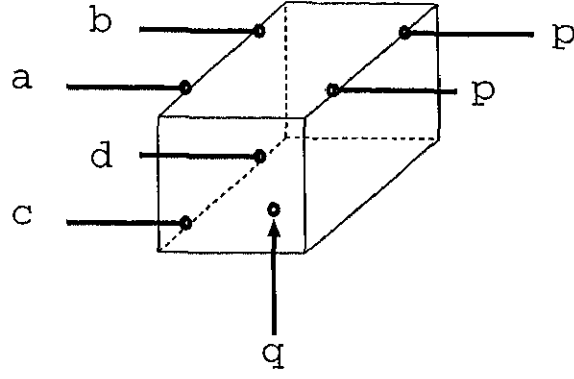
Figure A.11: 4 × 2 re-arrangeable output switching element Type 3.

$$p = \frac{1}{2}a + \frac{1}{2}b + \frac{1}{2}c + \frac{1}{2}d - \frac{1}{4}ab - \frac{1}{4}ac - \frac{1}{4}bd$$
$$-\frac{1}{4}ad - \frac{1}{4}bc - \frac{1}{4}cd + \frac{1}{8}abc + \frac{1}{8}abd$$
$$+\frac{1}{8}acd + \frac{1}{8}bcd - \frac{1}{16}abcd$$
$$+\frac{1}{2}q - \frac{1}{4}aq - \frac{1}{4}bq - \frac{1}{4}cq - \frac{1}{4}dq$$
$$+\frac{1}{8}abq + \frac{1}{8}acq + \frac{1}{8}adq + \frac{1}{8}bcq + \frac{1}{8}bdq + \frac{1}{8}cdq$$
$$-\frac{1}{16}abdq - \frac{1}{16}acdq - \frac{1}{16}bcdq - \frac{1}{16}abcq + \frac{1}{32}abcdq. \tag{A.19}$$

For the original 2-dilated banyan network, every input rate of each input port is the same, i.e., $a = b = c = d$. Then the output rate p is:

$$p = 2a - \frac{3}{2}a^2 + \frac{1}{2}a^3 - \frac{1}{16}a^4. \tag{A.20}$$

In section 4.1, the restricted Type 1 and Type 3 switching elements, called by the lower and upper switching elements, are discussed. Since all of their input rates are the same, their output rates are inferred from (A.17) to (A.19). For the lower switching element, the output rate p and the output rate r of the bypass link are:

$$p = 2a - \frac{3}{2}a^2 + \frac{1}{2}a^3 - \frac{1}{16}a^4 + \frac{1}{2}a - aq + \frac{3}{4}a^2q - \frac{1}{4}a^3q + \frac{1}{32}a^4q, \tag{A.21}$$

$$r = 3a^2 - 2a^3. \tag{A.22}$$

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For the upper switching element, the output rate p is:

$$p = 2a - \frac{7}{2}a^3 + \frac{67}{16}a^4 - \frac{9}{4}a^5 + \frac{19}{32}a^6 - \frac{1}{16}a^7. \qquad \text{(A.23)}$$

A.1.4 Input Rate and Output Rate of 4×2 Re-Arrangeable Output Switching Elements with Two Bypasses

In section 4.1, the 4×2 re-arrangeable output switching element with two input or output bypass links, called the lower or upper switching element respectively, is introduced. All of the input rates of each switching element are restricted to the same probability (a in below), and both input and output bypass links are not inserted. This subsection infers the output rates of the lower and upper switching elements.

For the lower switching element in Fig. A.12, the output rate p equals to (A.20), since there is no bypass input link. In the followings, the output rate r of each output bypass link is calculated.
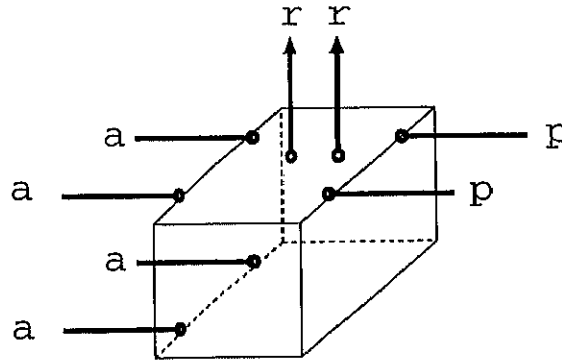

Figure A.12: The lower switching element.

- When no cell arrives at any input ports, the probability of this case is $(1 - a)^4$, but no cell is blocked. Then, the output rate of each bypass link is:

$$0 \times (1 - a)^4 \times 0 = 0.$$

- When there is an arriving cell at one of the four input ports, the probability of this case is $4a \times (1 - a)^3$, but no cell is blocked. Then, the output rate of each bypass link is:

$$0 \times 4a \times (1 - a)^3 \times 0 = 0.$$

- When there are arriving cells at two of the four input ports, the probability of this case is $6a^2(1-a)^2$ and the one of the cell blocking is $\frac{1}{2}$. But the blocked cell is only one and forwarded to the one of the two bypass links. The probability that the blocked cell is forwarded to each bypass link is $\frac{1}{4}$. Then, the output rate of each bypass link is:

$$6a^2(1-a)^2 \times \frac{1}{4} = \frac{3}{2}a^2(1-a)^2.$$

- When there are arriving cells at three of the four input ports, the probability of this case is $4a^3(1-a)$ and more than one cell must be blocked. One cell is blocked for the probability of $\frac{6}{8}$, two cells are also done for the rest of the probability, i.e, $1-\frac{6}{8} = \frac{2}{8}$. The probability that the blocked cell is forwarded to each bypass is $\frac{6}{8} \times \frac{1}{2} + \frac{2}{8} = \frac{5}{8}$. Then, the output rate of each bypass link is:

$$4a^3(1-a) \times \frac{5}{8} = \frac{5}{2}a^3(1-a).$$

- When there are arriving cells at all of the four input ports, the probability of this case is a^4 and more than two cells must be blocked. The probability that the blocked cell is forwarded to each bypass is 1. Then, the output rate of each bypass link is:

$$a^4 \times 1 = a^4.$$

From the above results, the total output rate p is calculated as follows:

$$p = 2a - \frac{3}{2}a^2 + \frac{1}{2}a^3 - \frac{1}{16}a^4, \qquad (A.24)$$

and the total output rate of each bypass link is:

$$r = \frac{3}{2}a^2 - \frac{1}{2}a^3. \qquad (A.25)$$

For the upper switching element in Fig. A.13, there is no output bypass link. When 0 or 1 cell is forwarded from the input bypass link, the output rates are obtained as the case 1 or 2 in the previous subsection, though the probability of each case is different.
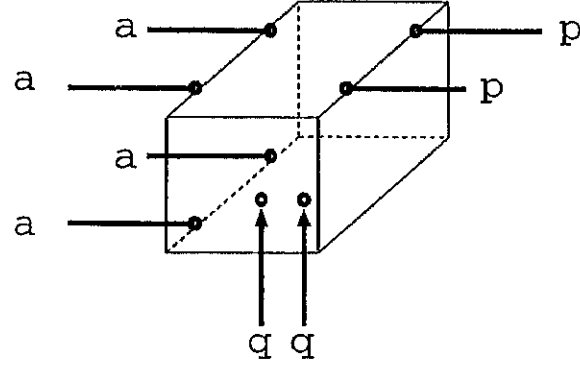
Figure A.13: The upper switching element.

Case 1: No cell arrives at the input bypass link. The probability of this case is $(1 - q)^2$. From case 1 in the previous section and $a = b = c = d$, the total output rate of this case is:

$$[0 + 2a(1 - a)^3 + \frac{9}{2}a^2(1 - a)^2 + \frac{7}{2}a^3(1 - a) + \frac{15}{16}a^4](1 - q)^2.$$

Case 2: A cell arrives at one of the two input bypass links. The probability of this case is $q(1 - q)$. From case 2 in the previous subsection and $a = b = c = d$, the total output rate of this case is:

$$[\frac{1}{2}(1 - a)^4 + 3a(1 - a)^3 + \frac{21}{2}a^2(1 - a)^2 + \frac{15}{4}a^3(1 - a) + \frac{31}{32}a^4]q(1 - q).$$

Case 3: Two cells arrive at both of two input bypass links.

- When no cell arrives at any input ports, the probability of this case is $(1 - a)^4 \times q^2$ and the output probability of each output port is $\frac{3}{4}$. Then, the output rate of this case is:

$$(1 - a)^4 \times q^2 \times \frac{3}{4} = \frac{3}{4}(1 - a)^4 q^2.$$

- When there is an arriving cell at one of the four input ports, the probability of this case is $4a(1 - a)^3 \times q^2$ and the output probability of each output port is $\frac{7}{8}$. Then, the output rate of this case is:

$$4a(1 - a)^3 \times q^2 \times \frac{7}{8} = \frac{7}{2}a(1 - a)^3 q^2.$$

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- When there are arriving cells at two of the four input ports, the probability of this case is $6a^2(1-a)^2 \times q^2$ and the output probability of each output port is $\frac{15}{16}$. Then, the output rate of this case is:

$$6a^2(1-a)^2 \times q^2 \times \frac{15}{16} = \frac{45}{8}a^2(1-a)^2q^2.$$

- When there are arriving cells at three of the four input ports, the probability of this case is $4a^3(1-a) \times q^2$ and the output probability of each output port is $\frac{31}{32}$. Then, the output rate of this case is:

$$4a^3(1-a) \times q^2 \times \frac{31}{32} = \frac{31}{8}a^3(1-a)q^2.$$

- When there are arriving cells at all of the four input ports, the probability of this case is $a^4 \times q^2$ and the output probability of each output port is $\frac{63}{64}$. Then, the output rate of this case is:

$$a^4 \times q^2 \times \frac{63}{64} = \frac{63}{64}a^4q^2.$$

From the above results, the total output rate p of each output port is:

$$
\begin{aligned}
p = \ & 2a - \frac{3}{2}a^2 + \frac{1}{2}a^3 - \frac{1}{16}a^4 + q - q^2 \\
& -2aq + \frac{3}{2}a^2q - \frac{1}{2}a^3q + \frac{1}{16}a^4q + \frac{3}{4}q^2 \\
& +\frac{1}{2}aq^2 - \frac{3}{8}a^2q^2 + \frac{1}{8}a^3q^2 - \frac{1}{64}a^4q^2.
\end{aligned}
\tag{A.26}
$$

From (A.25), the probability q of each input bypass link is $\frac{3}{2}a^2 - \frac{1}{2}a^3$. Therefore, the output rate of the upper switching element is generally presented as follows:

$$
\begin{aligned}
p = \ & 2a - 3a^3 + \frac{21}{8}a^4 - \frac{21}{16}a^6 \\
& +\frac{15}{16}a^7 - \frac{81}{256}a^8 + \frac{7}{128}a^9 - \frac{1}{256}a^{10}.
\end{aligned}
\tag{A.27}
$$

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A.1.5 Input Rate and Output Rate of 2×4 Re-Arrangeable Input Switching Element

In this section, the output rate of 2×4 re-arrangeable input switching element as shown is inferred as shown in Fig. A.14.
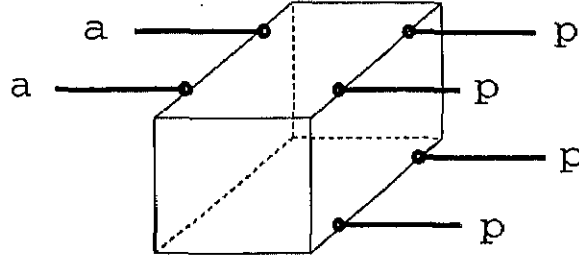

Figure A.14: 2×4 re-arrangeable input switching element.

Since the 2×4 re-arrangeable switching element blocks no cell, it is not needed to have bypass. Therefore it has only one type of switching elements, and all of their input rates are equal (i.e., $a = b$).

- When no cell arrives at any input ports, no cell is sent to the output ports. Then, the output rate of this case is:

$$(1 - a)^2 \times 0 = 0.$$

- When there is an arriving cell at one of the two input ports, the probability of this case is $2a(1 - a)$ and the output probability of each output port is $\frac{1}{4}$. Then, the output rate of this case is:

$$2a(1 - a) \times \frac{1}{4} = \frac{1}{2}a(1 - a).$$

- When there are arriving cells at both of the input ports, the probability of this case is a^2 and the output probability of each output port is $\frac{1}{2}$. Then, the output rate of this case is:

$$a^2 \times \frac{1}{2} = \frac{1}{2}a^2.$$

For the above results, the total output rate p of each output port is:

$$p = \frac{1}{2}a. \tag{A.28}$$

A.2 The Structures of Switching Elements and the Estimation of the Hardware Size and Delay

This section introduces the structures of all switching elements used in this thesis. From this results their hardware size and switching delay of all switching elements are estimated. Since the purpose of this section shows the example structures of switching elements, their hardware size and delay are estimated only the upper bounds, i.e., not optimum. Switching designers may construct more simpler, smaller and faster switching elements than the follows.

A.2.1 Banyan Network

The structure of the original banyan switching element is illustrated in Fig. A.15. It has two input and two output ports connected with two demultiplexers and two multiplexers. The demultiplexer examines the destination bit in a cell, selects a link to pass the cell based on the value of the bit. If the bit is 0, the upper output link is selected, and if the bit is 1, the lower output link is selected. The multiplexer can forward one cell to the output port. When two cells enter the same multiplexer, one of them is randomly chosen to be forwarded and the other is deleted.
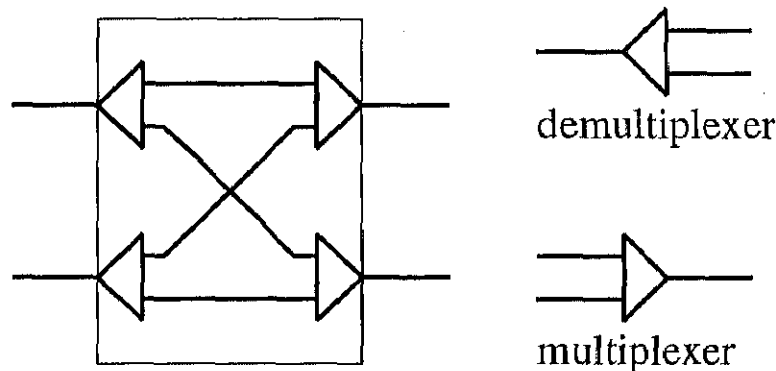

Figure A.15: Original banyan switching element.

Fig. A.16 shows the structure of banyan switching elements Type 1 to 3 with bypasses. In this figure, the demultiplexer is same as Fig. A.15. There are three kinds of switching elements shown as a box with an arrow. All of them work like the original banyan switching element. When one cell enters from one of input ports of a switching element, the cell is forwarded to the output port where the arrow is directed. When more than two cells arrive, the cells of the number of the output ports are randomly selected, and forwarded to the output ports, but the others are blocked. One of the blocked cells in Type 1 and 2 is forwarded through the

bypass link to the upper banyan switching element. The rest of blocked cells in this case and all blocked cells in Type 3 are eliminated. Note that only one cell is forwarded from the lower banyan switching element with bypasses at the same time, though two bypass links connects between banyan switching elements.
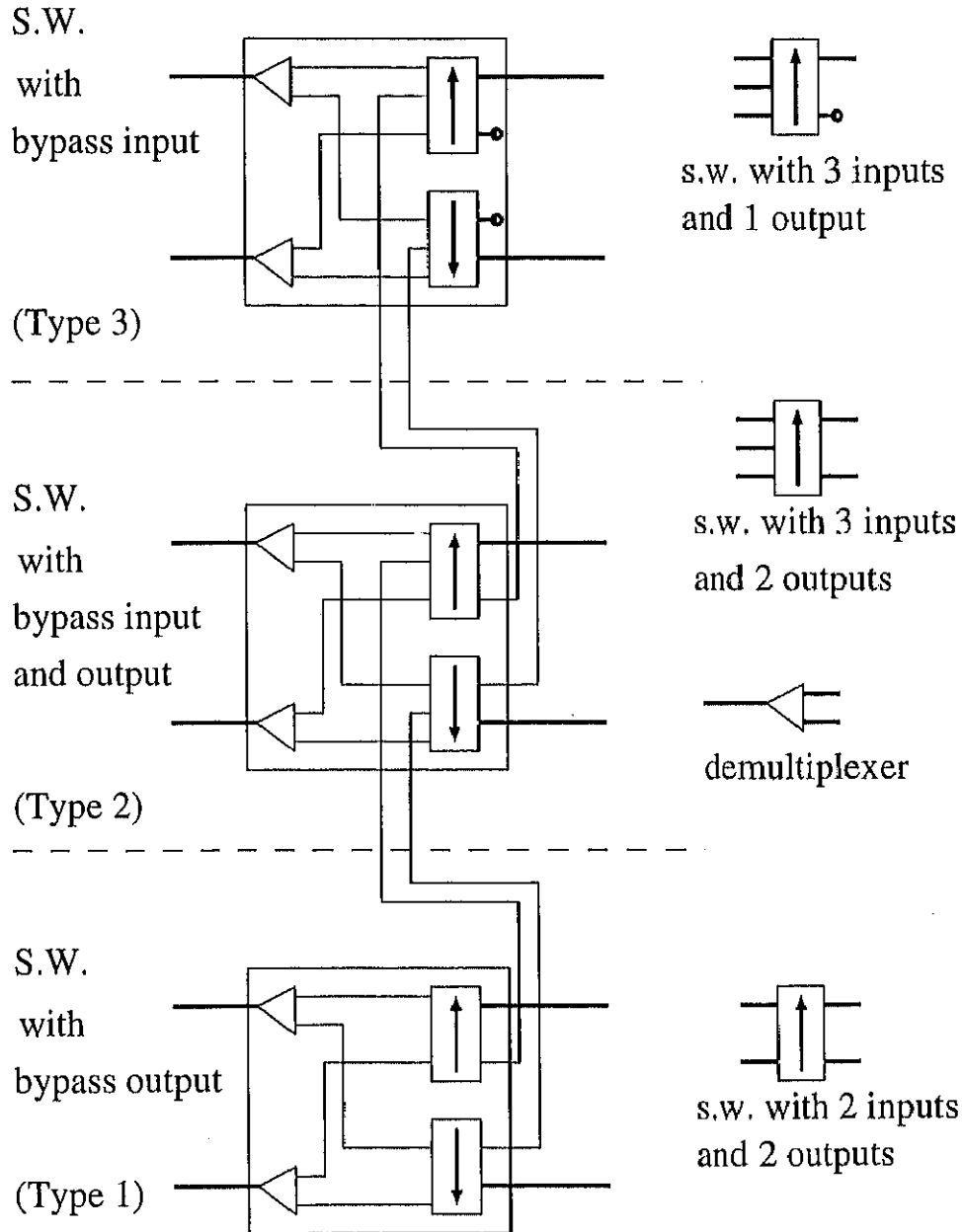

Figure A.16: Banyan switching element with bypasses.

Hardware Size

Let B be the hardware size of the original banyan switching element in Fig. A.15. A $2^n \times 2^n$ banyan network has n stages and $\frac{2^n}{2}$ banyan switching elements per each stage. Then, its

hardware size is estimated as follows:

$$n \times \frac{2^n}{2} \times B = (n \times 2^{n-1}) \times B. \tag{A.29}$$

For the banyan switching elements with bypasses in Fig. A.16, although each switching element in Type 1 to 3 properly includes the function of the original banyan switching element, its size roughly estimated to B in this thesis. Each banyan switching element with bypasses has two demultiplexers and two switching elements, and its size is $2.5B$. Since the final stage has no bypass, the hardware size of a $2^n \times 2^n$ banyan network with all-bypass-connection is:

$$\begin{aligned} & 2.5B \times \frac{2^n}{2} \times (n-1) + B \times \frac{2^n}{2} \times 1 \\ = \ & (2.5n - 1.5) \times 2^{n-1} \times B, \end{aligned} \tag{A.30}$$

and the hardware size of a $2^n \times 2^n$ banyan network with one-bypass-connection is the same result of (A.30).

Delay

From Fig. A.15, each cell in the original banyan switching element must be switched through a demulteplexer and a multiplexer. Then, the process time during the demulteplexer and the multiplexer is the delay in the original banyan switching element. All of the original banyan switching elements in each stage can process concurrently, and the delay of all stages is the same. Let D be the delay in each stage of the original banyan network. Then, the largest delay among all stages of a $2^n \times 2^n$ original banyan network is estimated to D.

For the banyan switching element with bypass in Fig. A.16, a cell must be forwarded through a demultiplexer and a switching element. Therefore, the delay in this case is approximated to $1.5D$. However, each banyan switching element with bypasses in each stage must be processed sequentially, since the switching element in the upper one cannot begin its process before the lower one ended. The process of the demultiplexer in the upper one can be overlapped to the one for the lower one. Thus, the delay of the upper one is estimate to D.

In the case of the banyan network with all-bypass-connection, the largest delay occurs in the first stage and is estimated as follows:

$$1.5D + (\frac{2^n}{2} - 1)D = (2^{n-1} + 0.5) \times D. \tag{A.31}$$

In the case of the banyan network with one-bypass-connection, the delay of all stage except the final one is the same, where cells are through Type 1, a bypass link and a switching element in Type 3. Thus, the the largest delay among all stages is estimated as follows:

$$1.5D + D = 2.5 \times D. \tag{A.32}$$

If all stages in the above networks synchronized to the stage with the largest delay, the total delay of the network is n times of the largest delay. Otherwise it may be shorten by the implementation of the network. Indeed, the delays of each stage in the banyan network with all-bypass-connection are quite differ each other. The minimum total delay of this network is twice of (A.31) in logical.
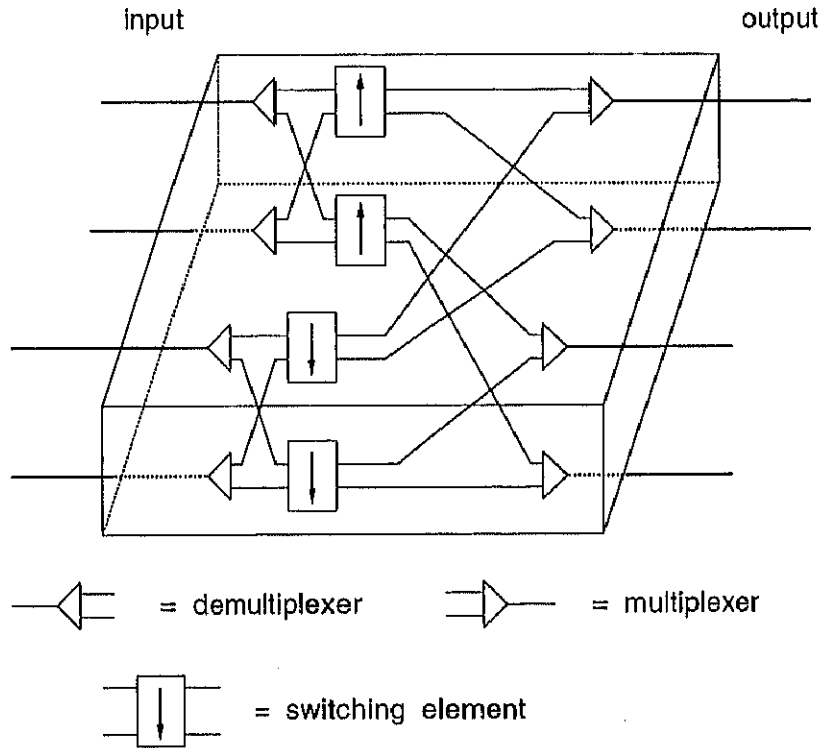
A.2.2   2-Dilated Banyan Network

Figure A.17: 2-dilated banyan switching element.

This subsection mentions the construction of a 2-dilated banyan switching element. Fig. A.17 shows the structure of the 2-dilated banyan switching element. It consists of four demultiplexers, four switching elements and four multiplexers. These contents are equal to the ones in Fig. A.15 and Fig. A.16, and are used in any switching elements in below.
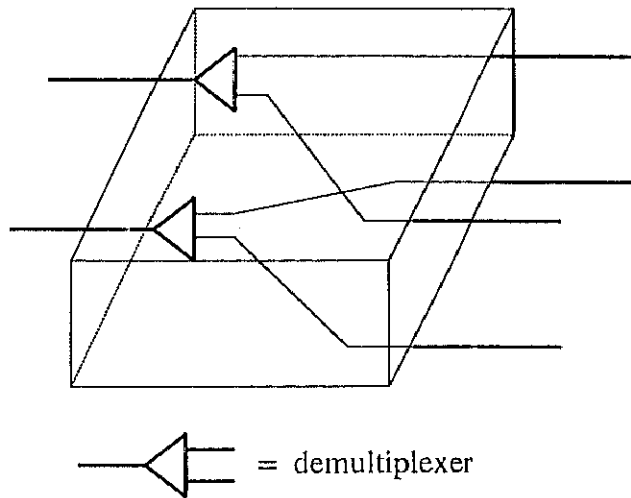
Figure A.18: 2 × 4 re-arrangeable input switching element.

The structures of the 2 × 4 re-arrangeable input switching element and the 4 × 2 re-arrangeable output switching element are shown in Fig. A.18 and Fig. A.19, respectively. The former consists of only two demultiplexers. The latter has two banyan switching elements and two multiplexers.
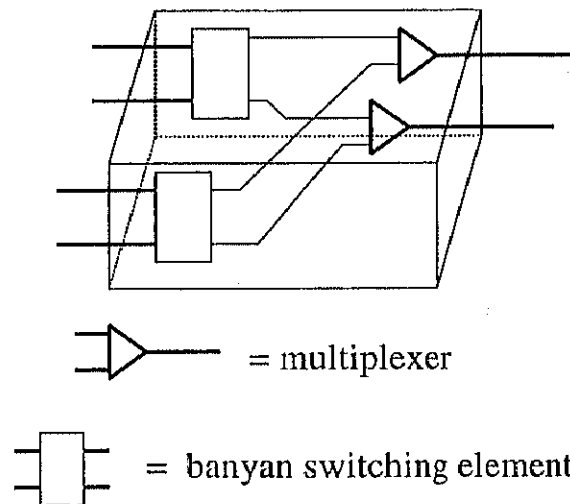

Figure A.19: 4 × 2 re-arrangeable output switching element.

The structure of the 2-dilated banyan switching elements with bypasses are illustrated in Fig. A.20. Each type consists of four demultiplexers and eight switching elements. In addition, Type 1 to 3 have a demultiplexer, a multiplexer and a demultiplexer, and a multiplexer, respectively, for bypass-connection to pass at most one cell to the upper switching elements.
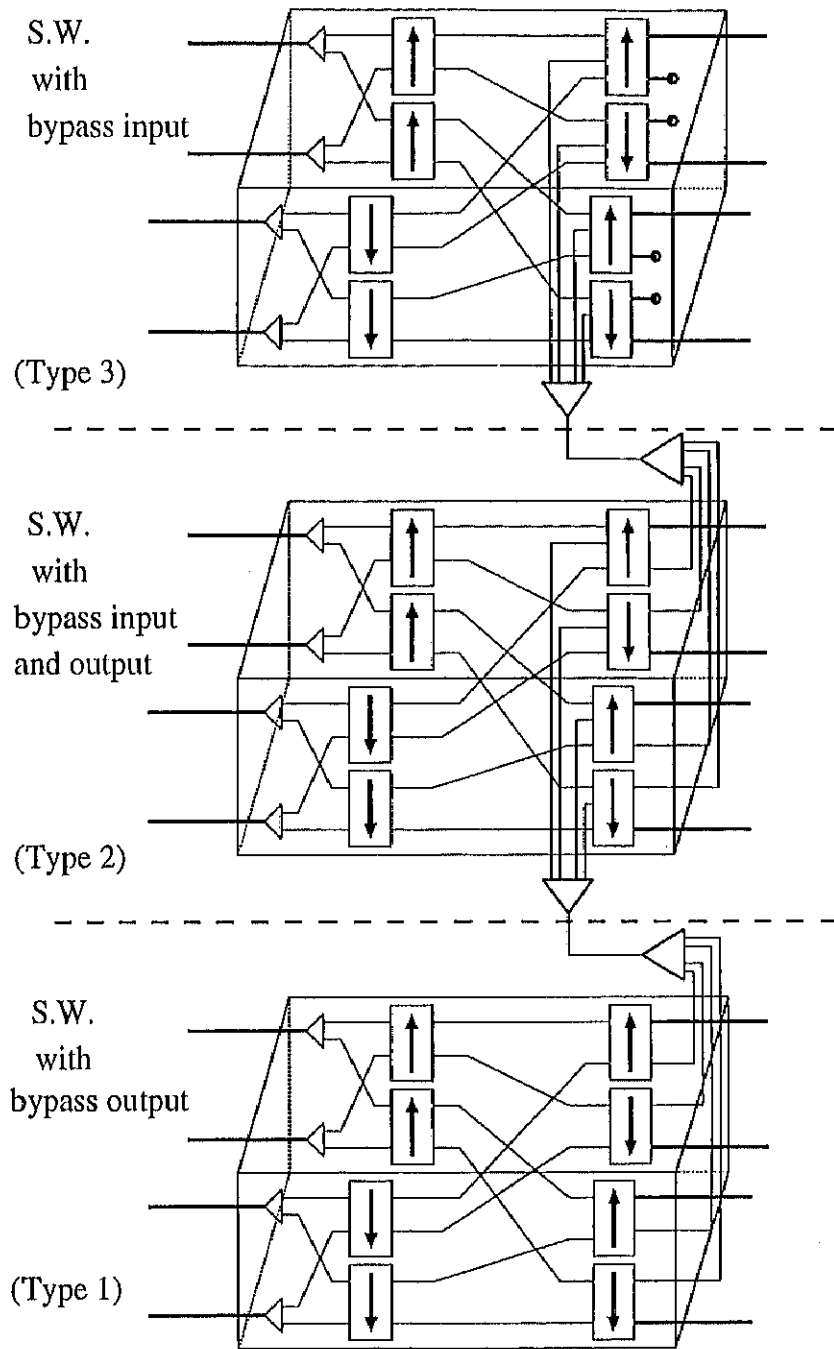
Figure A.20: 2-dilated switching element with bypasses.

Hardware Size

Since the banyan switching element has two demultiplexers and two multiplexers and its hardware size is defined by B, the hardware size of four demultiplexers and four multiplexers corresponds to $2B$. In addition, four switching elements are contained. For the 2-dilated banyan switching element in Fig. A.17, the hardware size of a 2-dilated banyan switching element is estimated as $6B$. The 2×4 re-arrangeable input switching element has only two demultiplexers and its hardware size roughly estimated to $0.5B$. For the 4×2 re-arrangeable

output switching element, the hardware size of two multiplexers is approximated to $0.5B$, and two banyan switching elements are contained. Then, the total hardware size is $2.5B$. A $2^n \times 2^n$ 2-dilated banyan network has the 2×4 re-arrangeable input switching elements at the first stage, $(n-2)$ stages of the 2-dilated banyan switching elements and the 4×2 re-arrangeable output switching elements at the final stages. From the above facts, the hardware size of a $2^n \times 2^n$ 2-dilated banyan network is estimated as follows:

$$[\frac{2^n}{2} \times 1 \times 0.5B] + [\frac{2^n}{2} \times (n-2) \times 6B] + [\frac{2^n}{2} \times 1 \times 2.5B]$$
$$= (6n - 9) \times 2^{n-1} \times B. \tag{A.33}$$

From the same discussion in the above, the hardware size of Type 1 to 3 of the 2-dilated banyan switching element with bypasses and a bypass link are $9.25B$, $9.5B$, $9.25B$ and $0.5B$, respectively. To estimate the hardware size of a $2^n \times 2^n$ 2-dilated banyan network with all-bypass-connection, it must be calculated from how many types of the 2-dilated banyan switching element at each stage are used. From section 4.2, the 2-dilated banyan switching elements from $((m-1)2^{n-d} + 1)$-th to $m2^{n-d}$-th column are sequentially connected by bypasses at the d-stage ($2 \le d \le n-1$, $m = 1, ..., 2^{d-1}$). Therefore, there are 2^{d-1} Type 1, $((2^{n-2} - 2) \times 2^{d-1})$ Type 2 and 2^{d-1} Type 3 of 2-dilated banyan switching elements at d-th stage. At the first stage, there are $\frac{2^n}{2}$ 2×4 re-arrangeable input switching elements. $\frac{2^n}{2}$ 4×2 re-arrangeable output switching elements also exist at the n-th stage. Then, the total hardware size of a $2^n \times 2^n$ 2-dilated banyan network with all-bypass-connection is estimated as follows:

$$\frac{2^n}{2} \times 0.5B + \sum_{d=2}^{n-1}(2^{d-1} \times 9.25B + (2^{n-1} - 2^d)9.5B + 2^{d-1} \times 9.25B) + \frac{2^n}{2} \times 2.5B$$
$$= [2^{n-1} \times 3B] + [(n-2)2^{n-1} \times 9.5B] - 0.25B\sum_{d=2}^{n-1}2^d$$
$$= [6 \times 2^{n-2}B] + [19(n-2)2^{n-2}B] - 0.25B(2^n - 4)$$
$$= [(19n - 33) \times 2^{n-2} + 1] \times B. \tag{A.34}$$

For a $2^n \times 2^n$ 2-dilated banyan network with one-bypass-connection, there are $\frac{1}{2} \times \frac{2^n}{2}$ pairs of Type 1 and Type 3 of 2-dilated banyan switching elements at all stages except the first and the final stage. Then, the hardware size of a $2^n \times 2^n$ 2-dilated banyan network with one-bypass-connection is estimated as follows:

$$[\frac{2^n}{2} \times 0.5B] + [(n-2) \times (\frac{1}{2} \times \frac{2^n}{2} \times (9.25B + 9.25B))] + [\frac{2^n}{2} \times 2.5B]$$

$$= (2 + 37(n - 2) + 10) \times 2^{n-3} \times B$$

$$= (37n - 62) \times 2^{n-3} \times B. \tag{A.35}$$

Delay

From Fig. A.17 to Fig. A.19, the delays of the 2-dilated banyan switching element, the 2×4 re-arrangeable input switching element and the 4×2 re-arrangeable output switching element are $2D$, $0.5D$ and $1.5D$, respectively. From the same discussion of the delay of the banyan switching element, the largest delay among all stages of a $2^n \times 2^n$ 2-dilated banyan network is estimated to $2D$.

As in the case of the banyan network with all-bypass-connection, the largest delay among all stages of a $2^n \times 2^n$ 2-dilated banyan network with all-bypass-connection occurs at the second stage, where two sequences of one Type 1, ($\frac{1}{2} \frac{2^n}{2} - 2$) Type 2 and one Type 3 of the 2-dilated banyan switching elements with bypasses exist. Then, it is estimated as follows:

$$3D + 2D \times (\frac{1}{2} \frac{2^n}{2} - 2) + 1.5D = (2^{n-1} + 0.5) \times D. \tag{A.36}$$

In the case of a $2^n \times 2^n$ 2-dilated banyan network with one-bypass-connection, the largest delay among all stages is estimated as follows:

$$3D + 1.5D = 4.5 \times D. \tag{A.37}$$

The total delays of the above networks can be concluded by the same discussion as the ones of the banyan networks in the previous subsection.

A.2.3 Hybrid Dilated Banyan Network

The hybrid dilated banyan network is constructed from the 2×4 re-arrangeable input switching elements, the 2-dilated banyan switching elements, the 4×2 re-arrangeable output switching elements and the original banyan switching elements. These structures are shown at Fig. A.15 and Fig. A.17 to Fig. A.19. For the 2-dilated banyan network with bypasses, three types of 4×2 re-arrangeable output switching elements with bypasses, whose structures are in Fig. A.21, are used. All of them consist of four banyan switching elements. In addition, Type 1 to 3 have a multiplexer and a demultiplexer at their bypass link. Each component in Fig. A.21 is the same as in Fig. A.20. The demultiplexers and the multiplexers at the bypass links in Fig. A.21 are also limited the number of cells through this link at the same time to one.
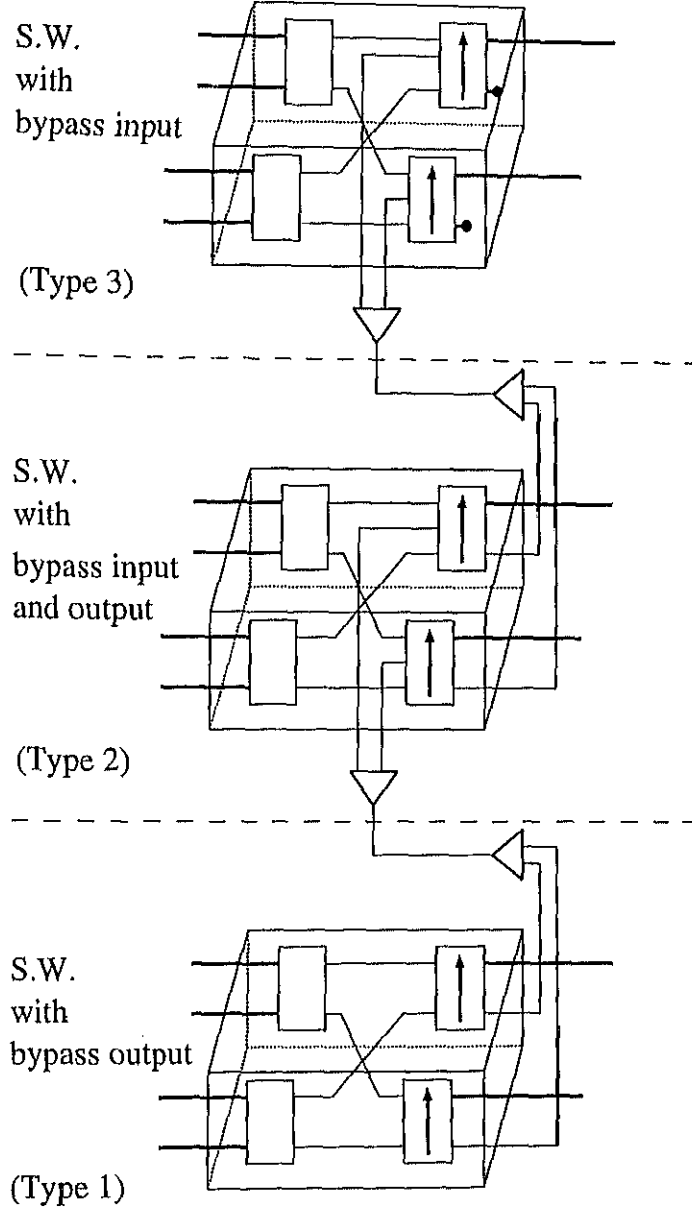
Figure A.21: 4×2 re-arrangeable output switching element with bypasses.

Hardware Size

In a $2^n \times 2^n$ hybrid dilated banyan network, let r be the number of stages of 2-dilated banyan switching elements $(n - 3 \geq r)$. In this case, the second to $(r + 1)$-th stages have 2-dilated banyan switching elements, and $(r + 3)$-th to n-th stages have banyan switching elements. From the results of the previous subsection, the hardware size of a $2^n \times 2^n$ hybrid dilated banyan network is estimated as follows:

$$[\frac{2^n}{2} \times 0.5B] + [\frac{2^n}{2} \times r \times 6B] + [\frac{2^n}{2} \times 2.5B] + [\frac{2^n}{2} \times (n - r - 2) \times B]$$

$$= (1 + 5r + n) \times 2^{n-1} \times B. \tag{A.38}$$

The hardware size of Type 1 to Type 3 of 4×2 re-arrangeable output switching elements with bypasses in Fig. A.21 are $4.25B$, $4.5B$ and $4.25B$, respectively. Let r be the number of stages of 2-dilated banyan switching element ($n - 3 \geq r$). As in the case of the 2-dilated banyan network with all-bypass-connection, the hardware size of a $2^n \times 2^n$ hybrid dilated banyan network with all-bypass-connection is estimated as follows:

$$\begin{aligned}
&[\frac{2^n}{2} \times 0.5B] + [\sum_{d=2}^{r+1}(2^{d-1} \times 9.25B + (2^{n-1} - 2^d) \times 9.5B + 2^{d-1} \times 9.25B)] \\
&+[2^{(r+2)-1} \times 4.25B] + [(2^{n-1} - 2^{r+2}) \times 4.5B] + [2^{(r+2)-1} \times 4.25B] \\
&+[\sum_{d=r+3}^{n-1} \frac{2^n}{2} \times 2.5B] + [\frac{2^n}{2} \times B] \\
=~& 2^{n-2}B + (19r2^{n-2} - 2^r + 1)B + (9 \times 2^{n-2} - 2^r)B \\
&+5(n - r - 3)2^{n-2}B + 2 \times 2^{n-2}B \\
=~& [(5n + 14r - 3) \times 2^{n-2} - 2^{r+1} + 1] \times B. \tag{A.39}
\end{aligned}$$

The hardware size of a $2^n \times 2^n$ hybrid dilated banyan network with one-bypass-connection is also estimated as follows:

$$\begin{aligned}
&[\frac{2^n}{2} \times 0.5B] + [r\frac{1}{2}\frac{2^n}{2}(9.25B + 9.25B)] + [\frac{1}{2}\frac{2^n}{2}(4.25B + 4.25B)] \\
&+[(n - r - 3)\frac{2^n}{2} \times 2.5B + \frac{2^n}{2} \times B] \\
=~& (5n + 13.5r - 3.5) \times 2^{n-2} \times B. \tag{A.40}
\end{aligned}$$

Delay

The hybrid dilated banyan network is constructed with four kinds of switching elements. Among of them, a stage of the 2-dilated banyan switching element has the largest delay. Then, the largest delay among all stages of a $2^n \times 2^n$ hybrid dilated banyan network is the same with that of the $2^n \times 2^n$ 2-dilated banyan network, i.e., $2D$.

The largest delay among all stages of a $2^n \times 2^n$ hybrid dilated banyan network with all-bypass-connection or one-bypass-connection is also equal to the one of a $2^n \times 2^n$ 2-dilated banyan network with all-bypass-connection or one-bypass-connection, whose the delay has $4.5 \times D$ or $(2^n + 0.5) \times D$. The total delays of the above networks are estimated as in Appendix A.2.1.