Ballistic MOSFET Reproduces Current–Voltage Characteristics of an Experimental Device

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***Abstract*—The ballistic MOSFET characteristics are compared in detail with those of the experimental 70-nm device at low temperatures reported by Sai-Halasz *et al.* The saturated region characteristics for $V_G \leq 0.8$ V show good agreement and a proper consideration of higher subbands significantly improves agreement for $V_G \geq 1.0$ V. The discrepancy is large in the linear region due to carrier scattering. The carrier backscattering mechanism and the bias effect are discussed.**

***Index Terms*—Cryogenic electronics, current density, MOSFETs, semiconductor device modeling, semiconductor devices, silicon, transistor.**

I. Introduction

RECENTLY, ultrasmall MOSFETs of around 20∼30 nm size are fabricated and their high performance is reported [1], [2]. On the other hand, the ballistic MOSFET has been proposed and is supposed to indicate the limiting high performance of the structure [3]. However, the comparison revealed that the experimental performance does not show a high performance like the limiting case, but is mostly less than 50% of the ballistic value [4]–[6]. This letter compares the ballistic MOSFET characteristics with those of the famous 70-nm low-temperature device reported by Sai-Halasz *et al.* [9]. The comparison shows an excellent agreement between the two in a limited bias range.

II. Current–Voltage (I–V) Characteristics of the Ballistic MOSFET

The drain current I_D per unit width and the inversion charge density Q near the source edge of an n-channel ballistic MOSFET on (100) surface of Si has been derived as [3]

$$I_D = \frac{\sqrt{2}q(kT)^{3/2}}{\pi^2\hbar^2}\sum_{\text{valley}}\sum_{n}\sqrt{m_y} \cdot \left[F_{1/2}\left(\frac{\phi_{FS}-E_n}{kT}\right) - F_{1/2}\left(\frac{\phi_{FS}-E_n-qV_D}{kT}\right)\right] \tag{1}$$

$$|Q| = C(V_G - V_t) = \frac{qkT}{2\pi\hbar^2}\sum_{\text{valley}}\sum_{n}\sqrt{m_x m_y}\ln\left\{\left[1+\exp\left(\frac{\phi_{FS}-E_n}{kT}\right)\right] \cdot \left[1+\exp\left(\frac{\phi_{FS}-E_n-qV_D}{kT}\right)\right]\right\} \tag{2}$$

where

k	Boltzmann constant;
T	temperature;
m_x (m_y)	electron effective mass along (across) the channel;
ϕ_{FS}	Fermi level of the source electrode;
C	MOS effective capacitance;
V_G, V_D, and V_t	gate bias, drain bias, and threshold voltage, respectively.

The potential curve within the channel (actually the lowest subband bottom curve) has a maximum point $E_{\max}$ adjacent to (or at) the source edge [3]. E_n is the nth subband energy at this maximum point. The Fermi–Dirac integral $F_{1/2}(u)$ [7] is defined as

$$F_{1/2}(u) = \int_0^\infty \frac{\sqrt{y}}{1+\exp(y-u)}\,dy. \tag{3}$$

In an ultrasmall MOSFET on a high-concentration substrate, it is shown that the lowest subband accommodates a majority of channel electrons, and the drain current is conveniently approximated by a closed analytical expression of terminal voltages (effective one-subband approximation) as [3], [4]

$$I_D = \frac{\sqrt{2m_t}\,q(kT)^{3/2}M_v}{\pi^2\hbar^2}\left[F_{1/2}(u) - F_{1/2}(u-v_d)\right] \tag{4}$$

$$u = \ln\left[\sqrt{(1+e^{v_d})^2 + 4e^{v_d}(e^{\rho}-1)} - (1+e^{v_d})\right] - \ln 2 \tag{5}$$

$$v_d = \frac{qV_D}{kT} \tag{6}$$

$$\rho = \frac{2\pi\hbar^2 C(V_G - V_t)}{qkTm_tM_v} \tag{7}$$

where $m_t = 0.19$ m$_0$ is the transverse electron mass of Si and $M_v \cong 2.2$ [88] is a parameter representing effective number of the lowest equivalent valley.[1]

III. Comparison of Ballistic MOSFET With the Experimental Device

In [9], Sai-Halasz *et al.* disclosed the current–voltage (I–V) characteristics of a sub-100-nm MOSFET for the first time. They fabricated a MOSFET with the 70-nm gate length as well as the relaxed oxide thickness of 4.5 nm on a 2-Ω cm p-type Si wafer. The implant boron for threshold control was so managed

[1]The parameter M_v is discussed in [4] in detail. It depends on the lowest subband population ratio, and the self-consistent Schrodinger–Poisson simulation discussed in the text yields the ratio of 90% indicating that $M_v = 2.2$.

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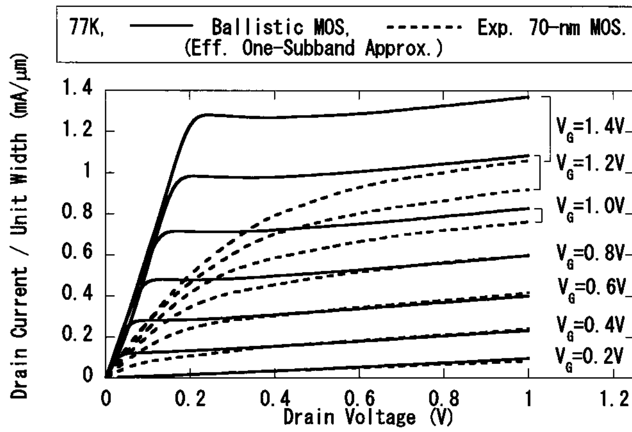

Fig. 1. I_D–V_D characteristics of the ballistic MOSFET (solid lines) in effective one-subband approximation [(4)–(7)] are compared with those of the experimental 70-nm device at 77K (dashed lines) reported by Sai-Halasz *et al.* [9]. The parameter is the gate bias from 0.2 V to 1.4 V at 0.2 V intervals.

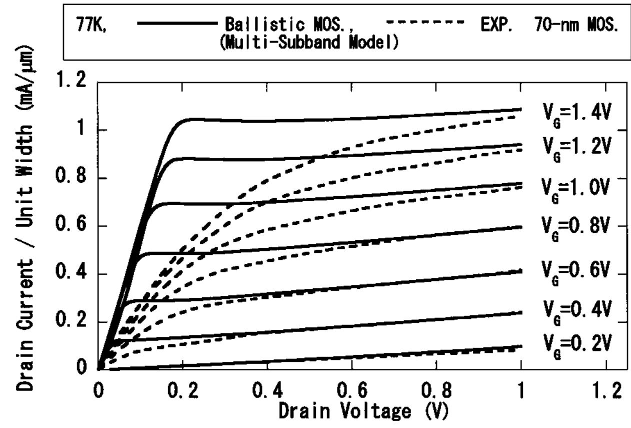

Fig. 2. I_D–V_D characteristics of the ballistic MOSFET (solid lines) where higher subband effects are considered according to (1) and (2), are compared with those of the same experimental device (dashed lines). The parameter is the same as in Fig. 1.

that the surface boron concentration be as low as possible for a given thermal budget. It was evaluated at 77 K, and the device characteristics with minimized carrier scattering were explored. The experimental I–V curves of the device are reproduced from their publication. The source and the drain parasitic resistance and the drain-induced barrier lowering (DIBL) effect need be considered so as to analyze the corresponding ballistic MOSFET characteristics. They report the combined source and drain resistance to be 250∼270 Ω per unit width [10], and we use an equal value 130 Ω for both electrodes. The potential drop within the source and the drain is predicted from experimental I_D and the net voltage applied to the channel is extracted. As for the DIBL effect, the saturation current of a ballistic MOSFET is a function of $|Q|$ [4], and hence of $(V_G - V_t(V_D))$. The derivative of I_D is derived as $(\partial I_D/\partial V_D) = -(\partial I_D/\partial V_G)(\partial V_t/\partial V_D)$, and the value of $(\partial V_t/\partial V_D)$ for large V_D and small V_G is extracted from the experimental I–V curves. The extrapolation of the I_D–V_G curve also yields the V_t for a fixed V_D, and the $V_t(V_D)$ is extracted as $V_t \cong (0.2\text{–}0.18V_D[V])$ V. We used $C = \varepsilon_{\rm ox}/t_{\rm ox}$ with $t_{\rm ox} = 4.5$ nm, since the experimental $t_{\rm ox}$ is estimated from the capacitance.

Fig. 1 compares the I–V characteristics of the experimental device with those of the ballistic MOSFET in the effective one-subband approximation [(4)–(7)]. The ballistic MOSFET curve shows a slight hump between the linear and the saturated region. The bias indicated in the figure is applied to terminals of the experimental device, and the net bias applied to channel is smaller by the potential drop due to the source and drain parasitic resistance. The "experimental" current increases in this region, then the potential drop increases, the net V_G decreases although the V_G at the terminal is constant, and so the "ballistic" current in saturation seemingly decreases, forming a hump. The ballistic curve well agrees with the experimental curve in restricted part of saturated region when $V_G \leq 0.8$ V. It is amazing that the ballistic MOSFET formula including only elementary parameters like q, $\hbar$, and m_t, well reproduces the absolute value of an experimental device.

The discrepancy is large for $V_G \geq 1.0$ V and also for the linear region. In contrast to the high-concentration substrate employed in recent sub-100-nm MOSFETs, a low-concentration one is used here, which tends to reduce the subband-energy spacing and enhances the higher subband effect. We compare the ballistic MOSFET current with the experimental data considering the higher subband effects. A 2-Ω cm p-type substrate is used in the experiment, but the exact impurity concentration is not known due to the B ion implantation. As for the subband-energy spacing, a self-consistent Schrodinger–Poisson simulation for the ballistic MOSFET in saturation yields values $E_0' - E_0 = 57.3$ meV, $E_1 - E_0' = 1.4$ meV, and $E_2 - E_1 = 38.3$ meV (the notation is after Stern [11]) at 77 K for low impurity concentration of 10^{17} cm^{-3}. Equations (1) and (2), as well as a choice of fixed values $E_0' - E_0 = 59.0$ meV, $E_1 - E_0' = 1.5$ meV, and $E_2 - E_1 = 40.1$ meV (which gives slight increase of doping, still higher subbands being neglected), significantly improve agreement for $V_G \geq 1.0$ V in the saturated region, as is shown in Fig. 2. The agreement indicates the higher subband effect is essential for prediction of saturation current with large gate biases.

Fig. 2 suggests the carrier scattering significantly reduces current in the linear and the low-drain-bias saturated region. The following mechanism qualitatively explains the bias effect there. We refer to the channel region of the length L_{BS} which extends from the $E_{\max}$-point to a point where the potential drops down to a value $(E_{\max} + E_{\rm el} - E_{\rm op})$ as the "backscattering region." Here $E_{\rm op}$ (=63 meV) is the optical phonon energy, and $E_{\rm el}$ the small mean kinetic energy at $E_{\max}$-point. The optical phonon emission is suppressed in this region because the carrier energy is not large enough. The absorption is rare at low temperatures, and the elastic or quasi-elastic scattering like the impurity (the surface-roughness) and the acoustic phonon scattering is dominant, occasionally carrying electrons back to the source. Once a carrier survives out of this region, it is exposed to the frequent optical phonon emission and immediately loses its energy. The enervated carrier has little chance to return to the source ever after and eventually exits from the drain. The reduction of current from the ballistic value is due to the backscattering of carriers in this "backscattering region." If $L_{BS} \ll l_0$, the carrier mean free path in the region, the MOSFET behaves like a bal-

listic device, and if $L_{BS} \gg l_0$ on the contrary, then the backscattering dominates and the current is reduced. The backscattering region extends to the whole channel when $V_D \leq (E_{\rm op} - E_{\rm el})/q$. The increase of V_D reduces L_{BS}, because it steepens the potential slope in the channel, and the ballisticity is improved. The point that the increased V_D reduces L_{BS} and improves ballisticity is analogous to the "kT layer" theory discussed by Lundstrom (see [12]) except that the length L_{BS} is controlled by inelastic scattering. Both mechanisms have the same origin of losing the longitudinal kinetic energy. Generally, nondegenerate thermal carriers escape backscattering when they have traveled across the kT layer thickness. However, if degenerate carriers in low temperatures have a mean energy $E_{\rm el}$ larger than the small kT at $E_{\rm max}$-point, they can be back-scattered beyond the "kT layer," and may need to exceed the previous L_{BS} to escape backscattering. The increase of V_G at a fixed V_D increases interface normal field and intensifies scattering [12], which reduces l_0 and enhances deviation from ballistic current.

IV. Conclusion

The $T = 77$ K characteristics of the 70-nm MOSFET reported by Sai-Halasz *et al.* [9] were compared with a ballistic model. The results show that under low drain bias, the device operated well under the ballistic limit, but for high drain bias, the device operates essentially at the ballistic limit. These results can be qualitatively understood in terms of a simple model for scattering.

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