

# Characteristics of a carbon nanotube field-effect transistor analyzed as a ballistic nanowire field-effect transistor

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A general expression of the current–voltage characteristics of a ballistic nanowire field-effect transistor (FET) is derived. At  $T=0$ , the conductance, which is equal to the quantum conductance multiplied by the number of channels at zero bias, decreases stepwise toward current saturation as the drain bias is increased. The current–voltage characteristics of a single-wall carbon nanotube FET in ballistic conduction are discussed based on the band structure of the nanotube. When both the gate overdrive and the drain bias are equal to 1 V, the device made of a (19,0) nanotube and a 2-nm high- $k$  gate insulator ( $\epsilon=40\epsilon_0$ ) flows a current of 183  $\mu\text{A}$ , which amounts to a current density 48 times as large as the counterpart of a silicon device. The high performance originates from a high carrier density due to the enhanced gate capacitance, and a large carrier velocity caused by the large group velocity of the original graphene band. Quantum capacitance also plays an important role in the device's characteristics. © 2005 American Institute of Physics. [DOI: 10.1063/1.1840096]

## I. INTRODUCTION

Recently, carbon nanotube (CN) field-effect transistors<sup>1</sup> (FETs) have attracted wide attention as promising candidates for components in the next generation of electronic devices. Both  $n$ - and  $p$ -channel devices have been fabricated and a surprisingly high performance per unit width has been reported. In spite of a large voltage drop across the contact to metallic electrodes, fabricated FETs have so far shown a high current level.<sup>2,3</sup> The device's conduction mechanism is not clear at present. Some cases have been explained as Schottky barrier FETs (Refs. 4–6) and a detailed analysis of the Schottky barrier FET model has been presented. Others are likely to be dominated by nanotube bulk conduction,<sup>3</sup> the Schottky barrier being suppressed by virtue of the improved contact technique. A near ballistic conduction is expected in metallic CNs,<sup>7,8</sup> while a CN FET, made of semiconductor CN, may also enjoy a near ballistic transport if the channel length is sufficiently less than the mean free path of the carriers.<sup>9</sup> In view of the high performance increased year by year in pursuit of ballistic conduction, it is pertinent to the issue to discuss the ballistic CN FET characteristics. A silicon nanowire transistor in a ballistic conduction has been computationally analyzed<sup>10</sup> at the wire's various cross sections. A semiclassical Monte Carlo simulation considering the carrier scattering in a CN (Ref. 11) or a CN FET (Ref. 9) has also been reported. It is interesting to know what performance is accessible if the ballistic transport from source to drain is realized. Assessments and performance projection of a CN FET in comparison to the silicon metal-oxide-semiconductor field-effect transistor (MOSFET) have been reported,<sup>12,13</sup> and many interesting features including the important role of quantum capacitance have been pointed out, although the detailed procedure is not clearly disclosed.

This paper presents a theoretical analysis of the current–

voltage ( $I$ – $V$ ) characteristics of a ballistic CN FET (Ref. 14) in close relation to the band structure of a CN. Detailed comparison with the characteristics of a ballistic silicon MOSFET has revealed a predominant performance over the silicon counterpart. The device's physics underlying the performance is also discussed. First, a general theory of a nanowire FET is derived, and the result is then applied to a CN FET.

## II. $I$ – $V$ CHARACTERISTICS OF A BALLISTIC NANOWIRE FET

A CN FET is structured as is illustrated in Fig 1. The source and the drain electrodes are mutually connected via a CN channel with the gate electrode set aside to control the channel conductance. This is the so-called top-gate structure.<sup>2</sup> A FET with a bottom-gate structure, where the substrate acts as the gate electrode via an insulator layer, is also fabricated. We first discuss the  $I$ – $V$  characteristics of a ballistic semiconductor nanowire FET, and apply the result to a CN FET. The characteristics of the nanowire device are obtained in a parallel manner to discuss the ballistic silicon MOSFET.<sup>15–17</sup> The source and the drain electrodes are assumed to be ideal reservoirs that supply sufficient carriers to channel and sink carriers from the channel without reflection.

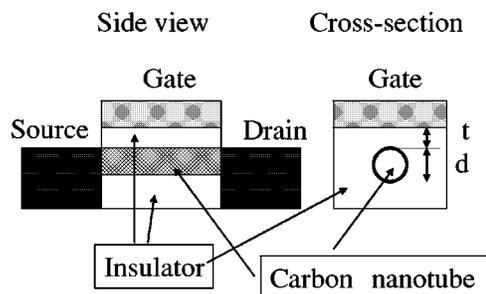


FIG. 1. The structure of the analyzed CN FET. No Schottky barrier is assumed between the channel and the source and drain.

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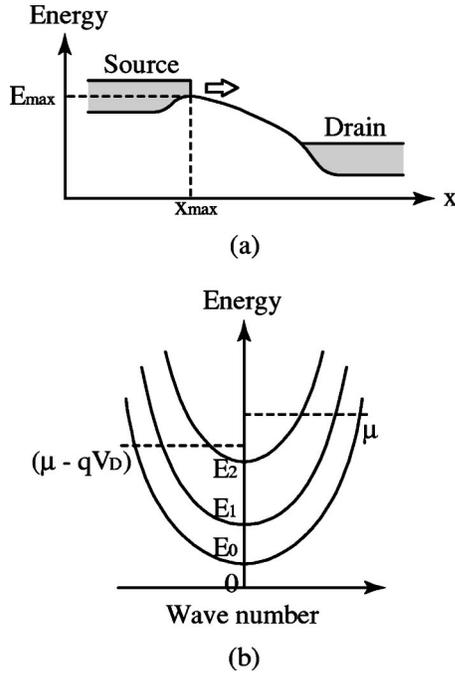


FIG. 2. Schematic diagrams of the potential profile along the channel (a), and the energy subband of nanowire (b).  $\mu$  and  $(\mu - qV_D)$  shows the Fermi level of the source and the drain, respectively.

The potential profile from the source to the drain along the channel of a ballistic FET is generally rendered as in Fig. 2(a).<sup>15</sup> The potential energy takes a maximum value at the point  $x_{\max}$  located at or near the source edge. This point acts as a bottleneck of current flow in the device, and the carrier flux that surpasses this maximum constitutes the device current. Along the approach of Landauer's formula, the device's current is expressed by a product of the carrier flux injected to the channel and the transmission coefficient, which is assumed to be unity in the ballistic limit, since the backscattering or reflection due to the scatterers or to the device structure in the course from source to drain is neglected. The carrier flux flowing into the channel is analyzed by using the plane wave propagating along the channel as an approximation of the electronic state around the bottleneck. The energy versus wave-vector relation is expressed by the one-dimensional subband illustrated in Fig. 2(b). Positive velocity states, i.e., those propagating toward the drain, referred to hereafter as the fore channel, are populated with carriers according to the source Fermi level, while the negative velocity states, referred to as the back channel (propagating toward the source), are populated according to the drain Fermi level, when scattering is absent in the channel. Thus the device's current  $I_D$  in the ballistic limit is approximately expressed by,

$$I_D = \frac{q}{\pi\hbar} \sum_i \int_{E_i} [f(E, \mu) - f(E, \mu - qV_D)] dE. \quad (1)$$

Here,  $E_i$  stands for the bottom energy of the  $i$ th subband, the summation  $i$  is over the subbands,  $q$  is the elementary charge,  $\mu$  the Fermi potential of the source,  $V_D$  the drain bias, and

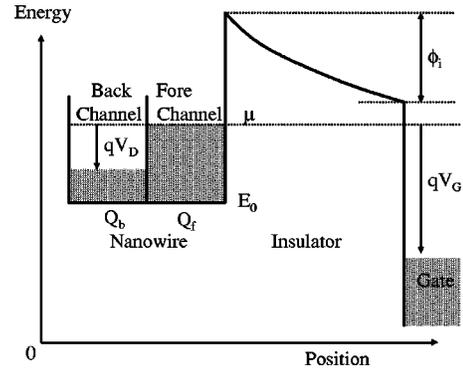


FIG. 3. Schematic potential-energy profile of the system of nanowire with the gate electrode around the  $x_{\max}$  point. The gate bias  $V_G$  is applied between the Fermi levels of the source and the gate. The potential-energy variation within the insulator is denoted by  $\phi_i$ . The fore channel (back channel) denotes conduction channel that consists of electronic states with the velocity heading toward the drain (source).

$$f(E, \mu) = \frac{1}{1 + \exp\left(\frac{E - \mu}{k_B T}\right)} \quad (2)$$

is the Fermi distribution function with Fermi energy  $\mu$ ,  $k_B$  the Boltzmann constant, and  $T$  the temperature. It is convenient to define  $\mu$  with respect to the origin of the nanowire subband, so that it varies as the population is varied. When the nanowire is a one-dimensional crystal, the upper limit of integration in Eq. (1) is the maximum value of the subband energy in the Brillouin zone. Substituting Eq. (2) for the Fermi functions in Eq. (1) and integrating, we obtain

$$I_D = \frac{qk_B T}{\pi\hbar} \sum_i \left( \sum_{dE(k)/dk \geq 0 \text{ branch}} \times \ln \left\{ \frac{1 + \exp[(\mu - E_{i \min}^+)/k_B T]}{1 + \exp[(\mu - E_{i \max}^+)/k_B T]} \right\} - \sum_{dE(k)/dk \leq 0 \text{ branch}} \times \ln \left\{ \frac{1 + \exp[(\mu - qV_D - E_{i \min}^-)/k_B T]}{1 + \exp[(\mu - qV_D - E_{i \max}^-)/k_B T]} \right\} \right), \quad (3)$$

where  $E_{i \max}^+$  ( $E_{i \min}^-$ ) denotes the maximum (minimum) energy in the positive velocity branch,  $dE/dk \geq 0$ , (negative velocity branch,  $dE/dk \leq 0$ ) of the  $i$ th subband. The unknown parameter  $\mu$  is evaluated as follows. Figure 3 schematically illustrates the potential-energy profile of the system of the nanowire with the gate electrode in the neighborhood of  $x_{\max}$ . The bias voltage  $V_G$  ( $V_D$ ) referring to the source Fermi level  $\mu$  is applied to the gate (drain) electrode. Figure 1 suggests that the CN and the gate electrode constitute a capacitor of capacitance  $C_i$  per unit length. The increase  $\delta V_G$  of the gate bias induces the increase  $\delta Q$  of the carrier charge density on CN (more precisely the charge is divided into the fore-channel part  $\delta Q_f$  and the back-channel part  $\delta Q_b$ ). It also induces the increase  $\delta\phi_i$  of the potential variation within the insulator, which is equal to  $\delta Q/C_i$ , and also the increase  $\delta(\mu - E_0)$  related to the population of the CN subband. Specifically, we have  $\delta V_G = \delta(\mu - E_0)/q + \delta\phi_i$ . If we recall that

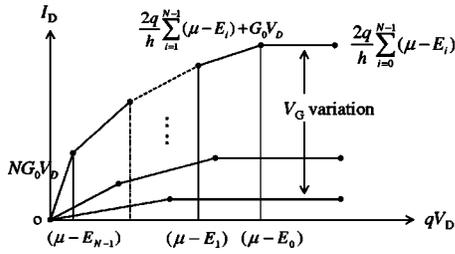


FIG. 4. Overall features of the  $I$ - $V_D$  characteristics of a nanowire FET at  $T=0$ .  $G_0$ ,  $E_i$ , and  $N$  are, respectively, the quantum conductance, the bottom of the  $i$ th subband, and the number of subbands involved in conduction. Conductance (slope of curve) for  $V_D \rightarrow 0$  is  $NG_0$  and decreases stepwise as  $V_D$  is increased.

$d|Q_f|/d[(\mu - E_0)/q] = C_Q$ , where  $C_Q$  is the quantum capacitance<sup>18</sup> per unit length of the fore channel by definition, it is rewritten as  $\delta V_G = \delta|Q_f|(1/C_Q + 1/C_i) + \delta|Q_b|/C_i$ . The fore-channel charge is controlled by a series connection of the quantum capacitance and the insulator capacitance. We assume that the nanowire is a semiconductor, and is neutral when  $V_D=0$  and  $V_G$  is so adjusted that there is no charge included in it. Therefore,  $Q \approx 0$  and  $\phi_i \approx 0$ , and this is the flatband condition,  $V_G \equiv V_{FB}$  ( $V_{FB}$  depends on the work-function difference as usual). The source Fermi potential at this point is denoted by  $\mu_0$  ( $\mu_0$  is located close to the center of the energy gap without doping). If we increase the gate bias to a value  $V_G$ , the drain bias to a value  $V_D$ , and raise the source Fermi potential to  $\mu$ , carriers are induced and populate the fore channel and the back channel as seen in Fig. 3. Then we have,

$$V_G - V_{FB} = \frac{\mu - \mu_0}{q} + \frac{|Q_f| + |Q_b|}{C_i}. \quad (4)$$

We assumed that the band gap is sufficiently large, so that the charge due to holes in the valence band is neglected. Substituting the integral expression for the charge density, we have

$$\begin{aligned} & C_i [(V_G - V_{FB}) - (\mu - \mu_0)/q] \\ &= 2q \sum_i \left[ \sum_{dE(k)/dk \geq 0} \int_{E_i^-}^{E_i^+} D_{i+}(E) f(\mu, E) dE \right. \\ & \quad \left. + \sum_{dE(k)/dk \leq 0} \int_{E_i^-}^{E_i^+} D_{i-}(E) f(\mu - qV_D, E) dE \right], \end{aligned} \quad (5)$$

where,  $D_{i+}(E)[D_{i-}(E)]$  is the density of states of the positive (negative) velocity branch of the  $i$ th subband. Once the bias voltages at the terminal electrodes as well as the subband structure of the nanowire are known, the solution of Eq. (5) provides the value of  $\mu$ , and substitution of the value in Eq. (3) yields the drain current  $I_D$ . The  $I$ - $V$  characteristics of a nanowire FET are computed without ambiguity if the subband structure is known.

Figure 4 schematically illustrates the overall features of the  $I$ - $V_D$  characteristics of a nanowire FET at  $T=0$ . The profile of the curve closely resembles that of an ordinary silicon FET. The slope of the curve for  $V_D \rightarrow 0$  is equal to

$NG_0$ , where  $G_0 = 2q^2/h = 78 \mu S$  is the quantum conductance and  $N$  is the number of subbands contributing to the current at  $T=0$  and  $V_D \rightarrow 0$ . The curve includes some kinks, and the slope abruptly changes, every time the increasing drain bias depresses the drain Fermi level to traverse the subband minimum, until the drain Fermi level is below the lowest subband bottom and the current saturates. In other words, the conductance decreases from  $NG_0$  to zero stepwise as the drain bias is increased. However, the conductance of each section of the curve does not precisely coincide with the multiple of quantum conductance except for the case  $V_D \rightarrow 0$ , because  $\mu$  itself slightly increases as  $V_D$  increases.

### III. BALLISTIC CARBON NANOTUBE FETS

Now we investigate the  $I$ - $V$  characteristics of a nanowire FET whose channel consists of a single-walled carbon nanotube (SWNT). We try to analyze the current of an  $n$ -channel device. Experimental devices usually exhibit  $p$ -channel characteristics due to the fact that the Fermi level of the electrode is located close to the valence-band edge of the CN. Such a device is known to be converted to an  $n$ -channel one by some types of heat treatment.<sup>19</sup> Device current is considered parallel for the  $p$ -channel and the  $n$ -channel devices due to the assumed symmetrical nature of the band structure of SWNT. The computed result also applies to a  $p$ -channel device if the polarity of the current as well as that of the bias voltage is appropriately converted.

The SWNT has a cylindrical structure such that a two-dimensional graphene sheet is rolled up to form a one-dimensional tubelike nanowire. Each kind of SWNT is specified by a vector called the chiral vector that characterizes in what manner the graphene sheet is rolled up. The electronic band of a SWNT is easily derived from that of a graphene sheet as follows. We assume the tight-binding expression for the  $\pi$  ( $\pi^*$ ) band structure of a graphene sheet as<sup>20</sup>

$$E_{g2D}(k_x, k_y) = \pm t \left\{ 1 + 4 \cos\left(\frac{\sqrt{3}k_x a}{2}\right) \cos\left(\frac{k_y a}{2}\right) + 4 \cos^2\left(\frac{k_y a}{2}\right) \right\}^{1/2}, \quad (6)$$

where  $(k_x, k_y)$  is the two-dimensional (2D) wave vector,  $a$  the distance between neighboring carbon atoms, and  $t$  the electronic transfer integral between the two atoms. The band structure of the rolled-up SWNT is obtained by imposing a periodicity of the chiral vector on the electronic states of the unrolled graphene honeycomb lattice. This procedure causes quantization of the wave-vector space along the direction of the chiral vector. Only wave vectors whose component along the chiral vector is equal to the multiple of  $2\pi$  divided by the magnitude of the chiral vector are allowed. The wave-vector component normal to the chiral vector represents a one-dimensional electronic wave propagation along the CN axis. This pair of components, one quantized along the chiral vector and the other normal to it, constitutes the one-dimensional subbands of the SWNT. The two branches denoted by  $\pm$  in Eq. (6) correspond to the conduction band and the valence band of the graphene sheet, and these two bands

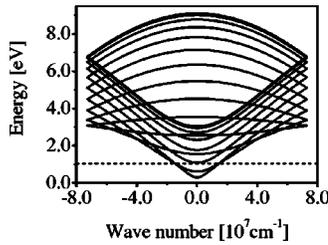


FIG. 5. The obtained band structure of the (19,0) single-wall carbon nanotube. The origin of energy is at the midpoint of the energy gap.

are known to touch each other at the high-symmetry point of  $K$  and  $K'$  located at the corner of the Brillouin zone. Therefore, the SWNT exhibits a metallic behavior if the chiral vector is so selected that the  $K$  and the  $K'$  points are on the subband. When we denote the chiral vector  $C_h$  as  $C_h = na_1 + ma_2 = (n, m)$ , where  $a_1$  and  $a_2$  are unit vectors of the unrolled honeycomb lattice and  $n$  and  $m$  integers, respectively, the CN is known to be metallic if the  $(n-m)$  is a multiple of 3.<sup>20</sup> We discuss a CN FET, and assume a semiconducting SWNT where  $(n-m)$  is not a multiple of 3 and therefore the energy gap exists between the valence band and the conduction band. Specifically, the conduction band of the SWNT with a chiral vector (19,0) is computed and the subband structure is shown in Fig. 5. The energy origin here is set at the zero of Eq. (6), which is the energy level of the  $K(K')$  point in the graphene band. Note that all subbands shown in Fig. 5 are doubly degenerate because the original graphene band structure in Eq. (6) has an inversion symmetry.

A CN FET with the structure illustrated in Fig. 1 is analyzed. The source and the drain electrodes are assumed to be connected via a (19,0) SWNT and the gate electrode is placed aside, separated by an insulator layer. Two sorts of insulators are assumed, the ordinary  $\text{SiO}_2$  with the dielectric constant  $\epsilon = 3.9\epsilon_0$  where  $\epsilon_0$  is the permittivity of a vacuum, and a high- $k$  gate dielectrics with  $\epsilon = 40\epsilon_0$  in view of  $\text{TiO}_2$ . The distance between the SWNT and the gate electrode is  $t = 2$  nm and the diameter  $d$  of the CN is 1.5 nm. No Schottky barrier is assumed between the SWNT and the source or the drain electrodes. The approximate value of the gate capacitance per unit length is estimated as a capacitance between two conductors, an infinite plane and a cylinder with diameter  $d$ , as

$$C_i = \frac{2\pi\epsilon}{\ln \frac{\sqrt{d+t} + \sqrt{t}}{\sqrt{d+t} - \sqrt{t}}}. \quad (7)$$

The capacitance per unit length of the simulated CN FET is evaluated as  $C_i = 7.036 \times 10^7 \text{q}(\text{V cm})^{-1}$ .

#### IV. RESULTS AND DISCUSSION

Applying the general theory of a ballistic nanowire FET as well as the band structure of a (19,0) SWNT, the current-voltage characteristics of the CN FET are derived. Room temperature  $T = 300$  K is assumed. The  $\mu_0$  is at the center of the band gap [origin of Eq. (6)] and  $\mu_0 = 0$ . The value of  $V_{\text{FB}}$  depends on the work-function difference and is not precisely known. Here we simply set  $V_{\text{FB}} = 0$ . Figures 6(a) and 6(b),

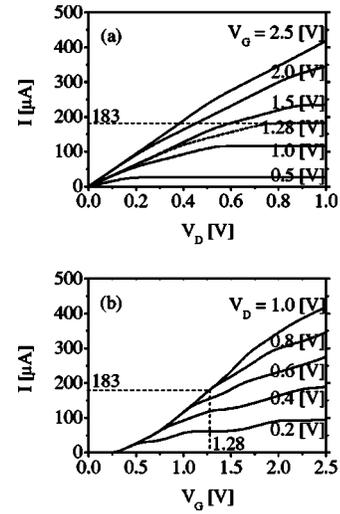


FIG. 6. The evaluated  $I$ - $V$  characteristics of a (19,0) SWNT CN FET. (a)  $I$ - $V_D$  characteristics. (b)  $I$ - $V_G$  characteristics.  $V_t = 0.28$  V and the FET flows  $183 \mu\text{A}$  at  $(V_G - V_t) = V_D = 1$  V.

respectively, show the  $I$ - $V_D$  and the  $I$ - $V_G$  characteristics of a (19,0) SWNT FET with a gate insulator of  $\epsilon = 40\epsilon_0$ . When  $V_G$  exceeds  $0.28$  V,  $\mu$  traverses the energy level  $E_0$  and carriers begin to accumulate in the lowest conduction subband leading to current flow. That is,  $V_G = 0.28$  V is the effective threshold voltage  $V_t$ . This value itself has no validity without any experimental background, but the gate overdrive  $(V_G - V_t)$  makes sense. The  $I$ - $V_D$  curves resemble those in Fig. 4 and show slight kinks or irregular shifts of slope at some points. This is because the number of subbands contributing to the current undergoes a change when the bias voltage is varied, just as in the case of Fig. 4. Overall, the current slowly and steadily increases as the bias is increased, in contrast to the ballistic silicon MOSFET, where the current first rapidly increases and soon saturates at small  $V_D$  values. At  $(V_G - V_t) = V_D = 1$  V, the current level shows saturation and points to  $183 \mu\text{A}$ . This value is exceedingly large compared to the reported value of experimental devices. The current per unit width of FET, obtained by dividing the value by the CN diameter of 1.5 nm, is convenient for comparison to the value of the silicon MOSFET. It yields  $122 \text{ mA}/\mu\text{m}$  and is 48 times as large as the current per unit width of the ballistic silicon MOSFET. We can easily verify that this large magnitude is reasonable. Figure 7 shows a magnification of the bottom part of the band structure shown in Fig. 5. At the gate overdrive  $(V_G - V_t) = 1$  V, Eq. (5) yields  $\mu = 1.03$  eV. Only

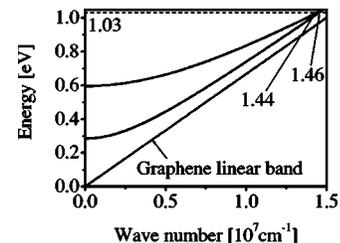


FIG. 7. Magnification of the bottom part of the band in Fig. 5. The source Fermi level is at  $\mu = 1.03$  eV for  $(V_G - V_t) = V_D = 1$  V, and the wave number at this energy in each subband is also shown. The dotted line is the linear band of an original graphene sheet.

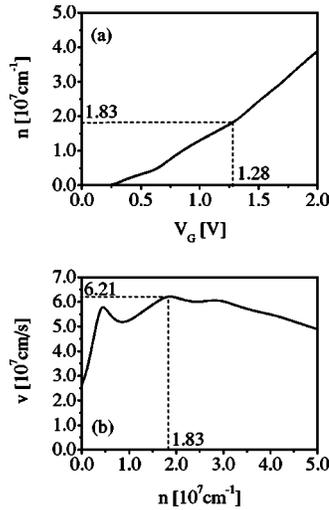


FIG. 8. Plots of (a) the carrier density  $n$ , and (b) the mean carrier velocity  $v$  around the  $x_{\max}$  point. The value for  $(V_G - V_t) = V_D = 1$  V is designated.

two kinds of subbands, each doubly degenerate, are heavily populated at the  $x_{\max}$  point, and there are four conduction channels; the lower pair whose bias window between the Fermi level  $\mu$  and the subband bottom is 0.75 eV, and the upper pair of 0.43 eV. The conductance of each pair of channels is  $2G_0 = 156 \mu\text{S}$ , and the total current amounts to  $156 \mu\text{S}(0.43 \text{ V} + 0.75 \text{ V}) = 184 \mu\text{A}$  in confirmation of the computed result.

The same result is expressed in terms of the carrier concentration and the carrier mean velocity. Figure 8(a) depicts the variation of the carrier concentration per unit length,  $n$ , of the CN at the bottleneck point as a function of the gate bias. A slightly superlinear increase is observed as  $V_G$  is increased, and  $n = 1.83 \times 10^7/\text{cm}$  at  $(V_G - V_t) = 1$  V. Figure 8(b) shows the mean value of the carrier velocity at the  $x_{\max}$  point as a function of  $n$ . This is the mean velocity of carriers injected from source to channel, and we call it the injection velocity  $v_{\text{inj}}$  in the case of silicon MOSFET.<sup>15</sup> It rapidly increases up to  $(5-6) \times 10^7$  cm/s and then almost saturates at further increases of  $n$ . Its value at  $n = 1.83 \times 10^7/\text{cm}$  amounts to  $6.21 \times 10^7$  cm/s.

Table I shows comparison of the CN FET characteristics in current saturation to its counterparts in a silicon ballistic MOSFET.<sup>17</sup> Due to the absence of carrier scattering, the MOSFET value indicates the maximal performance of an  $n$ -channel silicon device on a (100) surface at room tempera-

ture. The device's current per unit width in an equivalent bias condition is  $2.5 \text{ mA}/\mu\text{m}$  for the inversion carrier concentration  $10^{13}/\text{cm}^2$  near the source edge. The drift velocity near the source edge,  $v_{\text{inj}}$ , of the silicon MOS amounts to  $1.6 \times 10^7$  cm/s. The values for the CN FET are converted to ones per unit width by dividing the value by the CN diameter.

If  $\text{SiO}_2$  is used as the gate insulator of a CN FET, the device's current is  $46 \mu\text{A}$ , which is  $31 \text{ mA}/\mu\text{m}$  per unit width and is 12 times as large as that of a silicon device. This magnitude is realized both by the 3.3 times increase of carrier density  $n$  and the 3.6 times increase of carrier velocity compared to those of a silicon device. If  $\text{TiO}_2$  with  $\epsilon = 40\epsilon_0$  is used for the gate insulator, the device's current increases up to  $183 \mu\text{A}$ , and this value yields a current density 48 times as large as that of a silicon MOS. Here,  $n$  is 12 times and  $v_{\text{inj}}$  is 3.9 times as large as the silicon device counterparts, respectively.

The surprisingly high performance of a CN FET stems from a large carrier density  $n$  as well as from a large carrier velocity  $v_{\text{inj}}$ . The large carrier density is due to the enhanced capacitance of the FET structure. Equation (7) predicts that the capacitance of our CN device is enhanced up to 4.25 times that of the parallel-plate capacitance assumed in the MOS structure. This enhancement is due to the electric field covering the side of the CN, and is caused by the fringe effect of a parallel-plate capacitor. The enhancement ratio is larger if the ratio  $(t/d)$  is larger. The enhancement will be diminished or lost if multiple CNs are densely layed in parallel due to loss of the side field. The carrier density enhancement in the analyzed  $\text{SiO}_2$  gate CN FET is only 3.2 times that of the silicon counterparts and does not reach the expected value. In the case when a high- $k$  insulator with  $\epsilon = 40\epsilon_0$  is used in addition to the fringe effect, a simple-minded estimation predicts that the capacitance enhancement will be 42.5 times that of the silicon MOS, but the carrier density enhancement is only 12-fold. The total capacitance is a series of the contributions from the insulator and the quantum capacitance. Here, the effect of quantum capacitance  $C_Q$  due to density of states is significant compared to the gate insulator capacitance, and the total capacitance is reduced, yielding the reduced carrier density. Since  $(V_G - V_t) \approx Q/C_i + (\mu - E_0)/q$ , Fig. 7 suggests that 0.75 V of the applied gate overdrive  $(V_G - V_t) = 1$  V is consumed by filling the CN density of states. The remaining 0.25 V is applied to the insulator capacitance, and the carrier density in the channel is es-

TABLE I. Comparison of the performance of ballistic CN FET to the silicon MOSFET counterparts.  $I_D$ ,  $n$ , and  $v$  are, respectively, the device current, the carrier density, and the mean carrier velocity. Those values per unit width, obtained by dividing the FET width or the nanotube diameter, are also shown.  $\epsilon = 4\epsilon_0$  shows the case where  $\text{SiO}_2$  is used for the gate insulator.

	$I_D(I_D/W)$	Ratio	$n(n/W)$	Ratio	$v$	Ratio
Si MOS ( $\epsilon = 4\epsilon_0$ )	$(2.5 \text{ mA}/\mu\text{m})$	1	$(10^{13}/\text{cm}^2)$	1	$1.6 \times 10^7 \text{ cm/s}$	1
CN FET ( $\epsilon = 4\epsilon_0$ )	$46.2 \mu\text{A}$ $(30.8 \text{ mA}/\mu\text{m})$	12	$5.0 \times 10^6/\text{cm}$ $(3.3 \times 10^{13}/\text{cm}^2)$	3.3	$5.7 \times 10^7 \text{ cm/s}$	3.6
CN FET ( $\epsilon = 40\epsilon_0$ )	$183 \mu\text{A}$ $(122 \text{ mA}/\mu\text{m})$	48	$1.83 \times 10^7/\text{cm}$ $(1.22 \times 10^{14}/\text{cm}^2)$	12	$6.21 \times 10^7 \text{ cm/s}$	3.9

estimated to be  $C_i(0.25\text{ V})=1.8\times 10^7 q\text{ cm}^{-1}$  in accordance with the simulated value. The energy-dependent quantum capacitance is effectively expressed as  $C_Q=(Nq^2/\pi)(dk/dE)=Nq^2/(\pi\hbar v)$ , where  $v$  is the carrier velocity. If it takes a smaller value, it has a more remarkable effect on the total capacitance through the series connection. In CNs, the carrier velocity is large as is discussed below, and the quantum capacitance has a remarkable effect. If  $C_Q\ll C_i$ , the quantum capacitance dominates and the variation of  $V_G$  is wholly transferred to the variation of  $(\mu-E_0)$  as pointed out in Ref. 12.

The carrier velocity  $v_{\text{inj}}$  is given by  $(1/\hbar)[\partial E(k)/\partial k]$  averaged over all the occupied states in the band. That is the weighted average of the slopes at the occupied states in Fig. 7 and it amounts to  $6.2\times 10^7\text{ cm/s}$ . The dotted line passing the origin in the figure illustrates the linear band of the graphene sheet near the  $K$  point, and the group velocity given by its slope is  $1.01\times 10^8\text{ cm/s}$ . The one-dimensional lowest subband of our CN consists of a section of the two-dimensional band of the graphene sheet at a wave vector close to the  $K$  point, and the slope is strongly affected by the linear band. Figure 7 suggests that the carrier velocity enhancement in the CN FET originates from the large group velocity of the linear band of the graphene sheet. In the limit  $n\rightarrow 0$ , the carrier velocity does not vanish but tends to  $2.6\times 10^7\text{ cm/s}$ . This value coincides with  $\sqrt{2k_B T/(\pi m)}$ , the average velocity of the positive velocity carriers populated according to the Boltzmann distribution. Here  $m$  is the effective mass of the lowest subband,  $0.04m_0$ . The counterpart in the silicon MOSFET is  $1.2\times 10^7\text{ cm/s}$ . The CN discussed above has a large thermal velocity due to its small effective mass.

The  $I$ - $V$  characteristics of the CN FET at 0 K are also investigated. The overall behavior is similar, but the magnitude of the device's current is only slightly smaller compared to those at the room temperature. The irregular shifts of slope are more conspicuous and form kinks. As we see in Fig. 7, carriers populate the subband up to several hundreds of millivolts which is large compared to the thermal energy at room temperature  $k_B T=0.025\text{ eV}$ . The temperature plays a minor role and the device's characteristics are only slightly modified by temperature variation.

No device so far fabricated has shown the high performance described here. However, recent reports<sup>3,9</sup> on CN FETs and metallic CNs have presented large values of 25–40  $\mu\text{A}$ , which amount to 20% of our value. In experimental CN FETs, where the source and the drain are made of metals, Schottky barriers are expected between the nanotube and the metallic electrodes and the large contact resistance seriously degrades the current magnitude. The choice of a more suitable metal electrode improved the current flow and yielded an excellent performance.<sup>3</sup> In silicon MOSFETs, the source and drain made of highly doped silicon intervene between the silicon channel and the metal interconnect. The potential of the electrode is smoothly connected to the channel without the band discontinuity.

The measured conductance close to  $2G_0$  in nanotubes is sometimes regarded as a mark of ballistic conduction, but that is not necessarily the case. If a number of subbands, say,

$N$  doubly degenerate subbands, are involved in the conduction and constitute current channels, the conductance at  $V_D=0$  amounts to  $NG_0$  as we see in Fig. 4. In comparatively thick CNs, subbands are densely packed with small spacing between them, and the ballistic conductance with multiple channels may far exceed  $2G_0$ . The measured conductance close to  $2G_0$  might be a result of degradation due to the parasitic resistance. A better mark of a ballistic conduction is the confirmation of the stepwise decrease of conductance (step height is close to  $2G_0$ ) as  $V_D$  is increased in sufficiently low-temperature operation. The result will also reveal the number of subbands involved in the conduction. The dominance of parasitic resistance will obscure and degrade the step structure.

## V. CONCLUSION

The general expression of the  $I$ - $V$  characteristics of a ballistic nanowire FET is derived. At low temperatures, the conductance amounts to  $NG_0$  for  $V_D\rightarrow 0$ , and decreases stepwise toward the current saturation as  $V_D$  is increased. The  $I$ - $V$  characteristics of a ballistic CN FET are discussed. The ballistic CN FET analyzed in the present paper shows a high current level per unit width, as large as 48 times that of a ballistic silicon  $n$ MOSFET. The high performance is afforded by the large carrier density caused by the enhancement of gate capacitance, and also by a large carrier velocity. This gate capacitance enhancement is caused partly by the narrow wire structure and also by the assumed high- $k$  gate insulator. The large carrier velocity is due to the steep linear band near the  $K(K')$  point in the original graphene band structure. This large velocity also brings about the small density of states of the subband, and results in the small quantum capacitance. Serially connected to the insulator capacitance, the quantum capacitance will strongly affect the device's characteristics when a high- $k$  gate insulator is used.

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