Graduate School of Pure and Applied Sciences

Study on Si/Ge Core-Shell Nanowires and Their Alloy Structures for Future Electronic Devices

(次世代電子デバイスのための Si/Ge コアシェル構造および合金組成ナノワイヤの研究)

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Abstract

Since the development of semiconductor materials several decades ago, both theoretical and experimental work has been done to investigate the properties of devices made by them. Silicon (Si) and germanium (Ge) materials are advantageous for producing high-performance field-effect transistors (FETs), due to their high electron and hole mobilities. The electron and hole mobilities in Si are 1600 cm^2/VS and 430 cm^2/VS, while the values in Ge are 3900 cm^2/VS and 1900 cm^2/VS, respectively. Performance improvements in semiconductor devices follow Moore's Law, which states that the component density on an integrated chip doubles every two years[1], and the fabrication of traditional transistors continued to scale down following this rule. However, transistors have a practical limit, leading to leakage current as the gate length decreases.[1] This limit results in higher heat and fabrication cost. Miniaturizing the dimensions of devices has become a pressing need, which can increase not only a density on a chip but also improve the speed of transistors. One dimensional structure materials such as Si and Ge nanowires (NWs), have been considered as channels for nanoscale transistors with high speed, high integration, and low power consumption through gate-all-around transistors. The developments of NWs include the innovation of architecture between Si and Ge, such as core-shell, core-multishell, and alloy structures.[2,3] Because the core-shell structure can suppress scattering and separate carrier transport from impurity doped regions, a fast carrier transport can be realized with these devices. Impurity doping is also important to functionalize NWs for novel devices.[4–6] Therefore, p-Si/i-Ge core-shell NWs and p-Si/i-Ge/p-Si core-double shell NWs were fabricated to study this phenomenon. The precise analysis of NW structures and impurity doping in NWs was performed. In addition, the interface properties between Si and Ge layers was characterized to show the intermixing of core-shell structures. Moreover, SiGe alloy NWs with impurity doping were synthesized to study the properties of NWs. These results show that the good compatibility and scalable synthesis of Si and Ge NWs may provide remarkable progress for complementary metal-oxide semiconductor (CMOS)-integrated circuit technology and high-speed devices.

1. Formation of p-Si/i-Ge core-shell NWs by using bottom-up method

This chapter presents the formation and characterization of p-Si/i-Ge core-shell NWs grown using bottom-up method.[5] The growth of NWs were done by using chemical vapor deposition (CVD) with the vapor-liquid-

solid (VLS) mechanism.[7] This process is not only universal for a variety of catalysts (Au, Al, Cu) but also can be used with many different precursors (gaseous, liquid and solid). The VLS growth allows for easy modulation of nanowire diameter and length by controlling conditions such as deposition rate, temperature, and pressure. In this chapter, Au nanoparticles were selected as the catalyst for NW growth. Boron (B) impurities were introduced in the Si region to prepare p-type NWs, which is one of the fundamental methods of improving carrier transport in solids. p-Si/i-Ge core-shell NWs and p-Si/i-Ge/p-Si core-double shell NWs were fabricated to suppress impurity scattering. The schematic of these NWs is shown in Figure 1. The core-shell NW structure shows a sharp interface that is necessary for the realization of high mobility FETs by separating the carrier transport region from the impurity doped region. The generation of hole and electron gas in Si/Ge heterostructures can be detected, which is introduced by band offset between Si and Ge and controlled by impurity doping. Moreover, Si/Ge core-shell NWs show promise for suppressing surface scattering of carriers.

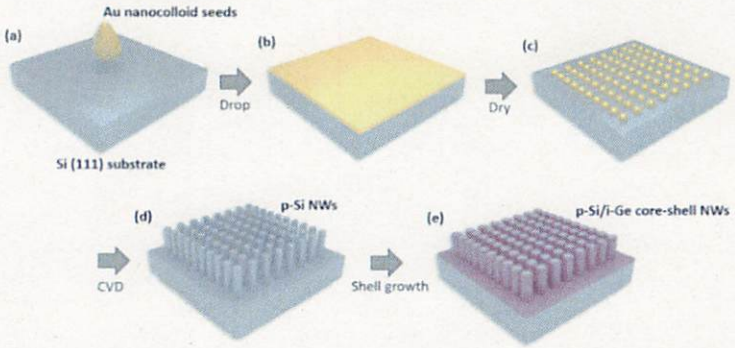

Figure 1. Schematic of the p-Si/i-Ge core-shell NW CVD growth process: (a)-(c) deposition of colloidal Au catalyst seeds on the Si (111) substrate; (d) formation of p-Si core NWs by SiH_4 gas flux; (e) final p-Si/i-Ge core-shell NWs.

Various methods were used to characterize the core-shell NWs. Raman measurement is a useful method to determine impurity doping and bonding states in NWs by identifying the vibrational modes of impurity atoms.[8,9] The positions and shape of Raman optical phonon peaks can be used to evaluate the electrical activity of dopant atoms. Crystallinity and interface of core-shell NWs can be characterized by TEM with EDX mapping. The stress between the core and shell layers can be analyzed by estimating the lattice constants of NWs with XRD measurements. First, p-Si/i-Ge core-shell NWs with B doping in Si core region were grown on Si (111) substrates in the CVD chamber. To avoid the oxidation and rough interfaces, the processing pressure was set to about 2×10^{-6} Pa. Before growth, the Si wafer was cleaned using water, ethanol, and isopropanol. Next, the native oxide on the Si wafer was removed with a hydrogen fluoride (HF) solution. SiH_4 (100%), GeH_4 (100%) and B_2H_6 (1% in H_2) gases were used to form p-Si/i-Ge core-shell NWs. TEM images with

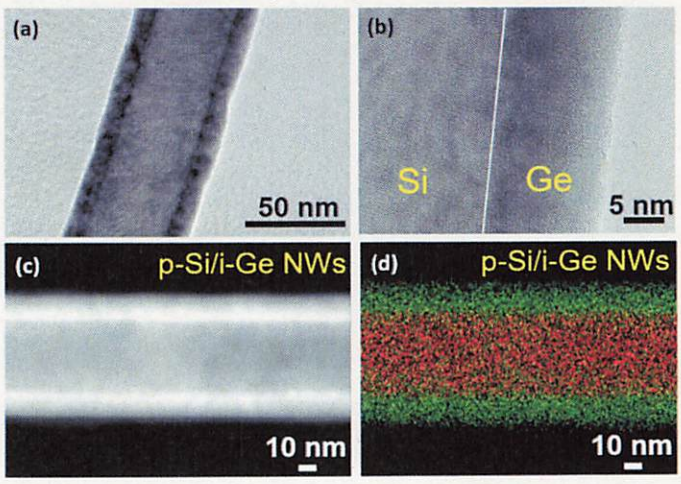

Figure 2. (a) Low and (b) high resolution TEM images of p-Si/i-Ge core-shell NW with a shell growth of 60 s. The scale bar of (a) and (b) are 50 nm and 5 nm, respectively. (c) STEM image and (d) EDX mapping with the scale bars of 10 nm. The red color and green colors are Si and Ge, respectively.

EDX mapping of p-Si/i-Ge core-shell NWs are shown in Figure 2. The low-resolution image in Figure 2 (a) shows a uniform structure along the NW growth axis. Clear lattice fringes are observed in the high-resolution image, as shown in Figure 2 (b), showing that the NW has good crystallinity. The i-Ge has a single crystal structure. From the STEM and EDX mapping images, in Figures 2 (c) and (d), the p-Si/i-Ge core-shell NWs show a clear interface without significant intermixing between the Si core and Ge shell layers, demonstrating the formation of a sharp interface.

Figure 3 shows the optical phonon peaks observed by Raman spectroscopy for the p-Si/i-Ge core-shell NWs. The comparisons of B_2H_6 doping gases fluxes from 0.1 sccm to 0.5 sccm are shown in Figures 3 (a) and (b). The peaks observed at around 300 cm^{-1} and 520 cm^{-1} correspond to the Ge and Si optical phonon peaks, respectively. Asymmetric broadening of the Si optical phonon peaks was observed with increasing B doping. This is due to the Fano effect caused by the interference between discrete optical phonons and the continuum of interband electron and hole excitations in degenerately doped NWs.[10,11] The same phenomenon can be detected in Ge optical phonon peaks, which can also be explained by the Fano effect induced hole gas accumulation in the i-Ge region. To confirm this, the out-diffusion of B atoms from the p-Si core to i-Ge shell layers was investigated. The diffusion of B atoms easily occurs if intermixing occured at the interface between the Si and Ge regions, leading to the SiGe optical phonon peak at around 400 cm^{-1} in the Raman spectrum. No SiGe optical phonon peaks were detected, indicating that intermixing is negligible. These results prove hole gas accumulation in the i-Ge region from the B doped p-Si region. A downshift of the Si optical phonon peak compared to bulk Si was also observed. This is due to tensile stress and B doping. Because the lattice constant of Ge is larger than that of Si, the formation of Ge shell layer induces tensile stress in the Si layer. In addition, the downshift can be also explained by the Fano effect due to impurity doping. The values of the Ge optical phonon peaks are higher than those of bulk Ge, showing the formation of compressive stress in core-shell NWs. The Ge peaks move to a lower wavenumber at higher B_2H_6 gas flux, due to increased hole gas accumulation. The Raman spectra of bulk-Ge, i-Ge NWs, i-Si/i-Ge core-shell NWs, and p-Si/i-Ge core-shell NWs are compared as shown in Figure 3 (c). The peak of i-Ge NWs shifted to a lower wavenumber compared to bulk Ge, due to the phonon confinement. The i-Si/i-Ge and p-Si/i-Ge core-shell NWs peaks show upshifted compared to the value of i-Ge NWs due to compressive stress. The peak of p-Si/i-Ge NWs shows a slight shift to low wavenumber due to hole gas accumulation in the i-Ge region.

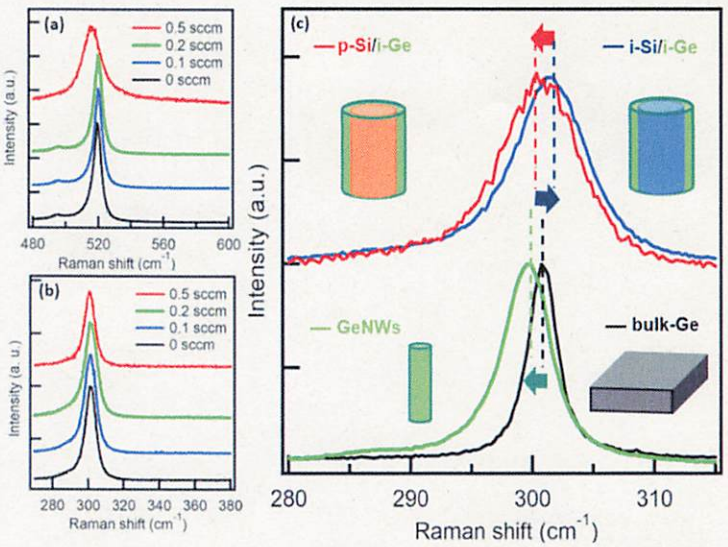

Figure 3. Raman spectra of p-Si/i-Ge core-shell NWs grown with B_2H_6 fluxes from 0 sccm to 0.5 sccm observed for (a) Si optical phonon peaks and (b) Ge optical phonon peaks. (c) Ge optical phonon peaks compared to bulk-Ge, i-Ge NWs, i-Si/i-Ge core-shell NWs, and p-Si-i-Ge core-shell NWs.

These results show that carrier transport region can be separated from the doping region (p-Si) by fabricating core-shell structure, which can provide an opportunity for next generation high mobility devices.

2. Formation of vertical and catalyst-free p-Si/i-Ge core-shell NWs by using top-down method

Although Si/Ge core-shell NWs exhibit the outstanding ability to suppress impurity scattering and improve carrier mobility in future devices, the NW growth requires a metal catalyst such as Au nanoparticles. Au atoms easily induce deep energy levels into the Si and Ge bandgaps, acting as recombination centers of carriers. This will reduce the electrical properties of NWs. In addition, the diffusion of Au atoms from the catalyst to the sidewall of the NWs also needs to be considered at high growth temperatures. Controlling the orientation and alignment for NWs is also a problem in VLS growth. Therefore, a catalyst-free method with good alignment control is necessary for realizing future NW devices.[2] Here, we use a top-down method based on nanoimprint lithography (NIL) to fabricate p-Si core NW arrays, which can effectively avoid metal catalyst contamination and produce vertically aligned NWs. Subsequently, p-Si/i-Ge core-shell NW arrays and p-Si/i-Ge/p-Si core-double shell NW arrays were formed and characterized.

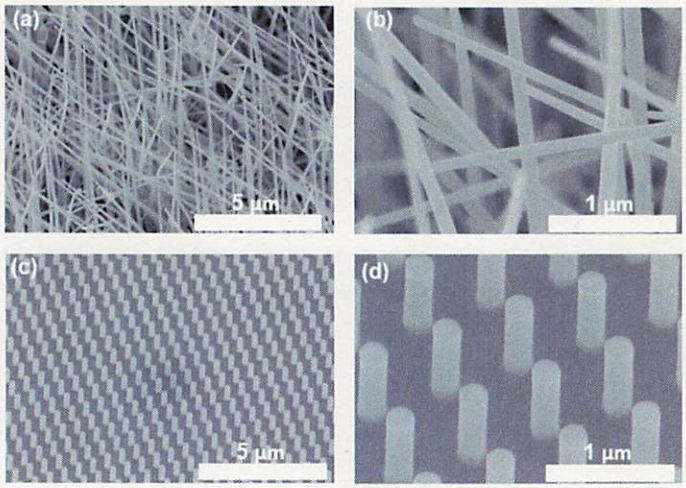

Figure 4. SEM images of Si NWs formed by (a), (b) bottom-up method, (c), (d) top-down method.

Figure 4 shows the compassion of NWs that were formed by the bottom-up and top-down method. In Figures 4 (a) and (b), Si NWs based on the bottom-up method grown by CVD show high density and random growth directions. The length of the NWs depends on the gas flux rate and growth time. In contrast, the Si NWs based on top-down method by using NIL show uniform and vertical structure, as shown in Figures 4 (c) and (d), which will be beneficial for integration with electronic devices. The NIL process includes UV-imprint lithography, lift-off, and Bosch etching using SF_6 and C_4F_8 plasma.[12,13] The diameter of p-Si is around 200 nm. To remove surface defects and control the diameter of NW arrays, the chemical etching and thermal oxidation were performed. The morphology and size of NWs were measured by SEM as shown in Figure 5. Chemical posish etching (CPE) solutions include hydrofluoric acid (HF), nitric acid (HNO_3), acetic acid (CH_3COOH), and deionized (DI) water. The

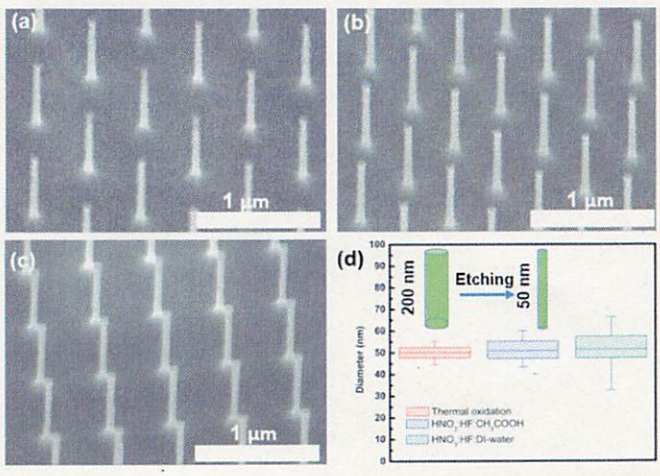

Figure 5. Si nanoarrays with the following conditions (a) HNO_3/HF/DI (50:1:20) etching, (b) HNO_3/HF/DI (400:1:20) etching, (c) thermal oxidation, (d) Si NW arrays diameter distribution.

thermal oxidation process involves forming a SiO_2 layer by O_2 annealing and subsequently HF etching the layer. The diameter of p-Si NWs is significantly reduced by CPE solutions while the roughness of surface increases as shown in Figures 5 (a) and (b). This can be explained by surface damage affecting the etching rate, resulting in an inhomogeneous etching. On the other hand, the thermal oxidation method reduces NW diameter and maintains a smooth surface, as shown in Figure 5 (c). The NW diameter distribution is shown in Figure 5 (d). The results of two CPE solutions show that there is a wide distribution of diameters for the HNO_3/HF/DI water solution and HNO_3/HF/CH_3COOH solution, corresponding to -40% to +30% and -25% to 20%, respectively, demonstrating that the CPE method leads to high surface roughness. On the other hand, the result of the thermal oxidation method shows a smaller distribution ($\pm$10%) than those by the CPE method, demonstrating that the thermal oxidation process is more suitable for reducing the diameter and maintaining a smooth NW surface. Various thicknesses of i-Ge shell layers were formed on p-Si core NWs to fabricate p-Si/i-Ge core-shell NW arrays. The crystallinity and stain in core-shell NWs were characterized by Raman spectroscopy and XRD measurements. The hole gas concentration in the i-Ge shell can be enhanced at longer shell growth time, resulting in an enhancement of the Fano effect. The lattice constants of Si and Ge are calculated using Bragg's Law, showing the relaxation of compressive stress of the Ge shell with increasing thickness. To further increase hole gas accumulation in the Ge region, a catalyst-free p-Si/i-Ge/p-Si NW array was fabricated. The outermost p-Si layer was formed by SiH_4(19 sccm) and B_2H_6 (0.2 sccm) gases at 700 °C. p-Si shell layers with different growth times of 30, 60, 80, and 100 s were made. Figure 6 shows that Ge optical

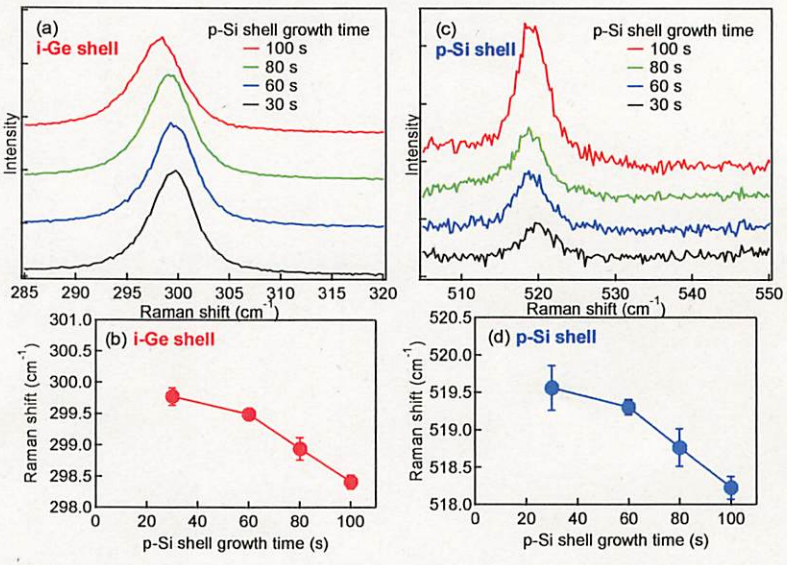

Figure 6. Raman spectra of p-Si/i-Ge/p-Si core-double shell NWs observed for various outer most p-Si shell growth times: (a) Ge and (c) Si optical phonon peaks and (b) Ge and (d) Si optical phonon peaks as a function of shell growth time.

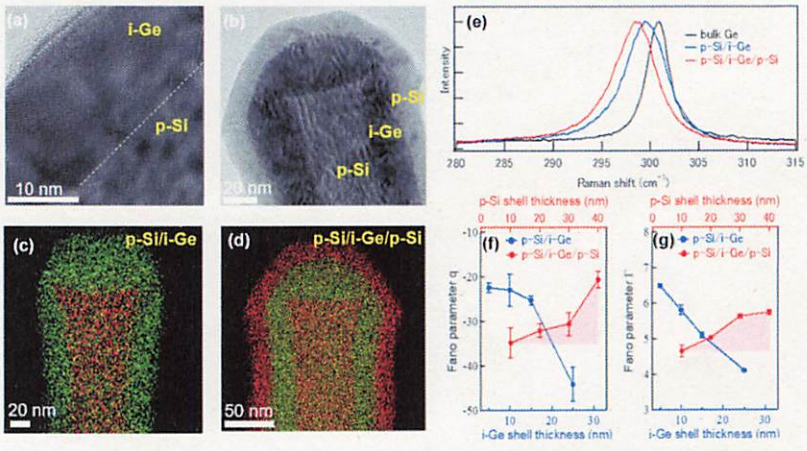

Figure 7. TEM and EDX mapping observed for (a) and (c) p-Si/i-Ge core-shell NWs, (c) and (d) p-Si/i-Ge/p-Si core-double shell NWs, (e) Ge optical phonon peaks observed for bulk-Ge, p-Si/i-Ge core-shell, and p-Si/i-Ge/p-Si core-double shell NWs, (f) q and (g) Γ observed for core-shell and core-double shell NWs.

phonon peaks have a downshift to lower wavenumbers and asymmetric broadening by increasing the outermost Si shell growth time. This is due to the increase in the hole gas accumulation in the Ge region, as both sides of the p-Si layers induce holes in the Ge region. The intensity of the Si optical phonon peaks increased with increasing shell growth time. The Si optical phonon peaks also showed downshifting when the p-Si shell growth time increased. This is also due to the Fano effect caused by B doping in the p-Si shell layers. In Figure 7, the TEM images and EDX mapping show the formations of p-Si/i-Ge core-shell NWs and p-Si/i-Ge/p-Si core-double shell NWs. The Ge shell layer clearly shows lattice fringes, indicating that i-Ge layer is single-crystalline. Figure 7 (e) shows a comparison of Ge optical phonon peaks observed for bulk Ge, p-Si/i-Ge core-shell NWs and p-Si/i-Ge/p-Si core-double shell NWs. The downshift and asymmetrical broadening could be observed in p-Si/i-Ge core-shell NWs, due to hole gas accumulation. In addition, the phenomenon was more obvious for the p-Si/i-Ge/p-Si core-double shell NWs, demonstrating enhancement in hole gas accumulation induced by the p-Si layers. To estimate the hole gas density in the i-Ge region, the Fano equation was used to fit the Ge optical phonon peaks observed for p-Si/i-Ge core-shell NWs and p-Si/i-Ge/p-Si core-double shell NWs. The equation is as follows:

$$I = I_0 \frac{(q+\varepsilon)^2}{1+\varepsilon^2}$$

where ω, q, and I_0 are wavenumber, asymmetry factor, and prefactor, respectively. ε is defined as $(\omega - \omega_p)/\Gamma$ where ω_p and Γ are the phonon wavenumber and line width, respectively. In Figures 7 (f) and (g), the value of q and Γ decreased with increasing i-Ge shell growth time for p-Si/i-Ge core-shell NWs, which can be attributed to the reduction in hole gas density caused by the increase in the thickness of i-Ge shell layers. However, both values increased for p-Si/i-Ge/p-Si core-double shell NWs with increasing outermost p-Si shell layers thickness. This is due to an increase in hole gas accumulation in the i-Ge shell region by the formation of the double p-Si shell layers, showing that hole gas can be effectively increased by constructing core-double shell structure.

3. Interfacial Intermixing of Ge/Si Core–Shell Nanowires by Thermal Annealing

Thermal annealing is a crucial process for optimizing electrical properties in electronic devices because it affects the crystallinity, dopant activation, and interface intermixing. In this part, the change in structure and thermal stability of i-Ge/p-Si core-shell NWs was investigated, showing the effects of temperature and pressure on the NWs during post-annealing. Figure 8 shows SEM images and Raman spectra for i-Ge/p-Si core-shell NWs under different annealing temperatures. Annealing was carried out between 500 and 900 °C for 1 min. The pressure condition was set to 100 Pa. Annealing below 800 °C has little effect on the surface morphology of the

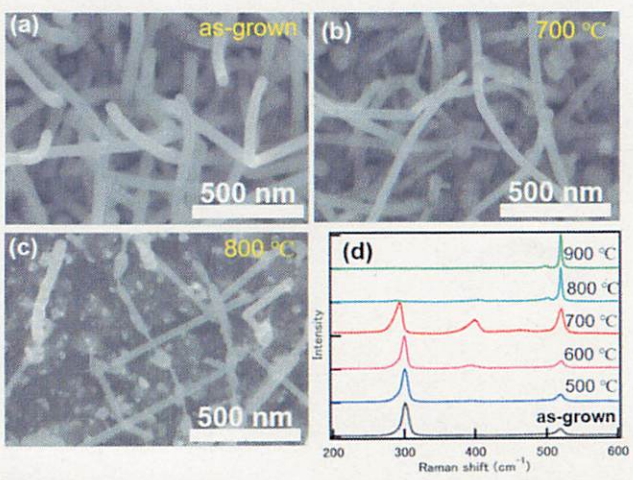

Figure 8. SEM images of i-Ge/p-Si NWs observed for (a) as-grown, samples after RTA AT (b) 700 °C, (c) 800 °C, (d) Raman spectra of i-Ge/p-Si NWs.

NWs. When the temperature increased from 500 to 700 °C, three peaks were observed in the Raman spectra at around 300, 400, and 520 cm^{-1}, corresponding to Ge-Ge, Si-Ge, and Si-Si vibrational optical phonon modes, respectively, as shown in Figure 8 (d). The observation of Si-Ge peaks is due to intermixing at the interface between Ge and Si layers. The Ge-Ge peaks show a downshift to lower wavenumbers, which is due to compressive stress relaxation caused by the intermixing of Ge and Si atoms. The enhancement of the Si-Si peak intensity and its upshift are due to improved crystallinity thanks to the annealing process. To further elucidate the intermixing, the effect of the pressure of the annealing environment was investigated by varying it from 4 to 50 Pa, as shown in Figure 9. The i-Ge/p-Si core-shell NWs didn't show drastic changes at pressures lower than 20 Pa, while the NWs were significantly broken by annealing at a pressure of 50 Pa. This can be attributed to the enhanced bond breaking of Si-Si and Ge-Ge by high-pressure annealing. The Si-Si peaks intensity increased due to the improved crystallinity of the Si shell layers. The Si-Ge peak appeared and the intensity of Ge-Ge peaks reduced with increasing pressure, indicating the intermixing of Si and Ge atoms. Figure 10 (a) shows a comparison of samples annealed at 4 and 6 × 10^{-6} Pa, respectively, showing that low pressure can suppress intermixing, while it can be increased at higher pressure. Figures 10 (b) and (c) show TEM images with EDX mapping with and without treatments. A clear core-shell structure is shown for the as-grown sample, as shown in Figure 10 (b). However, a non-sharp interface between Ge and Si layers can be observed, due to the intermixing of Ge and Si after annealing. These results confirmed that intermixing occurred at the interface

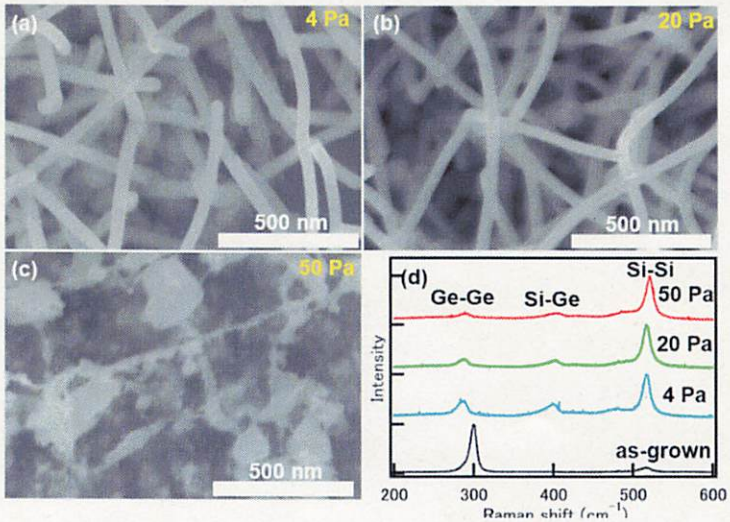

Figure 9. SEM images of i-Ge/p-Si NWs after RTA under N_2 pressure of (a) 4 Pa, (b) 20 Pa, (c) 50 Pa at 800 °C. (d) Raman spectra of i-Ge/p-Si NWs.

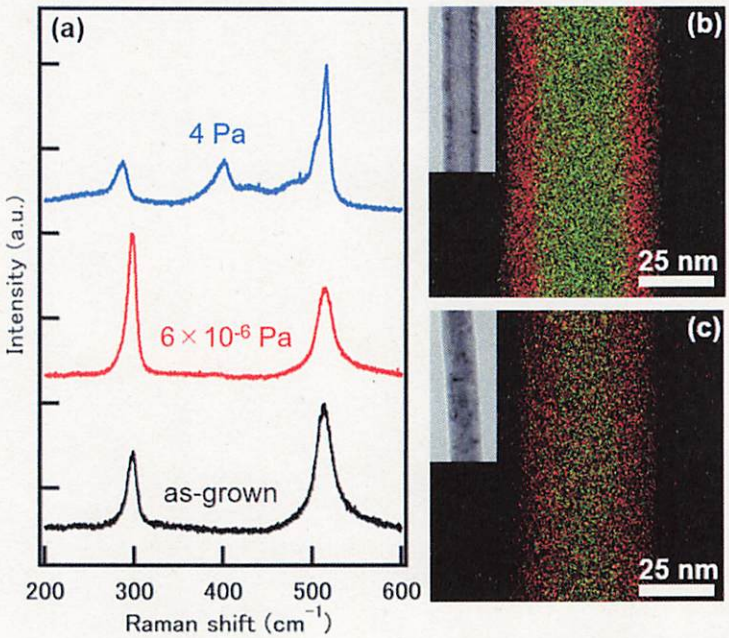

Figure 10. (a) Raman spectra of i-Ge/p-Si NWs observed for as-grown sample, the samples under the pressure of 4 Pa and 6 × 10^{-6} Pa annealing. TEM images and EDX mapping of (b) as-grown sample, (c) annealing sample.

of the core–shell NWs due to the thermal annealing.

4. Formation of SiGe alloy NWs and their impurity doping

$Si_{1-x}Ge_x$ alloy NWs is also an important Si-Ge nanowire structure. The alloy composition can be reproducibly controlled over a wide range of compositions by controlling the SiH_4 and GeH_4 precursors. Impurity doping in $Si_{1-x}Ge_x$ alloy NWs can be used to produce n-type or p-type NWs, showing intriguing potential technological applications. The effects of growth temperature, flow rate of SiH_4 and GeH_4, and B_2H_6 gas doping on $Si_{1-x}Ge_x$ alloy NWs were investigated. Figure 11 shows the schematic and SEM images of the alloy NWs at various growth temperatures. The sample ratio of SiH_4 and GeH_4 was set to 6:1. Uniform alloy NWs were observed when the growth temperature was lower than 520 °C, as shown in Figures 11 (a) and (c). Au catalyst can be observed on the tip of NWs, indicating the NWs were grown by the VLS mechanism. However, a further increase in the growth temperature caused the formation of a tapered NW structure, due to vapor-solid (VS) growth on the sidewalls of the NWs, as shown in Figures 11 (b) and (d).

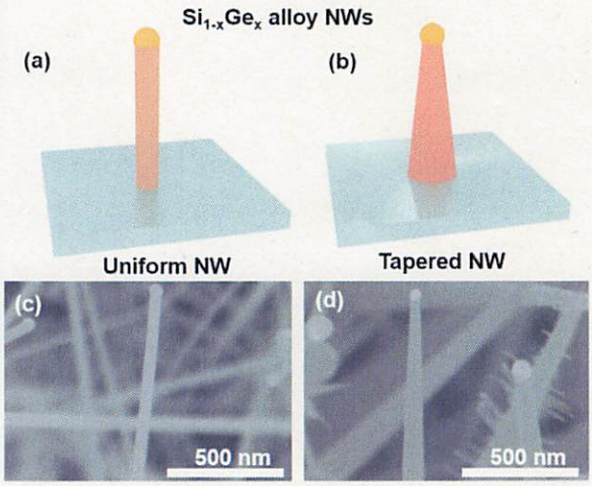

Figure 11. Schematic and SEM images of the $Si_{1-x}Ge_x$ alloy NW (a), (c) uniform and (b), (d) tapered structure.

TEM measurements were used to evaluate the crystallinity of $Si_{1-x}Ge_x$ alloy NWs, as shown in Figure 12. The growth temperature was 420 °C. The alloy NWs are single crystalline. The EDX mapping and line-scan profile revealed that Si and Ge atoms were uniformly distributed in $Si_{1-x}Ge_x$ alloy NWs, as shown in Figures 12 (c) and (d). The compositions of Si and Ge were 40 % and 60 %, respectively. In addition, the sample at the growth temperature of 375 °C showed 25 % and 75 % for Si and Ge, respectively, showing that the Ge concentration in alloy NWs increased at lower growth temperatures. The composition can be controlled not only by changing the growth temperature but by modulating the ratios of SiH_4 and GeH_4 precursor gases. Ratios of SiH_4 and GeH_4 from 2:1 to 10:1 were investigated. The growth temperature was set to 475 °C. The tapered NW structure was obtained for ratios from 2:1 to 4:1, while the sample formed by the ratio from 6:1 to 10:1 were untapered. Figure 13 shows Raman and XRD measurements for different ratios of SiH_4 and GeH_4. The Raman peaks were dominated at about 300, 400, and 500 cm^{-1}, corresponding to

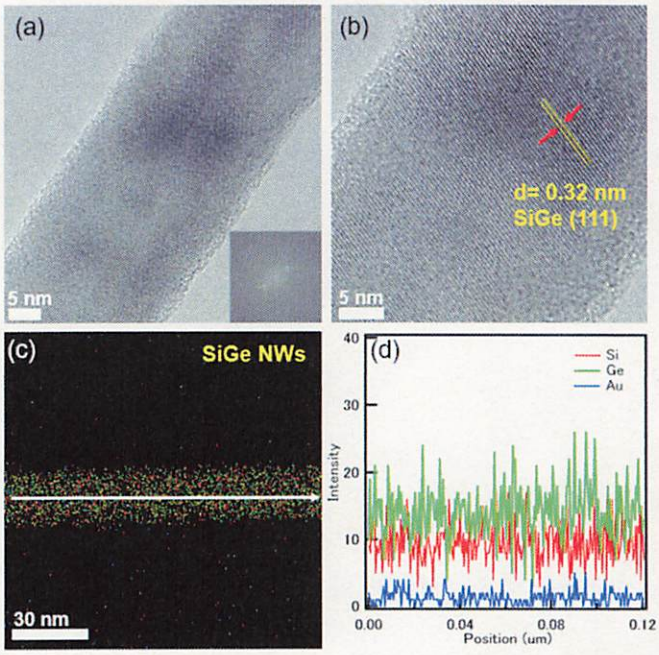

Figure 12. (a) and (b) high resolution TEM images of $Si_{1-x}Ge_x$ alloy NWs. (Growth condition: SiH_4:GeH_4 = 10:1.7; temperature: 420 °C). (c) EDX mapping, (d) line scan of the NWs.

the Ge-Ge, Si-Ge, Si-Si vibrational modes, respectively, as shown in Figure 13 (a). In Figures 13 (a) and (c-e), the several weak peaks between 420 and 460 cm^{-1} were also observed, which could be interpreted as local Si-Si vibration in the presence of neighboring Ge atoms. The Si-Si mode shifted towards higher frequency and were also narrower and more symmetric compared to lower ratios of SiH_4 and GeH_4, which could be attributed to a change in composition of Si and Ge.[14] The linewidth and asymmetric shapes of Si-Ge and Ge-Ge peaks are also important for estimating the composition of the alloy NWs.[14] The intensity of Ge-Ge peaks decreased with an increasing ratio of SiH_4 to GeH_4. Asymmetric broadening to lower wavenumbers was observed, implying that the Ge atoms are gradually being replaced by Si atoms to form a Si-Si local structure because of excess Si atoms. The Si-Ge mode exhibited a shift towards higher wavenumber that could be attributed to the decrease of Ge atoms surrounded by the vibrations of Si atoms at Si-Ge local modes.[15] The process is probably that the lighter Si atoms replaced the heavier Ge atoms. In Figures 13 (b) and (f), XRD measurements were used to determine the lattice constants and strain as a function of alloy composition. The $Si_{1-x}Ge_x$ (111) reflection was highlighted for the various ratios of alloy NWs. As the ratio of SiH_4 to GeH_4 increased, a clear shift in the (111) peaks was observed from bulk Ge (27.28°) to bulk Si (28.45°). Pure Si and Ge peaks were not found in the alloy NWs, demonstrating that alloy NWs were formed. The average lattice constants were calculated using Vegard's law, showing a decrease with increasing Si gas flux, as shown in Figure 13 (f) due to the increasing Si content in alloy NWs.

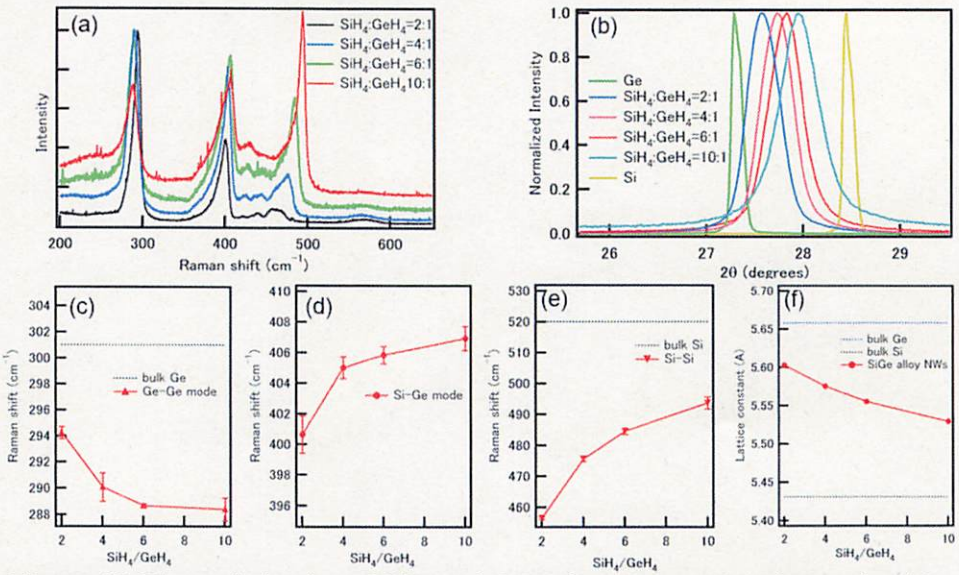

Figure 13. The varied ratios of SiH_4 and GeH_4 from 2:1 to 10:1 observed at (a) Raman spectra, (b) XRD; Raman peaks positions as a function of (c) Ge-Ge mode, (d) Si-Ge mode, (e) Si-Si mode; (f) lattice constants as a function of the varied ratios.

Conclusion

The growth and characterization of Si/Ge core-shell NWs and their alloy NWs for future high-performance transistors were investigated in this thesis. The first chapter addresses the growth of p-Si/i-Ge core-shell NWs using the bottom-up method of CVD, which can produce materials with suppressed impurity scattering and a sharp interface between the Si and Ge layers. Hole gas accumulation can be detected in the Ge region when selective doping was performed in the Si region, demonstrating that the carrier transport region can be separated from impurity doped region by constructing the core-shell NWs. In the second chapter, the catalyst-free formation of p-Si/i-Ge core-shell and p-Si/i-Ge/p-Si core-double shell NWs was performed using a top-

down method as this method can prevent metal catalyst contamination. Vertically aligned NW arrays were fabricated, providing a possibility for future vertical high-speed transistors. Hole gas concentration can be effectively increased by forming p-Si/i-Ge/p-Si core-double shell NWs. In the third chapter, the post-annealing treatment of Ge/Si core-shell NWs was investigated. The crystallinity of Si and Ge can be improved after annealing. Intermixing between Si and Ge region was formed by using high-temperature and high-pressure treatments. In the last chapter, $Si_{1-x}Ge_x$ alloy NWs were synthesized. The composition and crystallinity of alloy NWs were investigated by controlling the parameters of growth temperature, gas flow ratio and boron doping. The results clearly showed the VS growth also occurred at higher growth temperatures and higher ratios of SiH_4 and GeH_4. Raman spectra and XRD measurements were used to investigate the composition and strain between Si and Ge. Boron doping was performed, showing Ge content increased with increasing B doping.

References

(1) Thompson, S. E.; Parthasarathy, S. Moore's Law: The Future of Si Microelectronics. *Mater. Today* **2006**, *9*, 20–25.

(2) Zhang, X.; Jevasuwan, W.; Sugimoto, Y.; Fukata, N. Controlling Catalyst-Free Formation and Hole Gas Accumulation by Fabricating Si/Ge Core–Shell and Si/Ge/Si Core–Double Shell Nanowires. *ACS Nano* **2019**, acsnano.9b06821.

(3) Fukata, N.; Yu, M.; Jevasuwan, W.; Takei, T.; Bando, Y.; Wu, W.; Wang, Z. L. Clear Experimental Demonstration of Hole Gas Accumulation in Ge/Si Core-Shell Nanowires. *ACS Nano* **2015**, *9*, 12182–12188.

(4) Cui, Y.; Lieber, C. M. Functional Nanoscale Electronic Devices Assembled Using Silicon Nanowire Building Blocks. *Science.* **2001**, *291*, 851–853.

(5) Zhang, X.; Jevasuwan, W.; Pradel, K. C.; Subramani, T.; Takei, T.; Fukata, N. Hole Gas Accumulation in Si/Ge Core–shell and Si/Ge/Si Core–double Shell Nanowires. *Nanoscale* **2018**, *10*, 21062–21068.

(6) Fukata, N.; Sato, K.; Mitome, M.; Bando, Y.; Sekiguchi, T.; Kirkham, M.; Hong, J. Il; Wang, Z. L.; Snyder, R. L. Doping and Raman Characterization of Boron and Phosphorus Atoms in Germanium Nanowires. *ACS Nano* **2010**, *4*, 3807–3816.

(7) Wagner, R. S.; Ellis, W. C. Vapor-Liquid-Solid Mechanism of Single Crystal Growth. *Appl. Phys. Lett.* **1964**, *4*, 89–90.

(8) Fukata, N.; Chen, J.; Sekiguchi, T.; Okada, N.; Murakami, K.; Tsurui, T.; Ito, S. Doping and Hydrogen Passivation of Boron in Silicon Nanowires Synthesized by Laser Ablation. *Appl. Phys. Lett.* **2006**, *89*, 203109.

(9) Fukata, N.; Chen, J.; Sekiguchi, T.; Matsushita, S.; Oshima, T.; Uchida, N.; Murakami, K.; Tsurui, T.; Ito, S. Phosphorus Doping and Hydrogen Passivation of Donors and Defects in Silicon Nanowires Synthesized by Laser Ablation. *Appl. Phys. Lett.* **2007**, *90*, 153117.

(10) Fano, U. Effects of Configuration Interaction on Intensities and Phase Shifts. *Phys. Rev.* **1961**, *124*, 1866–1878.

(11) Fukata, N. Impurity Doping in Silicon Nanowires. *Adv. Mater.* **2009**, *21*, 2829–2832.

(12) Chou, S. Y.; Krauss, P. R.; Renstrom, P. J. Nanoimprint Lithography. *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.* **1996**, *14*, 4129.

(13) Chang, C.; Wang, Y. F.; Kanamori, Y.; Shih, J. J.; Kawai, Y.; Lee, C. K.; Wu, K. C.; Esashi, M. Etching Submicrometer Trenches by Using the Bosch Process and Its Application to the Fabrication of Antireflection Structures. *J. Micromechanics Microengineering* **2005**, *15*, 580–585.

(14) Mooney, P. M.; Dacol, F. H.; Tsang, J. C.; Chu, J. O. Raman Scattering Analysis of Relaxed GexSi1-Xalloy Layers. *Appl. Phys. Lett.* **1993**, *62*, 2069–2071.

(15) Lu, Q.; Adu, K. W.; Gutiérrez, H. R.; Chen, G.; Lew, K. K.; Nimmatoori, P.; Zhang, X.; Dickey, E. C.; Redwing, J. M.; Eklund, P. C. Raman Scattering from Si1-xGex Alloy Nanowires. *J. Phys. Chem. C* **2008**, *112*, 3209–3215.