Performance Improvement of Discontinuous Current Mode Grid-Tied Inverters with Model-Based Control

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To my parents and family

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Abstract

The photovoltaic (PV) system has gained more and more attentions over last decades. With the continuous development of residential PV markets, low-power grid-tied inverters are being applied as micro-inverters or AC modules for photovoltaic applications. From the point of view of cost reduction and easy fabrication, minimization of the size volume of grid-connected inductor plays an important role For these low-power grid-tied inverters, since the they usually occupy a lot of spaces in the converter and being relatively costly.

Generally, the volume of grid-connected inductors can be reduced by increasing switching frequency. However, the current controls can become difficult under low inductance conditions if the converter is designed to operate in conventional continuous current mode (CCM). For this reason, the volume reduction can be limited even with increased switching frequency in CCM. In order to address this problem, the converter can be designed to operate in discontinuous current mode (DCM). Conventionally, the current control is based on feedback, however, the detection of inductor current can be a challenge in DCM, particularly under high frequency operations. A model-based control, which is based on the feed-forward, can be advantageous and suitable for DCM inverters designed with high frequency. The detection of high frequency DCM current is no longer required with the model-based control. The DCM can be a promising design for the purpose of further reduction of inductor volume for a low-power grid-tied inverter.

However, the current distortions can be generated if an imperfect model is used, and they become severer along with the increasing of switching frequencies. The distortions cannot be

eliminated under the feed-forward control. This shortcoming makes the high frequency DCM impractical for the grid-tied inverter applications since the harmonics should be restricted to meet the grid requirements. Further more, the high peak inductor current in DCM can result in higher conduction losses in comparison with that in a CCM grid-tied inverter. To reduce the conduction losses, devices with low on-state resistance are preferred, however, the trade-off relationship between the on-state resistance and parasitic output capacitance of devices limits the uses of such devices, because the turn-on losses and total harmonic distortion can be even higher. For a DCM grid-tied inverter designed with conventional control methods, the switching frequency cannot be selected to a very high value for a given device. Consequently, the volume reduction of inductors can be limited even with the DCM and WBG devices.

This dissertation discusses the control of a high frequency DCM grid-tied inverter to achieve low harmonic distortion. The problems in terms of current control and harmonic distortions for the DCM grid-tied inverter with high frequency design are studied and discusses. Several control and modulation methods, which aim at realizing the reduction of harmonic distortions, peak current reduction and soft-switching, are proposed to address the problems.

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Chapter 1

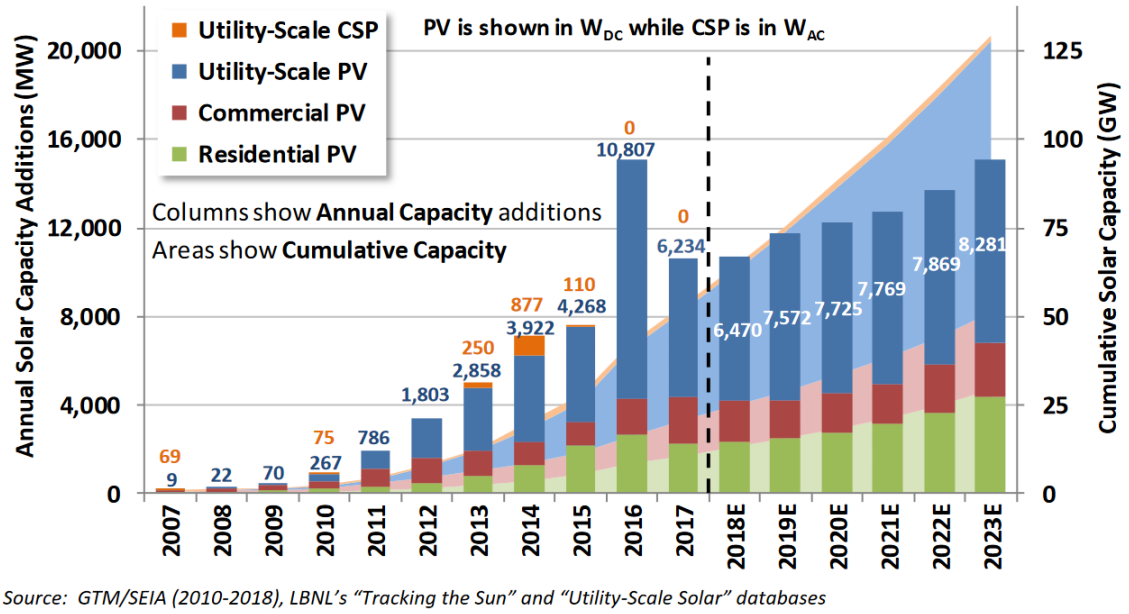
Introduction

1.1 Background

As one of the renewable energies, sunlight has gaining more and more visibility with the increased power demands in the world. For photovoltaic (PV) applications, grid-tied inverters are used as interfaces between solar panels and electrical grids. The grid-tied inverters convert DC power generated from solar cells into AC power, and feed it into the electrical grid. Since the inverters are connected to the grids, harmonic standards given by the grids, such as EN61000-3-2 [1] or IEEE1547 [2], must be obeyed. In addition, the grid-tied inverters should also equip other functionalities, such as the ability to detect island situation and perform island operation, the capability of low voltage ride through (LVRT) or the ability to provide reactive power injection [3–5].

Table 1.1 Classification of PV inverters Based on Power level [6]

Rated power	Application	Grid connection
< 10 kW	Residential and small commercial	Single or spilit phase
10-100 kW	Small commercial	Three-phase
100-250 kW	Large commercial	Three-phase
250-1000 kW	Utility	Three-phase



Source: GTM/SEIA (2010-2018), LBNL's "Tracking the Sun" and "Utility-Scale Solar" databases

Fig. 1.1 Historical and projected PV and CSP capacity by sector in the United States [7].

Generally, the power level of PV inverters can be classified into residential, commercial and utility. Table 1.1 shows the classified power levels of PV inverters and their corresponding applications. For residential and small commercial applications, the power rating of inverters are relatively low, while inverters power levels are relatively high for large commercial or utility applications. Fig. 1.1 shows a historical capacity of concentrating solar-thermal power (CSP), utility-scale PV, commercial-scale PV and residential-scale PV in United States [7]. Although the utility-scale PV has dominated the market in the last decade, a continuous growth of market in residential-scale PV applications can be observed; and the market of residential PV is approximated to increase further in the future.

The topology of utility-scale and commercial-scale PV systems are usually based on a centralized type [3–5]. The PV solar panels are connected in series to form a string with this type of inverter, and these strings are connected in parallel to provide sufficient high power levels, as shown in the left plot of Fig. 1.2. However, several issues, such as high voltage in the DC cables, mismatch losses and string diodes losses can degrade the performance of inverter in terms of safety problems and efficiencies. In addition, the non-flexible design of

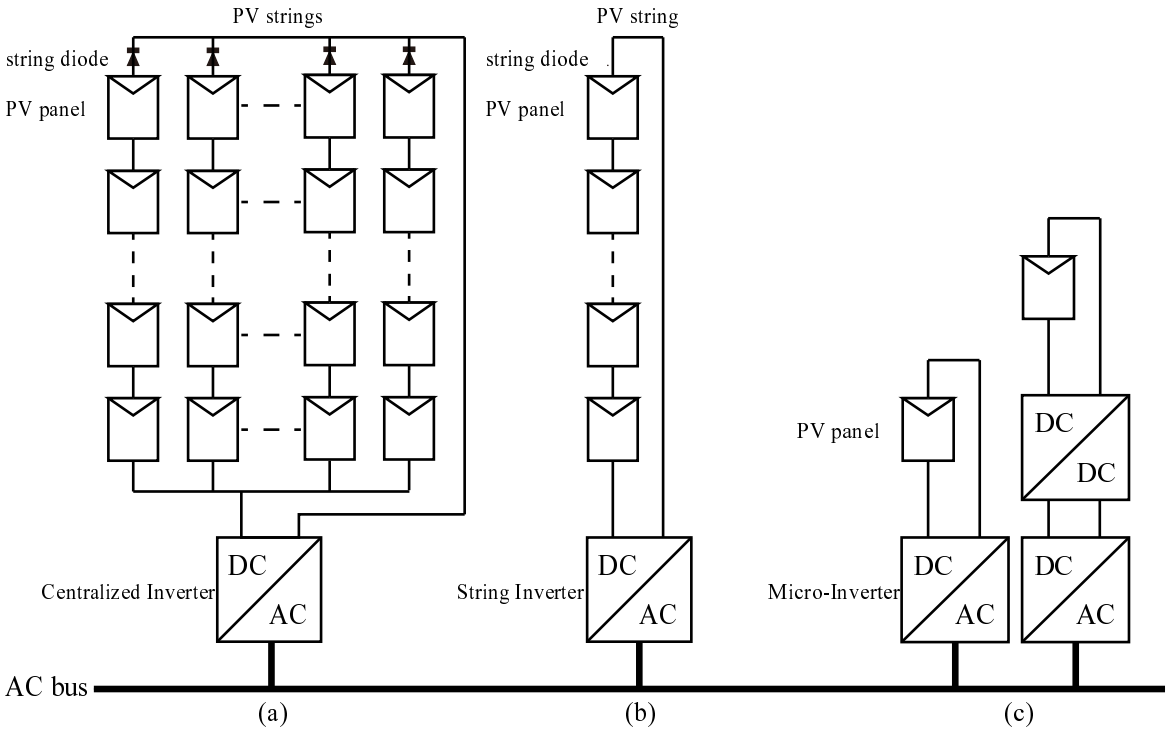


Fig. 1.2 PV inverter system with (a)Centralized type, (b)String type and (c)AC-module type.

this type of inverter, where the benefits of mass production could not be reached, can be the limitation [3].

For residential PV inverters, the power rating is relatively low (in kilowatt ranges) in comparison with the utility and commercial-scale PV systems. A reduced power version of centralized inverter, which is referred to as string inverter, is a popular solution for the residential PV system [8–10]. The topology of a string inverter system is shown in the middle plot of Fig. 1.2. A single string formed by several PV panels connected in series is connected to a grid-tied inverter. The losses from string diodes can be avoided and the maximum power point tracking (MPPT) can be performed separately for each string. Therefore, relatively high efficiencies can be achieved with this kind of string type inverter.

In recent years, a new concept, which is referred to as AC-module or micro-inverter, has been proposed and gained more and more attentions in academic researches [11–20]. Each PV panel is connected with a low power grid-tied inverter in this type of PV system,

as shown in the right plot of Fig. 1.2. It allows person who has no knowledge of electrical installations to use this kind of “plug-and-play" device. The mismatch losses can be removed and the maximum power point tracking (MPPT) can be optimized individually. However, the price per watt of micro-inverters can be higher than that of centralized and string type inverters. Consequently, this type of inverter intends to be mass produced in order to reduce the cost per watt. The micro-inverter can be considered as a good candidate for residential PV system from the point of views of safety, easy installation and relatively low retail costs in comparison with other twos. In the dissertation, the low-power grid-tied inverters, such as the micro-inverters, is considered as the research target.

Generally, the micro-inverters can be classified into single-stage and multi-stage topologies [21]. The single-stage micro-inverters usually compose of a single or interleaved flyback converter together with an unfolder [22–36]. A rectified AC current is generated in the flyback converter, and it is converted to AC current through the unfolder. In the multi-stage micro-inverters, a DC/DC converter is required to boost the low voltage output from the PV panel and perform MPPT; and the DC/AC converter injects the AC current into electrical grid [37–41]. The DC/AC stage is conventionally designed based on voltage source converter (VSC). Although various topologies has been proposed [42–45], such as HERIC, H5 or H6 inverter, the H-bridge topology is still considered as the most common topology for the DC/AC stage due to its simplicity and less components being required. In this dissertation, the research of DC/AC stage is focused on and the single-phase H-bridge is considered as the topology.

1.2 Impact of Wide Bandgap Devices

The emergence development of wide-bandgap (WBG) semiconductor device technologies have brought a huge impact on power converter designs [46]. The WBG devices, such as silicon carbide (SiC) MOSFETs, feature high breakdown electric field, low specific on-

resistance, fast switching speed and high capability of junction temperature in comparison with conventional Silicon (Si) devices [47, 48]. For a given chip size, lower conduction on-resistance can be realized owing to the higher bandgap therefore increased critical breakdown electric field. For the same on-resistance, a reduced chip size therefore smaller parasitic capacitance can be achieved. High temperature tolerance, high switching frequency operation with relatively low switching losses become possible with WBG devices therefore a volume reduction of heat sink can be achieved. In comparison with power converters designed with conventional silicon insulated gate bipolar transistor (IGBT) devices, the performance of converter including power density and efficiency can be improved by adopting SiC-MOSFETs with the design for much higher switching frequency [49].

Although high switching frequency can also be achieved by adopting Si-MOSFETs and Si super-junction (SJ) MOSFETs, the poor reverse recovery characteristic can result in undesired switching losses. The reverse recovery problem can be mitigate by adding a parallel connected Schottky barrier diode (SBD). The switching losses, however, do not necessarily reduced due to the increased total parasitic capacitance [50]. On the other hand, SiC-MOSFETs or GaN-HEMTs exhibit much better reverse recovery characteristics than that of Si-MOSFETs and Si-SJ-MOSFETs. It has been reported that the total switching losses of some SiC-MOSFETs without applying SBD does not exceed the losses with SBD even at 150°C [48, 50]. With the superior performance of SiC-MOSFETs, the elimination of SBD can be achieved and that leads to lower cost and higher power density of power converters.

1.3 Volume Distribution of Grid-Tied Inverters

In the past decades, researches on low-power inverters have been seldom reported because the power rating of inverters are usually high, until the concept of AC modules for PV application is proposed. On the other hand, low-power AC/DC converters including active factor correction (PFC) converters have been widely studied over the last decades [51].

Therefore, some design concepts used in the AC/DC converters or PFC converters can be also applied to the design of low-power inverters.

It is similar with low-power PFC converters, low cost, small size and light weight are also preferred for low-power grid-tied inverters. In order to realize an inverter with these features, it is of importance to reduce the size and volume of components which take large space in the inverter. Generally, the heat dissipation components, DC-link capacitors and grid-connected inductors can occupy lots of space particularly in low power grid-tied inverters. The volume of heat sink can be reduced by adopting semiconductor devices with high temperature tolerance; or by reducing power losses generated from the semiconductor devices. In order to reduce the DC-link capacitors, electrolytic capacitors are usually used. However, the electrolytic capacitors have the problem of limited lifetime. For this reason, film capacitors are preferred rather than electrolytic capacitors. However, the film capacitors also have the problem of lower energy density, which can result in large volumes. In order to address this issue, the active power decoupling techniques can be a good solution [52]. By applying the active power decoupling techniques to the grid-tied inverter, the DC-link capacitor can be reduced. On the other hand, the minimization of grid-connected inductors can also be considered as one of the key techniques to achieve high power density. However, some difficulties with respect to the current control can be obtained when a reduced grid-connected inductor is applied.

1.4 Design of Grid-Tied Inverters

In conventional designs, the inverter is operated in continuous current mode (CCM). A relatively high inductance is usually selected for the grid-connecting inductor to achieve an acceptable level of ripples in the output current, and that results in a large volume of the inductor. In order to reduce the inductance and achieve volume reduction of the grid-connected inductor, high switching frequency is preferred. This can be achieved by adopting

the WBG devices, such as SiC-MOSFETs or GaN-HEMTs. Generally, linear control with proportional-integral (PI) controller is usually applied to CCM grid-tied inverters to regulate the inductor current [53]. However, the current control that based on error-based feedback can become highly difficult under extremely low inductance condition, because the increased disturbance response gain [54, 55]. For instance, even small changes on the inverter output voltage can cause large current ripples. The output current can be distorted under such low inductance. Consequently, the inductance cannot be reduced to the value which is determined by the ripple limitation even with higher switching frequency. The difficulty related to the current control can be a limitation of further volume reduction of inductor in the CCM grid-tied inverter. To remove this limitation and achieve further reduction of the grid-connected inductors, the boundary conduction mode (BCM) or discontinuous current mode (DCM) can be alternative solutions. BCM or DCM is a popular designs in PFC converter applications [51, 56], and the design concept can also be applied to the low-power grid-tied inverters. The inductance can be reduced further with BCM or DCM design due to the different control strategies.

The current control of BCM is generally based on hysteresis control [57–60] or model-based control [61–63]. The detection of inductor current being equal to a given reference value or zero is usually required to determine the timings of turn-on and turn-off in BCM. However, the detection can be sensitive to the switching noises [64]. In addition, the overshoot of inductor current can also be caused by the propagation delay of control [65]. Further more, the inductor current has a triangular waveform with the switching frequency and therefore contains high-frequency components with high amplitudes. Requiring current sensors with high band-width and low delay can be one drawback of the BCM controls.

On the other hand, another purpose of applying BCM is to realize zero voltage switching (ZVS) for turn-on, which is essentially important for high frequency converters. However, the wide variations of switching frequency can be another drawback. Further more, the range

of switching frequency can be even wider under low power operations. The turn-off and inductor losses can increase significantly, even though the turn-on losses can be minimized by the ZVS. Consequently, the BCM design is also not a suitable solution for high frequency grid-tied inverter.

The current control of DCM can be both feedback and feed-forward. In feedback control, such as linear PI control, the inductor current is required to be sensed. Accurate current information can be obtained only if the sampling frequency is sufficient high in comparison with the switching frequency [66]. However, this kind of sampling can be a challenge for the digital controller, particularly under high switching frequency condition. Consequently, the sampling frequency is generally synchronous with the switching frequency. However, sensors with high band-width and low delay is still required even with this technique, because the inductor current is a triangular shape with large ripples. Further more, the sampling errors, which is caused by the non-linearity of DCM, should be corrected [67]. Consequently, the feedback control also has difficulties with respect to the sensing of inductor current in DCM grid-tied inverters.

As an alternative solution to the feedback control, a model-based control which is based on the feed-forward can also be applied to DCM. It is safe to apply this control strategy to DCM, because the errors can be reset in every switching cycle due to the existence of zero current period. The motivation of applying the feed-forward control is to eliminate the detection of triangular inductor current. This can be advantageous under high frequency condition. With the model-based control, a DCM grid-tied inverter can be operated without conventional feedback current control. On the other hand, the variation of switching frequency has more degree of freedom, and it can be even constant in the DCM. The excessive loss caused by the wide range of switching frequency then can be avoid. Therefore, the DCM can be considered as a good candidate for a low-power grid-tied inverter under high frequency design. In this

dissertation, research of DCM with model-based control is focused on rather than other two design approaches.

1.5 Research Objectives

Conventionally, the model-based control for DCM grid-tied inverter is based on the feed-forward control. One drawback of the feed-forward control is the control errors that in the output current cannot be correct adaptively. Consequently, current distortions, that are caused by the use of an imperfect model, cannot be eliminated by the controller. This problem makes the model-based control sometimes impractical for the grid-tied inverter application, since the harmonics current should fall below the grid standards. For a DCM grid-tied inverter designed with conventional control methods, the switching frequency cannot be selected to a very high value in order to avoid the high distortions. Consequently, the volume reduction of inductors can be limited even with the DCM and WBG devices. On the other hand, the high peak inductor current in DCM can result in higher conduction losses than that in CCM grid-tied inverters. To reduce the conduction losses, devices with low on-state resistance are preferred. However, the parasitic output capacitance of such devices are relatively large due to the increased chip size. The trade-off relationship between the on-state resistance and parasitic capacitance of devices can limit the design possibilities, because the turn-on losses and total harmonic distortion can be even higher. Consequently, the efficiency improvement can also be restricted as long as this problem being exist.

For a DCM grid-tied inverter with model-based control, the problems of current distortion have to be addressed in order to improve the converter performance and make it practical for grid-tied application. The objective of this dissertation is to reduce the harmonic distortion for a DCM grid-tied inverter designed with high frequency operation by using control techniques. The problems in terms of current control and harmonic distortions in the DCM grid-tied inverters are studied and discussed. Several control and modulation methods, which aim at

realizing the reduction of harmonic distortions, peak current reduction and soft-switching, are proposed to address the above problems.

1.6 Overview of This Dissertation

The overview of this dissertation is shown in Fig. 1.3. The dissertation is divided into five chapters. The main focus in this dissertation is control and modulation techniques for DCM grid-tied inverters with model-based control. In Chapter 2, the state-of-the-art of the current control strategies for grid-tied inverters are reviewed. The control strategies for grid-tied inverter with high frequency operation are discussed and compared. It is pointed out that the DCM design with model-based control is a promising and suitable choice for the purpose of realizing high frequency operation. However, the problems, such as current distortions that can be caused by the use of imperfect model, is also discussed for conventional model-based controlled DCM. These problems can be addressed by improved modulation techniques.

In Chapter 3, a hybrid switching scheme and its modulation method are proposed in order to avoid zero-crossing distortion and reduce peak inductor current. The proposed hybrid switching scheme is a combination of the conventional unipolar and bipolar switching. Therefore, it provides higher control degree of freedom in comparison with the conventional ones. The operation model can be both bipolar DCM and unipolar DCM with the proposed hybrid switching. The problem of zero-crossing distortion then can be addressed by operating the converter in bipolar DCM while in unipolar DCM during other switching cycles to reduce the peak inductor current.

In Chapter 4, an improved DCM model and two modulations are proposed to reduce the high-order harmonics for a DCM grid-tied inverter designed with high frequency. The proposed modulations control the length of zero current period that based on the model by two different approaches. Both approaches can achieve the same initial current at turn-on

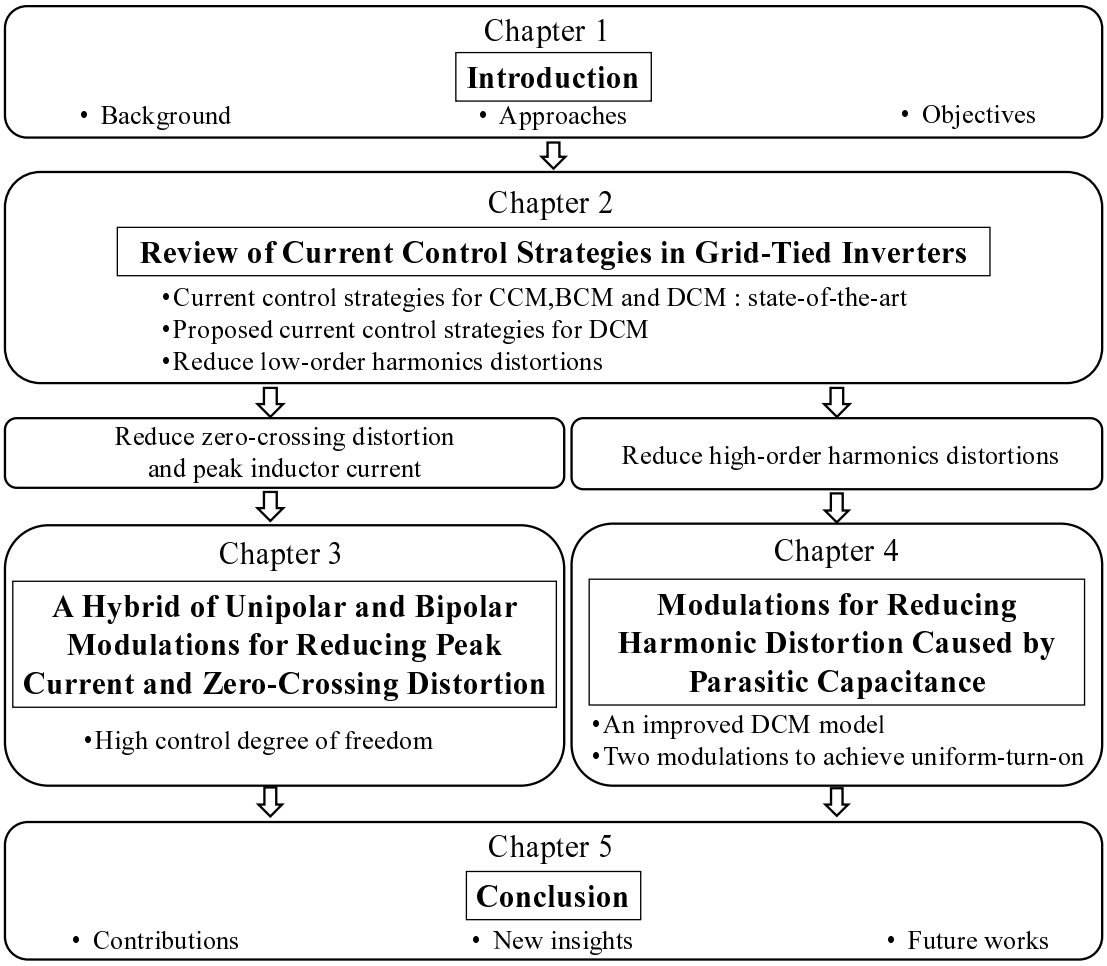


Fig. 1.3 Overview of this dissertation.

without adding any additional components or detection, so that the high-order harmonic distortions can be reduced.

With the proposed control strategies, the problem of current distortions that exists in the DCM grid-tied inverter can be addressed. The trade-off relationship between the switching frequency and parasitic capacitance of switching device can be improved. The converter can be designed with further high frequency; and with lower on-resistance of device being applied. Therefore, the realization of grid-tied inverter with high power density, high efficiency and low harmonic distortion becomes possible. Finally, the summary of this dissertation, new insights and future works are presented in Chapter 5.

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Chapter 2

Review of Current Control Strategies in Grid-Tied Inverters

2.1 Overview of Control Methods in Grid-Tied inverters

In the last decades, control methods of power converters have been researched through numerous studies. Among them, some well established methods have been already applied to the industrials. The current control schemes for power converters and drives are classified into several categories, as discussed in [1]. The current control methods that can be applied to grid-tied inverters are shown in Fig. 2.1. Fundamentally, control loop of a system can be divided into two types, which are known as closed-loop(feedback) and open-loop(feed-forward). For a grid-tied inverter with CCM design, the current controls are usually based on the feedback control. The classic control methods for CCM are the hysteresis control and linear control. In addition to these classical control methods, some modern control techniques, such as sliding-mode control and predictive control, for power converters have also been proposed and gained more and more attentions due to their superior performances.

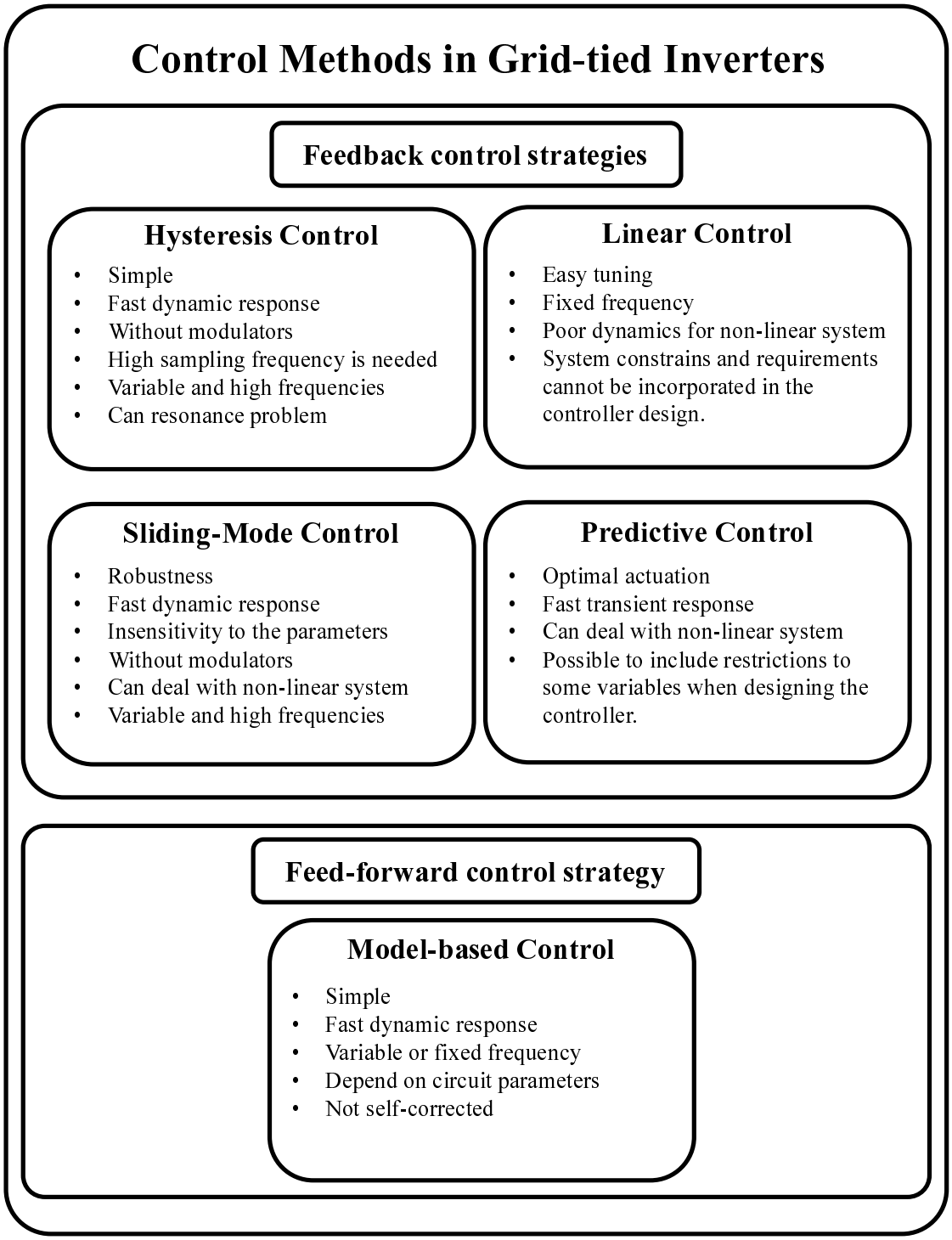

Fig. 2.1 Overview of control strategies in that can be applied to grid-tied inverters.

2.1.1 Hysteresis Control

In hysteresis current control, the current are compared with two references using hysteresis comparators. The switching states are changed when the current reaches the predefined references. The method of hysteresis current control features simple control and implementation, fast dynamic response and no need of modulators. However, high sampling frequency is required. The disadvantage of this kind of control strategy is the variable and high switching frequencies, which are dependent on width of hysteresis, load parameters and operation conditions. Consequently, it is not suitable for low-power converters due to the excessive switching losses [2]. In addition, the variable frequency operation sometimes can also trigger the resonance of the filter.

2.1.2 Linear Control

In linear control, the errors between the actual and reference current is input into a linear controller and the voltage reference is generated by the controller. The non-linear characteristic of converter is then linearized by a modulator, and the control signals are generated by the modulator. The most common strategy of linear control is based on the proportional-integral (PI) controller and pulse width modulation (PWM). The switching frequency can be fixed by using a carrier with constant frequency in the modulator. The design of a PI controller is simple and has been well established in the previous studies. However, this control method has poor dynamics when it is used to control a non-linear system. In addition, some constrains and requirements, such as total harmonic distortion and maximum current, cannot be incorporated in the controller design [3].

2.1.3 Sliding-Mode Control

The sliding-mode control is a non-linear control method that can be used to control a non-linear system [4–7]. The advantages of this kind of control strategy are the strong robustness

to the variation of parameters and fast dynamic response. Recently, the sliding-mode control has also been applied to control the grid-tied inverters [8–12]. Despite of the excellent performance, a problem of the sliding-mode control is the variable and high switching frequency [4]. Therefore, it has the similar problems with the hysteresis control.

2.1.4 Predictive Control

The predictive control uses the model of system to predict the future behavior of control variables. Then the optimal actuation can be obtained in accordance with a predefined optimization criterion [1]. The predictive control can be further classified into hysteresis based control [13], deadbeat control [14, 15], trajectory based control [1] and model predictive control [16]. The advantages of predictive control strategies include simple and intuitive concept, fast dynamic response, easy implementation. It can also be applied to control a non-linear system and it is possible to include restrictions to some variables when designing the controller. However, the high amount of calculations in comparison with the classic control schemes can be a disadvantage.

2.1.5 Model-based Control

Although most of the current control methods is based on the feedback control in grid-tied inverters, the feed-forward control can also be used in some cases. The feed-forward control is based on knowledge about the process in the form of a mathematical model of the process and knowledge about or measurements of the process disturbances [17]. Therefore, it can be considered as a model-based control. The feed-forward can achieve zero control error if a perfect mathematical model is used. This is, however, impractical in real control systems, particularly in CCM designed grid-tied inverters. The control errors can accumulated and they cannot be eliminated or reset. Consequently, the feed-forward control is usually applied together with a feedback control, e.g. in order to perform grid-voltage feed-

forward compensation [18–21] or duty ratio feed-forward [22]. The feed-forward control features simple control and fast dynamic response. However, parameter dependency can be a drawback of this kind of control strategy.

2.2 Overview of Operation Modes in Grid-Tied inverters

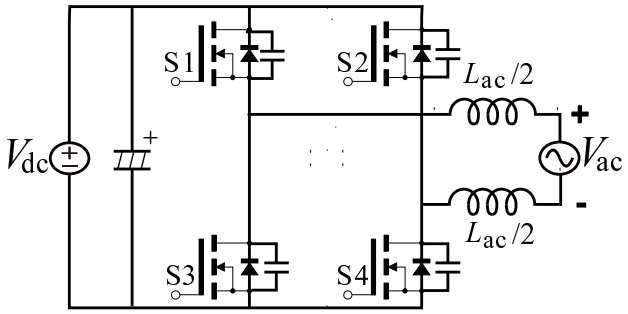

Fig. 2.2 Single-phase H-bridge grid-tied inverter with an inductive (L) filter.

For a single-phase grid-tied inverter with H-bridge topology, inductive (L) filter, (shown in Fig. 2.2) and inductive-capacitive-inductive (LCL) filter (shown in Fig. 2.3) are the two typical filters to interface the inverter and electrical grid. In comparison with the L filter, the LCL filter introduces an improved attenuation performance, and at the same time with a reduced overall size [23]. Therefore, it can be a good candidate for grid-tied inverters to achieve high power density. The minimization of grid-connected inductor can be considered as one of the key techniques to achieve low cost and small size of a low-power grid-tied

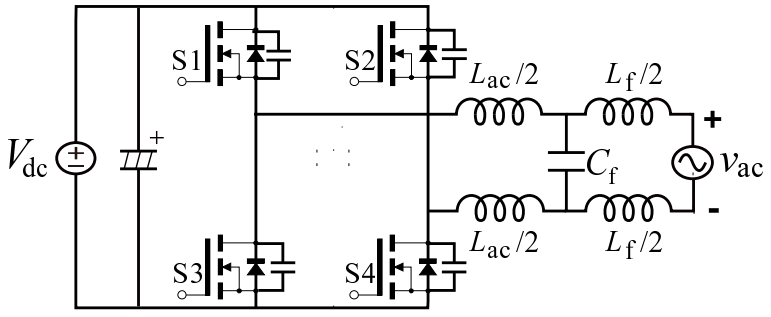

Fig. 2.3 Single-phase H-bridge grid-tied inverter with an inductive-capacitive-inductive (LCL) filter.

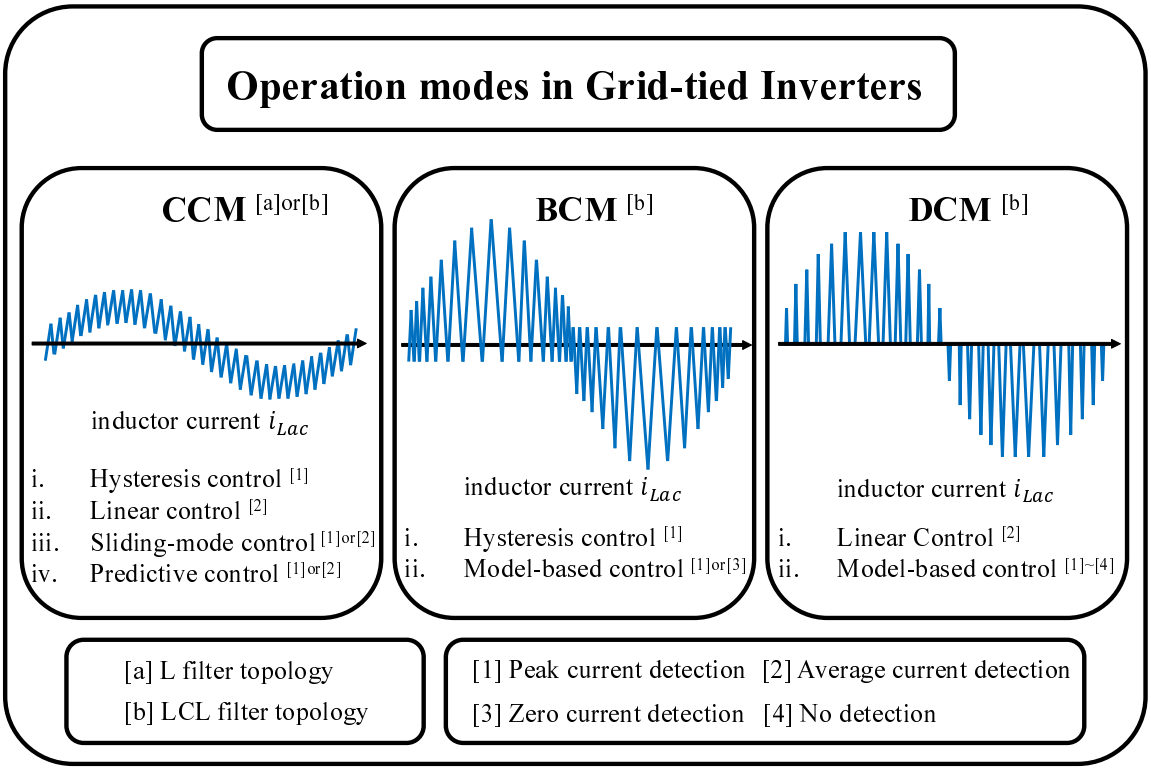

Fig. 2.4 Typical operation modes in grid-tied inverters.

inverter, as discussed in Chapter 1. Generally, the volume of inductor can be reduced by minimizing the inductance and the inductance can be reduced by increasing the switching frequency.

Fig. 2.4 depicts a classification of operation modes in according with the behavior of inductor current in single-phase grid-tied inverters. Generally, the inductor current can be controlled to operated in continuous current mode (CCM), discontinuous current mode (DCM) and the boundary between CCM and DCM. The latter is usually referred to as boundary conduction mode (BCM) or critical conduction mode (CRM). The CCM can be applied to a grid-tied inverter with both L and LCL filter. The DCM or BCM is only valid for grid-tied inverter with LCL filter.

2.2.1 Continuous Current Mode

The classic control strategies for CCM grid-tied inverters are the hysteresis control and linear PI control. Although the sliding-mode control and predictive control exhibit superior performances than the classic controls, they requires complicated algorithm and high amounts of calculations. Consequently, in comparison with the well established hysteresis control and linear PI control, they are currently not suitable for industrials and still need further researches. On the other hand, the hysteresis control is not suitable for low-power grid-tied inverters due to the excessive switching losses as discussed in Section 2.1.1. Therefore, the discussions of current control for CCM grid-tied inverters are based on linear PI control with PWM modulation only in this dissertation.

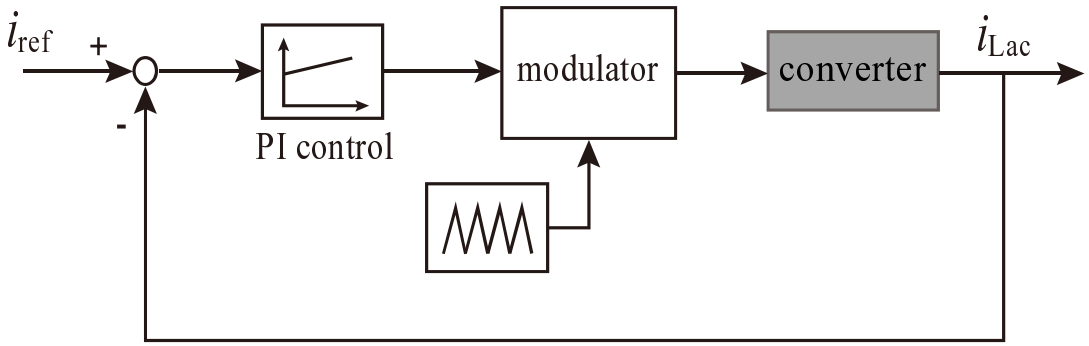

Fig. 2.5 Block diagram of a linear control with PI controller and PWM modulator.

Fig. 2.5 depicts a typical block diagram of a linear control with PI controller and PWM modulator. The average values of inductor current is sensed and compared with the reference current. Then the errors are processed by the PI controller and the generated voltage reference is compared with a carrier in the PWM modulator. The converter can be considered as a gain, where the inductor current is inverse proportional to the inductance. Although the inductance can be reduced under high frequency operation. The disturbance response gain can increase under low inductance condition [24]. For instance, small changes on the inverter output can cause large current ripple and the current control can become difficult. Consequently,

the inductance can not be reduced to the values determined by ripple limitation even with increased switching frequency in a grid-tied inverter with CCM design.

2.2.2 Boundary Conduction Mode

The BCM is a popular design in low-power PFC converters. Recently, an increased number of researches have proposed to apply this kind of control to low-power grid-tied inverters. The main purpose of applying BCM control is to realize the zero-voltage-switching (ZVS) for turn-on, which is essentially important for high frequency converters. However, the variation of switching frequency is usually wide and it increases further at low power levels. Therefore, the excessive turn-off and inductor losses can be a problem despite of the realization of ZVS turn-on. The current control schemes of BCM are usually based on hysteresis control [25, 26] and model-based control [27, 28].

Conventionally, high sampling frequencies and precise measurement are required to obtain accurate current information in order to guarantee ZVS over the entire line cycle. However, the A/D converters in the existed digital controllers can not perform such accurate sampling of inductor current at high frequencies. The switching states can be also determined by the use of analog circuits. Fig. 2.6 depicts the schematic waveform of BCM operation and its control diagram while the hysteresis control strategy is considered. This kind of control is also referred to as dual current programmed mode (DCPM) control [25, 26]. The control loop of DCPM consists of a current-sensing resistor, a differential amplifier, two comparators and a flip-flop. In the DCPM control, two current references, $i_{\mathrm{ref}+}$ and $i_{\mathrm{ref}-}$ are predefined and the inductor current, i_{Lac}, flows through in between these two references. i_{Lac} is measured through a shunt resistance. The switch states are changed when i_{Lac} reaches the predefined reference. To ensure the ZVS turn-on, a sufficient negative current is necessary. By doing this, the peak inductor current is also required to increase in order to maintain the same average current. Consequently, it result in higher conduction losses. One drawback of

the DCPM control is that it can suffer from the switching noise and control delay, particularly at high frequencies [25, 26].

Fig. 2.7 depicts the schematic waveform of BCM operation and its control diagram while the model-based control strategy is considered. The use of analog circuit have the problem of reliability and they can decrease the power density [27]. The time for turn-on and turn-off can also be calculation from the model of BCM by the use of micro-controller, such as the digital signal processor (DSP). Therefore, a control strategy that combines model-based control and peak current detection has been proposed. In this kind of control strategy, the time for turn-on is calculated for each operation point over the line cycle in the digital controller. Therefore, the timings of turn-off no longer depend on the detection of peak inductor current. However, a reset is required in order to avoid the errors being accumulated. When the inductor current, i_{Lac}, reaches a predefined negative boundary (i.e. the reset as shown in Fig. 2.7), the switches are turned on again. Consequently, this kind of control still relies on the detection of inductor current. Generally, a current transformer with large core size is required for the purpose of measuring both switching and fundamental components [27]. In order to reduce the size of the components, a measurement method combining a high-frequency current transformer and a low-frequency hall-effect sensor is proposed. The high-frequency and low-frequency components are measured separately and added together to obtained the current of inverter-side inductor, which simplifies the current detection [27, 29].

Fig. 2.8 depicts the schematic waveform of BCM operation and its control diagram while another model-based control strategy is considered [28, 30, 31]. The turn-on and turn-off times are calculated on the basis of model built for BCM operation. In order to determine the timing of turn-on instants, information regarding to zero-crossing of the inductor current, i_{Lac}, is required. Consequently, the converter also cannot be operated without inductor current detection with this kind of model-based control.

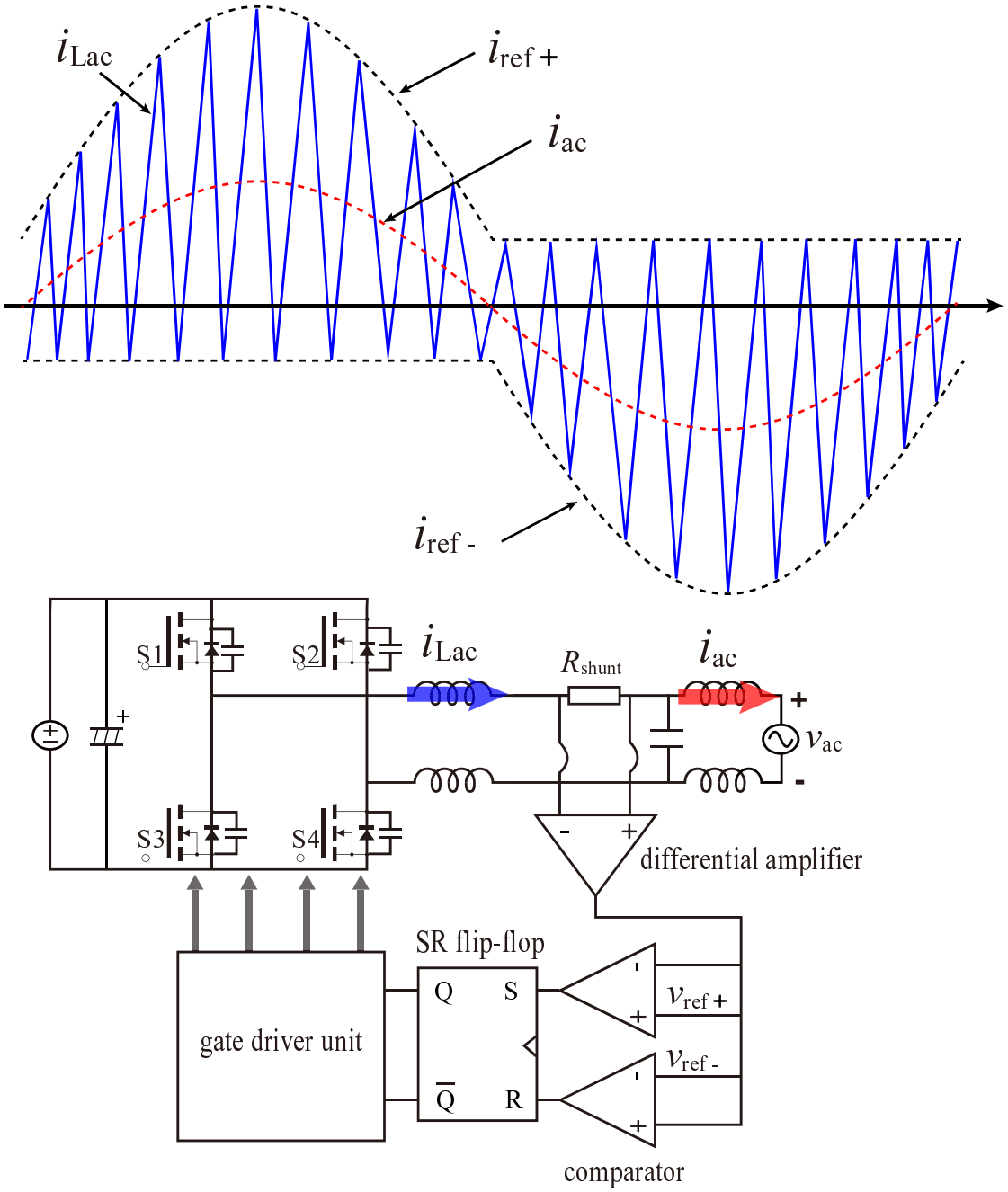

Fig. 2.6 Overview of the hysteresis BCM control scheme. [25, 26]

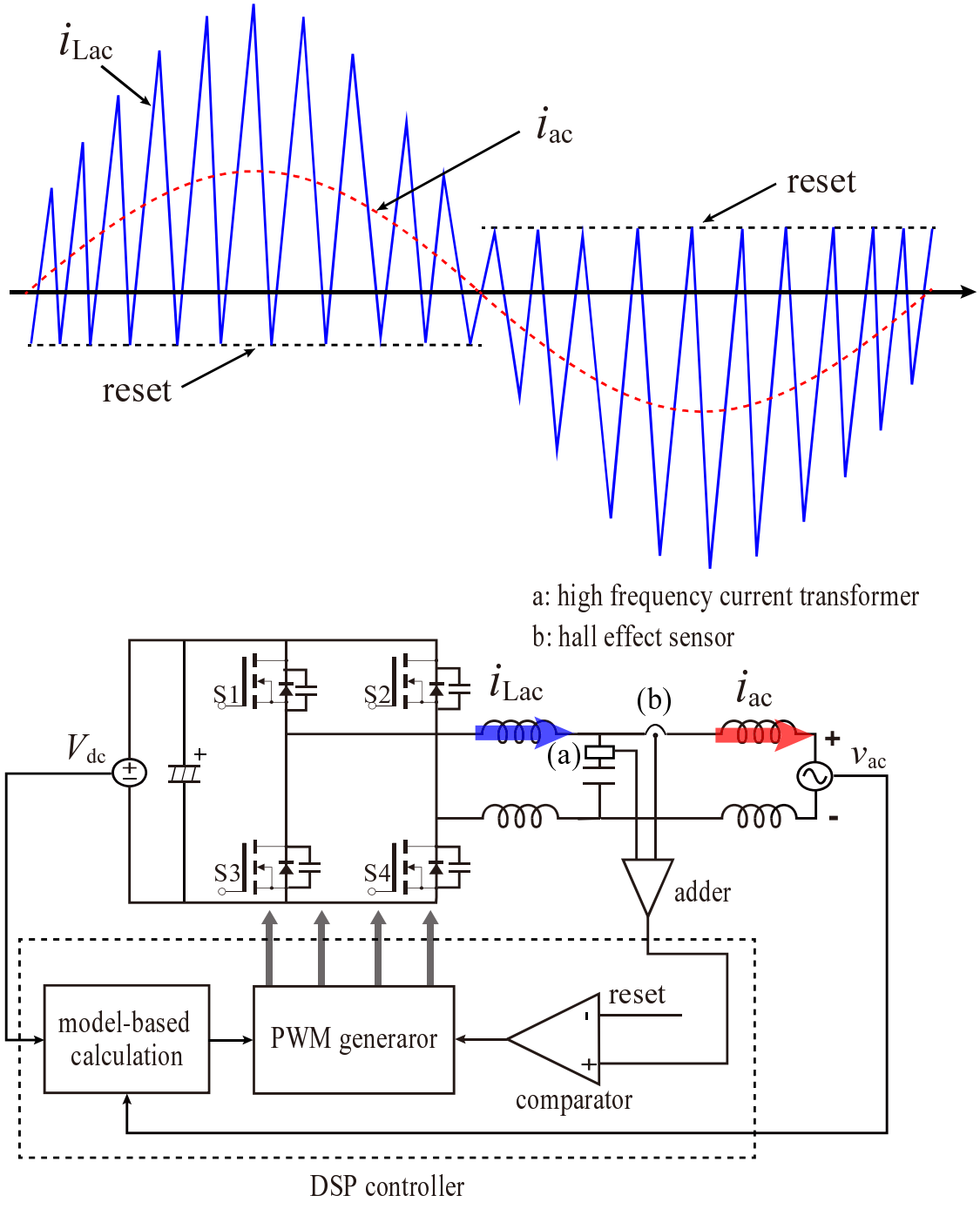

Fig. 2.7 Overview of the model-based BCM control scheme with peak current detection [27]

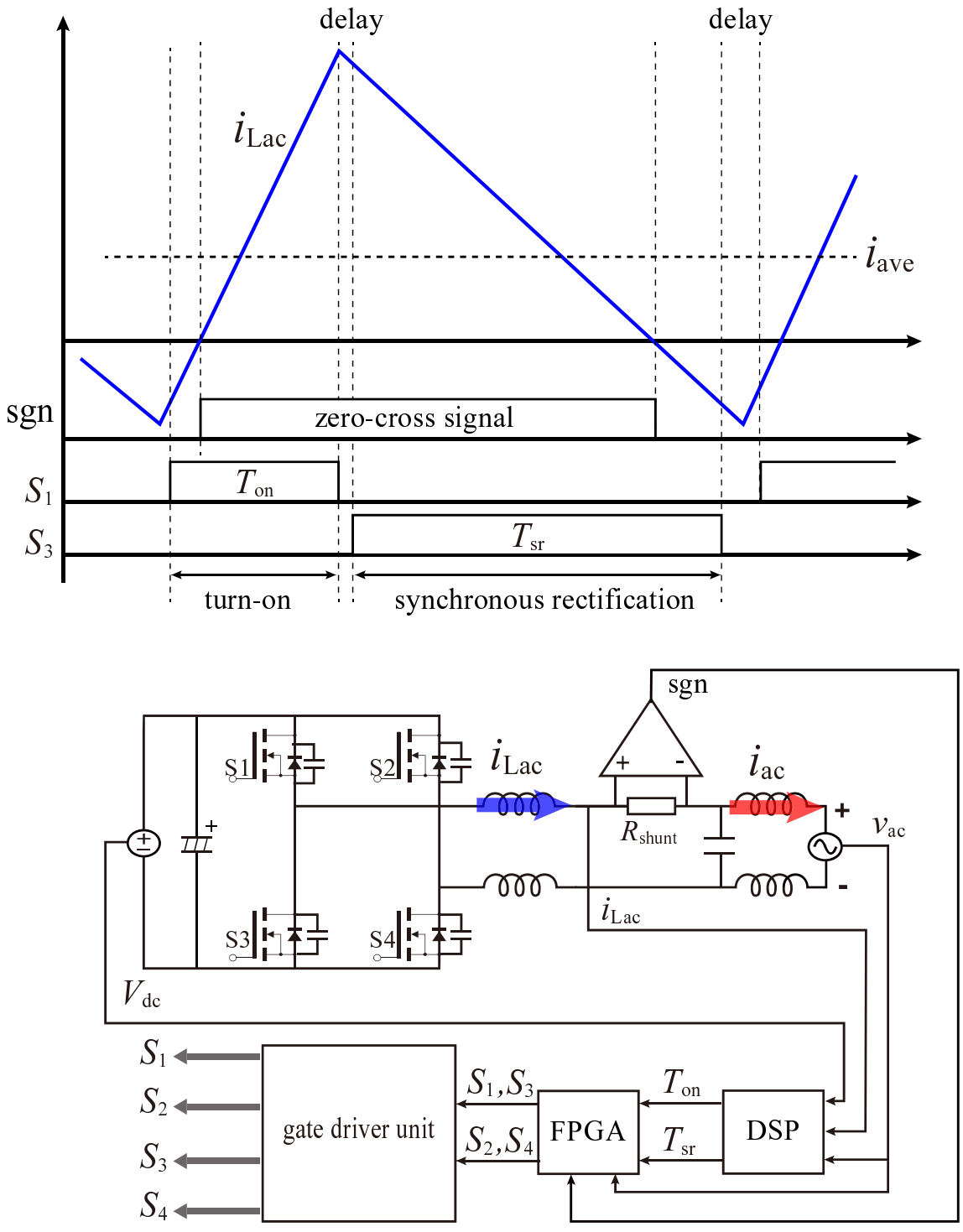

Fig. 2.8 Overview of the model-based BCM control scheme with zero-cross detection. [28]

The inductance can be reduced further with BCM since the current control is not error based. However, the BCM has some challenges in the face of the detection of triangular inductor current therefore contains high frequency components, particular under high frequency operations.

2.2.3 Discontinuous Current Mode

DCM is also a popular design in low-power AC/DC converters. The DCM has a so-called "zero current interval" where the inductor current being zero in every switching cycle. Therefore, the variations of switching frequencies have more degrees of freedom and it can be even fixed. For current control strategies, linear PI control and model-based control can be applied to the DCM grid-tied inverters. It is similar with the BCM design, the inductance can also be reduced further by designing the converter to operate in DCM.

In DCM, the duty ratios are not proportional to the output voltage of inverter due to the exsitance of zero current interval. Consequently, the duty-ratio-to-inductor-current transfer function is non-linear [32]. This problem results in lower gain in comparison with that in CCM. For this reason, the PI controller should be designed with a high gain in order to obtain good dynamics. Another approach is to compensate the non-linearity in the transfer function [33]. With this technique, a PI controller designed for CCM can provide the same dynamic for DCM. Nevertheless. the current control is based on feedback so that the detection of inductor current is required.

The sensing of inductor current has some challenges in DCM. Firstly, a high bandwidth and low delay sensor is required in order to sample the large ripple current. Secondly, the sampling errors is required to be corrected in DCM. Generally, sufficient high sampling frequencies is required to obtain the accurate current information. However, this can be a challenge if the switching frequency is already high. Therefore, the sampling frequencies is generally synchronized with the switching frequency [34]. Fig. 2.9 depicts a digital

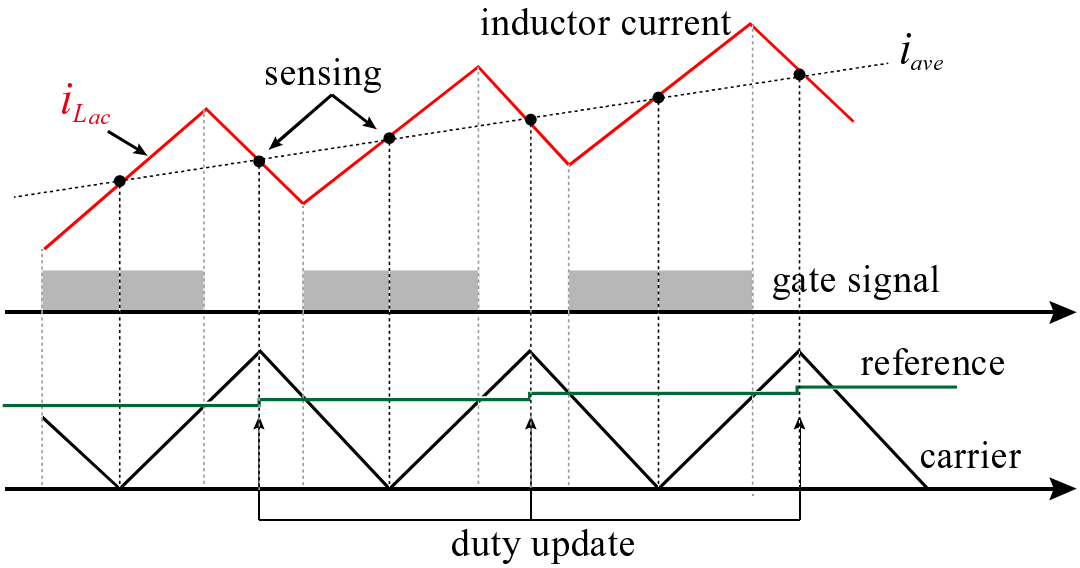

Fig. 2.9 Digital sampling process performed in CCM. The sampled values represents the average inductor current owing to the linear relationship.

sampling process performed in CCM design. The analog-to-digital (A/D) converter can be triggered when the carrier counter reaches a predefined peak value or a minimum value. When the rising-edge-sampling (RES) or falling-edge-sampling (FES) is applied, the values of inductor current at the center of the turn-on time or turn-off time of the switches are sampled. Therefore, the sampled values can represent the average inductor current in CCM. However, this relationship no longer exists when the current becomes discontinuous, as shown in Fig. 2.10. The middle of the rising or falling inductor current does not represented the average current due to the exsitance of zero current interval. Consequently, corrections for the sampling errors are necessary in order to obtain the information of average current in DCM [34]. The average inductor current can also be measured through a low-pass filter, however, the delays in control can be a problem particularly under high frequency and low inductance conditions. Consequently, one drawback of the feedback control in DCM is the difficulties related to current sensing. Another drawback is that it cannot perform the so-called synchronous rectification only with the linear PI control, because the switching scheme is not always complementary in DCM. This can be a problem in some cases. e.g.

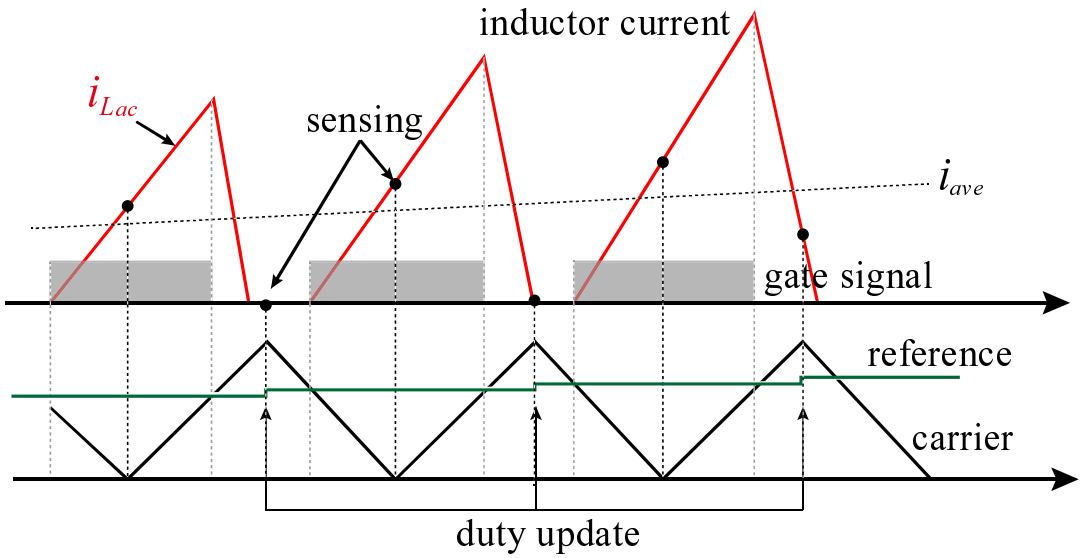

Fig. 2.10 Digital sampling process performed in DCM.The sampled values do not represent the average inductor current due to the non-linearity.

the forward voltage of body diode in SiC-MOSFETs are usually high so that the diode rectification can result in more conduction losses.

Fig. 2.11 depicts the schematic waveform of DCM operation and its control diagram while the model-based control strategy is considered. In the model-based control, the times for turn-on and synchronous rectification are calculated on the basis of a model built for the DCM operation. It is different from the control strategy shown in Fig. 2.7, the reset is naturally achieved by the zero current interval. Therefore, the model-based control can be realized without any detection of inductor current, i_{Lac}, in DCM. This is essentially advantageous in high frequency designed inverters, since the difficulties related to the current sensing and sampling corrections no longer lying. Fig. 2.12 depicts the control block diagram of a model-based control used in DCM. The model-based controller itself can be used as a current controller, which is different from that in CCM. This is because the accumulated errors, which are caused by the use of an imperfect model, can be reset by the zero current period of every switching cycle. Therefore, it is safe to apply the model-based controller only to perform current regulation in DCM. Further more, the problem of non-linearity of

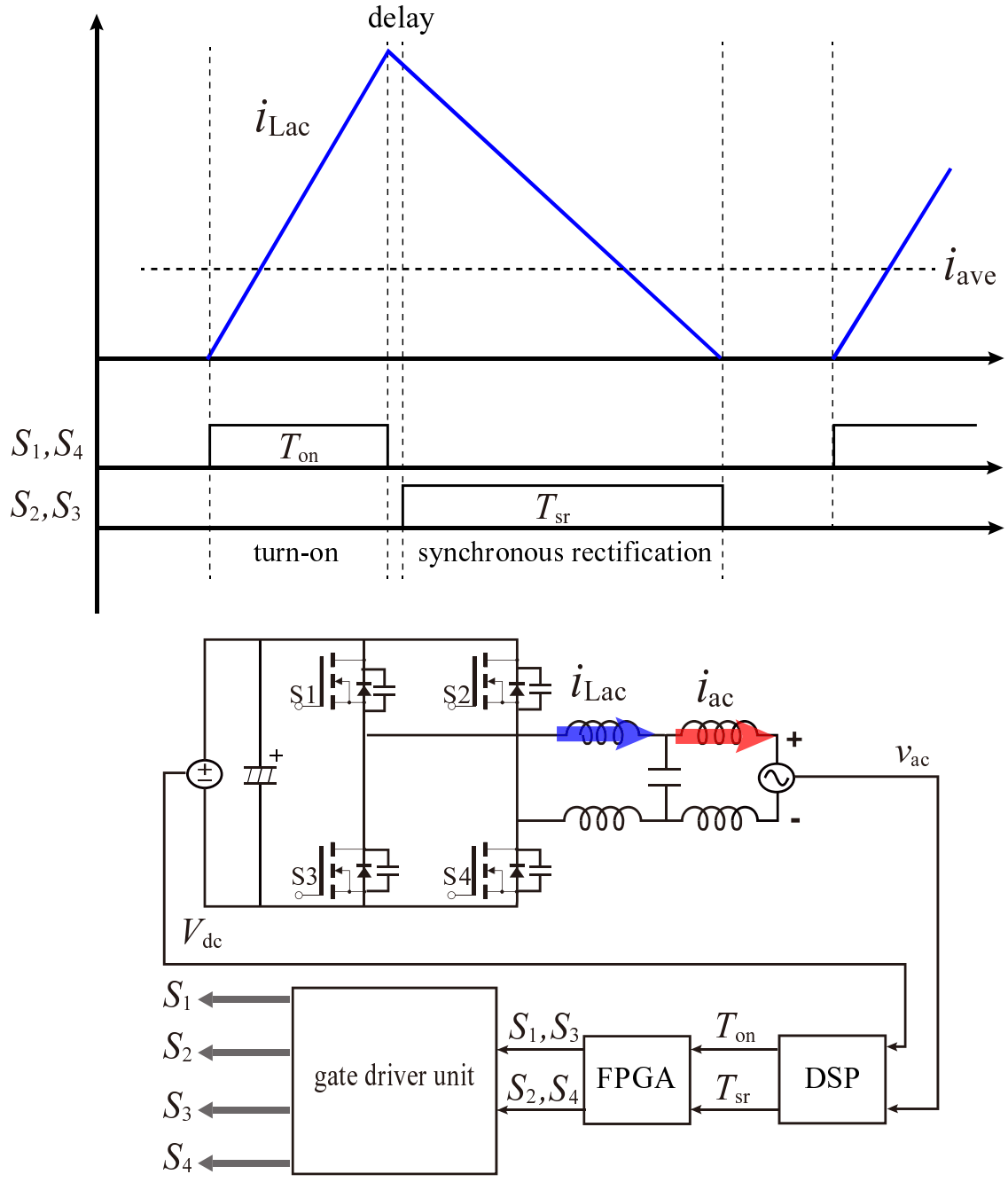

Fig. 2.11 Overview of the model-based DCM control scheme.

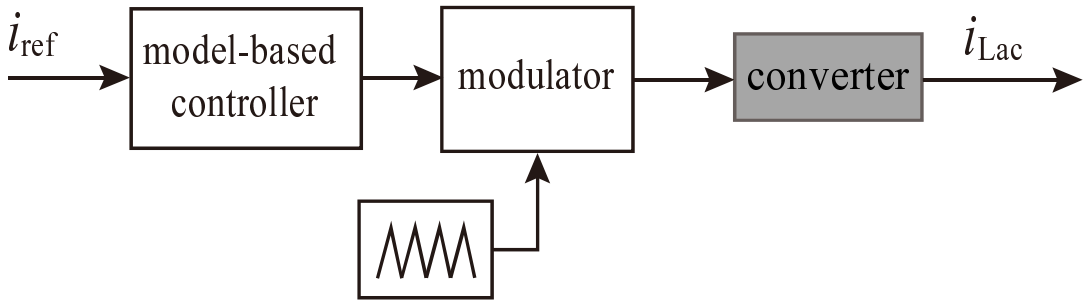

Fig. 2.12 Block diagram of a model-based control used in DCM.

the discontinuous current can also be corrected by the model-based calculation. Therefore, synchronous rectification is also easy to be realized with this kind of control strategy. By using different DCM models, the inverter can operate under fixed switching frequency [35, 36] or variable switching frequency [37–41].

2.2.4 Comparison of CCM, BCM and DCM Controls for Low-Power Grid-Tied Inverters

Table 2.1 shows a comparison among CCM, BCM and DCM with different classic control strategies. For CCM, neither hysteresis nor linear PI control are suitable for high frequency operation due to the excessive switching losses and difficulties in current control under low inductance condition. Consequently, a low-power grid-tied inverter being designed with CCM is not suitable for very high switching frequency operation.

For BCM, the inductance can be reduced further to an extreme low value. However, both hysteresis and model-based controlled BCM lead to a wide variation of switching frequencies. The wide variation of switching frequencies can result in excessive switching losses and inductor losses at low power operations, in despite of the realization of ZVS turn-on. In addition, the high peak inductor currents result in high conduction losses, turn-off losses and inductor losses in comparison with those in CCM. Moreover, the detection of inductor current that contains high frequency components can be the main challenge.

Table 2.1 Comparison of CCM, BCM and DCM Controls

Operation mode	CCM		BCM		DCM	
Control method	hysteresis	linear	hysteresis	model-based	linear	model-based
Use extremely low inductance	✓	×	✓	✓	✓	✓
Without detecting i_{Lac}	×	×	×	×	×	✓
No excessive switching frequency	×	✓	×	×	✓	✓
Enable soft-switching	–	–	✓	✓	–	–
High peak current	✓	✓	×	×	×	×
Suitable for high frequency	×	×	–	–	–	✓

× : poor/difficult, –: fair/average, ✓: good/yes

For DCM with linear PI control, the inductance can be reduced further. However, it has the same problems in terms of current detection with the BCM controls. This problem can be addressed by applying the model-based control. The switching frequency can be fixed or has some variations. Therefore, excessive switching losses can be avoid in DCM. However, the high peak currents can still be a problem like that in BCM.

To sum up, the DCM with model-based control can be considered as the most suitable and promising method of current control for grid-tied inverters, especially with high frequency designs.

2.3 Overview of Model-Based Controlled DCM Grid-Tied Inverters

2.3.1 Constant Frequency Control Strategy

The average current control strategy has been widely studied in low-power PFC converters that operates in DCM completely. It is different from the conventional constant on-time control strategy, the duty cycles are controlled to be variable values in order to follow the sinusoidal reference current [42]. This control strategy is also valid for DCM grid-tied inverters.

Fig. 2.13 depicts the schematic waveforms and corresponding control diagram of an average current control for single-phase DCM grid-tied inverters. In this kind control strategy, the average values of the triangular inductor current, i_{Lac}, is controlled to be equal to a given reference current. The duty ratios are usually calculated by means of certain equations being derived from a reduced-order or full-order model built for the DCM [43]. The calculations are dependent on the circuit and design parameters, such as inductance and switching frequency, and operation condition in the corresponding switching cycle, i.e. the DC link voltage and instantaneous line voltage. The calculated duty ratios for turn-on and synchronous rectification are then compared with a carrier with constant frequency to generate PWM signals.

The average current control can be easily implemented in a digital signal processor (DSP) without any complicated algorithms. The current control loop is usually based on feed-forward. A feedback loop of voltage control is implemented outside this current control loop in order to regulate the DC-link voltage and generate current reference, i_{ref}. In this dissertation, only the current control loops are discussed. The average current control has been implemented in a MHz operated DCM grid-tied inverter; and it is demonstrated that the

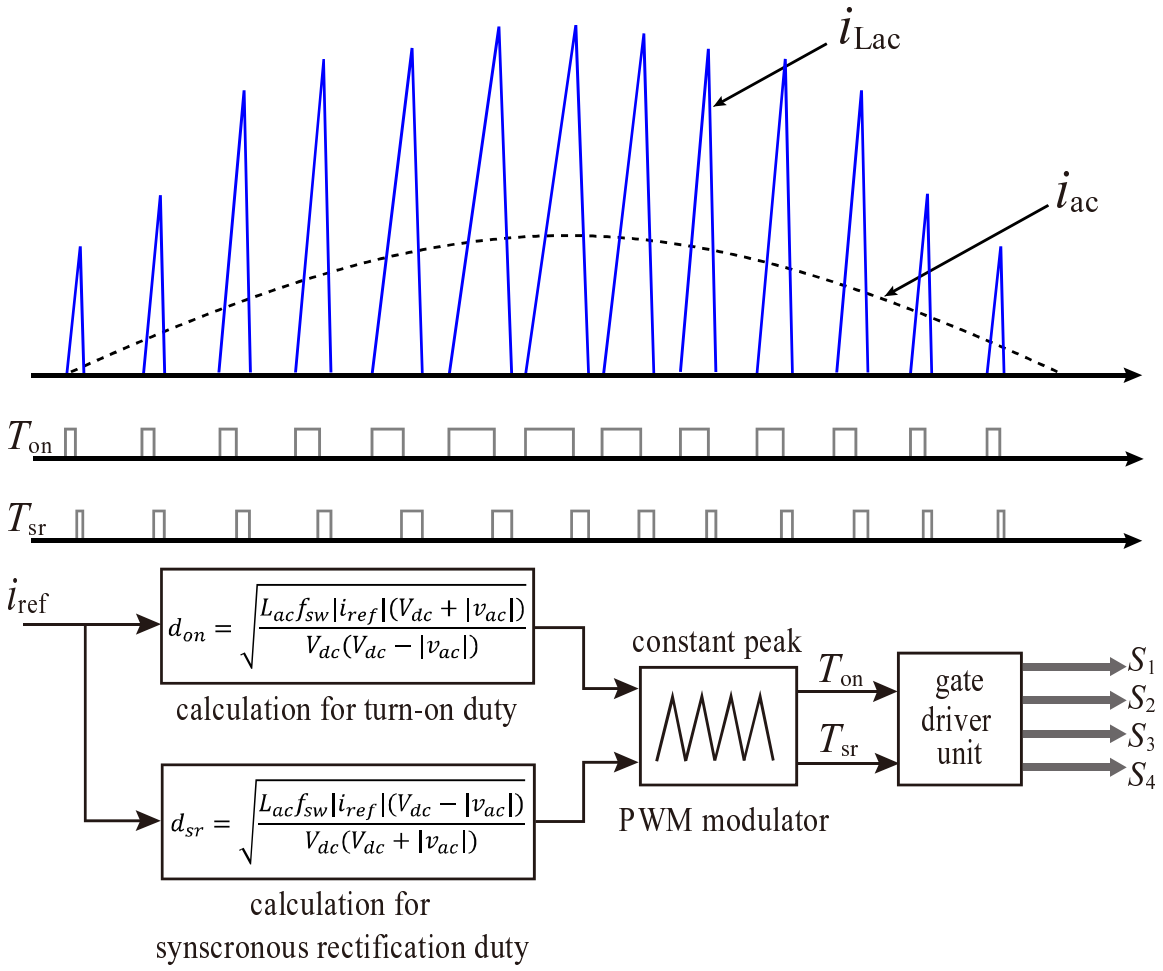

Fig. 2.13 Overview of the average current control scheme for single-phase DCM grid-tied inverters [35, 36].

current control without any significant difficulties can be achieved even under extremely low inductance condition [36].

2.3.2 Constant Peak Current Control Strategy

Fig. 2.14 depicts the schematic waveforms and corresponding control diagram of a constant peak current control scheme for single-phase DCM grid-tied inverters. This control strategy has been implemented in an inverter with DC/DC converter and unfolder topology [37] and a H-bridge inverter [38].

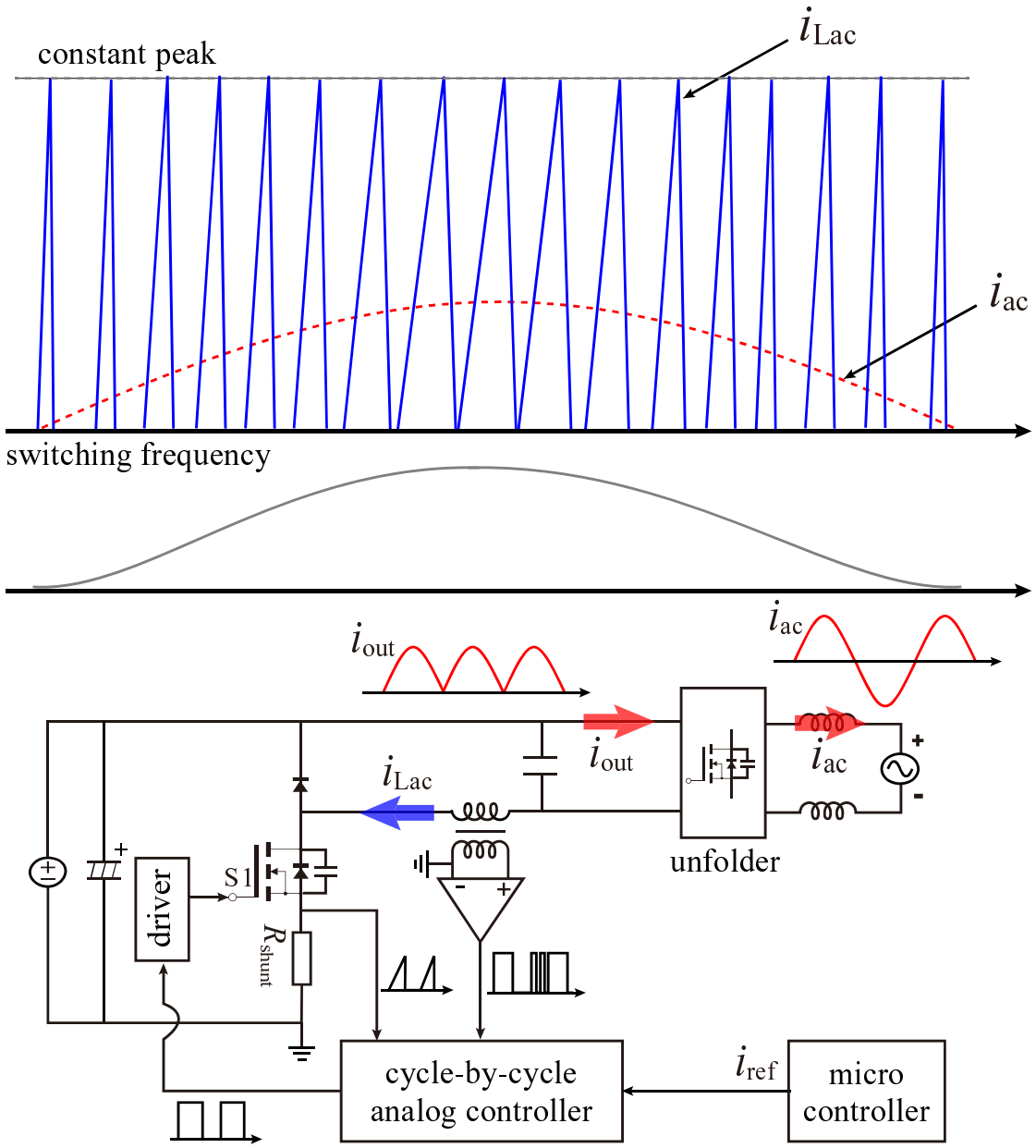

Fig. 2.14 Overview of the constant peak current control scheme for single-phase DCM grid-tied inverters [37, 38].

In this kind of control strategy, the peak values inductor current, i_{Lac}, are controlled to be equal to a predefined value which is constant over half line cycle. Therefore, the switching frequency becomes variable under this kind of control strategy. By setting a constant peak current over half line cycle, the switching frequency reduced significantly around zero-crossing areas. Therefore, the switching losses are possible to be minimized with this control concept.

In order to implement the constant peak current control, the peak values of the inductor current, i_{Lac}, and the total conduction time are required to be detect. The inductor current can be measured by a current sensing resistor. The total conduction time can be measured by a voltage sensor that detects the transient of voltage that occurs when the inductor current becomes zero [37]. Consequently, it has the similar problems with the BCM control. A disadvantage of this constant peak control is that the switching frequency can reduce to the audible ranges around zero-crossing points. To avoid this issue, a modified version is discussed in [38]. Another drawback can be the high root-mean-square (r.m.s.) value of i_{Lac}, which can cause higher conduction loss at high power levels.

2.3.3 Variable Peak Current Control Strategy

Fig. 2.15 depicts the schematic waveforms and corresponding control diagram of a variable peak current control for single-phase DCM grid-tied inverters. It is similar with the constant peak current control, the peak current is also under controlled. However, this control strategy does not require current detection. The control of peak current and switching frequency is completely based on the mode-based calculation, which is similar with the average current control strategy. An example of this control strategy for the DCM grid-tied inverter is proposed in [39]. The switching frequencies are controlled to decrease along with the changing of power and current phase angles in order to minimized the switching losses. The peak inductor current is calculated on the basis of a DCM model in accordance with

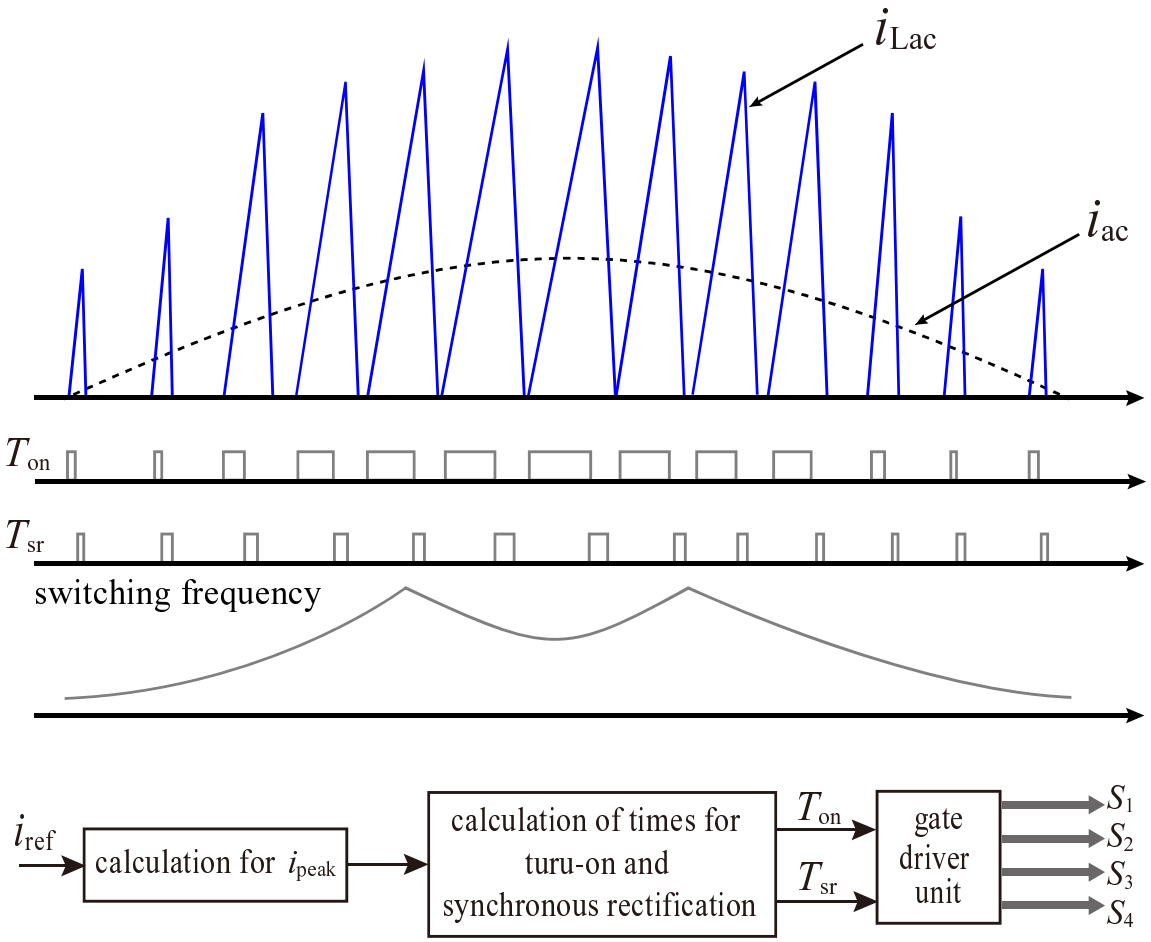

Fig. 2.15 Overview of the variable peak current control scheme for single-phase DCM grid-tied inverters [39].

predefined off-times of the switches firstly. Then the duty ratios and switching frequencies are calculated from the reference of peak currents. The switching losses can be significantly reduced by decreasing the switching frequencies. Therefore, the efficiencies can be improved, particularly at low power operations.

2.3.4 Dual Mode Control Strategy

Fig. 2.16 depicts the schematic waveforms and corresponding control diagram of a dual-model control scheme for single-phase DCM grid-tied inverters. This control strategy is actually a combination of BCM and DCM and the concept is to operate the inverter under

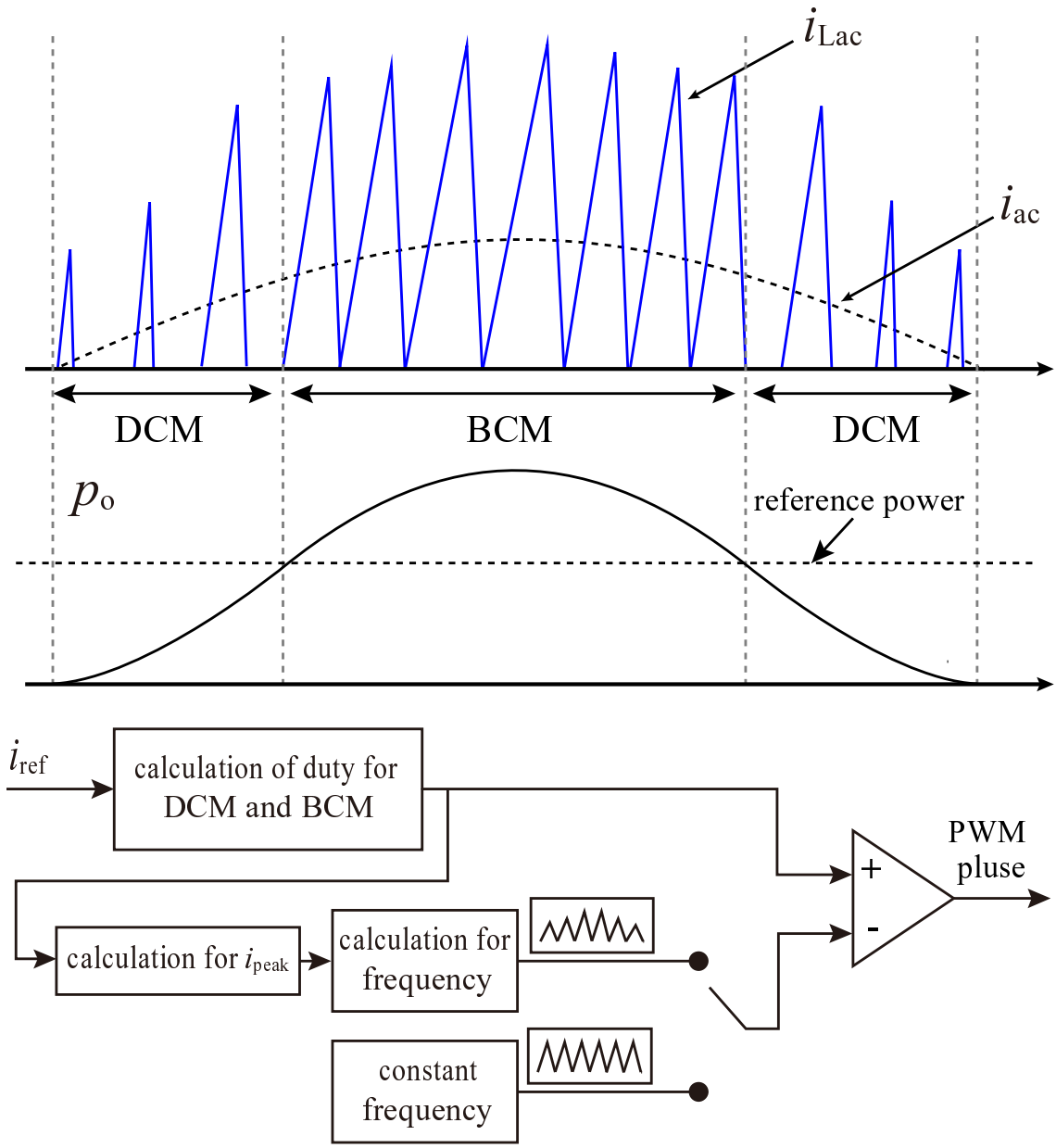

Fig. 2.16 Overview of the dual-model control scheme for single-phase DCM grid-tied inverters [40, 41].

both BCM and DCM in accordance with a predefined level. When the power is higher than a predefined level, the operation mode switches to BCM; and the operation mode shifts to DCM when the power is lower than the predefined level. In the part of BCM, the variable peak current control is applied to calculate the switching frequency; in the part of DCM, the control is similar with the average current control.

2.3.5 A Bipolar Switching Scheme for DCM Grid-Tied Inverter

Operation principle

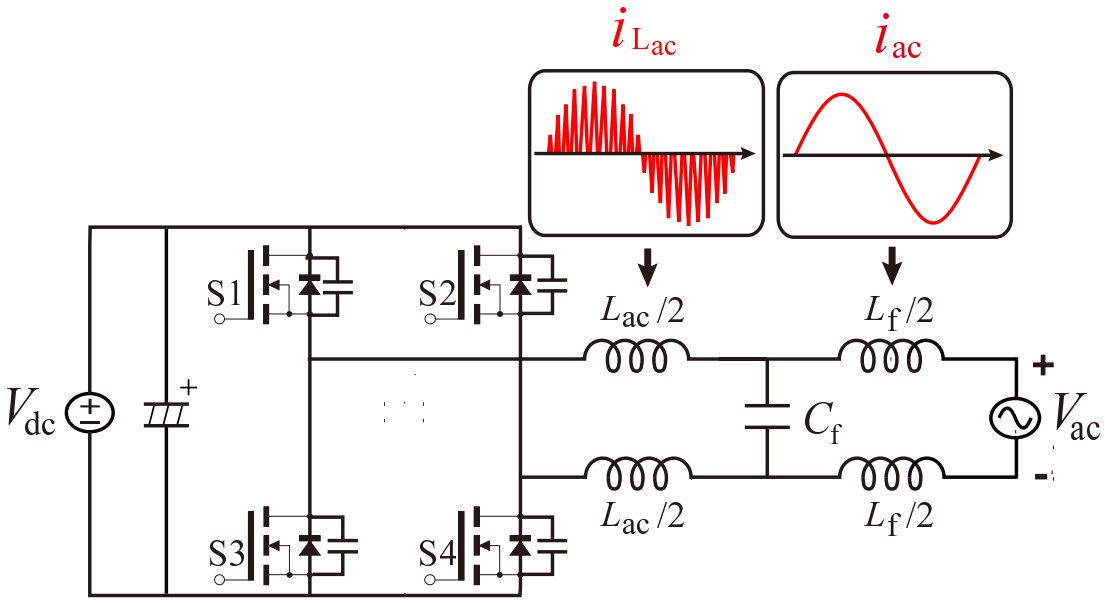

Fig. 2.17 Single phase H-bridge grid-tied inverter with LCL filter operating in DCM.

Conventionally, bipolar and unipolar switching are the two popular switching schemes that can be applied to an single phase H-bridge grid-tied inverter [44]. Fig. 2.17 depicts an H-bridge single-phase grid-tied inverter with LCL filter operating in DCM. In DCM, the current flowing through the inverter-side inductor, L_{ac}, is a triangular shape that reduces to zero in every switching cycle. The filter capacitor, C_f, and the grid-side inductor, L_f, forms a low-pass LC filter. The switching harmonics in the inverter-side inductor current, i_{Lac},

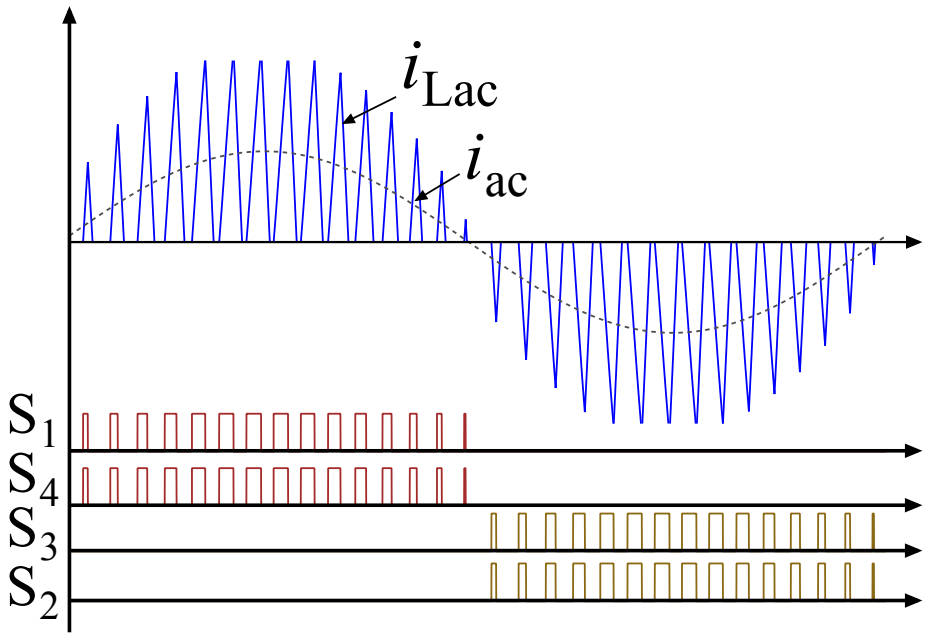

Fig. 2.18 Bipolar switching patterns and corresponding inductor waveforms for DCM.

are attenuated by the low-pass filter. A smooth current, i_{ac}, flowing through L_{f} then can be obtained.

Fig. 2.18 depicts the schematic waveforms of i_{Lac}, i_{ac} and a bipolar switching scheme for DCM. The pair of diagonal switches S_1 and S_2 or S_2 and S_3 can be controlled to turn on and off simultaneously to create the a positive and negative output voltage. Therefore, this switching scheme is referred to as bipolar DCM. By neglecting the capacitor current, the average current of i_{Lac} is equal to the output current i_{ac}.

Fig. 2.19 depicts the schematic waveforms and possible current paths of one switching cycle operation with the bipolar DCM, for positive grid voltage, V_{ac}. There are three main intervals during one switching cycle operation. In the following discussions, the operation principles that for positive V_{ac} are described, since similar operation principles can also be derived for negative V_{ac}.

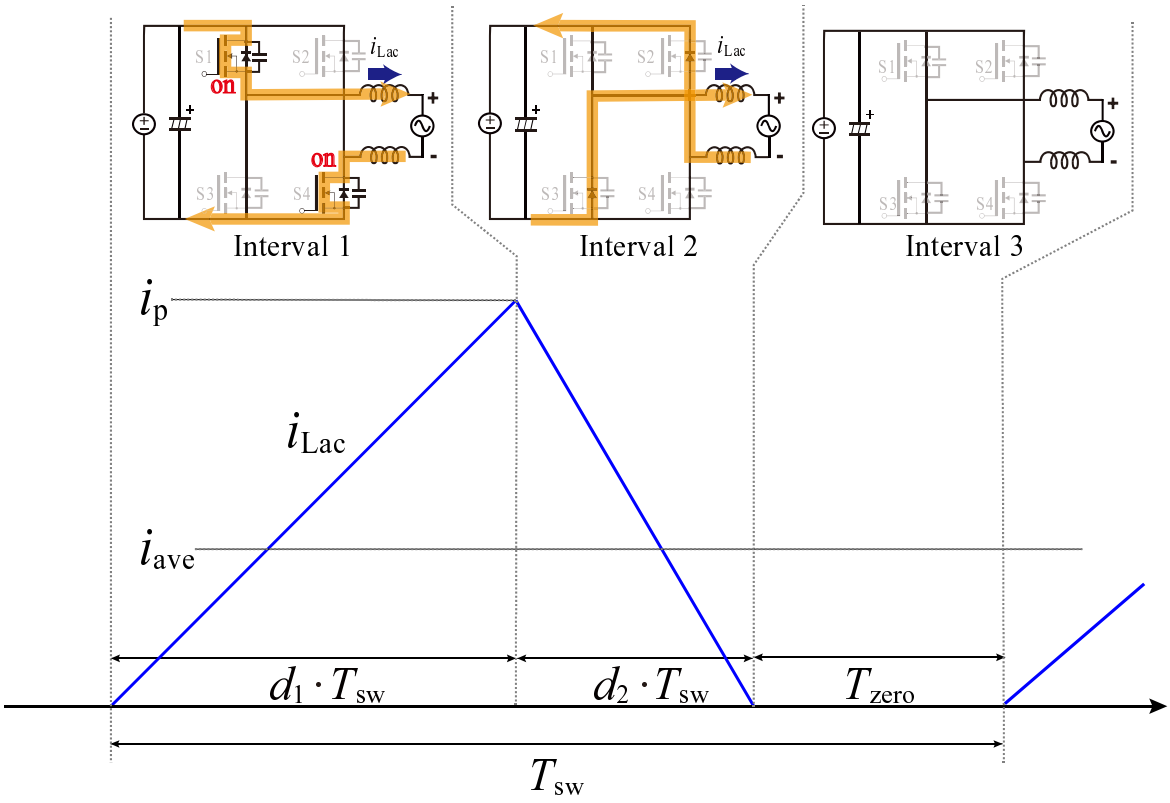

Fig. 2.19 Possible current paths of one switching cycle operation in bipolar DCM for positive grid voltage V_{ac}.

Interval 1:

During interval 1, switches S_1, S_4 are in on-state, switches S_2, S_3 are in off-state. The inverter-side inductor current, i_{Lac}, increases linearly. The peak value of i_{Lac}, i_p, during this interval can be expressed as

$$i_p = \frac{V_{dc} - v_{ac}}{L_{ac}} d_1 T_{sw}, \tag{2.1}$$

where V_{dc} denotes the input DC voltage. v_{ac} denotes the instantaneous value of grid voltage and it can be assumed constant in one switching period, since the switching frequency is much higher in comparison with the grid frequency. L_{ac} denotes the inductance of the inverter-side inductor. d_1 denotes the duty ratio of turn-on for S_1 and S_4. T_{sw} denotes the switching period. The interval 1 ends when the switches S_1 and S_4 are turned off.

Interval 2:

After S_1, S_4 are turned off, i_{Lac} decreases linearly through the body diode of S_2 and S_3. S_2 and S_3 can also be turned-on to achieve the so-called synchronous rectification during this interval. According to the voltage-second balance, i_{p} during this interval can be expressed as

$$-i_{\mathrm{p}} = \frac{-V_{\mathrm{dc}} - v_{\mathrm{ac}}}{L_{\mathrm{ac}}} d_2 T_{\mathrm{sw}}, \tag{2.2}$$

where d_2 is the duty ratio of turn-on for S_2 and S_3 to achieve the synchronous rectification. This interval ends when i_{Lac} reduces to zero.

Interval 3:

During interval 3, the inductor current should be zero theoretically. Therefore, this interval is referred to as zero current interval. T_{zero} denotes the length of the zero current interval, as shown in shown in Fig. 2.19. After this interval, S_1 and S_4 are turned on again and a new switching cycle begins.

Model-Based Calculation for Duty Ratios

The conventional average current control is considered and the derivation for duty ratios with this control strategy is reviewed in the following discussions. The average current of i_{Lac}, i_{ave}, in one switching cycle can be derived from the average current model built for DCM operation. i_{ave} can be expressed as

$$i_{\mathrm{ave}} = \frac{S}{T_{\mathrm{sw}}} = \frac{0.5 i_{\mathrm{p}} (T_{\mathrm{on}} + T_{\mathrm{sr}})}{T_{\mathrm{sw}}} = \frac{0.5 i_{\mathrm{p}} (d_1 + d_2) T_{\mathrm{sw}}}{T_{\mathrm{sw}}}, \tag{2.3}$$

where S is the area of the triangular inductor current, i_{Lac}, during one switching cycle. T_{on} and T_{sr} are the time for turn-on and synchronous rectification, respectively.

The relationship between d_1 and d_2 can be expressed as

$$d_2 = \frac{V_{\mathrm{dc}} - v_{\mathrm{ac}}}{V_{\mathrm{dc}} + v_{\mathrm{ac}}} d_1. \tag{2.4}$$

i_{ave} during one switching cycle should be equal to the given current reference, i_{ref}, and can be obtained by substituting (2.1) into (2.3). i_{ave} then can be expressed as

$$i_{\mathrm{ref}} = i_{\mathrm{ave}} = \frac{V_{\mathrm{dc}} - v_{\mathrm{ac}}}{2L_{\mathrm{ac}}} d_1 (d_1 + d_2) {T_{\mathrm{sw}}}^2. \tag{2.5}$$

The duty ratio for turn-on, d_1, and synchronous rectification, d_2, then can be derived by combining (2.4) and (2.5), and can be expressed as

$$d_1 = \begin{cases} \sqrt{\dfrac{L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}} (V_{\mathrm{dc}} + v_{\mathrm{ac}})}{V_{\mathrm{dc}} (V_{\mathrm{dc}} - v_{\mathrm{ac}})}} & (i_{\mathrm{ref}} > 0) \\ \sqrt{\dfrac{L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}} (V_{\mathrm{dc}} - v_{\mathrm{ac}})}{-V_{\mathrm{dc}} (V_{\mathrm{dc}} + v_{\mathrm{ac}})}} & (i_{\mathrm{ref}} < 0) \end{cases} \tag{2.6}$$

and

$$d_2 = \begin{cases} \sqrt{\dfrac{L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}} (V_{\mathrm{dc}} - v_{\mathrm{ac}})}{V_{\mathrm{dc}} (V_{\mathrm{dc}} + v_{\mathrm{ac}})}} & (i_{\mathrm{ref}} > 0) \\ \sqrt{\dfrac{L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}} (V_{\mathrm{dc}} + v_{\mathrm{ac}})}{-V_{\mathrm{dc}} (V_{\mathrm{dc}} - v_{\mathrm{ac}})}} & (i_{\mathrm{ref}} < 0) \end{cases} \tag{2.7}$$

, respectively, where f_{sw} denotes the switching frequency.

2.3.6 An Unipolar Switching Scheme for DCM Grid-Tied Inverter

Operation principle

The schematic waveforms and switching patterns of the unipolar switching scheme are shown in Fig. 2.20. This kind of switching scheme is popular in totem-pole bridgeless PFC converters with H-bridge topology [45] and it can also be applied to inverter operation [46].

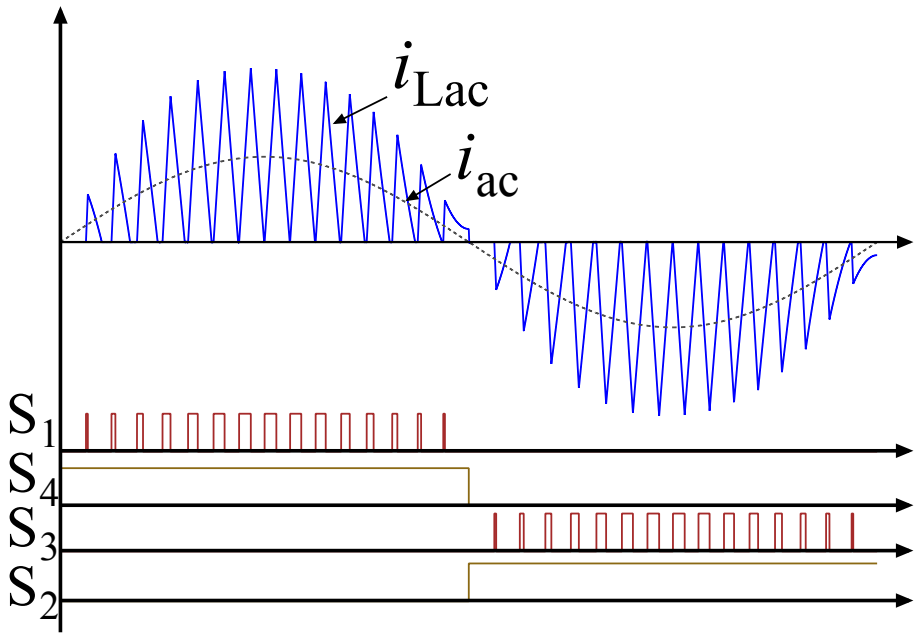

Fig. 2.20 Asymmetry unipolar switching patterns and corresponding inductor waveforms for DCM.

In the unipolar switching scheme, one leg of the inverter (e.g. S_2 and S_4) commutates the current at line frequency (LF) as a rectifier; another leg of the inverter (e.g. S_1 and S_3) switches work at high frequency (HF) with pulse width modulation. The output voltage of inverter switches either between zero and positive DC voltage, $+V_{dc}$, during positive half cycle or between zero and negative DC voltage, $-V_{dc}$, during negative half cycle of the fundamental frequency. It is similar to the well known unipolar switching in CCM control, however, this switching scheme is not symmetrical. Therefore it is referred to as asymmetry unipolar switching scheme. One of the advantages of the asymmetry unipolar DCM is lower switching losses, since only two switches work at high frequency.

The possible current path during one switching cycle with the asymmetry unipolar switching, for positive line voltage, is shown in Fig. 2.21. There are three main intervals during one switching cycle operation. In the following discussions, S_2 and S_4 are assumed to operate at line frequency while S_1 and S_3 being switched at high frequency. The operation

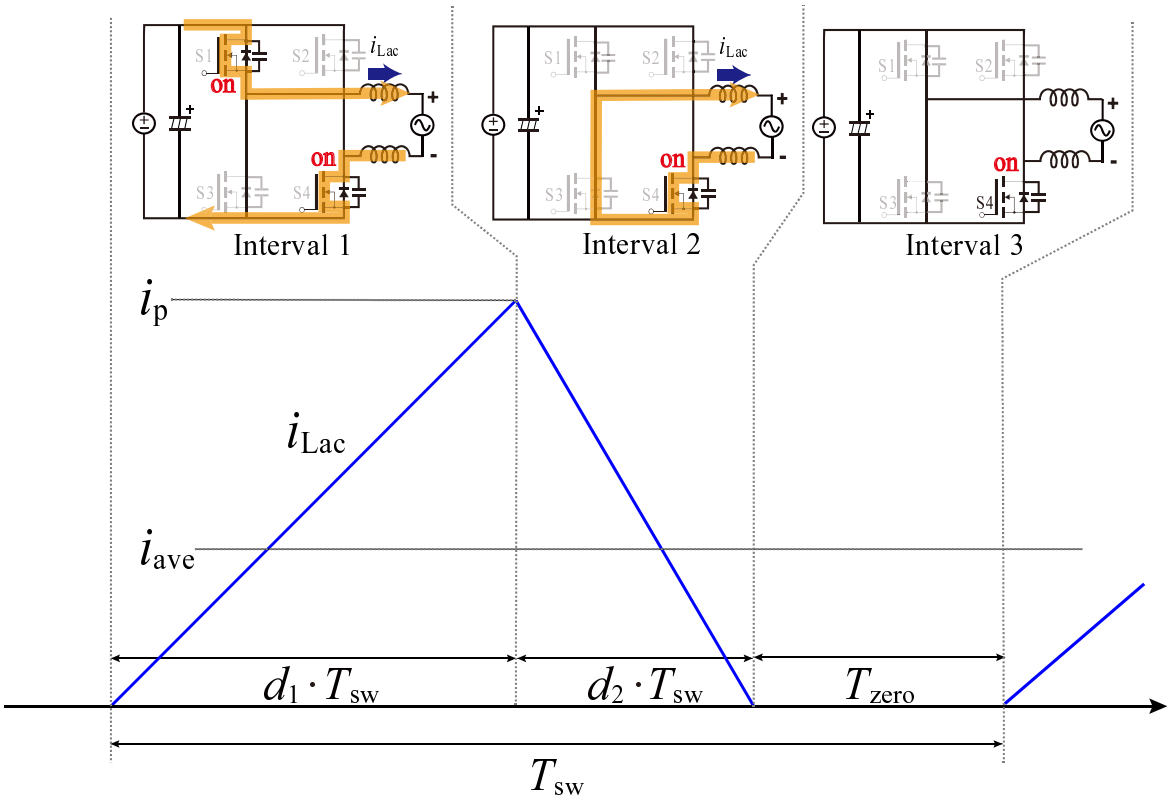

Fig. 2.21 Possible current paths of one switching cycle operation in asymmetry unipolar DCM for positive grid voltage V_{ac}.

principles for positive line voltage only is discussed, since similar principles can also be derived for negative line voltage.

Interval 1:

During interval 1, switches S_1, S_4 are turned on simultaneously, switches S_2, S_3 are in off-state. The inverter-side inductor current, i_{Lac}, increases linearly. The peak value of i_{Lac}, i_p, during this interval can be expressed as

$$i_p = \frac{V_{dc} - v_{ac}}{L_{ac}} d_1 T_{sw}. \tag{2.8}$$

The interval 1 ends when the switch S_1 is turned off.

Interval 2:

During this interval, only S_4 is in on-state. i_{Lac} then decreases linearly through the body diode of S_3. S_3 can be turned-on to achieve the so-called synchronous rectification during this interval. According to the voltage-second balance, i_{p}, during this interval can be expressed as

$$-i_{\mathrm{p}} = \frac{-v_{\mathrm{ac}}}{L_{\mathrm{ac}}} d_2 T_{\mathrm{sw}}, \tag{2.9}$$

where d_2 denotes the duty ratio to achieve the synchronous rectification for S_3. This interval ends when i_{Lac} reduces to zero.

Interval 3:

During this interval, the inductor current should be zero theoretically. After this interval, S_1 is turned on again and a new switching cycle begins.

Model-Based Calculation for Duty Ratios

The average value of i_{Lac} in one switching cycle, i_{ave}, can be expressed as

$$i_{\mathrm{ave}} = \frac{S}{T_{\mathrm{sw}}} = \frac{0.5 i_{\mathrm{p}} (d_1 + d_2) T_{\mathrm{sw}}}{T_{\mathrm{sw}}}, \tag{2.10}$$

The relationship between d_1 and d_2 can be derived from (2.8) and (2.9), and expressed as

$$d_2 = \frac{V_{\mathrm{dc}} - v_{\mathrm{ac}}}{v_{\mathrm{ac}}} d_1. \tag{2.11}$$

i_{ave} during one switching cycle should be equal to the given current reference, i_{ref}. i_{ave} then can be derived form (2.8) and (2.10), and expressed as

$$i_{\mathrm{ref}} = i_{\mathrm{ave}} = \frac{V_{\mathrm{dc}} - v_{\mathrm{ac}}}{2 L_{\mathrm{ac}}} d_1 (d_1 + d_2) T_{\mathrm{sw}}^2. \tag{2.12}$$

The duty ratio for turn-on, d_1, and synchronous rectification, d_2, then can be derived by combining (2.11) and (2.12), and being expressed as

$$d_1 = \begin{cases} \sqrt{\dfrac{2L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}} v_{\mathrm{ac}}}{V_{\mathrm{dc}}(V_{\mathrm{dc}} - v_{\mathrm{ac}})}} & (i_{\mathrm{ref}} > 0) \\ \sqrt{\dfrac{2L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}} v_{\mathrm{ac}}}{V_{\mathrm{dc}}(V_{\mathrm{dc}} + v_{\mathrm{ac}})}} & (i_{\mathrm{ref}} < 0) \end{cases} \tag{2.13}$$

and

$$d_2 = \begin{cases} \sqrt{\dfrac{2L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}} (V_{\mathrm{dc}} - v_{\mathrm{ac}})}{V_{\mathrm{dc}} v_{\mathrm{ac}}}} & (i_{\mathrm{ref}} > 0) \\ \sqrt{\dfrac{2L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}} (V_{\mathrm{dc}} + v_{\mathrm{ac}})}{V_{\mathrm{dc}} v_{\mathrm{ac}}}} & (i_{\mathrm{ref}} < 0) \end{cases} \tag{2.14}$$

, respectively, where f_{sw} is the switching frequency.

2.3.7 LCL Filter Design Procedure

Inverter-Side Inductance Design for Bipolar DCM

The inverter-side inductor current, i_{Lac}, should always be discontinuous even at the maximum power. The duty utilization factor, k, can be expressed by d_1 and d_2, and expanded by using (2.4) as

$$k = d_1 + d_2 = \frac{2V_{\mathrm{dc}}}{V_{\mathrm{dc}} + v_{\mathrm{ac}}} d_1, \tag{2.15}$$

where k is a function of the line phase angle, ωt. The inductance of the inverter-side inductor, L_{ac}, should be designed to make maximum k, k_{max}, to be equal to a given value, which should be less than 1 in order to guarantee the DCM operation and high as possible to reduce i_{p}. The maximum value of d_1, $d_{1.\mathrm{max}}$, then can be easily calculated on the assumption that the AC voltage is sinusoidal, and can be expressed as

$$d_{1.\mathrm{max}} = k_{\mathrm{max}} \frac{V_{\mathrm{dc}} + \sqrt{2} V_{\mathrm{ac}}}{2V_{\mathrm{dc}}}, \tag{2.16}$$

where V_{ac} is the root mean square (r.m.s.) value of the AC voltage.

On the other hand, the average current in one switching cycle, i_{ave}, that should be equal to the instantaneous load current can be expressed as

$$i_{ave} = \frac{kd_1(V_{dc} - \sqrt{2}V_{ac}\sin\omega t)}{2L_{ac}f_{sw}}. \tag{2.17}$$

By substituting $d_{1.max}$ for d_1 and k_{max} for k in (2.17), and assuming the load current with unity power factor, the maximum instantaneous load current, i_{max}, that can be achieved at $\omega t = 90^\circ$, can be expressed as

$$i_{max} = {k_{max}}^2 \frac{{V_{dc}}^2 - 2{V_{ac}}^2}{4V_{dc}L_{ac}f_{sw}}. \tag{2.18}$$

By assuming a sinusoidal current reference, i_{max} can be expressed as

$$i_{max} = \sqrt{2}I_{ac.rated}, \tag{2.19}$$

where $I_{ac.rated}$ is the rated output current in r.m.s. Through (2.18) and (2.19), L_{ac} then can be calculated as

$$L_{ac} \leq {k_{max}}^2 \frac{{V_{dc}}^2 - 2{V_{ac}}^2}{4\sqrt{2}f_{sw}V_{dc}I_{ac.rated}}. \tag{2.20}$$

Inverter-Side Inductance design for Asymmetry Unipolar DCM

It is similar with the inductance designed for the bipolar DCM, the inverter-side inductor current, i_{Lac}, should also be discontinuous even at the maximum power in the asymmetry unipolar DCM. The duty utilization factor, k, then can be expressed by d_1 and d_2, and

expanded by using (2.11) as

$$k = d_1 + d_2 = \frac{V_{\mathrm{dc}}}{v_{\mathrm{ac}}} d_1. \tag{2.21}$$

k is a function of the line phase angle, ωt. The inductance of the inverter-side inductor, L_{ac}, should be designed to make maximum k, $k_{\max}$, to be equal to a given value, which should be less than 1 in order to guarantee the DCM operation and high as possible to reduce i_{p}. The maximum value of d_1, $d_{\mathrm{on.max}}$, then can be easily calculated on the assumption that the AC voltage is sinusoidal, and can be expressed as

$$d_{1.\max} = k_{\max} \frac{\sqrt{2} V_{\mathrm{ac}}}{V_{\mathrm{dc}}}, \tag{2.22}$$

where V_{ac} is the r.m.s value of the AC voltage.

On the other hand, the average current in one switching cycle, i_{ave}, that should be equal to the instantaneous load current can be expressed as

$$i_{\mathrm{ave}} = \frac{k d_1 (V_{\mathrm{dc}} - \sqrt{2} V_{\mathrm{ac}} \sin \omega t)}{2 L_{\mathrm{ac}} f_{\mathrm{sw}}}. \tag{2.23}$$

By substituting $d_{1.\max}$ for d_1 and $k_{\max}$ for k in (2.23), and assuming the load current with unity power factor, the maximum instantaneous load current, $i_{\max}$, that can be achieved at $\omega t = 90^\circ$, can be expressed as

$$i_{\max} = {k_{\max}}^2 \frac{\sqrt{2} V_{\mathrm{dc}} V_{\mathrm{ac}} - 2 {V_{\mathrm{ac}}}^2}{2 V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}}}. \tag{2.24}$$

By assuming a sinusoidal current reference, $i_{\max}$ can be expressed as

$$i_{\max} = \sqrt{2} I_{\mathrm{ac.rated}}, \tag{2.25}$$

where $I_{\text{ac.rated}}$ is the rated output current in r.m.s. Through (2.24) and (2.25), L_{ac} then can be calculated as

$$L_{\text{ac}} \leq {k_{\max}}^2 \frac{\sqrt{2}V_{\text{dc}}V_{\text{ac}} - 2{V_{\text{ac}}}^2}{2\sqrt{2}f_{\text{sw}}I_{\text{ac.rated}}V_{\text{dc}}}. \tag{2.26}$$

Parameter Design for LC Filter

The capacitance and inductance of the filter capacitor and inductor can be determined to achieve acceptable ripples in the capacitor voltage and grid-side current. It is assumed that all of the high frequency components in i_{Lac} flow into the filter capacitor, C_{f}. The maximum ripple of the capacitor voltage should be limited to an acceptable level after the capacitance of C_{f} is determined, therefore C_{f} can be calculated as

$$C_{\text{f}} \geq \frac{i_{\text{p.max}}}{8f_{\text{sw}}v_{\text{ripple.max}}}, \tag{2.27}$$

where $i_{\text{p.max}}$ is the maximum peak to peak value of i_{Lac}, $v_{\text{ripple.max}}$ is the maximum allowable voltage ripple of C_{f}.

The maximum current ripple of i_{ac} should also be limited to an acceptable level after the inductance of L_{f} is determined, therefore L_{f} can be calculated as

$$L_{\text{f}} \geq \frac{\Delta v_{\max}}{8f_{\text{sw}}i_{\text{ripple.max}}}, \tag{2.28}$$

where $i_{\text{ripple.max}}$ is the maximum acceptable ripple of i_{ac}.

2.4 Problems with Model-Based Control for DCM

2.4.1 Classification of Current Distortions

The current control method discussed above are all based on model-based control and feed-forward. However, such kind of control strategy has one drawback. The current distortions can be generated with the applying of an imperfect model to the controller. The distortions cannot be corrected adaptively since the current control is not feedback. This problem makes the model-based control sometimes impractical for the grid-tied inverter application, since the harmonics current should fall below the grid standards.

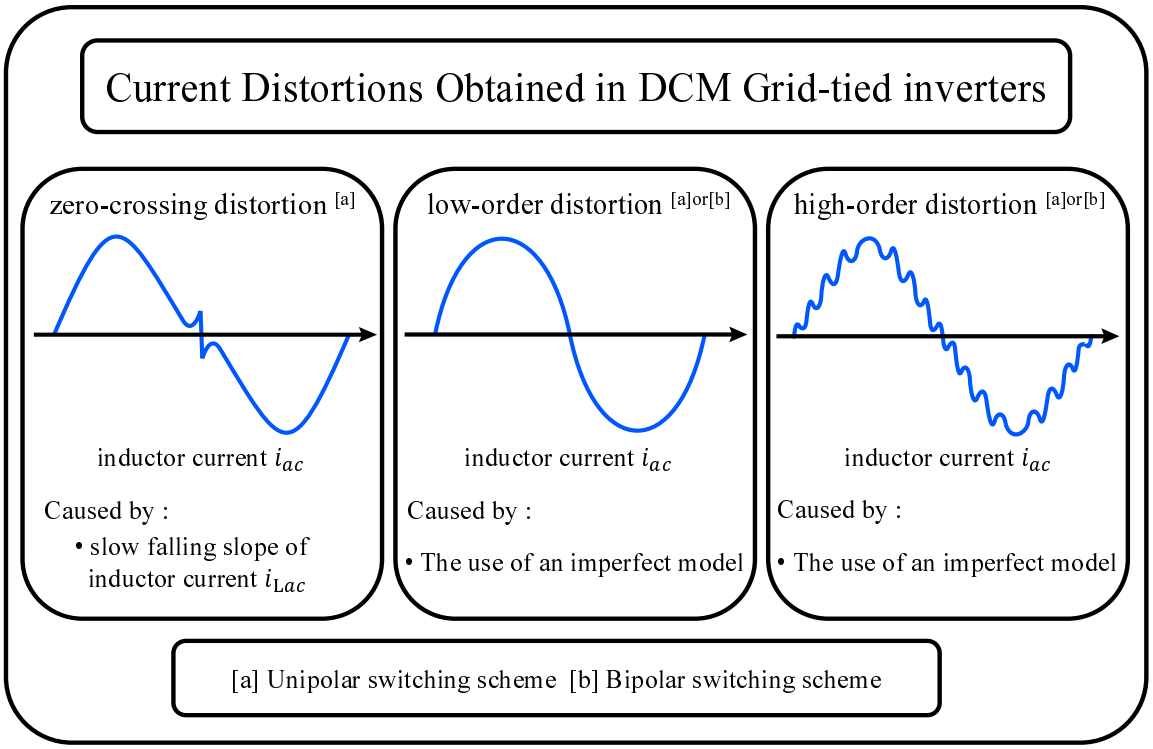

Fig. 2.22 Current distortions that can be obtained in DCM grid-tied inverters.

Fig. 2.22 depicts a classification of current distortions that can be obtained in a DCM grid-tied inverter. In this dissertation, the current distortions can be divided into three different types: zero-crossing distortion, low-order harmonic distortions and high-order harmonic distortions. The distortions can be caused by different reasons, such as the applied switching

schemes or the use of an imperfect model. These distortions will be discussed in the following sections. However, only the distortions caused by periodic errors are discussed.

2.4.2 Zero-Crossing Distortion

Over the past decades, the current distortion around zero-crossing areas is a common problem and it has been widely reported and studied in both AC/DC and DC/AC converters with CCM design [47–63]. Basically, the switching scheme used in a CCM grid-tied inverter can be both unipolar and bipolar. Many previous studies have pointed out that the zero-crossing distortion usually occurs in an inverter with unipolar PWM modulation [64–67]. In reference [64], the distortion caused by switching delays was studied. In reference [65], the slope of the actual current less than the reference current around zero-cross was ascribed as the reason for the zero-crossing distortion. In reference [66], it was reported that the narrow gate pulse around zero-cross can cause a pulse dropping effect and result in zero-crossing distortion. In reference [67], the distortion can be generated with non-unity power factor (PF) operation. The voltage may not be sufficient to magnetize the inductor current and that results in the zero-crossing distortion.

It is similar with the unipolar switched inverter with CCM, the zero-crossing distortion can also occur in DCM gird-tied inverters with unipolar switching. The main reason can be explained by the slow slope of inductor current in unipolar switching. In contrast to the unipolar switched inverter, however, the problem of zero-crossing distortion is negligible in the bipolar switched inverter. As a possible solution, a hybrid PWM modulation can be used to avoid the current distortion by operating with bipolar PWM around zero-cross, while unipolar PWM is applied for other switching cycles [66, 67]. To the best of the author's knowledge, this concept, however, has not been provided to the grid-tied inverter with DCM operation.

2.4.3 Low-Order Harmonic Distortions

In CCM designed grid-tied inverters, the low-order harmonics in the output current can be caused by the use of dead-time. The dead-time must be inserted to avoid the conduction overlap of high-side and low-side switches of one leg. However, the use of dead-time can cause a voltage error therefore distort the current around zero-cross. The dead-time compensation can be applied to compensate the voltage error and reduce the distortion [68–73].

On the other hand, the use of dead-time can also cause a zero-current-clamping effect around zero-cross where the operation mode changes from CCM to DCM. The dynamic changes suddenly between CCM and DCM. Consequently, a current controller designed for CCM only unable to control the DCM current well due to the different dynamic. As a result, the current becomes distorted. A dedicated current controller that being designed to control both CCM and DCM current is required to deal with this kind of mixed conduction mode (MCM) operation [24, 74, 75].

The model built for the DCM operation is the key in the model-based control. A perfect model achieves zero control errors between reference and output current. However, it is impractical to obtain such perfect model in real applications. The use of an imperfect model can cause some problems in the output current, such as low-order harmonic distortions. The low-order harmonics can be possibly caused by nonlinear characteristics of the B–H curve of the magnetic core, the use of dead-time, voltage drops on the semiconductor switches or cables or oscillations in the DC-link voltage or grid voltage [76–78]. In order to meet the harmonic standards being given from the grid, such as EN61000-3-2 [79] or IEEE1547 [80], it is of importance to eliminate these low-order harmonics. The influences of oscillations in the DC-link voltage or grid voltage, the use of dead-time and voltage drops on the semiconductor switches or cables are analyzed and discussed by a simulation software in the following text.

The Use of an Ideal Model

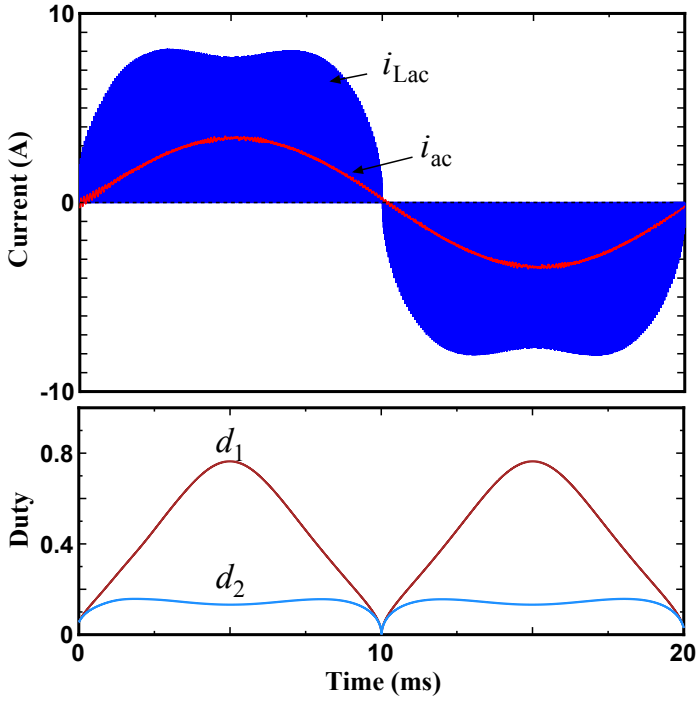

Fig. 2.23 Time domain simulation of a bipolar DCM modulation under a certain design specification. $V_{dc} = 400$ (V), $V_{ac} = 200$ (V), $f_{sw} = 100$ (kHz), $I_{rated} = 2.4$ (A), $L_{ac} = 119$ (μH), $L_f = 125$ (μH), $C_f = 2.2$ (μF).

Fig. 2.23 shows a simulation result of inverter-side inductor current, grid-side inductor current, and duty ratios with the bipolar DCM modulation at rated current operation. The simulation was conducted with an ideal model being considered. A clean sinusoidal waveform can be obtained in the grid-side inductor current, i_{ac}. It can also be observed that the peak values of i_{Lac} are not always two times higher than i_{ac}. These values are dependent on the ratio between DC-link voltage and grid voltage. In addition, the calculated duty ratios, d_1 and d_2, are non-linear over half line cycle. These duty ratios clearly demonstrate that how the model-based calculation compensate for the non-linear characteristics in the DCM. The harmonic components i_{ac} are calculated and shown in Fig. 2.24. Only slight third-order harmonic is obtained while other harmonics being almost zero. The total harmonic distortion of i_{ac} is 0.7%.

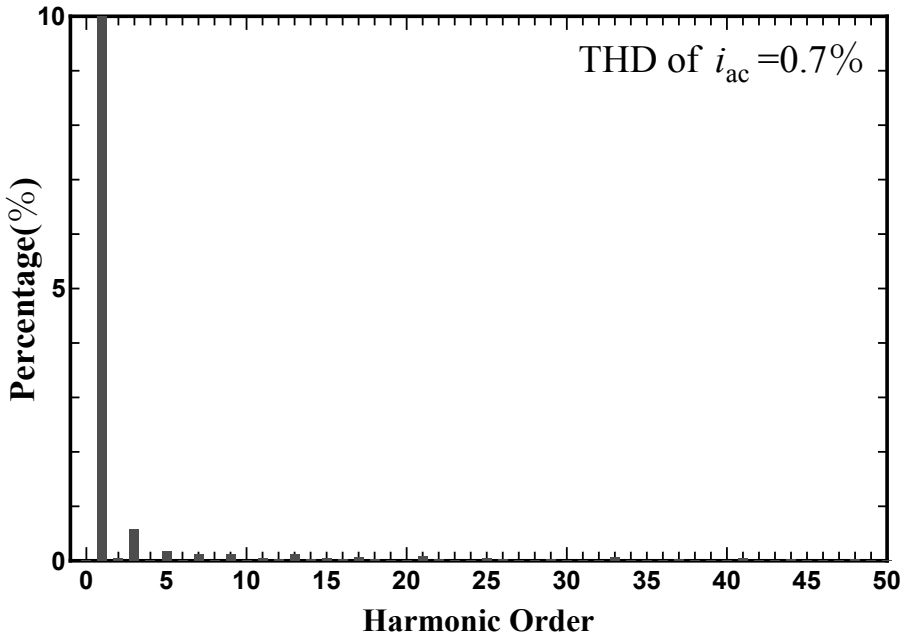

Fig. 2.24 Harmonic components in the grid-side inductor current i_{ac}.

Oscillation of DC-link Voltage

For a single-phase grid-tied inverter, an oscillation with frequency that corresponds to twice the line frequency can be obtained in the DC-link voltage. A large DC-link capacitor is usually required to decouple the double line frequency ripple of voltage. However, it is impractical to maintain a constant DC voltage since the required capacitance can be too large. Generally, the capacitance of the DC-link capacitor is designed to make the ripple voltage being within acceptable ranges. The oscillation in the DC-link voltage thus can cause low-order harmonics in the output current.

Fig. 2.25 shows a simulation result of conventional bipolar DCM when oscillating voltage with 5% of the DC voltage is considered in the DC-side. The distorted grid-side inductor current, i_{ac}, can be observed. The oscillating voltage in the DC-side results in higher or lower voltage being applied on the inverter-side inductor. Consequently, the average value of i_{Lac} can no longer follow the reference if the duty ratios is calculated on the basis of a constant DC-link voltage. This problem, however, can be addressed by taken the oscillating V_{dc} into

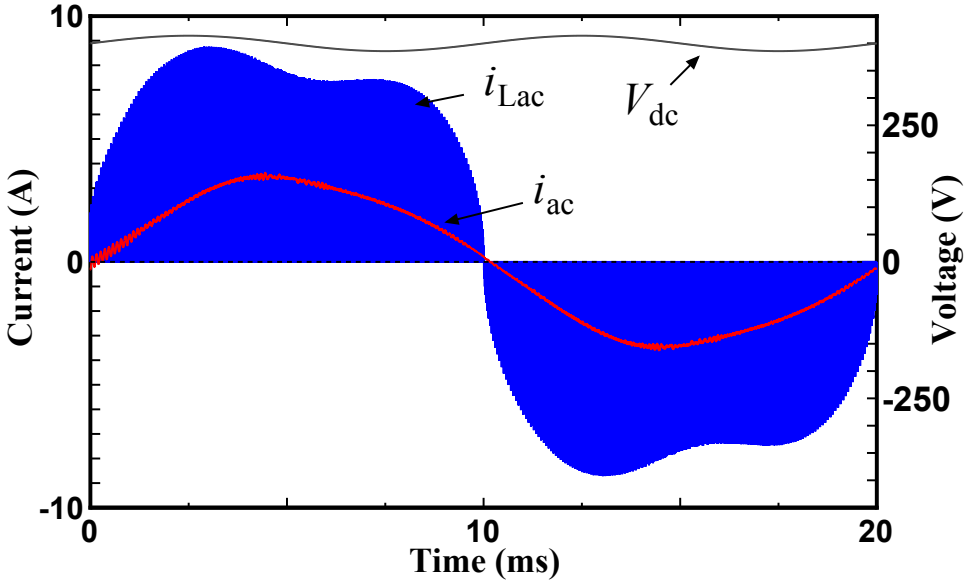

Fig. 2.25 Time domain simulation of a bipolar DCM modulation when oscillating voltage with 5% of the DC voltage is considered in the DC-side. Simulation conditions: $V_{dc} = 400$ (V), $V_{ac} = 200$ (V), $f_{sw} = 100$ (kHz), $I_{rated} = 2.4$ (A), $L_{ac} = 119$ (μH).

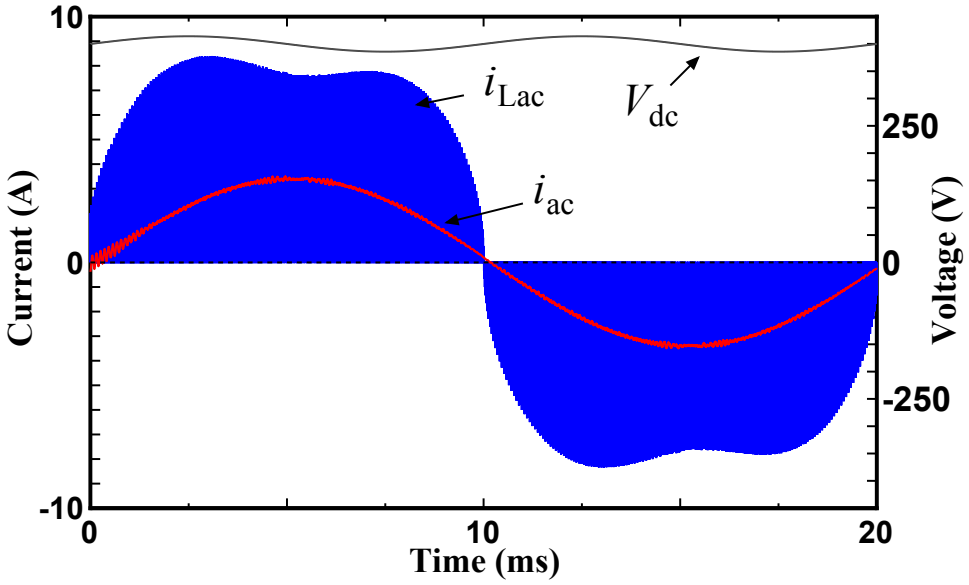

Fig. 2.26 Time domain simulation of a bipolar DCM modulation when V_{dc} is measured and its values are used in the duty calculation. Simulation conditions: $V_{dc} = 400$ (V), $V_{ac} = 200$ (V), $f_{sw} = 100$ (kHz), $I_{rated} = 2.4$ (A), $L_{ac} = 119$ (μH).

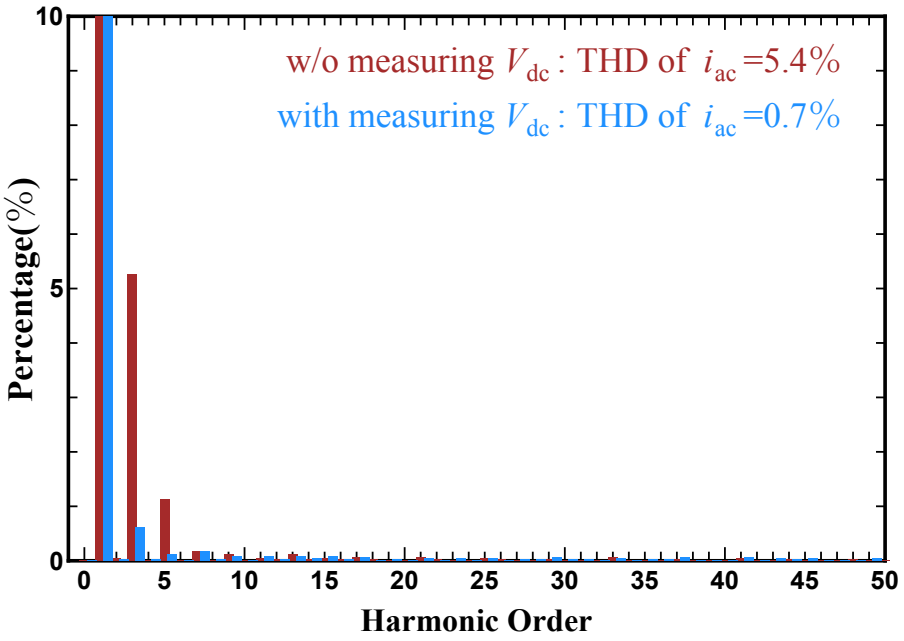

Fig. 2.27 Harmonic components in the grid-side inductor current i_{ac}.

account in the duty ratio calculations. Fig. 2.26 shows the simulation results in the case of V_{dc} being measured and its values being used in the duty calculation. The effect caused by the oscillating V_{dc} is corrected. Fig. 2.27 shows the harmonic components in i_{ac} for these two cases. It can be obtained that the oscillating V_{dc} mainly results in high low-order harmonics being obtained in the output current, particularly the third harmonics. The high low-order harmonics are reduced after the variation of V_{dc} is taken into account in the duty calculation. The THD of i_{ac} is then reduced from 5.4% to 0.7%.

Distortion of Grid Voltage

Fig. 2.28 shows a simulation result under distorted grid-voltage, V_{ac}. 3% of third-order harmonic in V_{ac} is considered. It is similar with the previous case, the current distortions can also be observed under distorted grid voltage. The distorted V_{ac} can cause effects, that is similar with the oscillating DC-link voltage, on the average current. Therefore, this problem can also be addressed by using the instantaneous values of v_{ac} in the duty calculations. This concept is similar with the grid-voltage feed-forward that used in CCM grid-tied inverter [81].

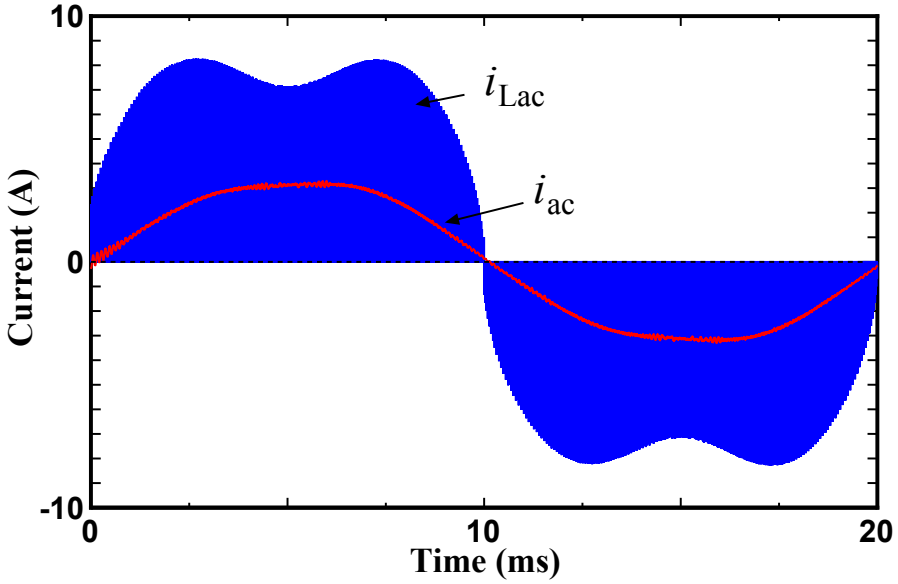

Fig. 2.28 Time domain simulation of a bipolar DCM modulation under distorted V_{ac} with 3% of third-order harmonic being considered. Simulation conditions: $V_{dc} = 400$ (V), $V_{ac} = 200$ (V), $f_{sw} = 100$ (kHz), $I_{rated} = 2.4$ (A), $L_{ac} = 119$ (μH).

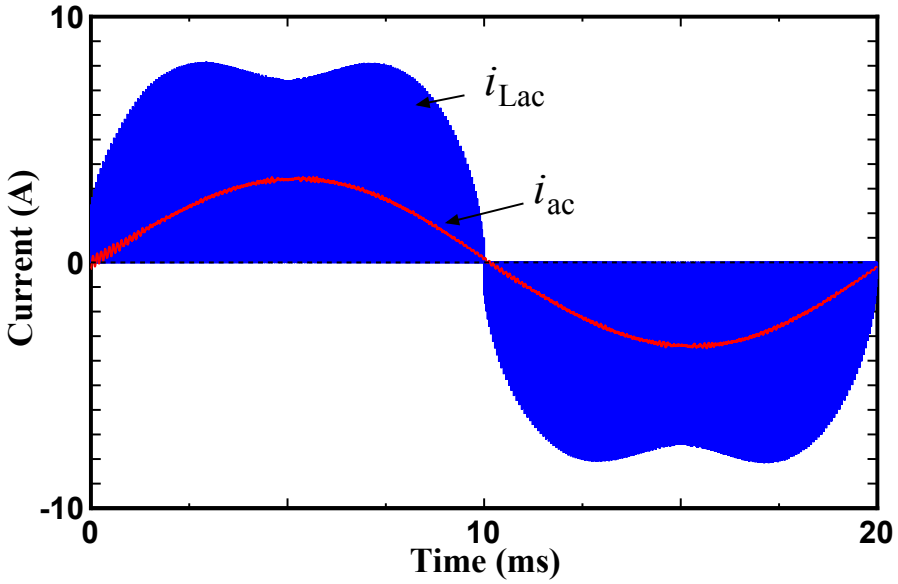

Fig. 2.29 Time domain simulation of a bipolar DCM modulation when v_{ac} is measured and its values are used in the duty calculation. Simulation conditions: $V_{dc} = 400$ (V), $V_{ac} = 200$ (V), $f_{sw} = 100$ (kHz), $I_{rated} = 2.4$ (A), $L_{ac} = 119$ (μH).

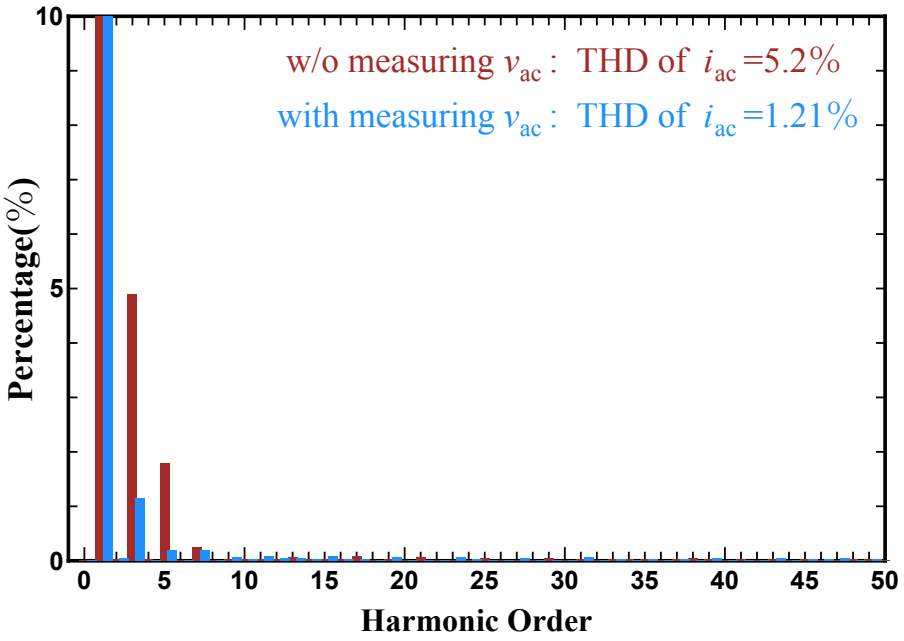

Fig. 2.30 Harmonic components in the grid-side inductor current i_{ac}.

Fig. 2.29 shows the simulation results with instantaneous v_{ac} being measured and used in the duty calculation. Fig. 2.30 shows the harmonic components in i_{ac} for these two cases. The distortion in the grid voltage also results in low-order harmonics being obtained in i_{ac}, particularly the third harmonic. The low harmonics are reduced after v_{ac} being used in the duty calculation. The THD of i_{ac} is then reduced from 5.2% to 1.21%.

Effect of Dead-Time and Voltage Drops

In CCM grid-tied inverters, the use of dead-time results in an effect of lost on the the inverter output voltage. This effect can cause current distortions around zero-crossing areas. This distortion is proportional to the switching frequency. It is similar with the dead-time effect occurred in CCM, this problem can also be obtained in DCM. Fig. 2.31 shows a simulation result of bipolar DCM modulation with dead-time of 500 (ns) being considered. Distortion around zero-crossing areas can be observed. Fig. 2.32 shows the harmonic components in i_{ac}. The low-order harmonics, particularly the third harmonic, can be caused by the dead-time effect.

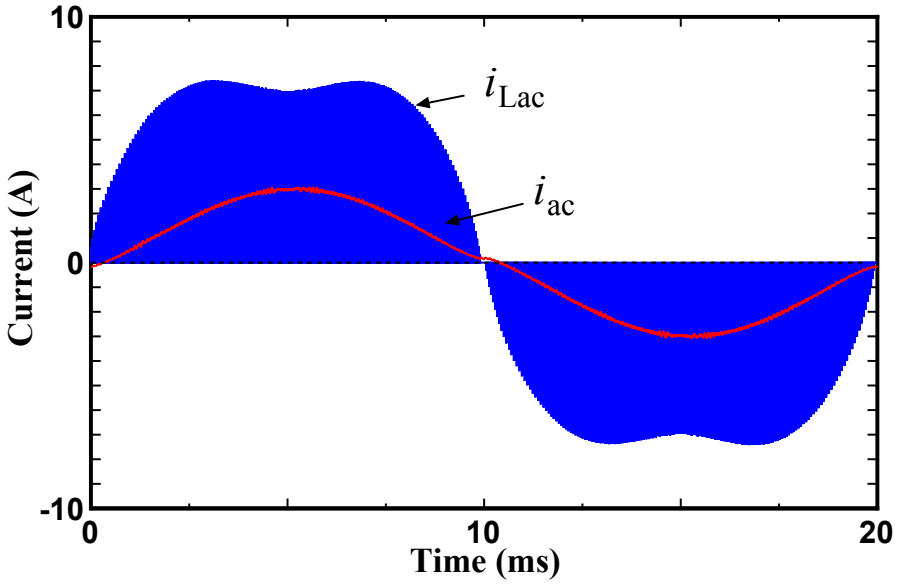

Fig. 2.31 Time domain simulation of a bipolar DCM modulation with dead-time of 500 (ns) being considered. Simulation conditions: $V_{dc} = 400$ (V), $V_{ac} = 200$ (V), $f_{sw} = 100$ (kHz), $I_{rated} = 2.4$ (A), $L_{ac} = 119$ (μH).

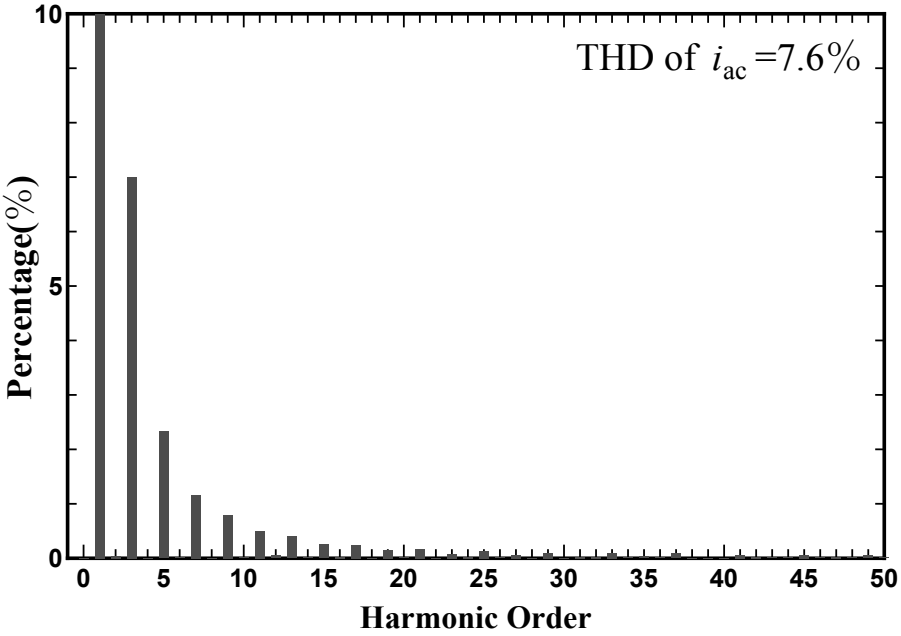

Fig. 2.32 Harmonic components in the grid-side inductor current i_{ac}.

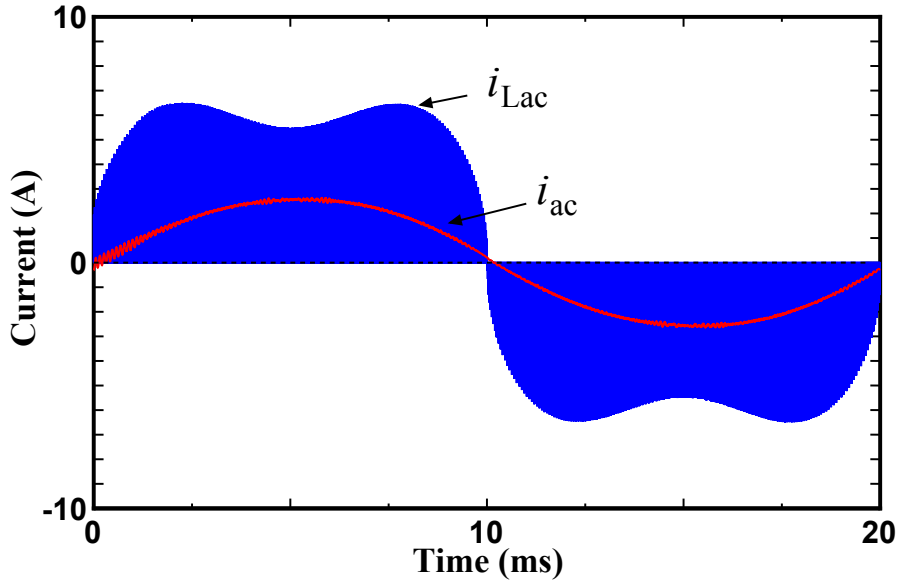

Fig. 2.33 Time domain simulation of a bipolar DCM modulation when 10 Ω of resistive components in the DC-bus being considered. Simulation conditions: $V_{dc} = 400$ (V), $V_{ac} = 200$ (V), $f_{sw} = 100$ (kHz), $I_{rated} = 2.4$ (A), $L_{ac} = 119$ (μH).

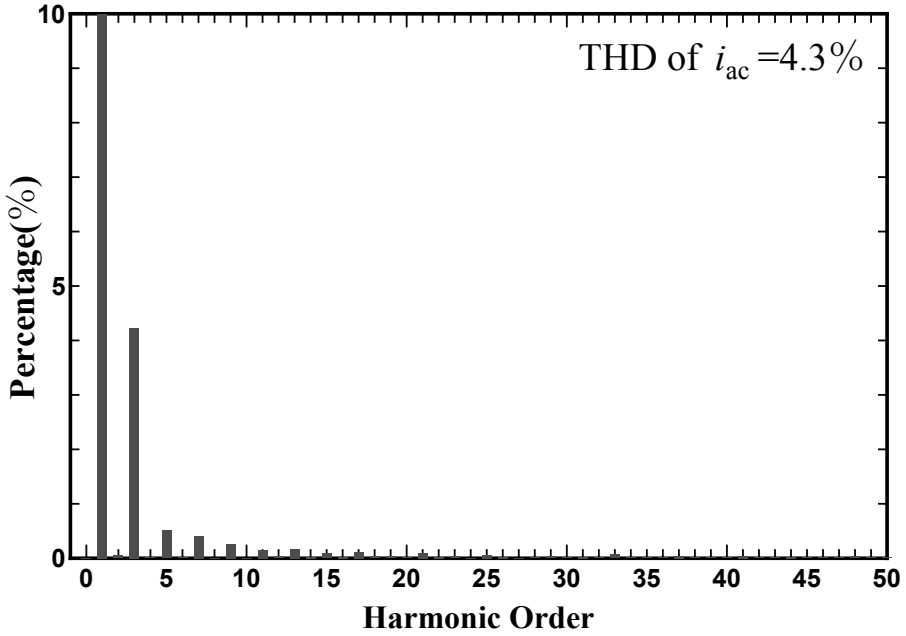

Fig. 2.34 Harmonic components in the grid-side inductor current i_{ac}.

The effect caused by voltage drops due to the resistive components is similar with the effect of lost on the inverter output. Fig. 2.33 shows a simulation result of bipolar DCM modulation when 10 Ω of resistive components in the DC-bus being considered. Fig. 2.34 shows the harmonic components in i_{ac}. The high third-harmonic can also be obtained in this case.

The oscillating DC-link voltage and distorted grid voltage can be measured and the effect of them can be corrected in the DCM model easily. However, the effect caused by the use of dead-time or voltage drops or other possible reasons, such as the non-linearity of B-H curve in the magnetic cores or limited PWM resolution [76], cannot be expressed by mathematical model in a simple way. Nevertheless, it is difficult to take all the possibilities into considerations when the DCM model being built. Consequently, the resultant distortions, particularly the third harmonic, cannot be corrected adaptively under conventional feed-forward control.

In CCM grid-tied inverters with linear controls, several approaches have been proposed to eliminate the low-order harmonics, such as by applying the selective harmonic compensation [82–84] or by the use of repetitive controllers [85]. However, solutions to the low-order harmonics for a DCM grid-tied inverter with model-based control are seldom reported.

2.4.4 High-Order Harmonic Distortions Caused by Parasitic Capacitance

This kind of distortion does not occur in CCM grid-tied inverters, however, it can be obtained in DCM grid-tied inverters. The distortion is caused by the use of an imperfect DCM model. In the DCM, the inductor current, i_{Lac}, is discontinuous and that results in a zero-current interval in every switching cycle. Conventionally, i_{Lac} is assumed to be zero during this interval. Therefore, the initial current at the next turn-on instant should be zero, as shown in Fig. 2.35. In practical; however, the switches are usually turned on with non-zero i_{Lac}

due to the resonance between inductor and parasitic capacitor of switching devices. This is referred to as non-uniform turn-on behavior [86, 87]. The non-zero initial current can

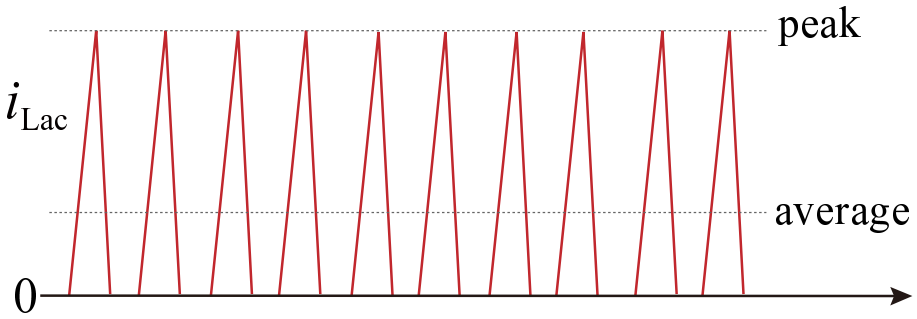

Fig. 2.35 Schematic views of the inverter-side inductor current caused by ideal turn-on behavior.

affect the average inductor current, as shown in Fig. 2.35; consequently, the output current becomes distorted, as shown in Fig. 2.37. The harmonic orders in the output current is usually around 20 th to 40 th. Therefore, this kind of distortion is referred to as high-order harmonic distortions. For a given switching device, the high-order distortions can become worse under higher switching frequencies; or for a given switching frequency, the distortion can be severe with a large parasitic capacitance is applied to the switching device. As a possible solution, the achievement of uniform turn-on, which means the initial inductor current at turn-on instant are the same, can be applied to reduce the high-order harmonic distortion. However,

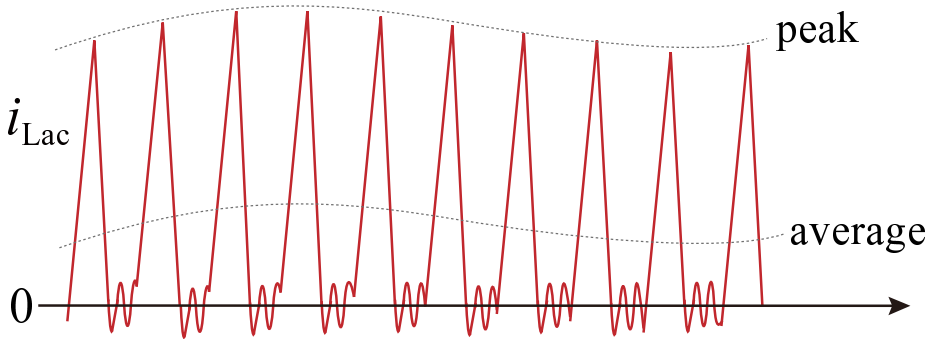

Fig. 2.36 Schematic views of the inverter-side inductor current caused by non-uniform turn-on behavior.

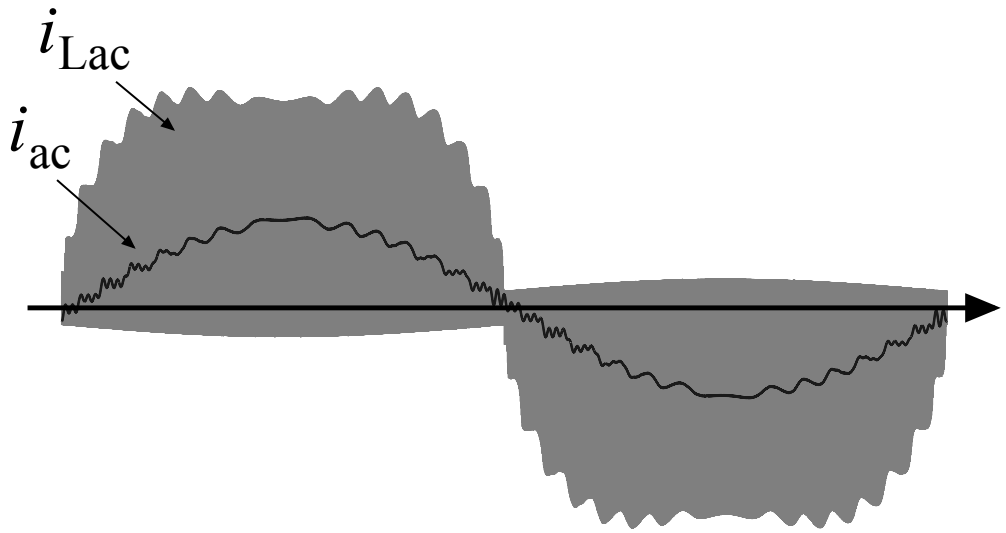

Fig. 2.37 Current distortion caused by non-uniform turn-on behavior.

this purpose cannot be realized with the conventional model-based DCM controls due to the low control degree of freedom.

2.5 Hybrid Control of Model-Based Control and Linear Feedback

2.5.1 Basic Structure

Generally, the model-based controller can be applied to DCM without using feedback, because the accumulated errors can be reset in every cycle. However, the control errors (i.e. current distortions) can be caused by inherent problem of switching scheme or by the use of imperfect models. The model-based controller unable to correct the errors adaptively, since it is feed-forward based. In CCM current control, several harmonic compensators (HCs) can be cascaded to a proportional-resonant (PR) controller to perform selective harmonic compensation (SHC) [88–90]. This concept can also be applied to the model-based controller for DCM grid-tied inverter.

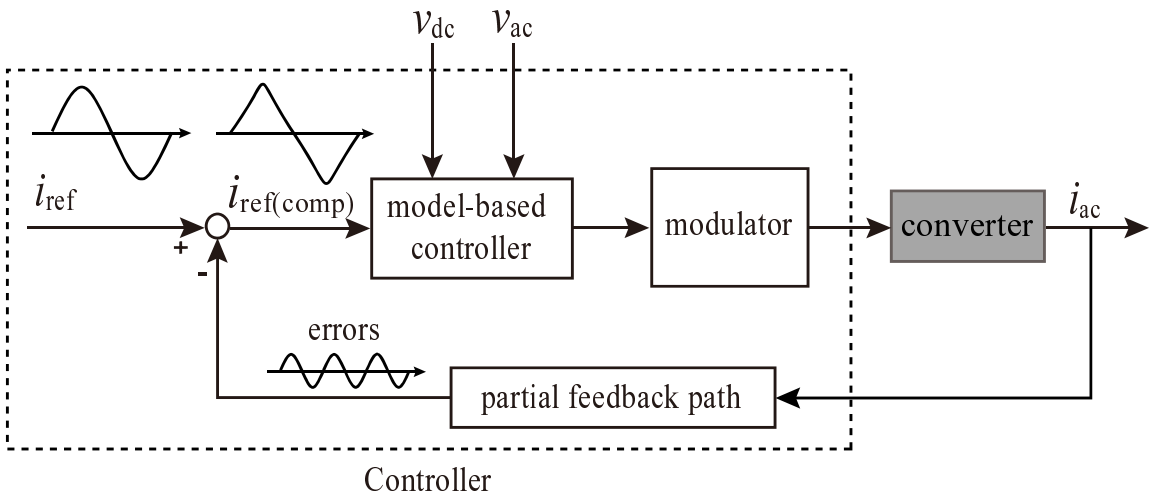

Fig. 2.38 Block diagram of a feed-forward control with partial feedback.

Fig. 2.38 shows a hybrid control concept of model-based control with linear feedback [91]. The basic concept of this control is to feed back the errors and modified the reference current, which is different from the linear PI control. Therefore, it is referred to as partial feedback control in this dissertation. Firstly, the errors between the output and reference current are extracted from the output current. The errors are then subtracted from the reference current. After that, the duty ratios are calculated on the basis of the compensated reference. To realize this purpose, the grid-side inductor current is sensed. It is relatively easy to sense the grid-side inductor current, since it is 50 Hz with small switching ripples. Therefore, the high frequency and low delay sensor is not essential in this case.

The partial feedback control can be used to eliminate low-order harmonics in the output current, i_{ac}, by modifying the current reference. Take the elimination for third harmonic as an example: if the third order harmonic is caused by periodic errors, it can be eliminated by injecting a compensation signal, $i_{ac(3)}$, to the reference current, i_{ref}, as depicts in Fig. 2.39. Similar concepts can also be applied to eliminate other low-order harmonics. In order to obtain the compensation signal, the amplitude and phase angle of the harmonic components

are required. These information can be obtained by extracting the harmonic components from the output current by means of a second order generalized integrator.

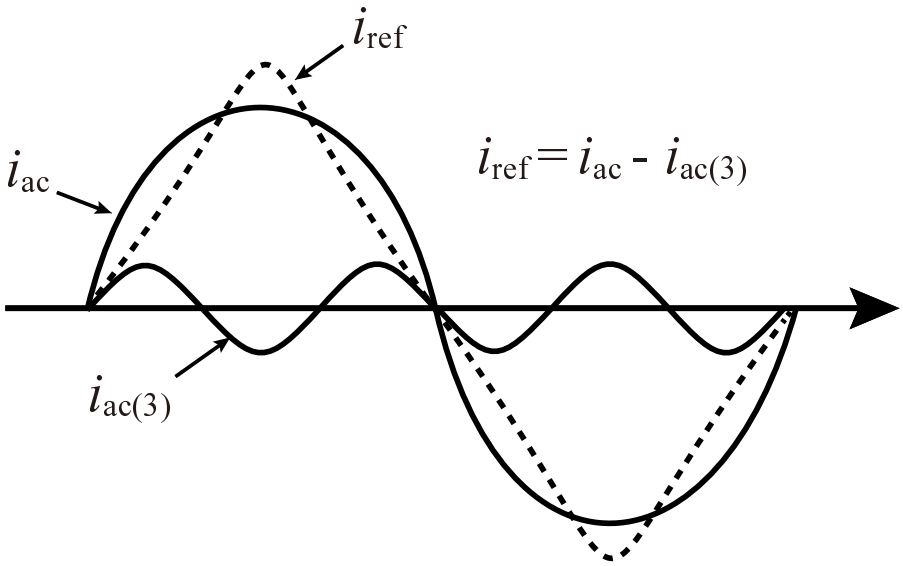

Fig. 2.39 The third-order harmonic can be cancelled by injecting a compensation signal, $i_{ac(3)}$, to the reference current, i_{ref}.

2.5.2 Second Order Generalized Integrator

The second order generalized integrator (SOGI) [92], which is also referred to as resonant controller, can be used to extract certain harmonic components from the output current. The transfer function of a modified version of the SOGI can be expressed as [93]

$$G(s) = \frac{i'(s)}{i(s)} = K_{\mathrm{p}} \frac{\omega s}{s^2 + \omega^2}, \tag{2.29}$$

where K_{p} is the control gain, ω is the grid angular frequency and the grid frequency is 50 Hz in this dissertation. Theoretically, the SOGI can achieve infinity gain at the resonant frequency and almost without gain outside of the resonant frequency [88]. (2.29) can be decomposed into two simple integrators in continuous time-domain, as shown in Fig. 2.40.

Fig. 2.41 depicts the bode plot of (2.29) with different $K_{\mathrm{p}} = 0.1, 1, 10$ and $\omega = 2 \cdot \pi \cdot 50$ being applied. A very high gain is achieved at the resonant frequency with a narrow frequency band being around the resonant frequency, which is at 50 Hz in this case. The gain and bandwidth are dependent on the control gain, as shown in the upper plot of Fig. 2.41. This feature of SOGI makes it suitable as a notch filter that being used to extract certain harmonics.

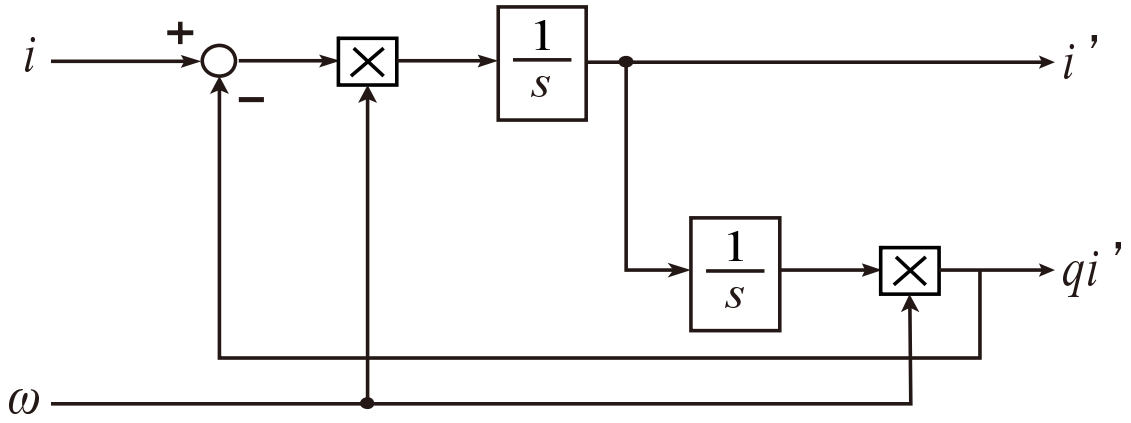

Fig. 2.40 Control block diagram of a second order generalized integrator in continuous time-domain.

Fig. 2.42 depicts the response of the SOGI in continuous time-domain. The input signal is a 50 HZ sinusoidal signal with $\omega = 2 \cdot \pi \cdot 50$ being set in the SOGI (i.e. the SOGI is tuned at 50 Hz). It can be obtained from Fig. 2.42 that the output of SOGI is also a 50 Hz signal with integrated amplitude and without any phase delay being obtained. If the SOGI is tuned at other frequencies, it can be used to extract the harmonics at those frequencies from the input signal. In this case, the SOGI can be treated as a harmonic compensator (HC) [88–90]. The transfer function of HCs that being designed to compensate certain harmonics can be expressed as

$$\sum_{h=2}^{h} G_{\mathrm{h}}(s) = K_{\mathrm{p(h)}} \frac{\omega s}{s^2 + (\omega \cdot h)^2}, \tag{2.30}$$

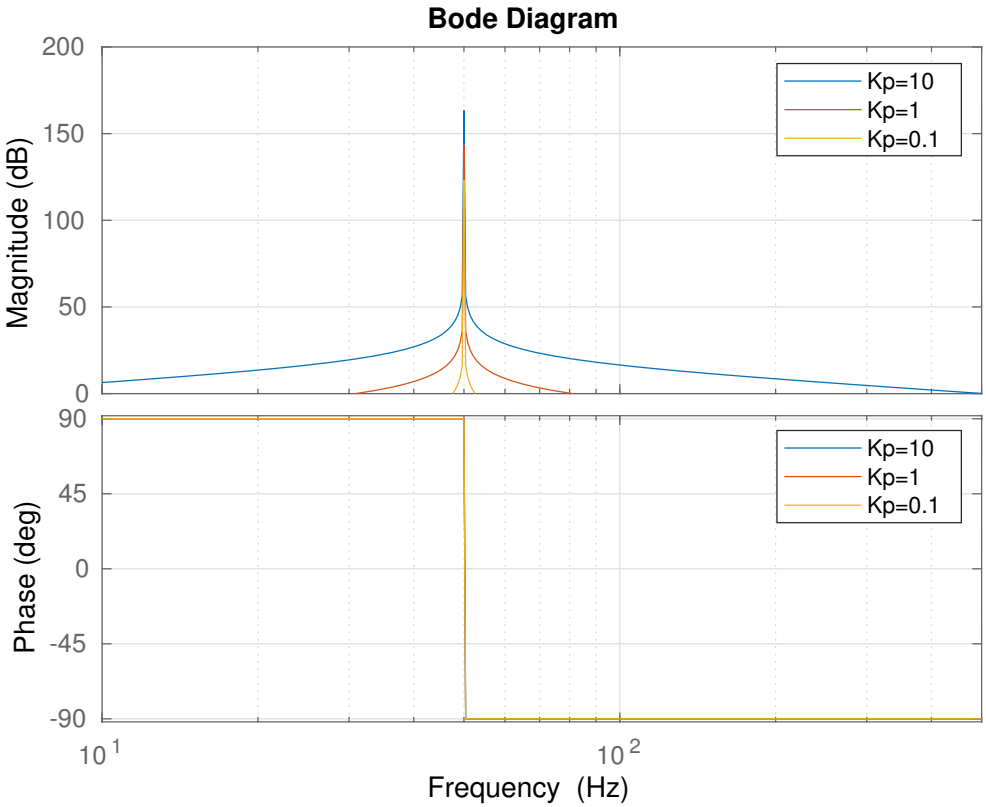

Fig. 2.41 Bode plot of the SOGI with different $K_{\mathrm{p}} = 0.1, 1, 10$ and $\omega = 2 \cdot \pi \cdot 50$ being applied.

where $K_{\mathrm{p(h)}}$ being the proportional gain designed for the certain harmonic and h being the harmonic order.

Fig. 2.43 depicts the response of the SOGI when the input contains third-order harmonic. The SOGI in this case is tuned at 3ω in order to extract the third-order component from the input signal. The 150 Hz signal with integrated amplitude being in phase with the fundamental signal can be obtained from the output of the SOGI.

2.5.3 Operation Principle of Low-Order Harmonic Compensation

Fig. 2.44 shows the operation principle of the low-order harmonic compensation using the resonant controller. The grid frequency is 50 Hz in all the experiments and simulations shown in this dissertation. i_{ac} is sensed by a current sensor and its value is input into the

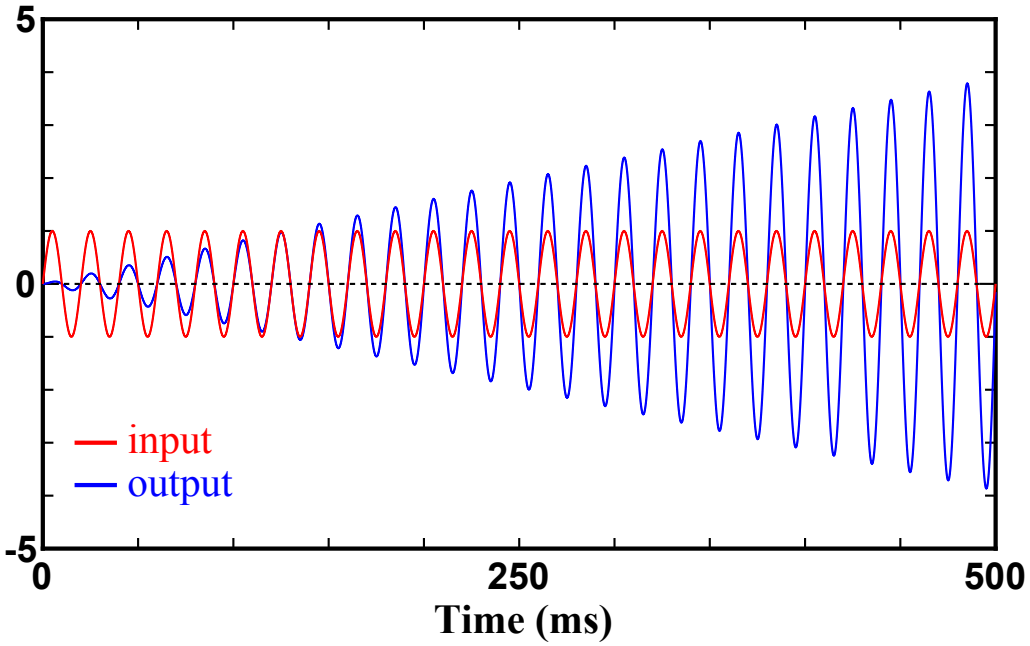

Fig. 2.42 Time-domain simulation of the input and output waveforms of a SOGI. K_p is set to be 0.1. The frequency of the input signal is 50Hz and SOGI being tuned at 50 Hz.

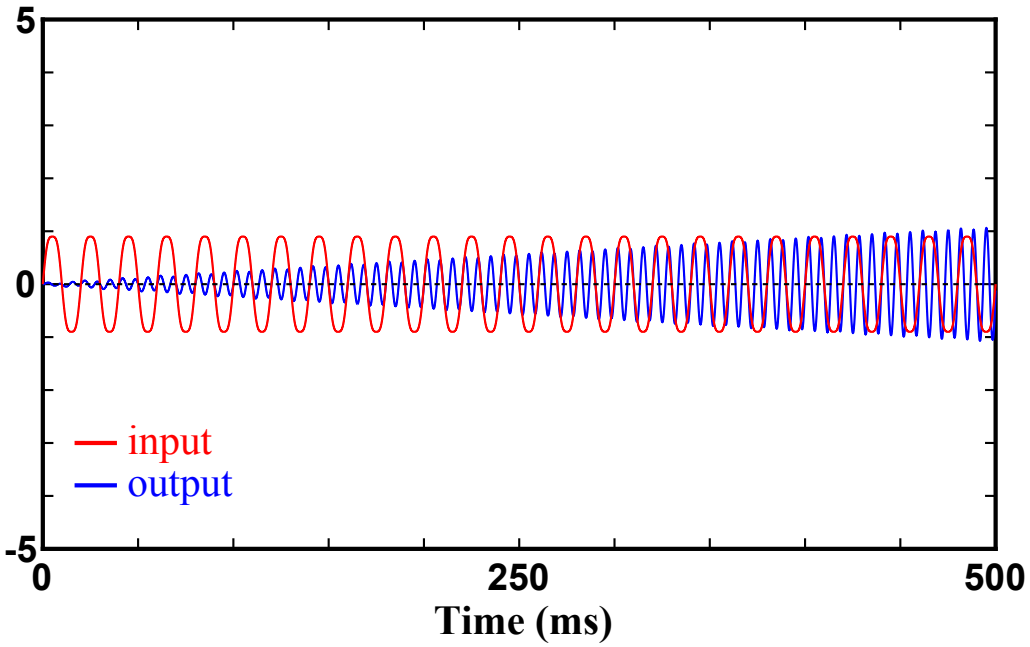

Fig. 2.43 Time-domain simulation of the input and output waveforms of a SOGI. K_p is set to be 0.1. The frequency of the input signal is 50Hz that contains 10% third-order harmonic and SOGI being tuned at 150 Hz

SOGIs tuned at the frequencies of the target harmonics. The band-passed in-phase signals with integrated amplitude, $i_{\mathrm{ac}(n)}$, are generated by the SOGIs and they are subtracted from the original current reference, i_{ref}. The duty ratio, d, is calculated base on the compensated current reference, $i_{\mathrm{ref(comp)}}$.

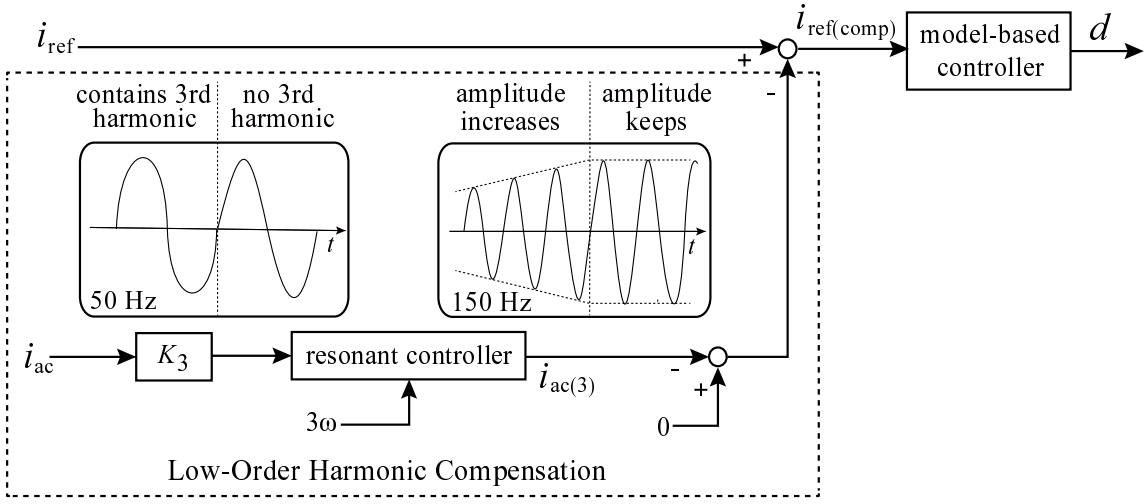

Fig. 2.44 Operation principles of the low-order harmonics compensation. The elimination of third-order harmonic is taken as an example.

The harmonic components in i_{ac} is reduced along with the increasing amplitude of $i_{\mathrm{ac}(n)}$, and the amplitude of $i_{\mathrm{ac}(n)}$ keeps constant after the disappearance of the harmonic components in i_{ac}. In other words, the compensation signals, $i_{\mathrm{ac}(n)}$, are always generated to compensate for the corresponding harmonic components in i_{ac} through this kind of partial feedback.

The experimental verification of the partial feedback control with respective to the low-order harmonic compensation is shown in Appendix A. On ther other hand, the zero-crossing distortions caused by inherent problem of switching scheme and the high-order harmonic distortions are difficult to be eliminated with the partial feedback control only. Consequently, these problems are addressed by other modulation techniques and the corresponding discussions will be presented in Chapter 3 and Chapter 4.

2.6 Conclusion

This chapter starts with a review of control strategies for grid-tied inverters. There are several well established control strategies that can be applied to perform the current control. However, some of them are not suitable for low-power applications or low inductance designs, such as CCM with hysteresis control or CCM with linear control. Some control strategy and operation modes allow further reduction of inductance, however, they rely on the detection of inverter-side inductor current, such as BCM with hysteresis and model-based control or DCM with linear control. The detection of inductor current can be challenges particularly for high frequency designed converters. On the other hand, the DCM with model-based control allows to eliminate the sensing of current of inverter-side inductor. This feature makes the model-based control more suitable and advantageous for low-power grid-tied inverters operating in high switching frequency. However, all of the conventional model-based controls have a drawback that makes this control strategy sometimes impractical for grid-tied applications. The current distortion including zero-crossing distortion, low-order and high-order harmonic distortions can be generated and they cannot be eliminated adaptively.

Conventionally, the model-based control for DCM grid-tied inverter is based on feed-forward control strategy. Consequently, the control errors, that being generated by the use of an imperfect model, cannot be corrected by the model-based controller. This problem can be improved by introducing a partial feedback control. The low-order harmonics caused by periodic errors then can be eliminated by cascading individual resonant controllers to the model-based controller. However, it is difficult to deal with the zero-crossing distortions and high-order harmonic distortions.

It also is interesting that the errors of fundamental components between the output and reference current can also be corrected with similar approach. The disadvantage of the model-based control, which is inductance dependency, thus can be addressed.

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Chapter 3

A Hybrid of Unipolar and Bipolar Modulations for Reducing Peak Current and Zero-Crossing Distortion

3.1 Introduction

This chapter presents a novel switching scheme and modulation for single-phase DCM grid-tied inverter. Conventionally, two popular switching schemes for pulse width modulation (PWM) modulations can be applied to the DCM grid-tied inverter. An asymmetry unipolar switching benefits from lower switching losses and lower peak values of inductor current. However, an inherent problem related to current distortions around zero-crossing areas can be the problem. This problem can be addressed by adopting a bipolar switching scheme. However, the bipolar DCM suffers from higher peak inductor current therefore conduction losses and switching losses. These problem can be addressed by combining the two conventional switching schemes. A novel switching scheme is proposed to realized this purpose. The proposed switching features high degree of freedom on controlling the inductor current. Therefore, operation modes can be changed freely between the bipolar and

asymmetry unipolar DCM. In addition, a modulation is proposed to reduce the peak inductor current and improve the problem of zero-crossing distortion.

This chapter is organized as follows: the problems of using conventional switching schemes are discussed in Section 3.2. Next, the proposed switching scheme and its modulation methods are presented in Section 3.3. After that, the experimental verification and analysis are presented in Section 3.4. Finally, the conclusion of this chapter is given in Section 3.5.

3.2 Problems with Conventional Switching Schemes

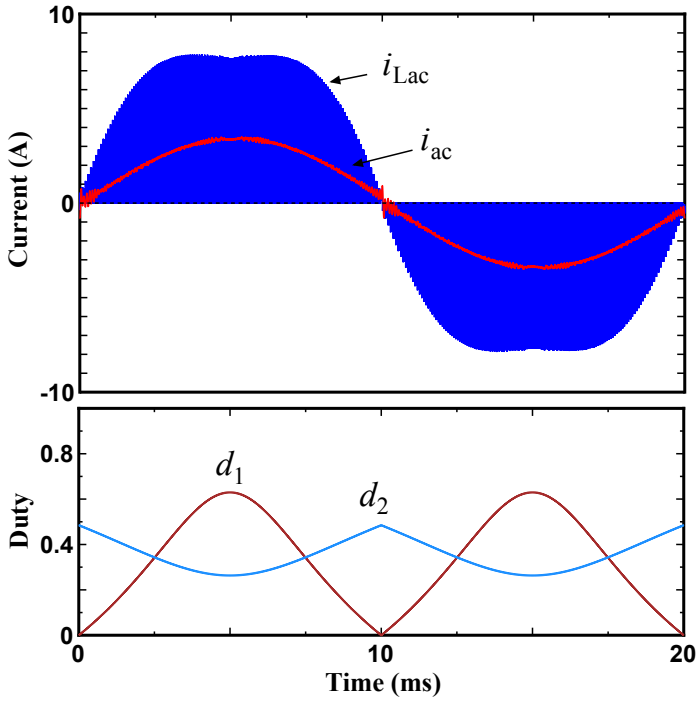

Fig. 3.1 Time domain simulation of a asymmetry unipolar DCM under a certain design specification. $V_{dc} = 400$ (V), $V_{ac} = 200$ (V), $f_{sw} = 100$ (kHz), $I_{rated} = 2.4$ (A), $L_{ac} = 98$ (μH), $k_{max} = 0.9$, $L_f = 125$ (μH), $C_f = 2.2$ (μF).

Conventionally, bipolar and asymmetry DCM can be applied to DCM grid-tied inverters, as discussed in Chapter 2. A simulation result of inverter-side inductor current, grid-side inductor current and calculated duty ratios with the asymmetry unipolar DCM, under rated

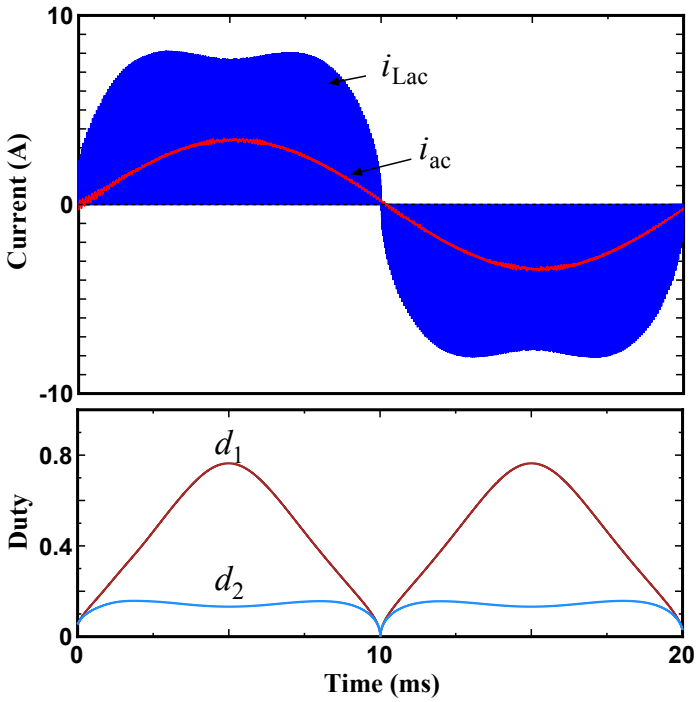

Fig. 3.2 Time domain simulation of a bipolar DCM modulation under a certain design specification. $V_{dc} = 400$ (V), $V_{ac} = 200$ (V), $f_{sw} = 100$ (kHz), $I_{rated} = 2.4$ (A), $L_{ac} = 119$ (μH), $L_f = 125$ (μH), $C_f = 2.2$ (μF).

current operation, is show in Fig. 3.1. A problem regarding to distorted current can be observed around zero-crossing areas where i_{ac} changes its polarity. This distortion, however, does not appear in the bipolar DCM, as shown in Fig. 3.2.

The non-linear duty ratios can be obtained in both asymmetry unipolar DCM and bipolar DCM. However, the duty of synchronous rectification, d_2, has some differences. In the bipolar DCM, d_2 decreases to zero when the current angle goes to zero or π. In contrast, d_2 increases along with the current angle goes to zero or π. This indicates that the utilization of duty ratios is higher in the asymmetry unipolar DCM. Low utilization of duty ratios can leads to high peak values of inductor current. For grid-tied inverters that designed to operate in DCM, the peak inductor currents are high and that results in high turn-off currents and high root mean square (r.m.s) values. Consequently, higher turn-off and conduction losses

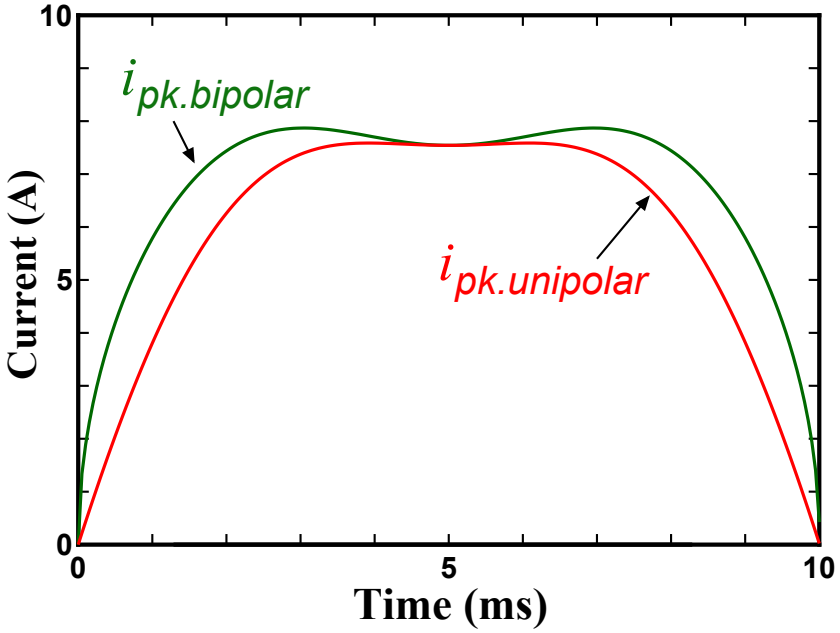

Fig. 3.3 Comparison of peak values of inverter-side inductor current, i_{Lac}, at rated current operation, based on a certain design, in which optimized inductance are applied.

can be obtained in comparison with that in CCM grid-tied inverters. From the point of view of losses reduction, the peak inductor currents should be as low as possible.

Fig. 3.3 depicts the peak values of the inverter-side inductor current, i_{Lac}, for every switching cycles over half line period.The data are taken from Fig. 3.1 and Fig. 3.2. It can be obtained that most of the peak values in the bipolar DCM modulation, $i_{\mathrm{pk.bipolar}}$, are higher than those values in the asymmetry unipolar DCM modulation, $i_{\mathrm{pk.unipolar}}$. In the bipolar and asymmetry unipolar DCM, peak currents are equal to the trun-off currents. Consequently, the resultant turn-off losses can be higher if bipolar DCM modulation is adopted. Further more, the inductor peak currents can also influence the design of inductor and core losses of inductor.

Fig. 3.4 depicts the r.m.s. values of the inverter-side inductor current, i_{Lac}, for every switching cycles over half line period. It can also be obtained that the r.m.s. values of i_{Lac} of bipolar DCM are higher than those of asymmetry unipolar DCM modulation. Consequently, the resultant conduction losses of semiconductor devices can be higher if the bipolar DCM

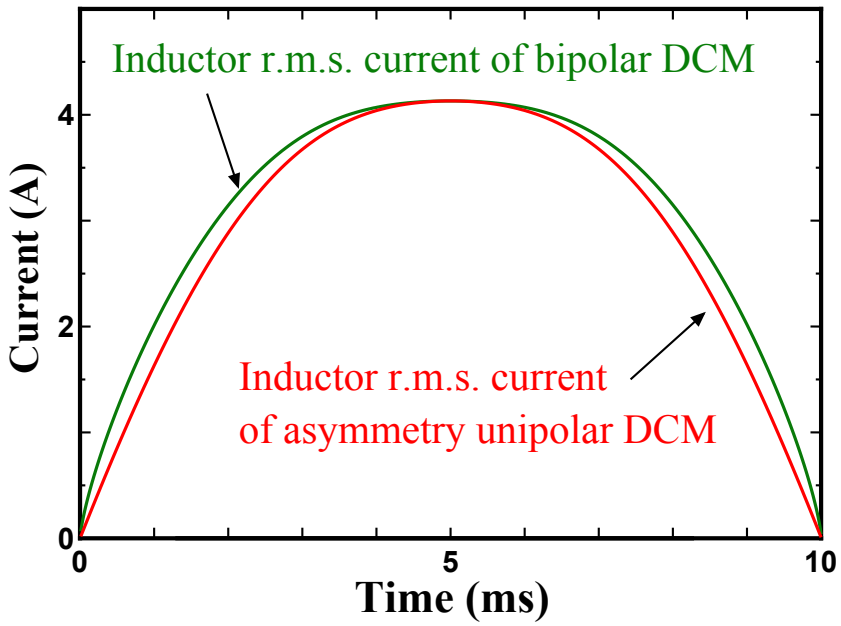

Fig. 3.4 Comparison of r.m.s. values of inverter-side inductor current, i_{Lac}, at rated current operation, based on a certain design, in which optimized inductance are applied.

modulation is adopted. In addition, the inductor r.m.s current can also influence the winding conduction losses of inductor. The application of asymmetry unipolar switching seems more suitable for the DCM grid-tied inverter in term of higher efficiency. However, the zero-crossing distortion can be a problem.

In conventional DC/AC or AC/DC converters with CCM design, a problem regarding to significant current distortion around zero-crossing areas of AC voltage can be obtained when a converter is designed with unipolar switching [1–17]. This problem can also occur in a DCM grid-tied inverter with the same switching scheme being applied, as demonstrated by Fig. 3.1. The current distortion around zero-crossing of AC voltage can be caused by the low speed of demagnetizing current during interval 2.

Fig. 3.5 shows simulation waveforms of the inverter-side inductor current, i_{Lac}, line voltage, v_{ac}, and the voltage cross the inverter-side inductor, v_{Lac}, with asymmetry unipolar DCM, around the zero-crossing of AC voltage. It can be observed that i_{Lac} becomes continuous within several switching cycles before and after v_{ac} changes it polarity. In contrast, i_{Lac} can

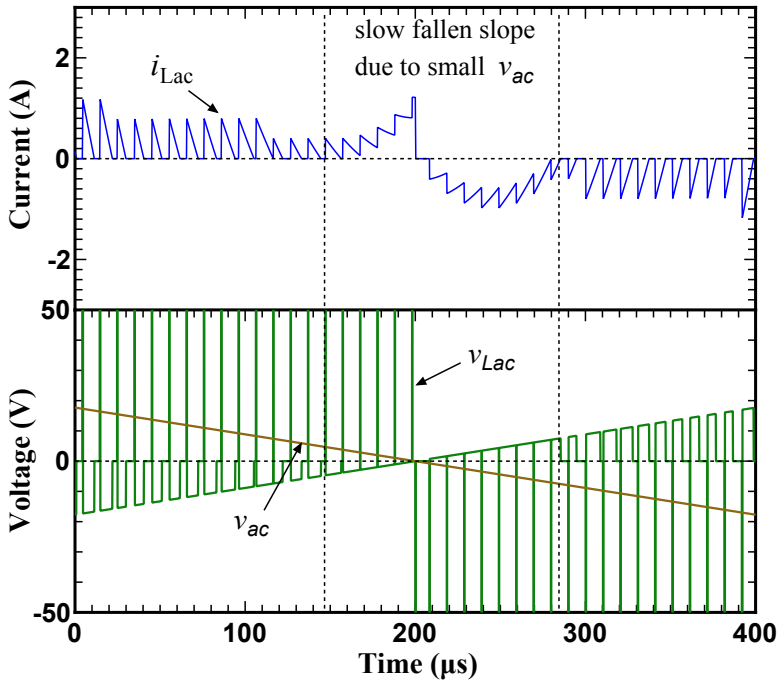

Fig. 3.5 Time-domain simulation of a asymmetry unipolar DCM around zero-crossing areas. i_{Lac} cannot reduce to zero due to the low fallen speed. Consequently, it becomes continuous and the distortion occurs when the polarity of current changes.

reduces to zero in every switching cycle around those areas with bipolar switching, as shown in Fig. 3.6. This can be explained by the factor of the different demagnetizing rates of the inductor current. If the asymmetry unipolar switching is applied, the inductor current is demagnetized at the rate of $v_{\mathrm{ac}}/L_{\mathrm{ac}}$. However, this can cause a problem when v_{ac} is close to zero-crossings. v_{ac} can be too small to demagnetize the inductor current within one switching period. As a result, i_{Lac} cannot reduce to zero and it become continuous eventually. If the bipolar switching is applied, however, the inductor current is demagnetized at the rate of $(V_{\mathrm{dc}} + v_{\mathrm{ac}})/L_{\mathrm{ac}}$ so that i_{Lac} can reduce to zero completely due to this sufficient high rate of demagnetizing.

A conclusion can be drawn that i_{Lac} can become continuous and result in significant overshoot of i_{Lac} when v_{ac} is close to zero in the asymmetry unipolar switching. Nevertheless, the asymmetry unipolar DCM is still preferred rather than the bipolar DCM because of lower switching and conduction losses. However, the slow rate of demagnetizing current

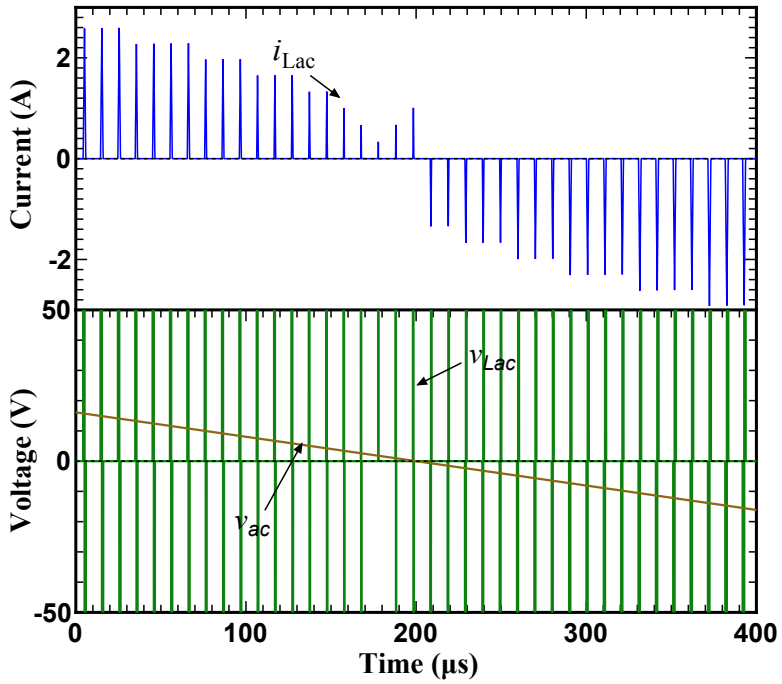

Fig. 3.6 Time-domain simulation of a asymmetry unipolar DCM around zero-crossing areas. i_{Lac} can reduce to zero due to the fast fallen speed of demagnetizing current.

can be a problem. The fast demagnetizing rate can be achieved in the bipolar switching. Therefore, the problem can be addressed by operating the converter in a hybrid of unipolar and bipolar mode. The converter can be operated with bipolar switching around zero-crossing of AC voltage to avoid distortion while unipolar switching being used for other switching cycles [18–20]. This concept is also valid for DCM operated inverter. In order to realize this purpose, a novel switching scheme and its modulation are proposed.

3.3 Proposed Switching Scheme and Modulation

3.3.1 Operation Principle

The proposed switching scheme and its modulation are proposed to elevate the demagnetizing rate of inductor current and improve the problem of zero-crossing distortion for asymmetry unipolar DCM. The schematic waveforms of inductor current and switching patterns of

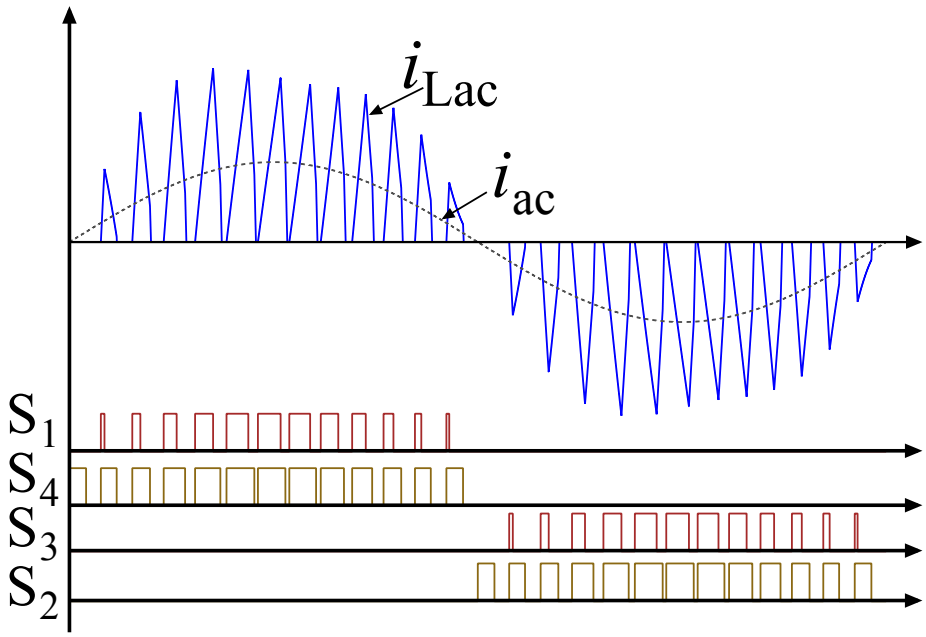

Fig. 3.7 Proposed switching patterns and corresponding waveforms for DCM.

the proposed switching are shown in Fig. 3.7. The scheme of proposed switching is a combination of the scheme of conventional bipolar and asymmetry unipolar. The diagonal switches S_1 and S_3 (for positive grid voltage) or S_2 and S_4 (for negative grid voltage) are turned on simultaneously, only one of the switches is turned off firstly, then another one is turned off. By applying this kind switching scheme, the inductor current can become a trapezium current shape. Therefore it is referred to as trapezium current mode (TPCM).

The schematic waveforms and current path of one switching cycle operation with the proposed TPCM is shown in Fig. 3.8. There are four main intervals within one switching cycle in the TPCM. The principles of one switching operation for the positive line voltage are described as follow:

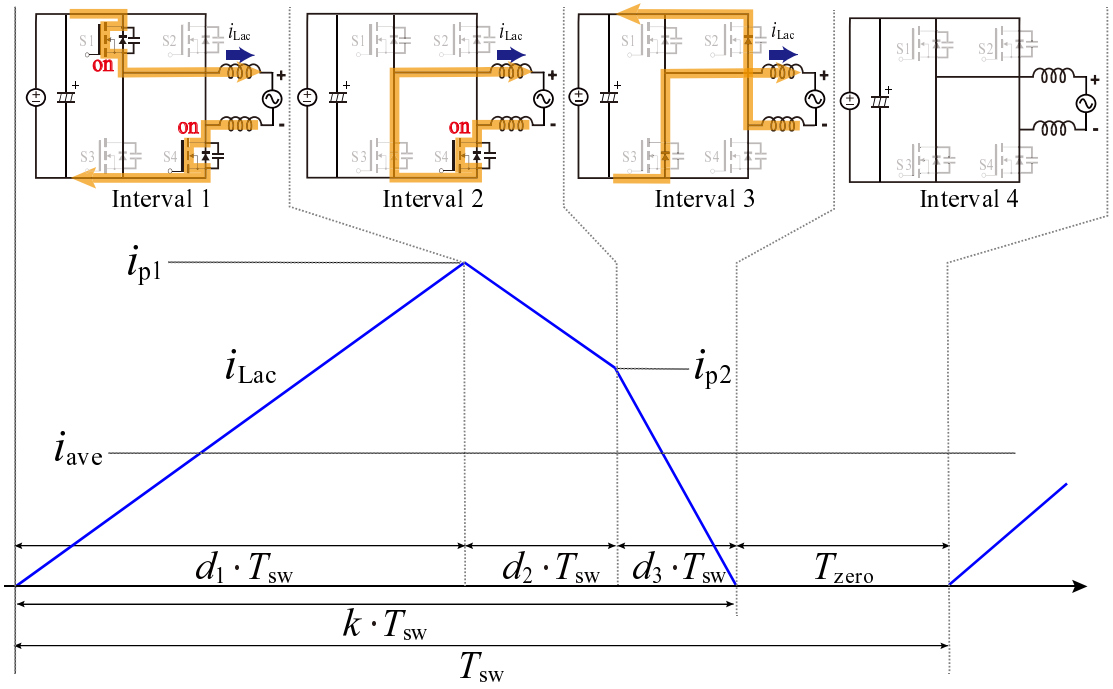

Fig. 3.8 Possible current paths of one switching cycle operation in TPCM for positive grid voltage V_{ac}.

Interval 1:

During interval 1, S_1, S_4 are turned on simultaneously and switches S_2, S_3 are in off-state. i_{Lac} increases linearly. The peak value of i_{Lac}, i_p, during this interval can be expressed as

$$i_p = \frac{V_{dc} - v_{ac}}{L_{ac}} d_1 T_{sw}, \tag{3.1}$$

where V_{dc} denotes the DC-link voltage, v_{ac} denotes the instantaneous line voltage and being assumed constant in one switching cycle. L_{ac} denotes the inductance of inverter-side inductor. d_1 denotes the duty ratio of turn-on for S_1, T_{sw} denotes the switching period. It should be mentioned that S_4 can also be turned off prior to S_4. In the following discussion, it is assumed that S_1 turns off prior to S_4. The interval 1 ends when the switch S_1 is turned off.

Interval 2:

The switching scheme in this interval is used in the asymmetry unipolar switching scheme. S_4 is still in on-state. i_{Lac}, decreases linearly through the body diode of S_3 after S_1 is turned off. S_3 can be turned-on to achieve the so-called synchronous rectification during this interval. The inductor current during this interval can be expressed as

$$-(i_{\mathrm{p}} - i_{\mathrm{p2}}) = \frac{-v_{\mathrm{ac}}}{L_{\mathrm{ac}}} d_2 T_{\mathrm{sw}}. \tag{3.2}$$

where i_{p2} is the value of i_{Lac} reduced to once S_4 is turned-off, d_2 is the duty ratio of turn-on for this interval and d_1+d_2 is the duty ratio of turn-on for S_4. The interval 2 ends when S_4 is turned off.

Interval 3:

The switching scheme in this interval is used in the bipolar switching scheme. After S_4 is turned off, i_{Lac} decreases linearly through the body diode of S_2 and S_3. S_2 can be turned-on to achieve the so-called synchronous rectification during this interval. i_{p2} during this interval can be expressed as

$$-i_{\mathrm{p2}} = \frac{-V_{\mathrm{dc}} - v_{\mathrm{ac}}}{L_{\mathrm{ac}}} d_3 T_{\mathrm{sw}}, \tag{3.3}$$

where d_3 denotes the duty ratio for S_2 and $d_2 + d_3$ denotes the duty ratio for S_3 to achieve the synchronous rectification. The interval 3 end when i_{Lac} reduces to zero.

Interval 4:

During this interval, the inductor current is zero theoretically. After this interval, S_1 and S_4 are turned on again and a new switching cycle begins.

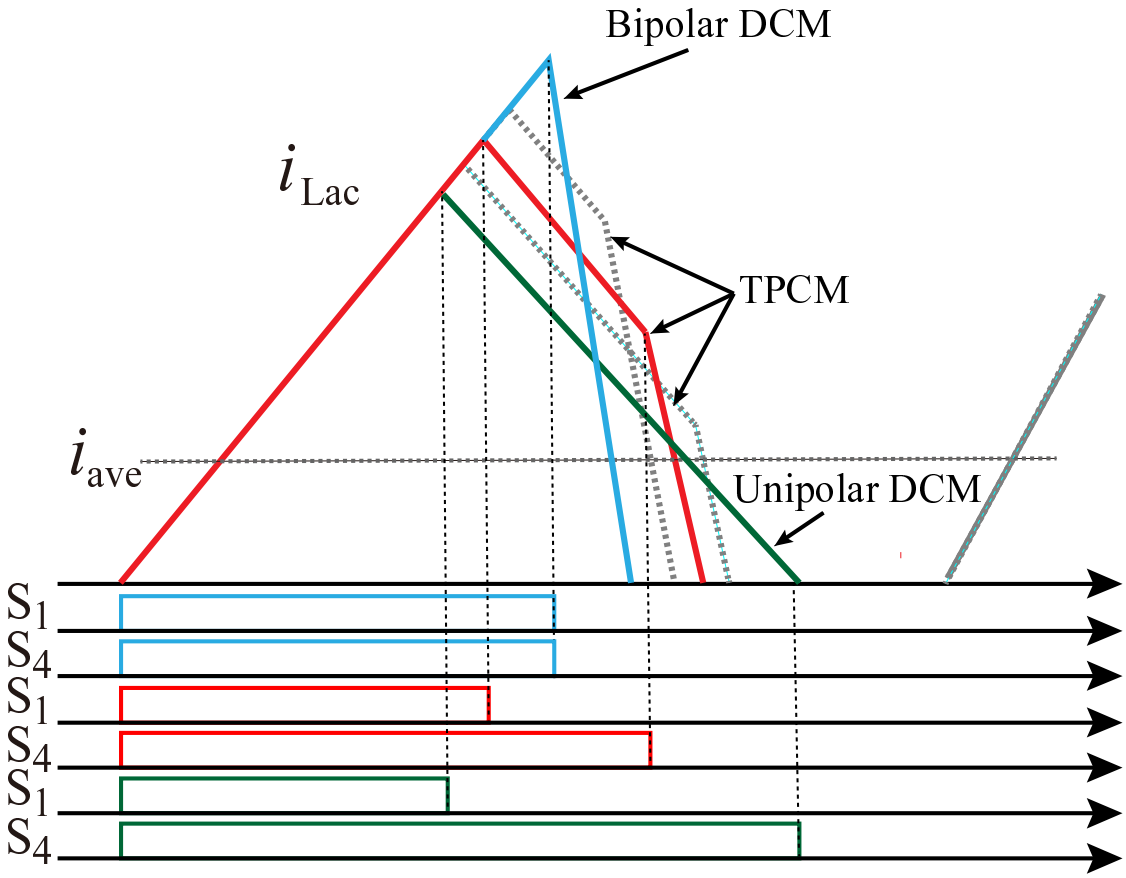

Fig. 3.9 Schematic waveforms of the possibilities on controlling inductor current for the same average current (when the same L_{ac} is applied).

The proposed switching scheme features more degrees of freedom on controlling the inductor current, as shown in Fig. 3.9. By controlling the turn-off time of the corresponding switches, different shape of i_{Lac} can be created for a given average current, i_{ave}. This feature allows the converter to operate in three modes, which are bipolar DCM, asymmetry unipolar DCM and TPCM. The operation mode can be shifted suddenly from the bipolar DCM to the asymmetry unipolar DCM; or shifted smoothly by using an additional trapezium current mode.

3.3.2 Model for Duty Calculation

The duty rations are derived from the average current model built for the trapezium inductor current. The average inductor current, i_{ave}, in one switching cycle can be expressed as

$$i_{\text{ave}} = \frac{S}{T_{\text{sw}}} = \frac{1}{T_{\text{sw}}} \int_0^{T_{\text{sw}}} i_{\text{Lac}} dt = \frac{S_1 + S_2 + S_3 + S_4}{T_{\text{sw}}}, \tag{3.4}$$

where S_1-S_4 are the areas in the trapezium as shown in Fig. 3.10. Only the current that in the main intervals are considered in the calculation and the current in interval 4 is assumed to be zero. By doing so, it comes down to a simple area calculation of the trapezium waveform.

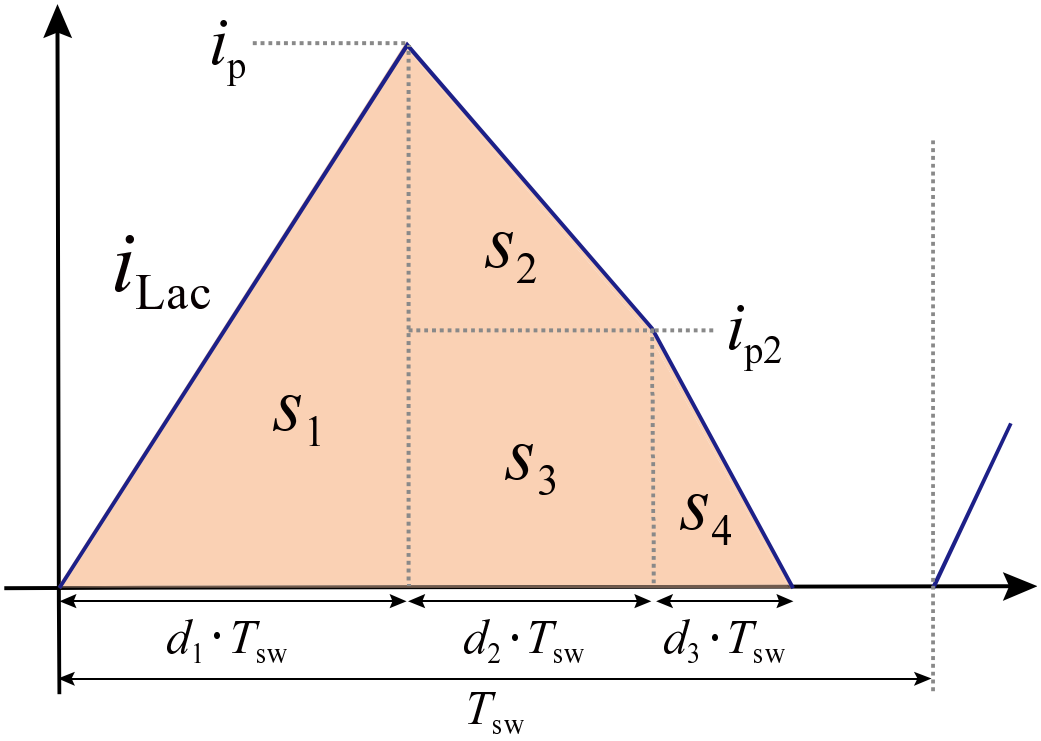

Fig. 3.10 Model-based calculation for TPCM in one switching cycle.

The areas S_1–S_4 can be expressed as

$$S_1 = \frac{1}{2} i_{\text{p}} d_1 T_{\text{sw}}, \tag{3.5}$$

$$S_2 = \frac{1}{2}(i_{\mathrm{p}} - i_{\mathrm{p2}})d_2 T_{\mathrm{sw}}, \tag{3.6}$$

$$S_3 = i_{\mathrm{p2}} d_2 T_{\mathrm{sw}}, \tag{3.7}$$

$$S_4 = \frac{1}{2} i_{\mathrm{p2}} d_3 T_{\mathrm{sw}}, \tag{3.8}$$

The sum of d_1, d_2 and d_3 is referred to as the duty utilization and it is express by k, as

$$d_1 + d_2 + d_3 = k. \tag{3.9}$$

The duty ratios, d_1, d_2, d_3, to achieve i_{ref} can be obtained by combining (3.4), (3.5), (3.6), (3.7), (3.8) and (3.9); and be expressed as

$$d_1 = \begin{cases} -\dfrac{\sqrt{k^2 {V_{\mathrm{dc}}}^2 - k^2 {v_{\mathrm{ac}}}^2 - 4V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}}}}{2V_{\mathrm{dc}}} + \dfrac{kV_{\mathrm{dc}} + kv_{\mathrm{ac}}}{2V_{\mathrm{dc}}} & (i_{\mathrm{ref}} > 0) \\ -\dfrac{\sqrt{k^2 {V_{\mathrm{dc}}}^2 - k^2 {v_{\mathrm{ac}}}^2 + 4V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}}}}{2V_{\mathrm{dc}}} + \dfrac{kV_{\mathrm{dc}} - kv_{\mathrm{ac}}}{2V_{\mathrm{dc}}} & (i_{\mathrm{ref}} < 0) \end{cases} \tag{3.10}$$

$$d_2 = \begin{cases} \dfrac{\sqrt{k^2 {V_{\mathrm{dc}}}^2 - k^2 {v_{\mathrm{ac}}}^2 - 4V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}}}}{V_{\mathrm{dc}}} & (i_{\mathrm{ref}} > 0) \\ \dfrac{\sqrt{k^2 {V_{\mathrm{dc}}}^2 - k^2 {v_{\mathrm{ac}}}^2 + 4V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}}}}{V_{\mathrm{dc}}} & (i_{\mathrm{ref}} < 0) \end{cases} \tag{3.11}$$

$$d_3 = \begin{cases} -\dfrac{\sqrt{k^2 {V_{\mathrm{dc}}}^2 - k^2 {v_{\mathrm{ac}}}^2 - 4V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}}}}{2V_{\mathrm{dc}}} + \dfrac{kV_{\mathrm{dc}} - kv_{\mathrm{ac}}}{2V_{\mathrm{dc}}} & (i_{\mathrm{ref}} > 0) \\ -\dfrac{\sqrt{k^2 {V_{\mathrm{dc}}}^2 - k^2 {v_{\mathrm{ac}}}^2 + 4V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}}}}{2V_{\mathrm{dc}}} + \dfrac{kV_{\mathrm{dc}} + kv_{\mathrm{ac}}}{2V_{\mathrm{dc}}} & (i_{\mathrm{ref}} < 0) \end{cases} \tag{3.12}$$

, respectively. It can be observed form (3.10), (3.11)and (3.12) that k is only variable that can be changed while other parameters are dependent on operation conditions. Therefore, different sets of duty ratios can be obtained by using different k.

3.3.3 Proposed Modulation to Improve Zero-Crossing Distortion

Fig. 3.11 depicts the schematic waveforms of the concept of the proposed modulation. In order to complete the demagnetization process, the interval 3 that has a fast demagnetizing rate of inductor current is required around zero-crossing areas. In order to maintain low peak currents, operation mode that being close to the asymmetry unipolar DCM is preferred in other switching cycles. In the proposed switching scheme, the mode changing between bipolar DCM and asymmetry unipolar DCM can be easily realized by giving appropriate k to (3.10), (3.11) and (3.12).

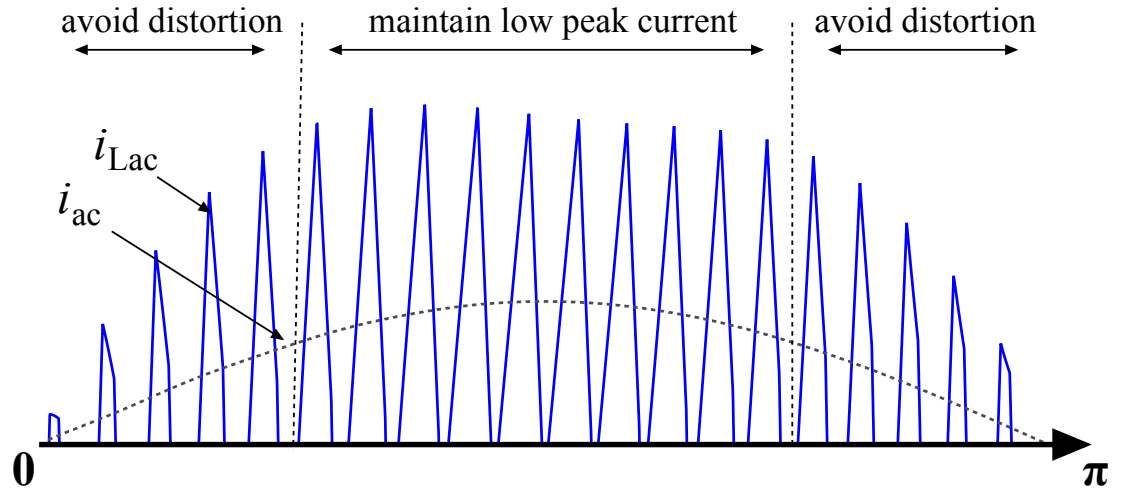

Fig. 3.11 Concept of the proposed operation to avoid high peak current and improve zero-crossing distortion.

3.3.4 Design Considerations

The following discussions assumes a unity power factor operation of the inverter. Assuming that the operation mode is always asymmetry unipolar DCM, the interval 3, which is the current path for bipolar DCM, should not exist, so that the inverter-side inductor current, i_{Lac}, becomes the same as that in the asymmetry unipolar DCM. By considering this circumstance, an upper boundary for k, k_{upper}, then can be determined. If (3.12) is always equal to zero,

k_{upper} can be calculated as

$$k_{\text{upper}} = \begin{cases} \sqrt{\dfrac{2V_{\text{dc}}L_{\text{ac}}f_{\text{sw}}i_{\text{ref}}}{v_{\text{ac}}(V_{\text{dc}}-v_{\text{ac}})}} & (i_{\text{ref}} > 0) \\ \sqrt{\dfrac{2V_{\text{dc}}L_{\text{ac}}f_{\text{sw}}i_{\text{ref}}}{v_{\text{ac}}(V_{\text{dc}}+v_{\text{ac}})}} & (i_{\text{ref}} < 0) \end{cases} \tag{3.13}$$

In a similarly way that the lower boundary for k, k_{lower}, can be determined by assuming the operation mode is always bipolar DCM. For this circumstance, the interval 2 that associates with the current path in the asymmetry unipolar DCM, should not exist. i_{Lac} thus becomes the same as that in the bipolar DCM. If (3.11) is always equal to zero, k_{lower} can be calculated as

$$k_{\text{lower}} = \begin{cases} \sqrt{\dfrac{4V_{\text{dc}}L_{\text{ac}}f_{\text{sw}}i_{\text{ref}}}{V_{\text{dc}}^2-v_{\text{ac}}^2}} & (i_{\text{ref}} > 0) \\ \sqrt{\dfrac{-4V_{\text{dc}}L_{\text{ac}}f_{\text{sw}}i_{\text{ref}}}{V_{\text{dc}}^2-v_{\text{ac}}^2}} & (i_{\text{ref}} < 0) \end{cases} \tag{3.14}$$

k can be any values within the two boundaries. Design of k has many possibilities, however, it should follow certain design rules to achieve the given purpose. As discussed above, fast demagnetizing rate of inductor current is required to complete the demagnetizing process. This means that the interval 3 should be as long as possible around zero-crossing areas. From this point of view, k should be close to k_{lower}. On the other hand, k should be close to k_{upper} in other switching cycles to keep the peak currents as low as possible. A simple implementation for k is proposed in accordance with the above design rule, as expressed as

$$k = \begin{cases} \sqrt{\dfrac{4V_{\text{dc}}L_{\text{ac}}f_{\text{sw}}i_{\text{ref}}}{V_{\text{dc}}^2-v_{\text{ac}}^2}} + k_{\text{offset}} & (i_{\text{ref}} > 0) \\ \sqrt{\dfrac{-4V_{\text{dc}}L_{\text{ac}}f_{\text{sw}}i_{\text{ref}}}{V_{\text{dc}}^2-v_{\text{ac}}^2}} + k_{\text{offset}} & (i_{\text{ref}} < 0) \end{cases} \tag{3.15}$$

Table 3.1 Circuit Parameters and Conditions

DC link voltage	V_{dc}	400 V
AC voltage	V_{ac}	200 V
Rated current	$I_{\mathrm{ac.rated}}$	2.4 A
Switching frequency	f_{sw}	100 kHz
Digital controller	DSP	TMS320F28377S
Switching device	SiC-MOSFET	SCT2160KE
LCL filter Design		
Inverter-side inductance for bipolar DCM	$L_{\mathrm{ac.bipolar}}$	119 μH
Percentage impedance of $L_{\mathrm{ac.bipolar}}$	$\%X_{\mathrm{Lac.bipolar}}$	0.045%
Inverter-side inductance for unipolar DCM	$L_{\mathrm{ac.unipolar}}$	98 μH
Percentage impedance of $L_{\mathrm{ac.unipolar}}$	$\%X_{\mathrm{Lac.unipolar}}$	0.037%
Inverter-side inductance for TPCM	L_{ac}	119 μH
Percentage impedance of $L_{\mathrm{ac.TPCM}}$	$\%X_{\mathrm{Lac.TPCM}}$	0.045%
Grid-side inductance	L_{f}	125 μH
Percentage impedance of X_{Lf}	$\%X_{\mathrm{Lf}}$	0.047%
Capacitance of filter capacitor	C_{f}	2.2 μF

k is proposed to be k_{lower} plus a certain offset, k_{offset}. k_{offset} can be calculated as

$$k_{\mathrm{offset}} = k_{\mathrm{upper(wt=90^\circ)}} - k_{\mathrm{lower(wt=90^\circ)}}, \tag{3.16}$$

where $k_{\mathrm{upper(wt=90^\circ)}}$ and $k_{\mathrm{lower(wt=90^\circ)}}$ are the values of k_{upper} and k_{lower} at the phase angle where $\omega t = 90^\circ$.

Fig. 3.12 shows examples of calculated k_{upper}, k_{lower} and k for rated current operation. The calculation is based on a certain specification that used in the experiment. The conditions and parameters are listed in Table 3.1. A maximum limitation for k, k_{max}, is required to guarantee the DCM operation even under maximum power operation. k_{max} is also used to calculated the inverter-side inductance. Any k that exceeds this limitation should be restricted to k_{max}. In this calculation, k_{max} is set to be 0.9. Fig. 3.13 depicts the examples of $k_{\mathrm{upper(wt=90^\circ)}}$, $k_{\mathrm{lower(wt=90^\circ)}}$ and k_{offset} under different current set-points, $I_{\mathrm{ac.set}}$.

Fig. 3.14 shows a simulation result of the inverter-side inductor current, grid-side inductor current and duty ratios with the proposed TPCM. The simulation conditions are listed in

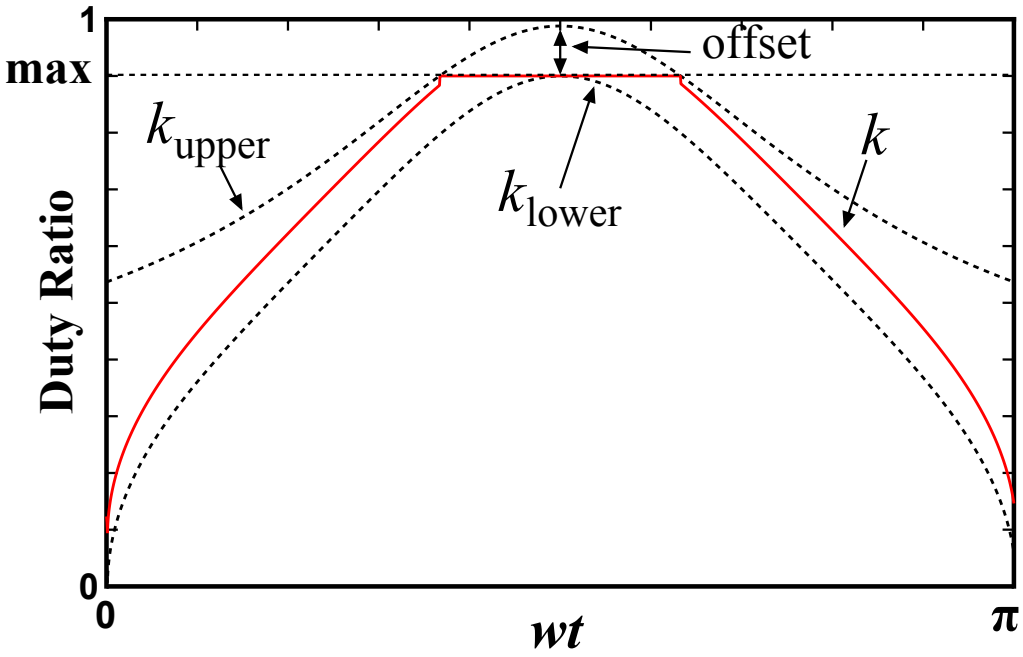

Fig. 3.12 Calculated upper, lower limitations and k for rated current case based on a certain design in which $L_{ac} = 119$ (μH).

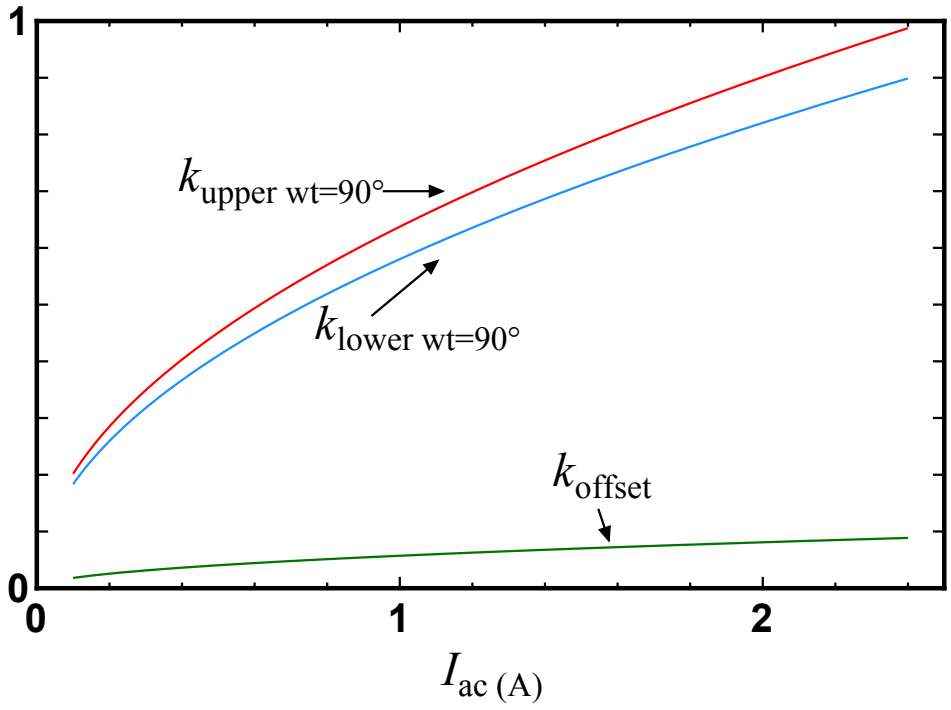

Fig. 3.13 Values of upper, lower limitations and k_{offset} at peak current phase for different I_{ac}.

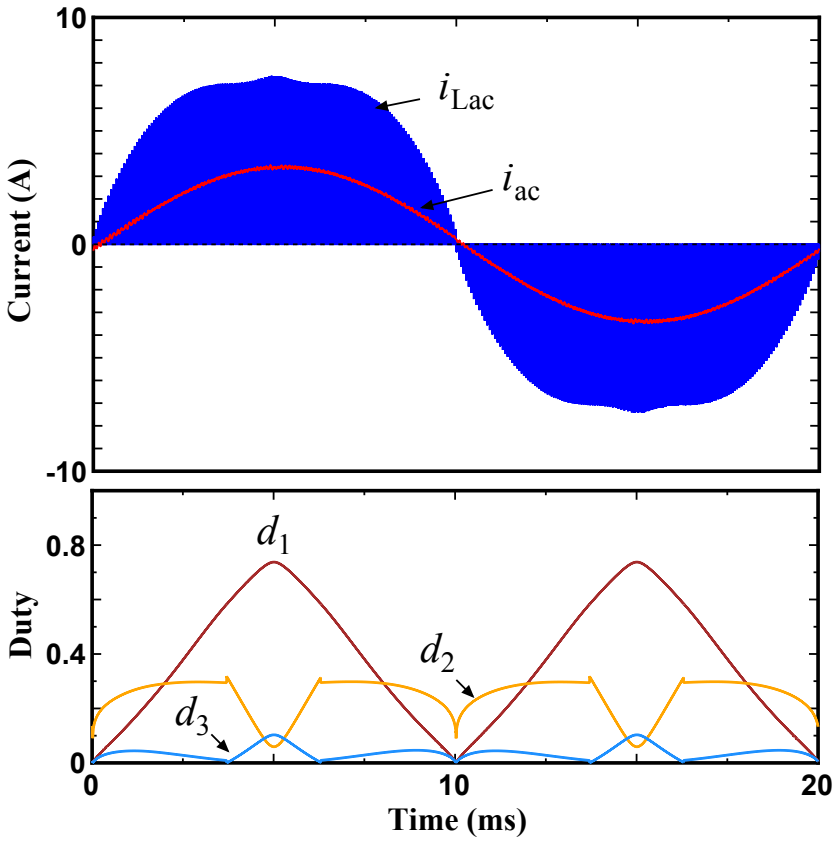

Fig. 3.14 Time domain simulation of the proposed TPCM based on a certain specification in which $L_{ac} = 119$ (μH).

Table 3.1. The non-linear duty ratios can also be obtained in the TPCM. It is shown that there is no distortions around zero-cross, meanwhile, the peak values of i_{Lac} are similar with the calculated results.

3.3.5 Calculations for Turn-off and Inductor R.M.S. Current

Fig. 3.15 shows a comparison of calculated turn-off currents of i_{Lac} for every switching cycles over half line cycle, rated current operation, with three modulations. The calculation conditions are on the basis of experimental conditions, as listed in Table 3.1. The optimized inductance are applied to each design. In bipolar and asymmetry unipolar DCM, the peak currents are equal to the turn-off currents; in the proposed TPCM, one of the switches can be turned of at lower current. therefore, there are two different turn-off currents in one switching

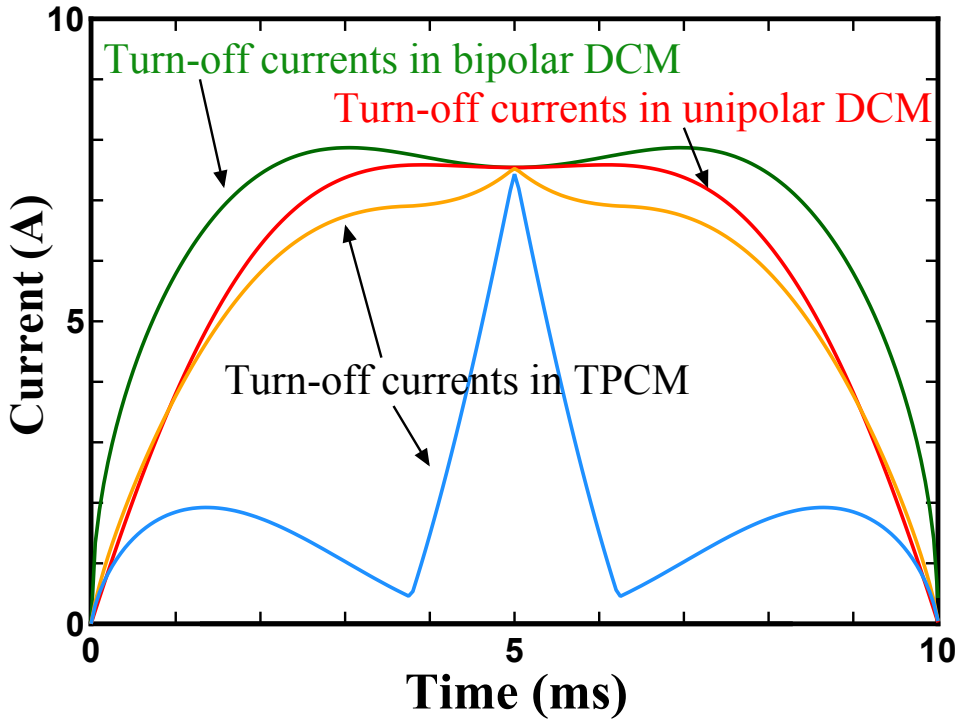

Fig. 3.15 Calculated turn-off currents for every switching cycles over half line period.

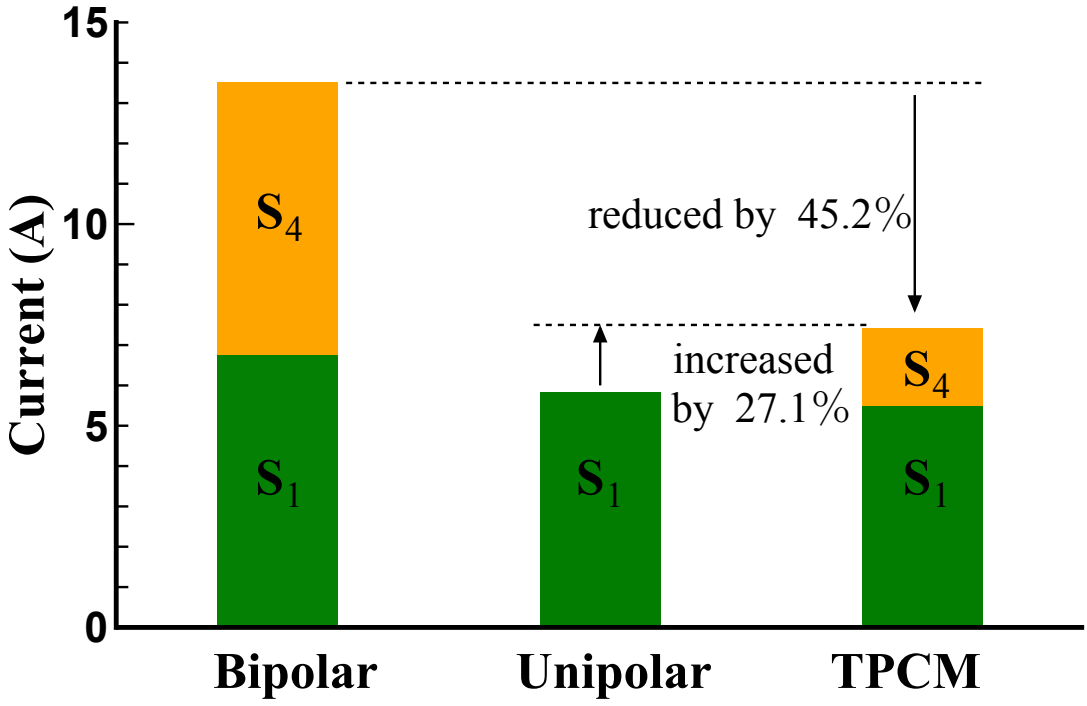

Fig. 3.16 Calculated average turn-off currents for one line period.

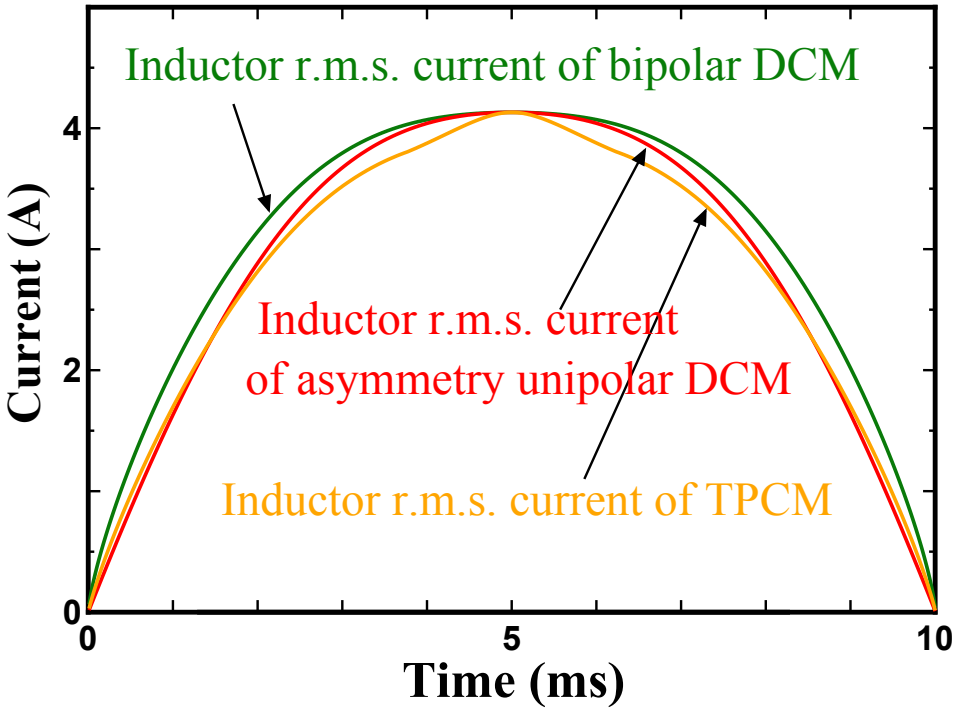

Fig. 3.17 Calculated inductor r.m.s. current for every switching cycles over half line period.

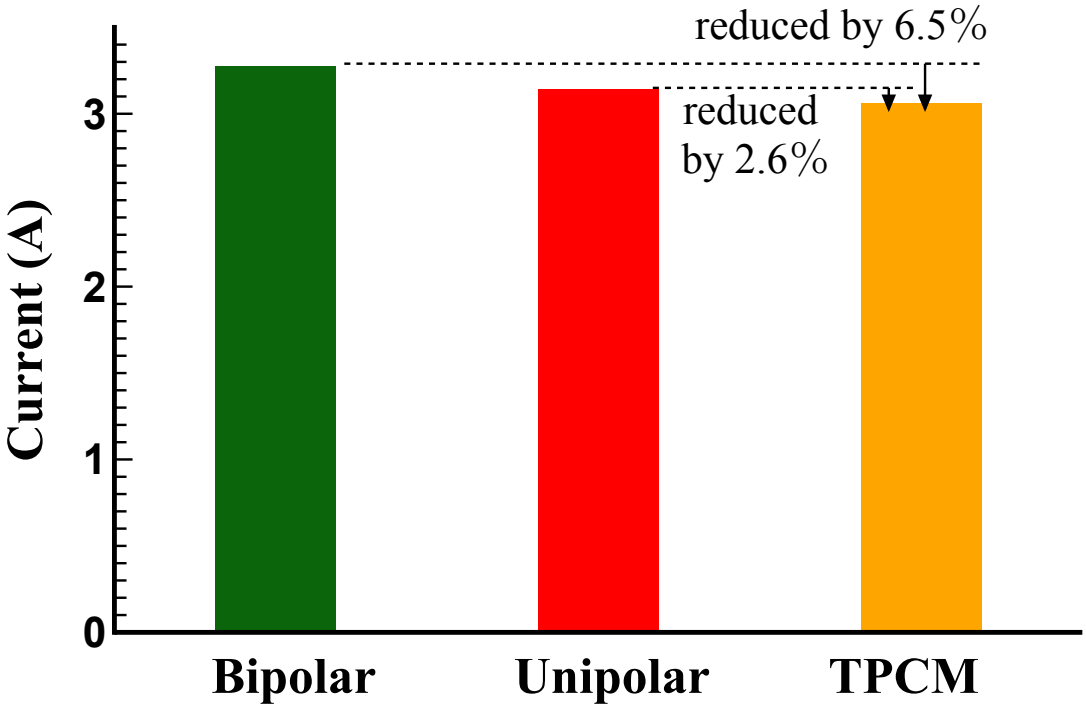

Fig. 3.18 Calculated inductor r.m.s. currents for one line period.

cycle. It can be obtained that the turn-off currents in the bipolar DCM are higher than those of asymmetry unipolar DCM as discussed in the previous sections. On the other hand, the two turn-off currents of proposed TPCM can be lower than those of conventional two DCMs.

Fig. 3.16 shows a comparison of average turn-off current for half line period. The average turn-off current can represent the turn-off losses. In bipolar and TPCM, two switches are turned off in every switching cycles, therefore, the average turn-off current are calculated separately and added together. The average turn-off current of TPCM can be reduced by 45.2% in comparison with that of bipolar DCM. However, it can be increased by 27.1% in comparison with the asymmetry unipolar DCM, since there is only one switch being turned off in the asymmetry unipolar DCM. This result indicates that the turn-off losses of TPCM can be reduced in comparison with that of bipolar DCM.

Fig. 3.17 shows a comparison of calculated inductor r.m.s. currents of i_{Lac} for every switching cycles over half line cycle, rated current operation, with three modulations. It can be obtained that the inductor r.m.s. values of TPCM are the lowest while the inductor r.m.s. values of bipolar DCM are the highest. Fig. 3.18 shows a comparison of inductor r.m.s. current for one line period. The TPCM can reduce the inductor r.m.s. current by 6.5% in comparison with bipolar DCM; and the inductor r.m.s. current of TPCM can be reduced by 2.6% in comparison with asymmetry unipolar DCM. This result indicates that the conduction losses of TPCM can also be reduced in comparison with conventional two DCMs. However, the reduction in conduction losses can be relatively small in comrarison with the reduction of turn-off losses.

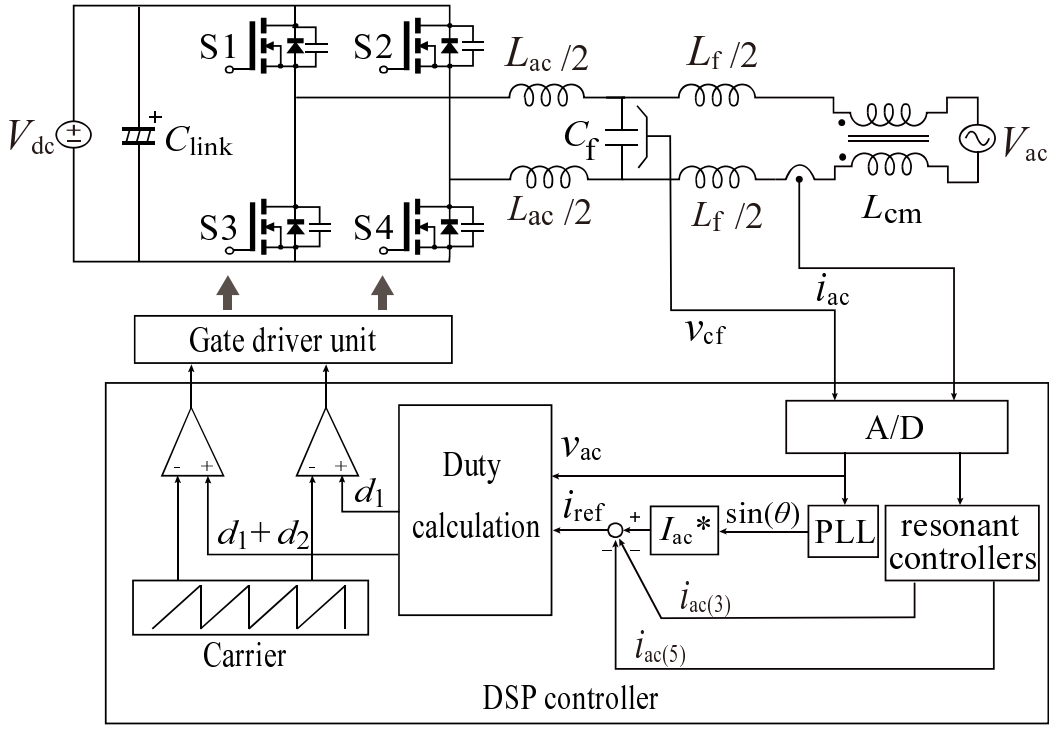

Fig. 3.19 Simplified structure of the fabricated single phase grid-tied inverter system.

3.4 Experimental Results and Analysis

3.4.1 Experimental setup

The schematic view of the fabricated experimental system is shown in Fig. 3.19. In this experiment, the DC link voltage was supplied from a DC power supply, therefore, V_{dc} was assumed to be constant and its value was not measured. The AC voltage was supplied from a linear AC voltage source with power dissipating resistors connected in parallel. The instantaneous capacitor voltage, v_{cf}, was sensed and used as AC voltage reference. i_{ref} was synchronized in phase with the AC voltage through a digital phase locked loop (PLL). A common mode choke was connected to the AC side of the inverter to suppress common mode noise in the experiment. The conventional bipolar DCM, conventional asymmetry unipolar DCM and proposed TPCM were implemented in a 480 W class prototype, which is controlled by a digital signal processor (DSP) TMS320F28377S. A periodic timer interrupt of 20 kHz

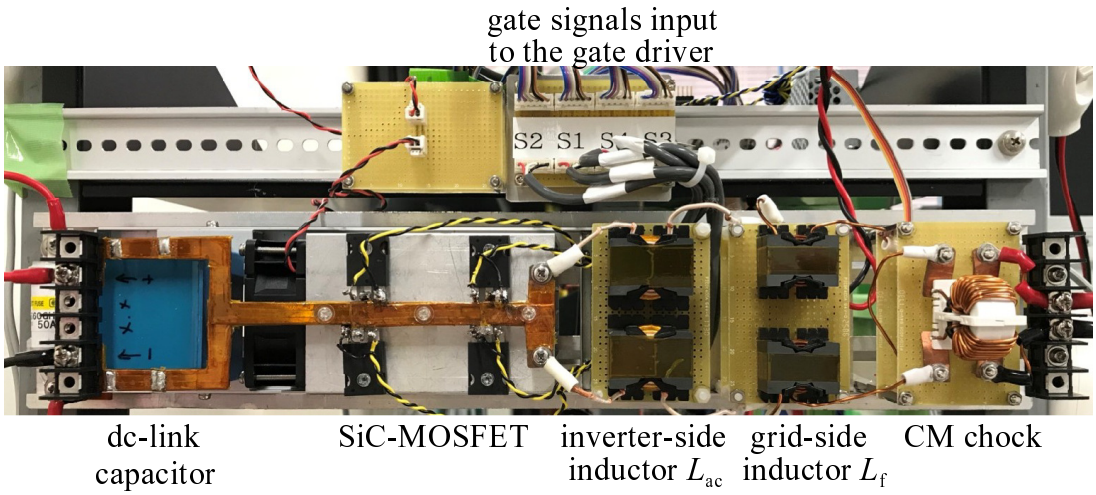

Fig. 3.20 Fabricated prototype.

was used to do all of the calculations. The experimental conditions are the same as that in the simulation and the parameters are listed in Table 3.1. The SiC-MOSFET (SCT2160KE, 1200 V, 22A) was used as the switching device and the switching frequency was set to be 100 kZ in order to achieve small volumes of inductor. The optimized inductance were applied to the bipolar DCM, asymmetry unipolar DCM and TPCM, respectively. However, the fabricated inductor whose inductance were not exactly the same as that in the calculation. The filter capacitance was designed to achieve an acceptable ripple of 1.5% of the maximum capacitor voltage. The grid-side inductance was designed to achieve an acceptable ripple of 1.5% of the maximum output current. Two resonant controllers were used to eliminate the third and fifth harmonics in the output current. A photo of the fabricated prototype of the inverter is shown in Fig. 3.20.

3.4.2 Waveforms Demonstration and Analysis

The experimental waveforms of the asymmetry unipolar DCM, bipolar DCM, and TPCM, at the rated current operation, are shown in Fig. 3.21, Fig. 3.22, and Fig. 3.23, respectively. Significant zero-crossing distortion in i_{ac} can be observed form Fig. 3.21. However, it is negligible if the bipolar DCM or TPCM is applied, as shown in Fig. 3.22 and Fig. 3.23,

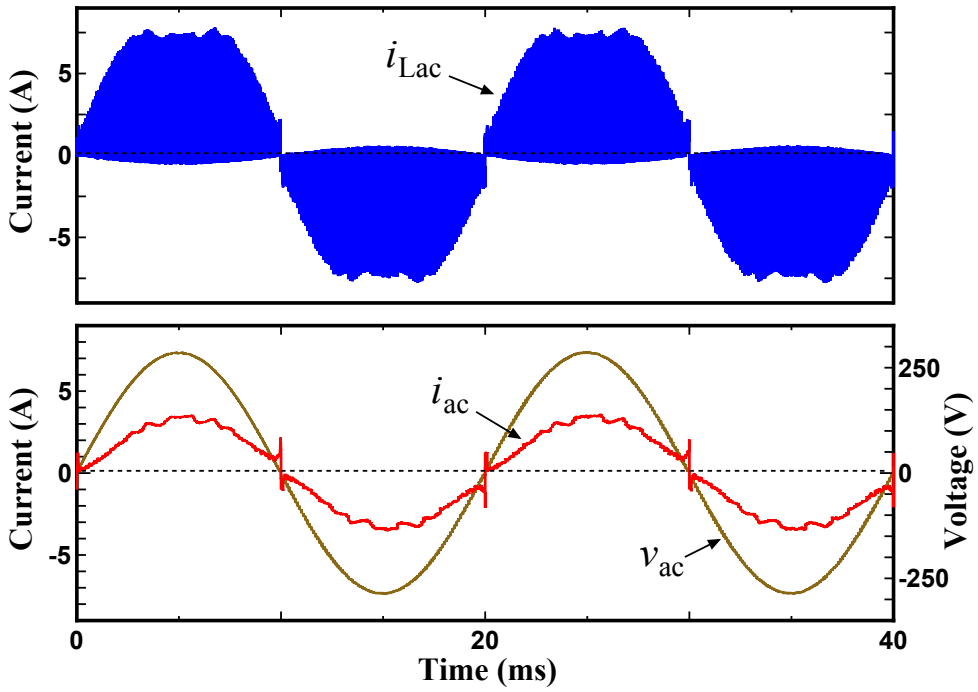

Fig. 3.21 Experimental waveforms of inverter-side inductor current, i_{Lac}, and grid-side inductor current, i_{ac}, with asymmetry unipolar DCM modulation.

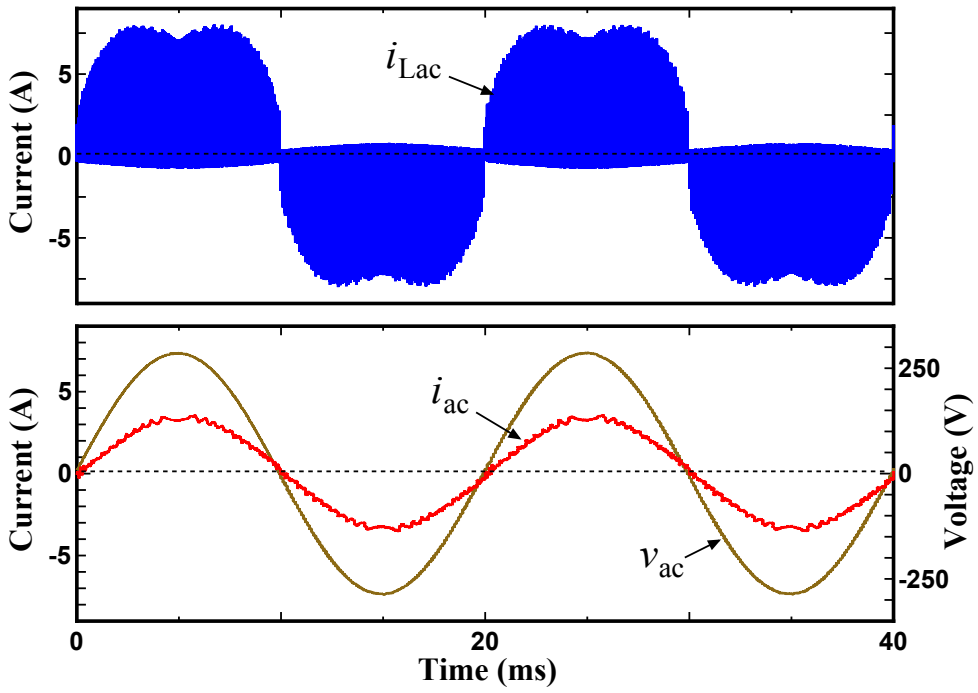

Fig. 3.22 Experimental waveforms of inverter-side inductor current, i_{Lac}, and grid-side inductor current, i_{ac}, with bipolar DCM modulation.

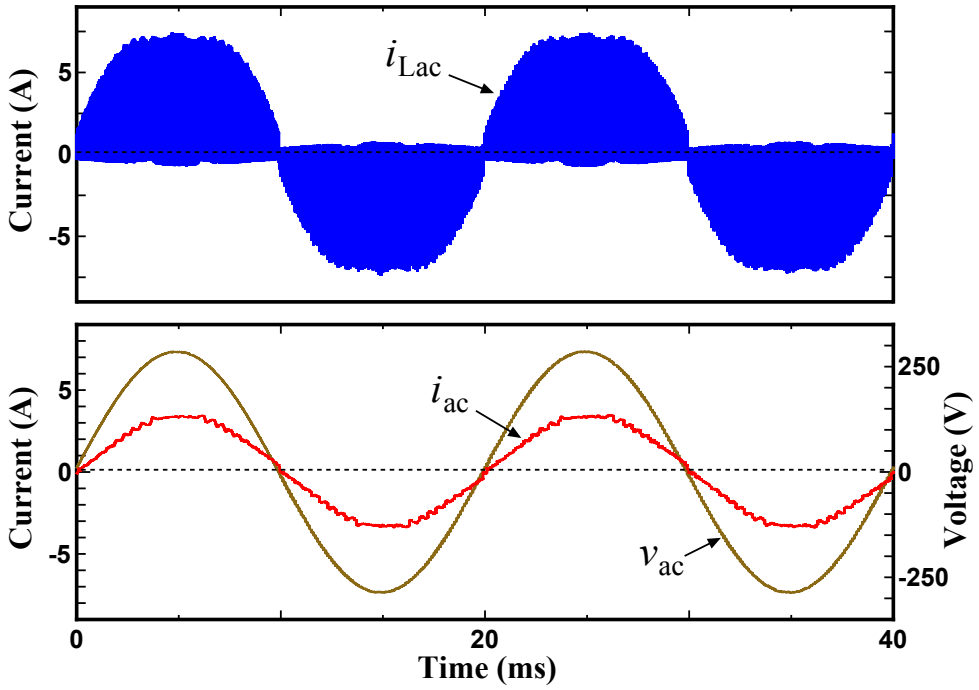

Fig. 3.23 Experimental waveforms of inverter-side inductor current, i_{Lac}, and grid-side inductor current, i_{ac}, with TPCM Modulation.

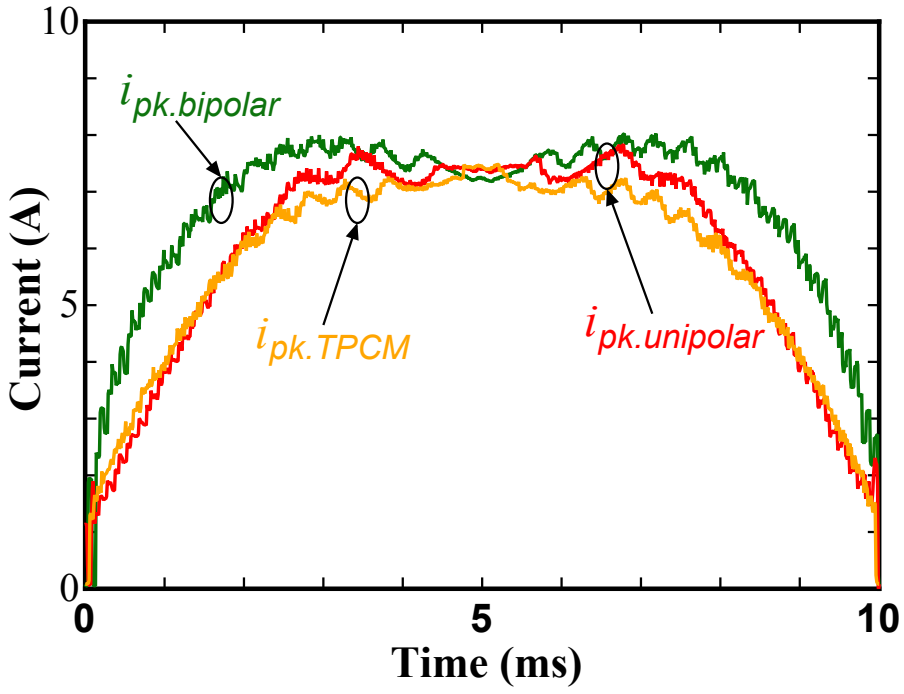

Fig. 3.24 Measured peak values of i_{Lac} over half line period for rated current case.

respectively. The peak values of i_{Lac} in Fig. 3.22, Fig. 3.21, and Fig. 3.23 over half line period are processed from the experimental data and depicted in Fig. 3.24. It is similar to the calculated results for turn-off currents, the lowest peak values of i_{Lac}, $i_{\text{pk.TPCM}}$, is obtained in TPCM and the highest peak values of i_{Lac}, $i_{\text{pk.bipolar}}$, is obtained in bipolar DCM. The peak values of i_{Lac} in unipolar DCM, $i_{\text{pk.unipolar}}$, are slight higher than $i_{\text{pk.TPCM}}$.

The efficiencies and total losses for asymmetry unipolar DCM, bipolar DCM and TPCMs were measured in the experiment and the results are shown in Fig. 3.25. The measurement was conducted by using a digital power meter (YOKOGAWA WT-1600). The range of measurement for DC input was 600 V/2 A and 300 V/5 A for AC side. The maximum errors of reading and measurement were calculated based on this condition, and the error bars are added. The American weighted efficiency [21] (only DC/AC stage) are calculated based on the measured results and shown in Table 3.2. The bipolar DCM has lowest weighted efficiency mainly due to its low efficiency at heavy loads; the weighted efficiency of TPCM can be almost the same as that of asymmetry unipolar DCM.

Table 3.2 Weighted Efficiency Comparison

Bipolar DCM	Asymmetry unipolar DCM	Proposed TPCM
95.7%	96%	96.1%

This improvement of efficiency brought by TPCM and asymmetry unipolar DCM can be explained by the reduced peak current, which leads to the reduction of turn-off and conduction losses. Fig. 3.26 shows an estimation of loss break-down for the rated current operation. The estimation for conduction and turn-off losses are conducted on the basis of experimental conditions and the datasheet of used semiconductor device. In this experiment, diode rectification was used. In order to perform a more accurate calculation, the conduction losses for channel and body diode were calculated separately. The channel conduction losses were obtained by using calculated r.m.s current and device on-state resistance. The diode conduction losses were obtained by using current flowing through the body diode

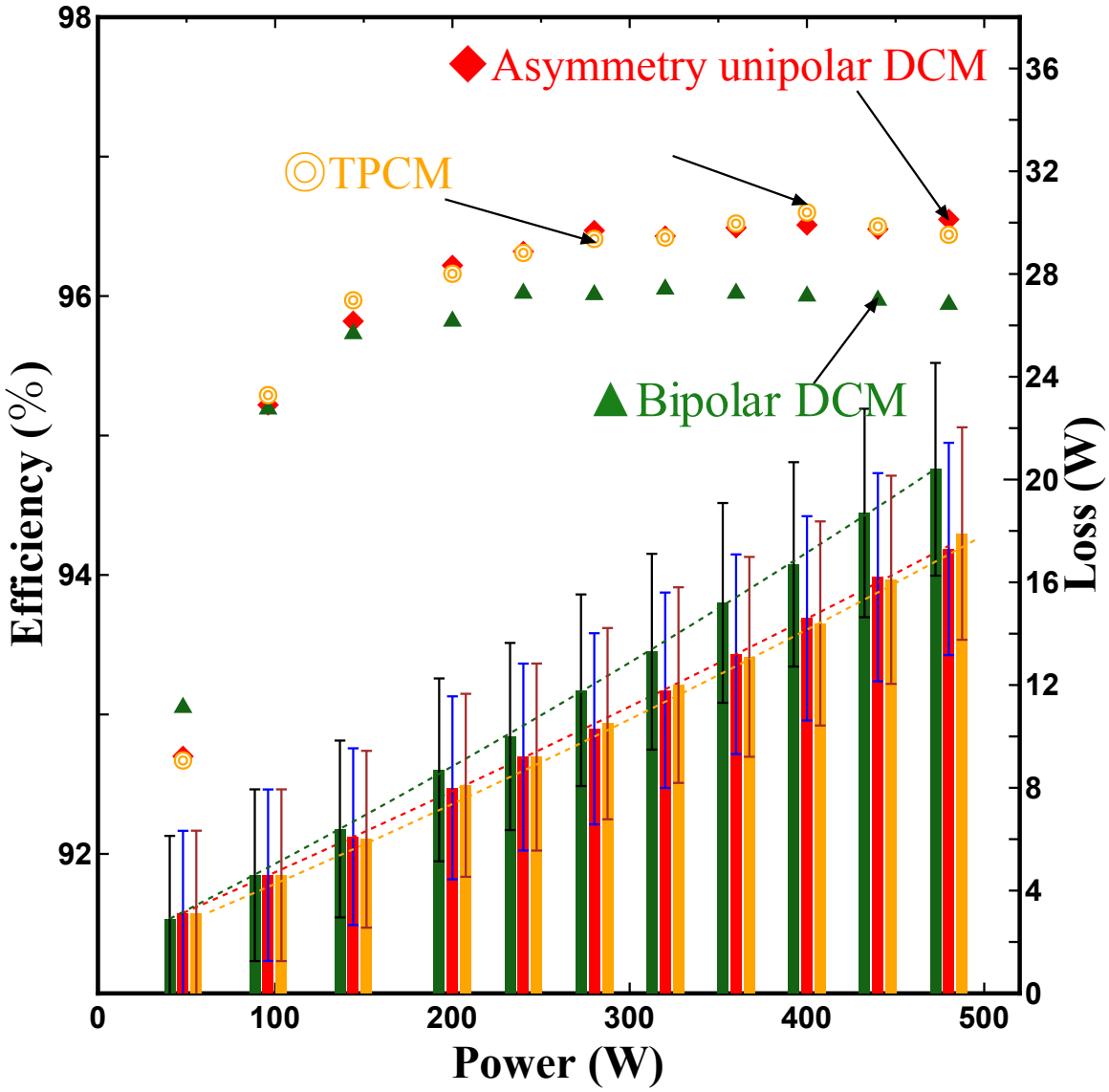

Fig. 3.25 Measured efficiencies against output power.

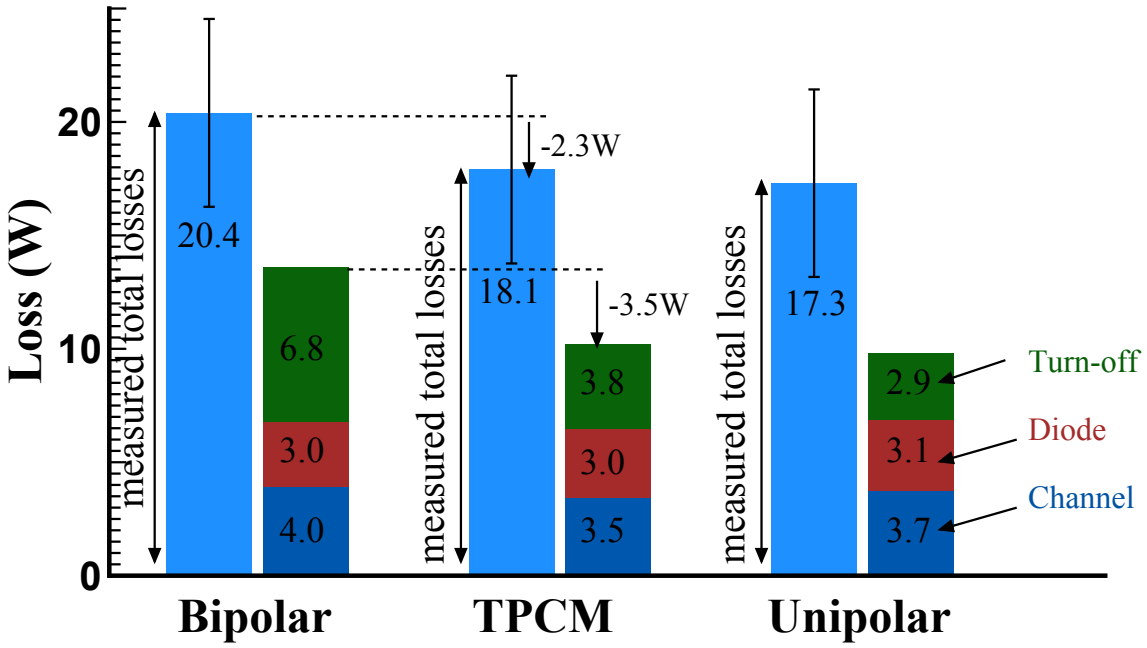

Fig. 3.26 An estimation of loss break-down for bipolar DCM, asymmetry unipolar DCM and proposed TPCM when $I_{\text{ac.set}} = 2.4$ A.

of corresponding switch (obtained in simulation) and I-V characteristic of the switch body diode shown in the datasheet. The turn-off losses were obtained by using calculated turn-off currents and data of turn-off losses shown in datasheet.

The reduction in semiconductor losses (-3.5W) almost agreed with the reduction in total losses (-2.3W). In comparison with bipolar DCM, the inductor r.m.s. current of TPCM is reduced by 6.5% and the resultant reduction in conduction losses is 7.1%; and the average turn-off current of TPCM is reduced by 45.2% and the resultant reduction in turn-off losses is 44.1%. Therefore, the reductions in conduction loss and turn-off loss can almost agreed with the reduced inductor r.m.s. current and average turn-off current, respectively. The reduction of turn-off losses contributed to the reduction in total losses more than the reduction of conduction losses. Therefore it can be considered as the main reason for the total loss reduction. In addition, the inductor losses can also be reduced by the reduced peak inductor current. However, it is difficult to discuss this further when the error bars (caused by measurement error) are taken into consideration.

3.5 Conclusion

The asymmetry unipolar DCM benefits from lower switching losses and peak currents, however, the distortions around zero-crossing of AC voltage can be caused by the slow magnetizing rate of inductor current. This problem does not exist in the bipolar DCM since the magnetizing rate of inductor current is sufficient high. In this chapter, a novel switching scheme that combines the conventional bipolar and asymmetry unipolar DCM is proposed. The proposed switching features high control degree of freedom so that the operation modes can be shifted freely in between the conventional twos. A modulation technique is also presented to reduce the peak inductor current and improve the zero-crossing distortion problem for the asymmetry unipolar DCM. The proposed modulation was verified by a 480 W class prototype in the experiment. The lowest peak currents were achieved in the proposed TPCM, meanwhile, without zero-crossing distortion problem being obtained. The reduced peak inductor current leads to the reduction of turn-off losses and conduction losses in TPCMs, and that leads to higher effciencies at heavy loads in comparison with the conventional bipolar DCM. The improved current quality regarding to no zero-cross distortion problem, makes the TPCMs more attractive than asymmetry unipolar DCM since similar efficiency can be obtained.

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Chapter 4

Modulations for Reducing Harmonic Distortion Caused by Parasitic Capacitance

4.1 Introduction

In this chapter, two modulation methods, which are based constant and variable switching frequency, are proposed to reduce the high-order harmonic distortions for DCM grid-tied inverters designed with high frequency operation. The high-order distortions are caused by resonance between inductors and parasitic capacitor of switching devices during the zero current period of DCM. For conventional model-based control, an ideal model that neglects the resonance is considered. However, the influence of parasitic capacitor becomes non-negligible under high frequency operations. In order to eliminate the current distortion, an improved model that considers the resonance is analyzed. The proposed modulation methods that based on this model are proposed to mitigate the effect caused by the resonance. The effectiveness with respective to harmonic reduction of the proposed methods is validated by experiment verification.

This chapter is organized as follows: in Section 4.2, the origin of high-order harmonic distortions that occurred in a DCM grid-tied inverter is explained in detail. The impacts of high-order harmonic distortions on the DCM grid-tied inverters are discussed. Several exist methods that can be used to reduce the distortions are discussed and their demerits are pointed out. The first modulation that based on constant switching frequency is proposed in Section 4.3. The second modulation that based on variable switching frequency is proposed in Section 4.4. The model-based calculation, model derivation for resonance and modulation concept for each method are present in these Sections. The proposed methods are validated and discussed by a simulation verification, as shown in Section 4.3.4 and Section 4.4.5, respectively. The experimental verification and analysis for the first modulation are presented in Section 4.3.5 and Section 4.3.6. The experimental verification and analysis for the second modulation are presented in Section 4.4.6. Finally, The conclusion of this chapter is given in Section 4.5.

4.2 Effect Caused by Parasitic Capacitance of Devices

4.2.1 Current Distortion and its Impacts on DCM grid-tied Inverters

In recent years, many researchers have proposed to change the design from CCM to DCM or BCM for the low-power grid-tied inverters, aiming at size reduction of the inductors and/or achieving soft-switching [1–14]. In Chapter 2, the comparison between BCM and DCM is shown, and it is pointed out that the DCM can be suitable for high frequency designed grid-tied inverters. For a DCM grid-tied inverter, a model-based control can be more advantageous and suitable, because the converter can be operated without sensing i_{Lac}. With the model-based control, difficulties that relates to current detection and sampling corrections are no longer lying. Owing to the different strategy of current control, the DCM gird-tied inverters can be designed to operate at further high frequency to reduce the volume

of grid-connected inductors. However, a distortion problem that caused by the parasitic capacitors of switching devices becomes non-negligible under high frequency operations, as discussed in Chapter 2.

Conventionally, the model built for the DCM is based on a assumption that the current flowing through inverter-side inductor, i_{Lac}, is an ideal triangular shape and has a zero current period [3, 4]. The corresponding switches are always turned on with zero current in this case. In practical; however, an oscillating current flows as i_{Lac} during the zero current period. This is caused by the resonance between the inductor and parasitic output capacitance of switching device. The initial values of i_{Lac} then cannot always be zero, which cause a behavior of non-uniform for the turn-on switches due to this oscillating current. As a result, the average current cannot follow the current reference any more due to the increased or decreased peak current; and the output current becomes distorted in consequence. Moreover, the distortion becomes more severe under high switching frequency conditions, which have impacts on further reduction of inductor volumes and efficiency improvements for the converter.

Fig. 4.1 shows a simulation result of conventional DCM under two different switching frequencies with a given parasitic output capacitance being applied to all the switches. In the top plot, the switching frequency, f_{sw}, is set to be 20 kHz; in the bottom plot, f_{sw}, is set to be 100 kHz. The grid-side inductor current, i_{ac}, are distorted in both top and bottom plots. However, the distortion of i_{ac} in the bottom plot is worse than that in the top plot. The total harmonic distortion (THD) of the grid-side inductor current i_{ac} is increased from 2.0% to 6.5% after the switching frequency is increased from 20 kHz to 100 kHz. Consequently, this kind of distortion can be severer under higher switching frequencies (i.e. when the inverter-side inductance becomes smaller) for a given device. The converter cannot be designed to operate at very high switching frequencies in order to avoid the distortion. Further reduction of inductor volumes thus can be limited due to this reason.

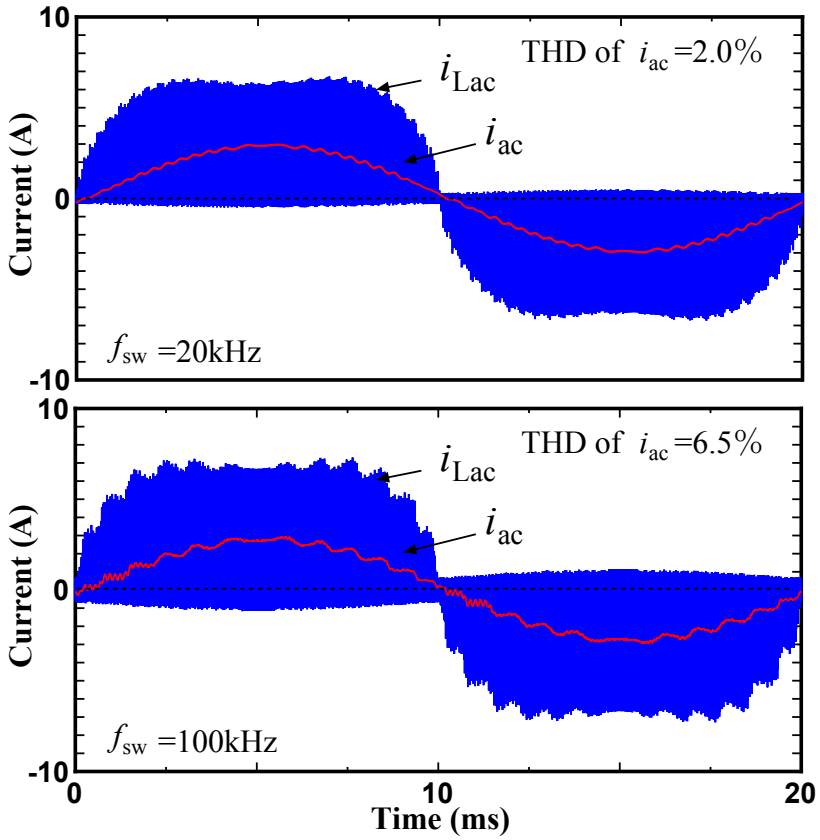

Fig. 4.1 Time domain simulation of a bipolar DCM modulation under two different switching frequencies. The drain-source capacitance, C_{ds}, was set at 0.4 nF. Simulation conditions: $V_{dc} = 400$ (V), $V_{ac} = 200$ (V), $I_{rated} = 2$ (A), $L_{ac} = 130$ (μH), $L_f = 125$ (μH), $C_f = 2.2$ (μF).

Fig. 4.2 shows a simulation results of conventional DCM with two different parasitic output capacitance being applied to the switching device, while the switching frequencies are the same. In the top plot, the parasitic output capacitance, C_{ds}, is set to be 0.1 nF; in the bottom plot, C_{ds}, is set to be 0.4 nF. Higher THD of i_{ac} can also be obtained with a large C_{ds} being applied. Consequently, the distortion can also be worse if a device with larger parasitic output capacitance is adopted for a given switching frequency. Devices with small chip size therefore small parasitic capacitance should be adopted to avoid the distortion. However, a small chip size in the device leads to large on-state resistance therefore more conduction losses. Further improvement on the converter efficiencies thus can be limited due to this reason.

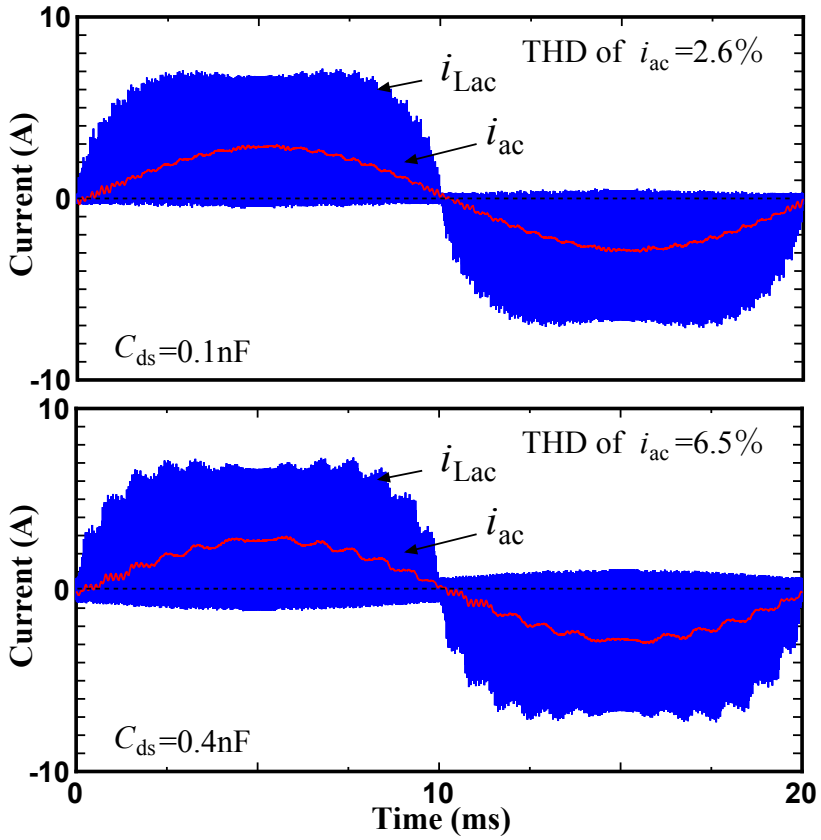

Fig. 4.2 Time domain simulation of a bipolar DCM modulation with two different drain-source capacitance applied to the switching device. The switching frequency, f_{sw}, was set to be 100 kHz. Simulation conditions: $V_{dc} = 400$ (V), $V_{ac} = 200$ (V), $I_{rated} = 2$ (A), $L_{ac} = 130$ (μH), $L_f = 125$ (μH), $C_f = 2.2$ (μF).

4.2.2 An Estimation of Generated Harmonics with Conventional DCM

In order to investigate how far the current quality of a DCM grid-tied inverter can be influenced by the parasitic capacitance, harmonics generation with conventional DCM under different power capacities are estimated and evaluated. The estimation is based on a 400 W single-phase converter, whose specifications are listed in Table 4.1. Design parameters of higher capacity of converters are calculated based on this design.

In order to evaluate the relative harmonics, several assumptions are made. The switching devices is assumed to have the same voltage rating but the current ratings of device are proportional to the capacities of converter. Parasitic capacitance of switching device, C_{ds}, is

Table 4.1 Based Design Parameter

DC link voltage	V_{dc}	400 V
AC voltage	V_{ac}	200 V
Fundamental current	$I_{1.\text{base}}$	2 A
Power	P	400 W
Parasitic capacitance	$C_{\text{ds.base}}$	0.2 nF
Inverter-side inductance	$L_{\text{ac.base}}$	135 μH
Switching frequency	$f_{\text{sw.base}}$	100 kHz
Switching device	SCT2160KE	1200 V, 22 A

assumed to be proportional to the device current rating therefore the power, P, as expressed as

$$C_{\text{ds}} = \frac{P}{P_{\text{base}}} \cdot C_{\text{ds.base}}, \tag{4.1}$$

where P_{base} is the power of converter with based design, $C_{\text{ds.base}}$ is the parasitic capacitance of switching device of the based design. The inductance, L_{ac}, is inverse-proportional to the current rating, therefore power, P; and it is also inverse-proportional to the switching frequency, f_{sw}, as expressed as

$$L_{\text{ac}} = \frac{P_{\text{base}}}{P} \cdot \frac{f_{\text{sw.base}}}{f_{\text{sw}}} \cdot L_{\text{ac.base}}, \tag{4.2}$$

where $f_{\text{sw.base}}$ is the switching frequency of based design, $L_{\text{ac.base}}$ is the inverter-side inductance of based design. The amplitude of resonant current, whose schematic view is shown in Fig. 4.3, with based design, $I_{\text{res.base}}$, has relationship with $C_{\text{ds.base}}$ and $L_{\text{ac.base}}$, and can be expressed as

$$I_{\text{res.base}} \propto \sqrt{\frac{C_{\text{ds.base}}}{L_{\text{ac.base}}}}. \tag{4.3}$$

Assuming that the switching frequency is the same with the based design, the amplitude of resonant current, I_{res}, can be expressed as

$$I_{\text{res}} \propto \sqrt{\frac{C_{\text{ds}}}{L_{\text{ac}}}} = \sqrt{\frac{\frac{P}{P_{\text{base}}} \cdot C_{\text{ds.base}}}{\frac{P_{\text{base}}}{P} \cdot L_{\text{ac.base}}}} = \frac{P}{P_{\text{base}}} \cdot I_{\text{res.base}}. \tag{4.4}$$

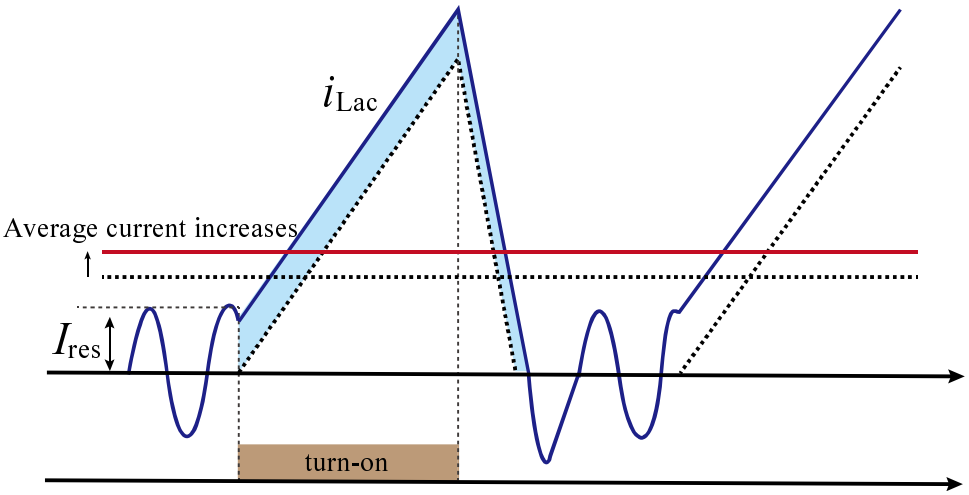

Fig. 4.3 Schematic view of the amplitude of resonant current, I_{res}.

The fundamental current with based design, I_1, can be expressed as

$$I_1 = \frac{P}{P_{base}} \cdot I_{1.base}, \tag{4.5}$$

where $I_{1.base}$ is the fundamental current of based design. It is difficult to expressed the total harmonic distortion (THD) directly. Consequently, the relative harmonic, h, is roughly estimated by using the above models, and expressed as

$$h = \frac{I_{res}}{I_1} = \frac{\frac{P}{P_{base}} \cdot I_{res.base}}{\frac{P}{P_{base}} \cdot I_{1.base}} = \frac{I_{res.base}}{I_{1.base}}. \tag{4.6}$$

The result indicates that the relative harmonics can be independent of converter power rating.

A simulation software (PSIM) is used to evaluate the harmonic distortions of several design examples. The results are shown in Fig. 4.4. An upper limitation of switching frequency can be found to keep the THD lower than 5% at rated operation. This limitation can be considered as the maximum designed frequency of the DCM converter. The simulation results almost agreed with the assumption that the harmonics does not increase even at higher power levels, though the limitation of switching frequency was slightly increased.

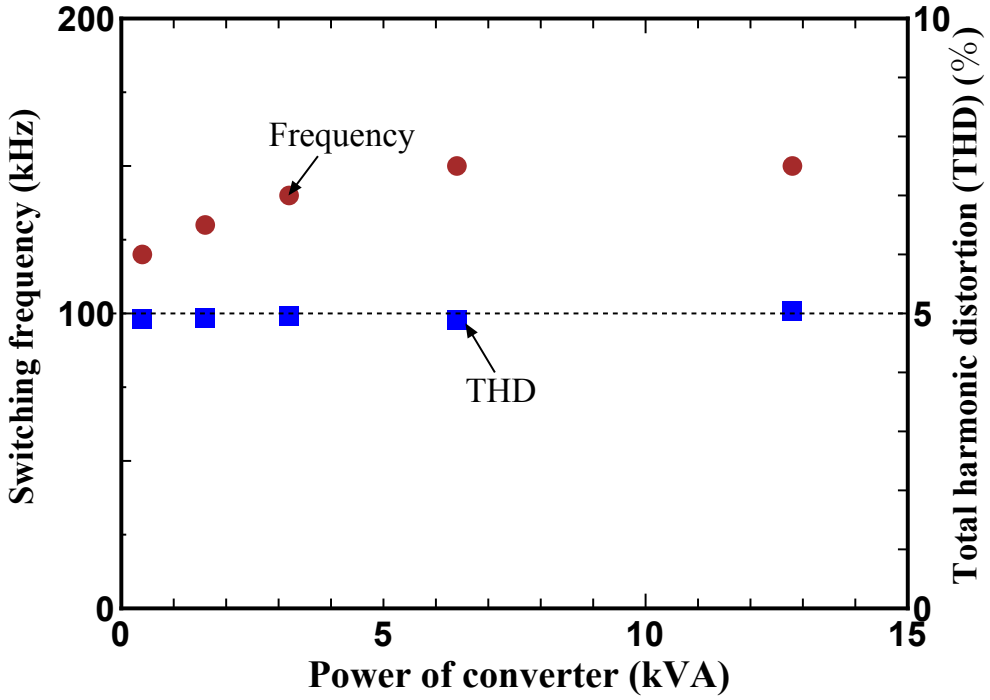

Fig. 4.4 Limitations of switching frequency against capacity of converter.

Consequently, it can be considered that the limitations of switching frequency for high-power levels are almost the same with those for low-power levels, with a given device technology and rule of design being applied. Generally, however, the designed switching frequency for high-power level inverters cannot be such high in comparison with that for low-power inverters in order to keep low power dissipation of semiconductor devices therefore less cooling requirements. Consequently, the influence of parasitic capacitance can be small on high-power inverters.

4.2.3 Possible Solutions to the Current Distortion

From the above estimations, it is found that the parasitic capacitance has more impact on low-power grid-tied inverters. In order to realize high frequency operation for low-power DCM grid-tied inverters, the distortions caused by parasitic capacitance of switching device is required to be eliminated. It is difficult to eliminate this kind of distortion by the partial

feedback control. Firstly, the order of harmonics in the distorted current are usually high, typically around fifteenth to fortieth order. Therefore, the frequency of harmonics are difficult to be predicted. Consequently, it is impractical to cascade the SOGIs that being tuned at each harmonic frequency to eliminate the distortion, because of the burden computations being required can be a problem. Secondly, the average values of inverter-side inductor is under controlled while the grid-side inductor current is measured. Therefore, phase delays that caused by the current going through the filter capacitor also make the high-order harmonics difficult to be corrected by the harmonic compensators.

This kind of current can be avoid if the peak current are controlled to be equal to a predefined reference [15]. By doing this, the peak current are not affected by the initial inductor current. Therefore, the inductor current area and average current can be almost the same with the desired values. However, the detection of triangular peak current can be a challenge under high frequency operation, as discussed in previous sections.

The distortion can also be eliminated by clamping the inductor voltage being constant during the oscillating current periods [16]. This requires the use of bi-directional switches being parallel connected to the inverter-side inductors. Consequently, the increased costs in terms of additional switches and driver circuits can be the drawback of this technique approach.

On the other hand, the high-order distortions can be reduced by damping the oscillating current [17]. In previous study with respective to a PFC converter application, several snubber circuits that consists of resistor, capacitor and diode have been proposed to damp the oscillating current so that the initial current at turn-on instant can be almost the same. This method is simple and effective, however, power dissipation of these snubber circuits can reduce the overall efficiencies of system.

A turn-on delay method can also be applied to make the corresponding switches to turn on with the same initial current [18]. After the inductor reduces to zero, a pre-programmed

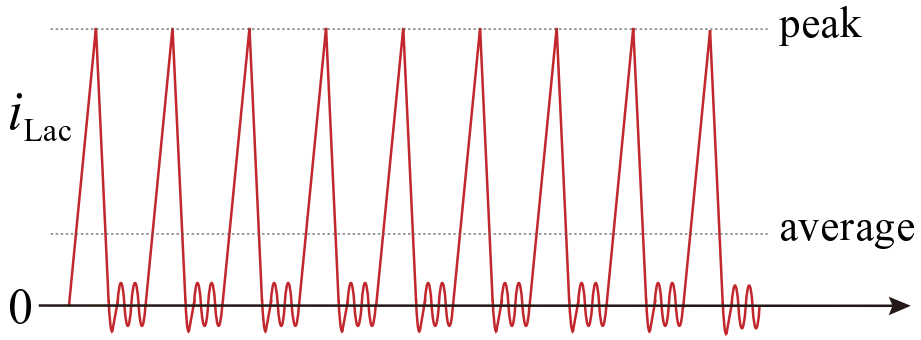

Fig. 4.5 Schematic views of the inverter-side inductor current caused by uniform turn-on behavior.

delay time is used to delay the turn-on instant. The switches can always be turned on at the same point by this kind of technique. However, it also rely on the detection of zero-cross of the triangular inductor current. Consequently, it has the same difficulty with the model-based BCM control.

In comparison with using additional components or inductor current detection, it is desired to rely on control methods only to reduce the high-order distortions. However, relatively solutions are seldom reported in the previous literature. Since the high-order current distortion is caused by the non-uniform turn-on behavior, it can be corrected by achieving an uniform turn-on behavior,in which the initial values of the inductor current, i_{Lac}, for every switching cycle become the same, as shown in Fig. 4.5. This purpose, however, cannot be realized with conventional DCM controls due to the low degree of freedom on controlling the inductor current. For a given switching frequency, there is only one set of duty ratios to achieve a given average current so that the length of resonance current period, which is dependent on the length of turn-on and turn-off times, cannot be changed freely. In order to control the length of resonance current period, more control degrees of freedom are necessary. From this point of view, two modulation strategies, which are based on different approaches, are proposed in this chapter. In the first approach, the trapezium current mode (TPCM), which is proposed in the Chapter 3, is used to achieve the uniform turn-on with

appropriate modulation strategies. In the second approach, a frequency variation modulation is proposed to achieve the uniform turn-on.

4.3 Proposed Modulation Based on Constant Frequency

4.3.1 Operation Principles of TPCM

Fig. 4.6 shows the possible current paths during one switching cycle operation in the TPCM, where the resonance current is considered during interval 4. The one switching cycle of TPCM composes four main intervals, the operation principles for the positive line voltage are briefly described as follow:

Interval 1:

S_1, S_4 are turned on simultaneously and switches S_2, S_3 are kept off. the current flowing through the inverter-side inductor, i_{Lac}, increases linearly. The interval 1 ends when the switch S_1 is turned off.

Interval 2:

S_4 is still in on-state. i_{Lac} decreases linearly through the body diode of S_3 after S_1 is turned off. The interval 2 ends when S_4 is turned off.

Interval 3:

After S_4 is turned off, i_{Lac} decreases linearly through the body diode of S_2 and S_3. The interval 3 end when i_{Lac} reduces to zero.

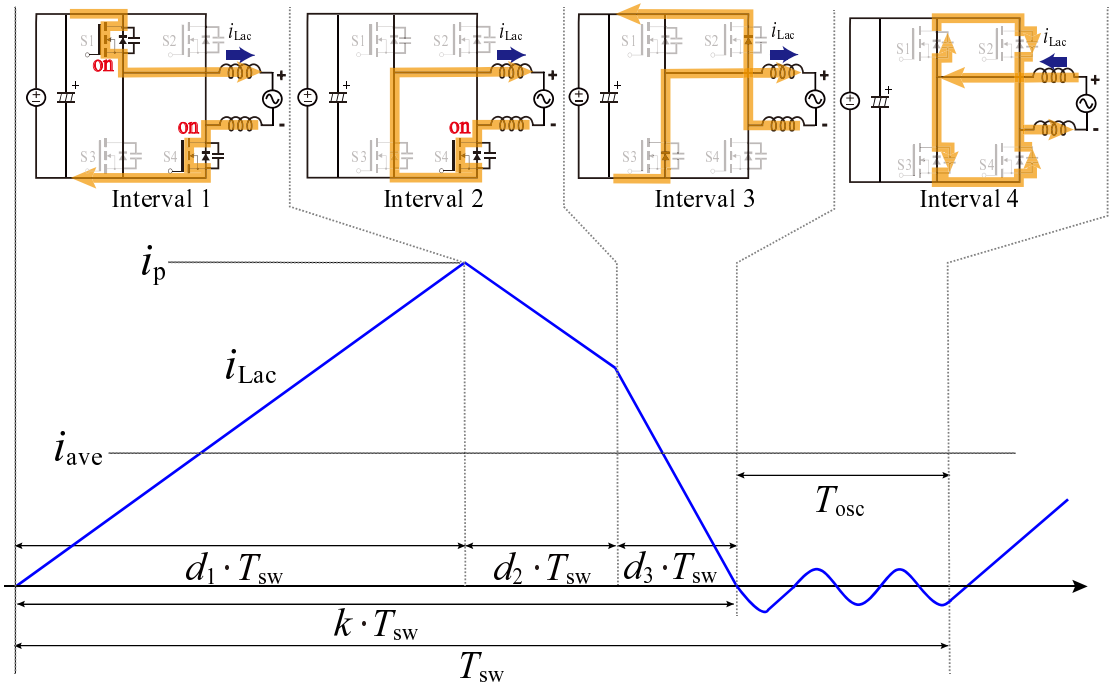

Fig. 4.6 Possible current paths of one switching cycle operation in TPCM for positive grid voltage V_{ac}.

Interval 4:

During this interval, the inductor current forms a resonant circuit with the parasitic capacitors of all the switches. i_{Lac} flows through the inductor and oscillates around zero with finite amplitudes. At the same time, the voltages cross the switches also oscillate freely due to the parasitic capacitor being charged and discharged by i_{Lac}. After this interval, S_1 and S_4 are turned on again and a new switching cycle begins. In order to compensate for the effect caused by the resonant current, i_{Lac} with same initial values should be achieved at next turn-on for the corresponding switches.

The feature of TPCM is that the inductor current shape can be changed freely for a given average current. The duty utilization can be controlled by using different sets of duty ratios, as discussed in Chapter 3. This feature also indicates that the length of interval 4, T_{osc}, and the behavior of resonance current, i_{Lac}, (therefore oscillating voltage across the switches) can be controlled.

4.3.2 Model of Resonance During Interval 4

A model considering the resonance behavior during the interval 4 is analyzed in this section. In the following sections, the discussions are based on the assumption of unity power factor operation for the inverter.

During interval 4, there are two kinds of resonance periods, as can be observed in Fig. 4.7. The first resonance period is referred to as T_1, and one period of the second resonance is referred to as T_2. The total duration of the resonance period, T_{osc}, can be expressed as

$$T_{\text{osc}} = T_1 + n \times T_2, \tag{4.7}$$

where n is the number of cycles for the second resonance. It is suggested to apply integer numbers for n so that both the uniform turn-on and the zero-voltage switching (ZVS) can be achieved.

During T_1, the switch voltage v_{S1} and v_{S4} resonate to zero first. By assuming that i_{Lac} is zero at t_4, v_{S1} and v_{S4} during the resonance process can be expressed as

$$v_{\text{S1}}(t) = v_{\text{S4}}(t) = \frac{1}{2}V_{\text{dc}}(\cos(\sqrt{2}\omega_{\text{r}}(t-t_4)) + 1) + \frac{1}{2}v_{\text{ac}}(\cos(\sqrt{2}\omega_{\text{r}}(t-t_4)) - 1), \tag{4.8}$$

where

$$\omega_{\text{r}} = \sqrt{\frac{1}{2L_{\text{ac}}C_{\text{ds}}}}, \tag{4.9}$$

where V_{dc} and v_{ac} denote the DC link and the instantaneous line voltage, respectively. L_{ac} denotes the inductance of inverter-side inductor, C_{ds} denotes the estimated drain-source capacitance of the power devices and assumed to be same for all the devices. ω_{r} represents the resonance angular frequency.

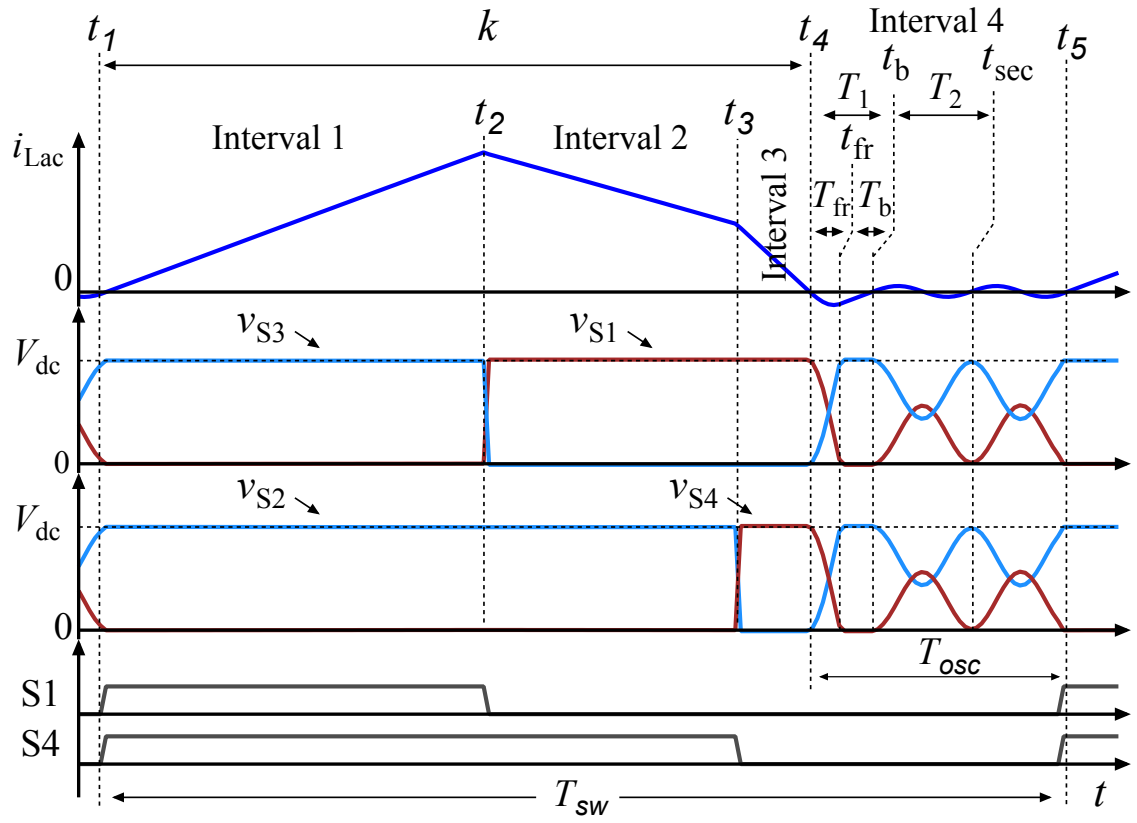

Fig. 4.7 Key waveforms during one switching cycle in TPCM.

The minimum voltage of v_{S1} and v_{S4} can be derived by substituting $\cos(\sqrt{2}\omega_r(t-t_4)) = -1$ into (4.8), which are

$$v_{S1} = v_{S4} = -v_{ac}. \tag{4.10}$$

The results indicate that v_{S1} and v_{S4} can reach zero always during T_1 since $-v_{ac}$ is always negative during the half line cycle with positive grid voltage.

T_{fr} is the time required to discharge v_{S1} and v_{S4} from V_{dc} to zero. T_{fr} can be calculated by solving $v_{S1} = 0$, and expressed by

$$T_{fr} = \frac{1}{\sqrt{2}\omega_r} \arccos\left(\frac{|v_{ac}| - V_{dc}}{|v_{ac}| + V_{dc}}\right). \tag{4.11}$$

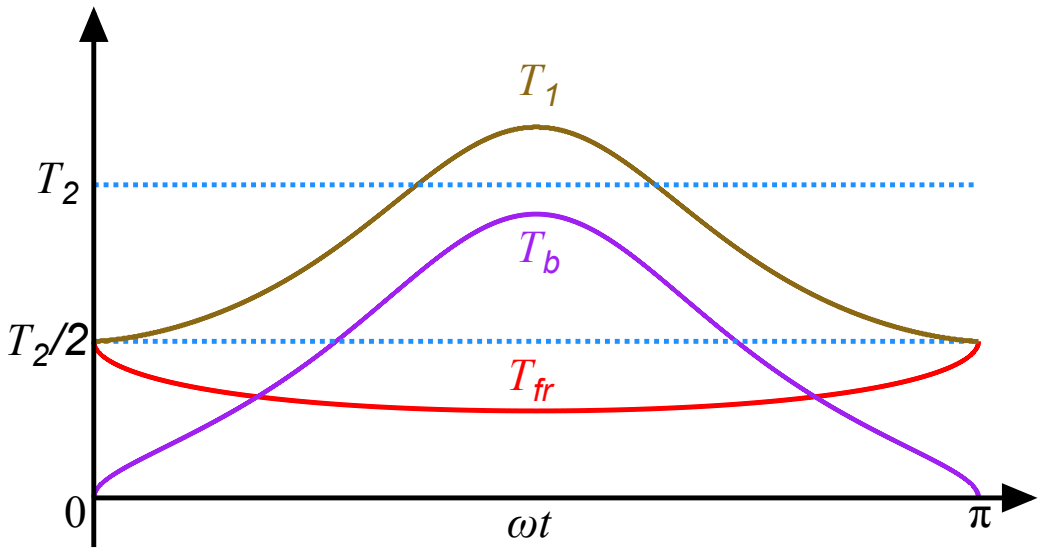

Fig. 4.8 Examples of T_{fr} and T_{b} over half line period calculated based on a certain specification for unity power factor operation.

After v_{S1} and v_{S4} become zero at t_{fr}, i_{Lac} will flow through the body diodes of S_1 and S_4, and the negative voltage is blocked by the body diodes. i_{Lac} during this process can be expressed as

$$i_{\mathrm{Lac}}(t) = \frac{(V_{\mathrm{dc}} - v_{\mathrm{ac}})}{L_{\mathrm{ac}}} \cdot (t - t_{\mathrm{fr}}) - \frac{\sqrt{2}(V_{\mathrm{dc}} + v_{\mathrm{ac}})}{2Z_{\mathrm{n}}} \cdot \sin(\sqrt{2}\omega_{\mathrm{r}} t_{\mathrm{fr}}), \tag{4.12}$$

where Z_{n} is

$$Z_{\mathrm{n}} = \sqrt{\frac{L_{\mathrm{ac}}}{2C_{\mathrm{ds}}}}. \tag{4.13}$$

When i_{Lac} becomes zero at t_{b}, the blocked period is end. The block time, T_{b}, can be calculated as

$$T_{\mathrm{b}} = \sqrt{L_{\mathrm{ac}} C_{\mathrm{ds}}} \left(\frac{V_{\mathrm{dc}} + |v_{\mathrm{ac}}|}{V_{\mathrm{dc}} - |v_{\mathrm{ac}}|} \right) \sin(\sqrt{2}\omega_{\mathrm{r}} T_{\mathrm{fr}}). \tag{4.14}$$

T_{fr} and T_{b} are functions of the grid voltage phase, ωt. Fig. 4.8 shows an example of T_{fr} and T_{b} over half line period calculated based on a certain specification.

T_2 is assumed to be constant, and approximated by

$$T_2 \approx 2\pi\sqrt{L_{ac}C_{ds}}. \tag{4.15}$$

During T_2, v_{S1} and v_{S4} start from zero and oscillate without touching boundary. If the oscillation is a pure LC oscillation, v_{S1} and v_{S4} during T_2 can be expressed as

$$v_{S1}(t) = v_{S4}(t) = \frac{1}{2}(V_{dc} - v_{ac})(-\cos(\sqrt{2}\omega_r(t-t_b)+1). \tag{4.16}$$

The valley voltage of v_{S1} and v_{S4} can be derived by substituting $\cos(\sqrt{2}\omega_r(t-t_b)) = 1$ into (4.16), which is

$$v_{S1} = v_{S4} = 0. \tag{4.17}$$

This indicates that v_{S1} and v_{S4} start from zero and can reach zero again at t_{sec} when $i_{Lac} = 0$; therefore, the ZVS and the uniform turn-on can be achieved in the next switching cycle by controlling T_{osc} to make this switching cycle terminated at this instant.

4.3.3 Modulation Method to Achieve Uniform Turn-On

In this section, the application of the TPCM to achieve the uniform turn-on and to improve the current distortion problem are proposed and discussed. In the proposed modulation with TPCM, T_{osc} is decided and calculated preliminary to satisfy (4.7), then the duty ratios are calculated and evaluated. The duty ratios of the interval 1, 2 and 3, d_1, d_2 and d_3, respectively, can be calculated from the model built for the inductor current, as discussed in chapter 4. The sum of d_1, d_2 and d_3 is referred to as the duty utilization, k, which is

$$k = d_1 + d_2 + d_3 = 1 - T_{osc}f_{sw}, \tag{4.18}$$

and should be set as

$$k = 1 - (T_1 + nT_2) f_{\mathrm{sw}}, \tag{4.19}$$

to achieve the uniform and ZVS turn-on.

The duty ratios, d_1, d_2, d_3, to achieve i_{ref} are expressed as

$$d_1 = \begin{cases} -\dfrac{\sqrt{k^2 {V_{\mathrm{dc}}}^2 - k^2 {v_{\mathrm{ac}}}^2 - 4V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}}}}{2V_{\mathrm{dc}}} + \dfrac{kV_{\mathrm{dc}} + kv_{\mathrm{ac}}}{2V_{\mathrm{dc}}} & (i_{\mathrm{ref}} > 0) \\ -\dfrac{\sqrt{k^2 {V_{\mathrm{dc}}}^2 - k^2 {v_{\mathrm{ac}}}^2 + 4V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}}}}{2V_{\mathrm{dc}}} + \dfrac{kV_{\mathrm{dc}} - kv_{\mathrm{ac}}}{2V_{\mathrm{dc}}} & (i_{\mathrm{ref}} < 0) \end{cases} \tag{4.20}$$

$$d_2 = \begin{cases} \dfrac{\sqrt{k^2 {V_{\mathrm{dc}}}^2 - k^2 {v_{\mathrm{ac}}}^2 - 4V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}}}}{V_{\mathrm{dc}}} & (i_{\mathrm{ref}} > 0) \\ \dfrac{\sqrt{k^2 {V_{\mathrm{dc}}}^2 - k^2 {v_{\mathrm{ac}}}^2 + 4V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}}}}{V_{\mathrm{dc}}} & (i_{\mathrm{ref}} < 0) \end{cases} \tag{4.21}$$

$$d_3 = \begin{cases} -\dfrac{\sqrt{k^2 {V_{\mathrm{dc}}}^2 - k^2 {v_{\mathrm{ac}}}^2 - 4V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}}}}{2V_{\mathrm{dc}}} + \dfrac{kV_{\mathrm{dc}} - kv_{\mathrm{ac}}}{2V_{\mathrm{dc}}} & (i_{\mathrm{ref}} > 0) \\ -\dfrac{\sqrt{k^2 {V_{\mathrm{dc}}}^2 - k^2 {v_{\mathrm{ac}}}^2 + 4V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}} i_{\mathrm{ref}}}}{2V_{\mathrm{dc}}} + \dfrac{kV_{\mathrm{dc}} + kv_{\mathrm{ac}}}{2V_{\mathrm{dc}}} & (i_{\mathrm{ref}} < 0) \end{cases} \tag{4.22}$$

, respectively. Different k can be obtained with different n being applied; therefore, different set of duty ratios can be found(or can not be found) for the same reference current. Since the switching frequency is fixed, T_{osc} becomes longer when the current phase angle is close to zero or π. Therefore, n can not be fixed and should be changed as function of the current phase angle.

Fig. 4.9 illustrates the flowchart of the sequence to determine n. The expression in the square root must be greater than zero, which can be expressed by a variable, Δ, as

$$\Delta = k^2 {V_{\mathrm{dc}}}^2 - k^2 {v_{\mathrm{ac}}}^2 - 4V_{\mathrm{dc}} L_{\mathrm{ac}} f_{\mathrm{sw}} |i_{\mathrm{ref}}| \geq 0. \tag{4.23}$$

In addition, d_1, d_2 and d_3 should always be positive values. It is obvious that d_2 is always positive. However, d_3 decreases along with the increasing of d_2. Consequently, negative

values of d_3 can sometimes be obtained in the duty calculations. Therefore, a minimum value for d_3, $d_{3.\min}$, is set in order to maintain the trapezium current shape. n should be selected to satisfy $\Delta \geq 0$ and $d_3 \geq d_{3.\min}$. Meanwhile, n should be low as possible in order to avoid useless high peak inductor current.

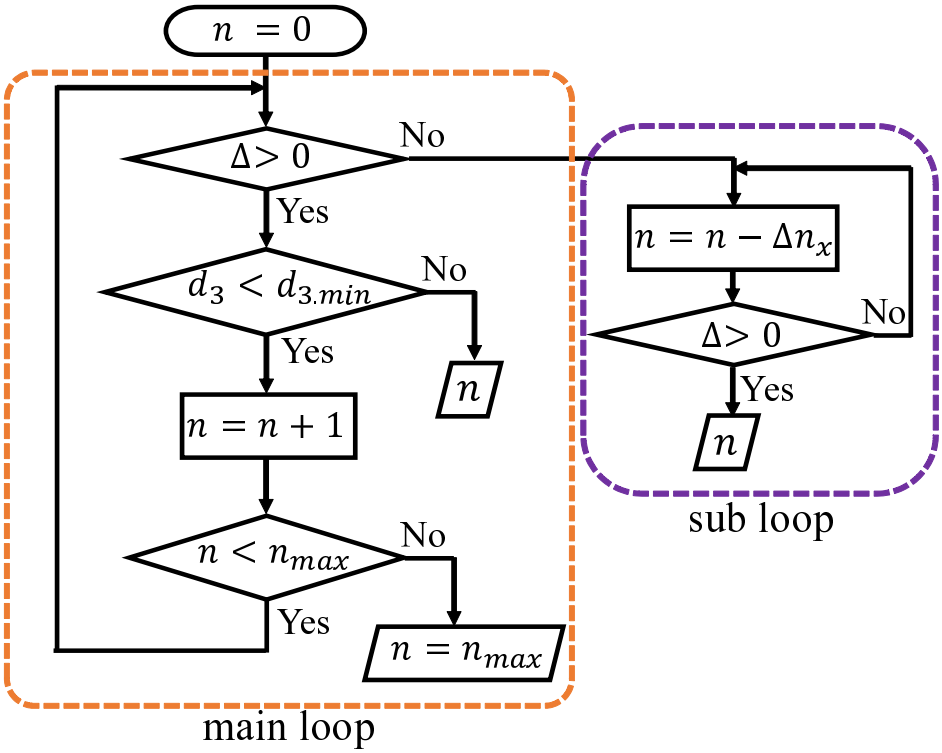

Fig. 4.9 Flowchart of the sequence to determine n.

There are still two problems in the process to find n. Firstly, the resultant of d_1, d_2 and d_3 can be close to zero around current zero-crossing. In this case, d_3 higher than $d_{3.\min}$ cannot be satisfied even n is increased. At the same time, n should be restricted in order to avoid infinite computations. The maximum value of n, $n_{\max}$, is defined and calculated by assuming d_1, d_2 and d_3 are zero and neglecting T_1, which is

$$n_{\max} = \lfloor T_{\rm sw}/T_2 \rfloor. \tag{4.24}$$

The proposed sequence evaluates n from zero to $n_{\max}$ whether it satisfies the conditions. However, any integer number to satisfy $d_3 > d_{3.\min}$ may not be found even if $n = n_{\max}$ is finally selected. Nevertheless, the influence can be ignored since the current is almost zero in that kind of situations.

Secondly, there can also be the cases that any integer number for n can not be found with satisfying $\Delta \geq 0$ and $d_3 \geq d_{3.\min}$ to achieve $i_{\text{ave}} = i_{\text{ref}}$ even for not small current reference. This can occur especially in the cases with relatively large C_{ds} due to the corresponding long oscillation cycles. For the cases, a resolution factor referred to as Δn_{x} can be used to modify n in order to find solutions. However, the ZVS and uniform turn-on can not be achieved if the modification is applied. Δn_{x} should not be very small in order to avoid too much computations; however, too large Δn_{x} may result in no solutions obtained.

4.3.4 Simulation Verification and Analysis

Estimation for Parasitic Output Capacitance of Device

Estimating the equivalent drain-source capacitance of the switch, C_{ds}, is required to operate converters with the proposed modulation method. In general, the parasitic capacitance of semiconductor devices exhibits a non-linear voltage dependency. However, the equivalent value of C_{ds} to be used for the calculation can be defined for a range of oscillating voltage. The value for the proposed modulation is same with that for the conventional DCM since the range of oscillating voltage is same. C_{ds} can be estimated from the resulting resonant time, T_2, with the assumption that the inductance, L_{ac}, is fixed. T_2 can be obtained by measuring it in a preliminary operation of the converter with the conventional DCM. C_{ds} can be approximated by

$$C_{\text{ds}} \approx \frac{{T_2}^2}{4\pi^2 L_{\text{ac}}}. \tag{4.25}$$

It should be noted that C_{ds} does not represent the real parasitic capacitance of the switching device. The time for the resonance can be fine-tuned by adjusting C_{ds} in the duty calculation. However, probable individual differences in C_{ds} and L_{ac} among switching devices and inductors in mass production, and the variation of L_{ac} caused by temperature change can be a challenge to achieve the perfect operation of the concept.

Table 4.2 Parameters and Conditions

Simulation and Experimental Conditions for SiC-Based Prototype		
DC voltage	V_{dc}	400 V
AC voltage	V_{ac}	200 V
Line frequency	f_{line}	50 Hz
Rated current	$I_{ac.rated}$	1.85 A
Switching frequency	f_{sw}	100 kHz
Estimated drain-source capacitance	C_{ds}	0.4 nF
Resolution factor	Δn_x	0.1
Minimum value of d_3	$d_{3.min}$	0.01

LCL Filter Design Parameters for SiC-Based Prototype		
Inverter-side inductance	L_{ac}	130μH
Percentage impedance of L_{ac}	$\%X_{Lac}$	0.036%
Grid-side inductance	L_f	125 μH
Percentage impedance of L_f	$\%X_{Lf}$	0.045%
Filter capacitance	C_f	2.2 μF

Simulation Results

A simulation was used to validate the proposed modulation and evaluate the improvements in comparison with the conventional modulation. The simulation conditions were the same with the conditions for the experiments shown in the next section, as listed in Table 4.2.

The simulation results of inverter-side inductor current, i_{Lac}, the grid-side inductor current, i_{ac}, and duty ratio, d_1, with the conventional modulation and the rated current operation are shown in Fig. 4.10. Unacceptable level of the current distortion in i_{ac} was observed. The total harmonic distortion (THD) of i_{ac} was 6.5% with this condition. It should be mentioned that the low-order harmonics were almost not generated in the simulation.

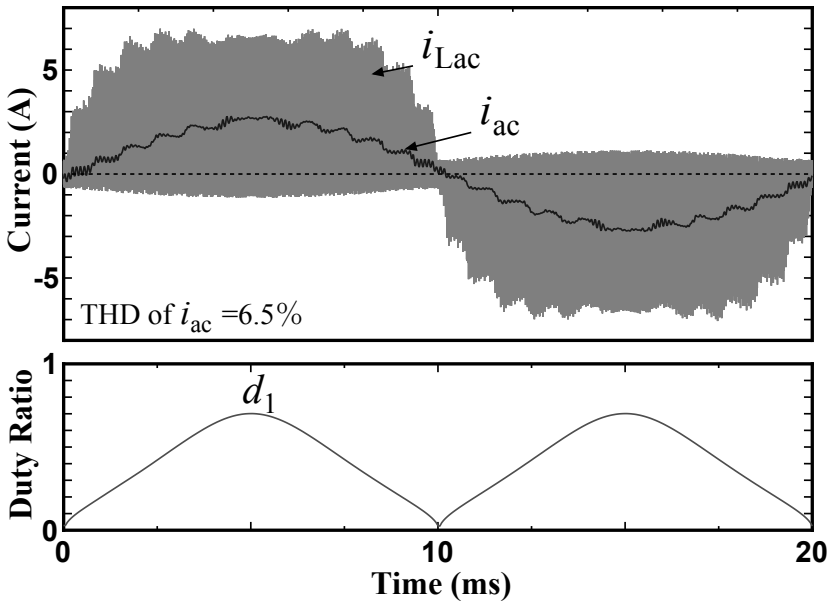

Fig. 4.10 Waveforms obtained by the time-domain simulation with the conventional DCM modulation and the rated current operation. The drain-source capacitance, C_{ds}, was set at 0.4 nF.

The time-domain simulations were also performed with the proposed modulation. The waveforms with four different values of C_{ds} were evaluated under the same value of f_{sw}. L_{ac} was optimized for each value of C_{ds} so that the ZVS and uniform turn-on is just achieved with $n = 0$ at the peak current phase of the rated current operation. Fig. 4.11, Fig. 4.12, Fig. 4.13 and Fig. 4.14 shows the resulting current waveforms and duty ratios with the proposed modulation and the rated current operations. Resultant of n for various current set-points including the rated current are also shown.

As can be seen from the figure, d_1, d_2 and d_3 became discontinuous forms. The discontinuous duty ratios clearly demonstrate how the proposed modulation concept works to compensate for the effect of the resonance. The distortions in i_{ac} were reduced in all the cases in comparison with that with the conventional modulation, and relatively clean sinusoidal waveforms were obtained. However, some distortions could still be observed in i_{ac} around peak current phase, particularly in Fig. 4.11 and Fig. 4.12. The reason is that the duty solutions with integer n were not found in those switching cycles due to the relatively large

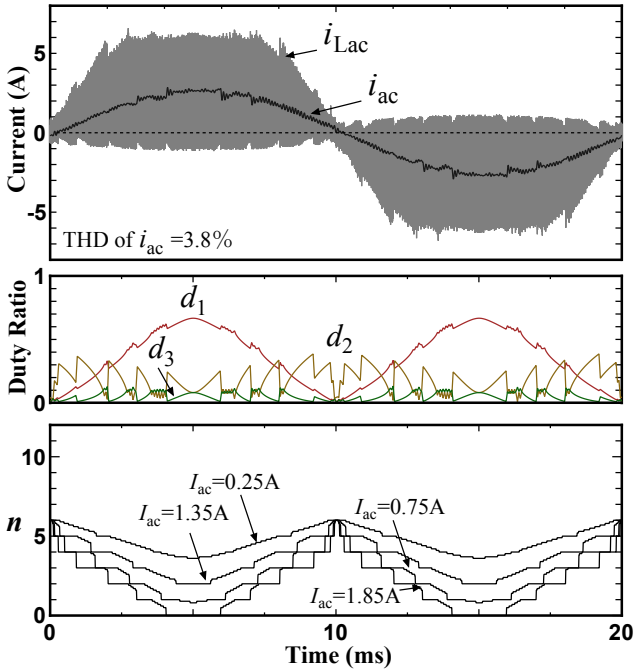

Fig. 4.11 Waveforms obtained by time-domain simulations with the proposed modulation, rated current operations, fixed switching frequency, and the circuit parameters of $C_{ds} = 0.4$ (nF) and $L_{ac} = 130$ (μH).

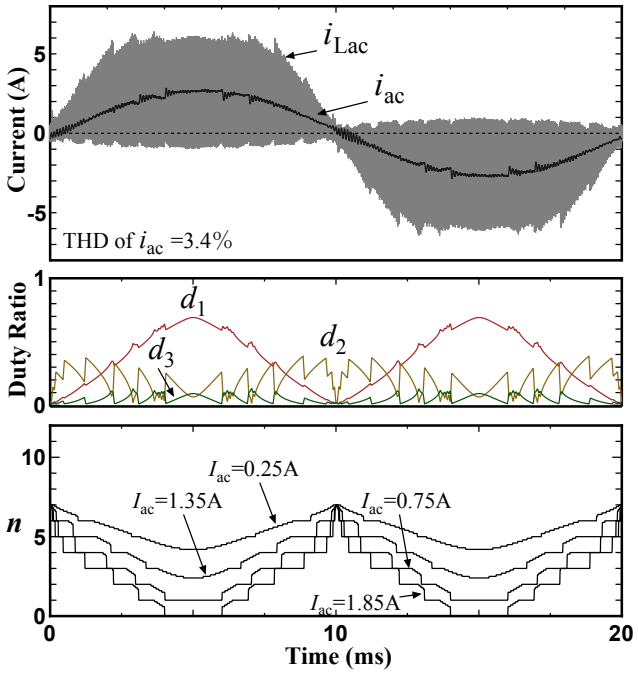

Fig. 4.12 Waveforms obtained by time-domain simulations with the proposed modulation, rated current operations, fixed switching frequency, and the circuit parameters of $C_{ds} = 0.3$ (nF) and $L_{ac} = 137$ (μH).

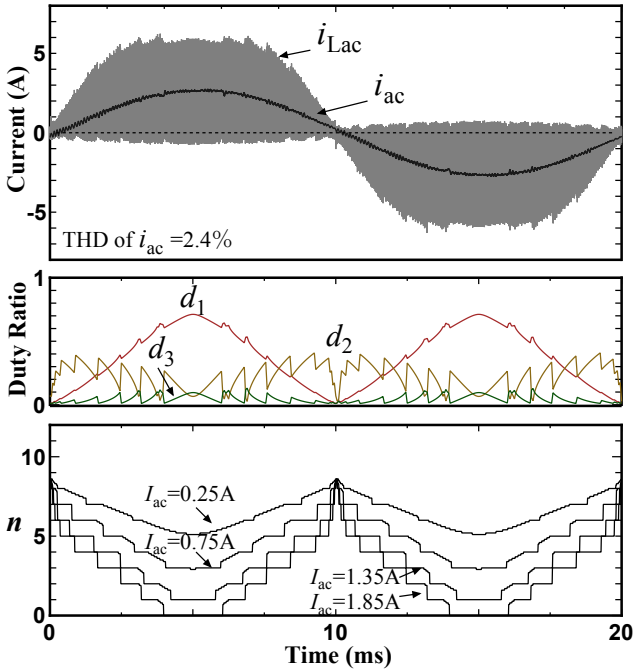

Fig. 4.13 Waveforms obtained by time-domain simulations with the proposed modulation, rated current operations, fixed switching frequency, and the circuit parameters of $C_{ds} = 0.2$ (nF) and $L_{ac} = 145$ (μH).

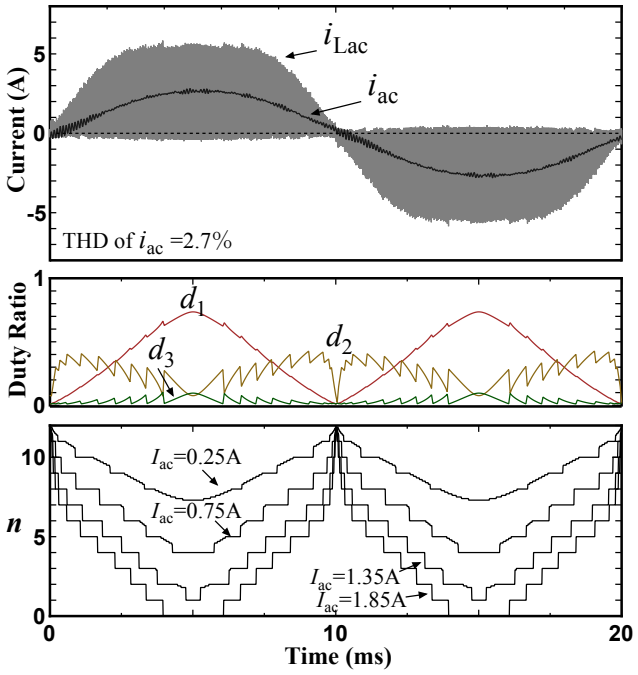

Fig. 4.14 Waveforms obtained by time-domain simulations with the proposed modulation, rated current operations, fixed switching frequency, and the circuit parameters of $C_{ds} = 0.1$ (nF) and $L_{ac} = 156$ (μH).

values for C_{ds}. The results indicate that the proposed modulation has a trade-off between the switching frequency, f_{sw}, and the drain source capacitance, C_{ds}; therefore, there is an upper limit of the switching frequency to achieve a certain level of the improvement by the proposed modulation for selected semiconductor devices.

It was also observed that the solutions for duty ratios with integer n could not be found in most of the switching cycles at light loads, especially when C_{ds} was relatively large. The results indicate that the proposed modulation can work well for high-order harmonic compensation at heavy loads; however, the performance can be reduced at light loads. It should be mentioned that the amplitude of the harmonic components generated at light loads are relatively low in comparison to the current rating.

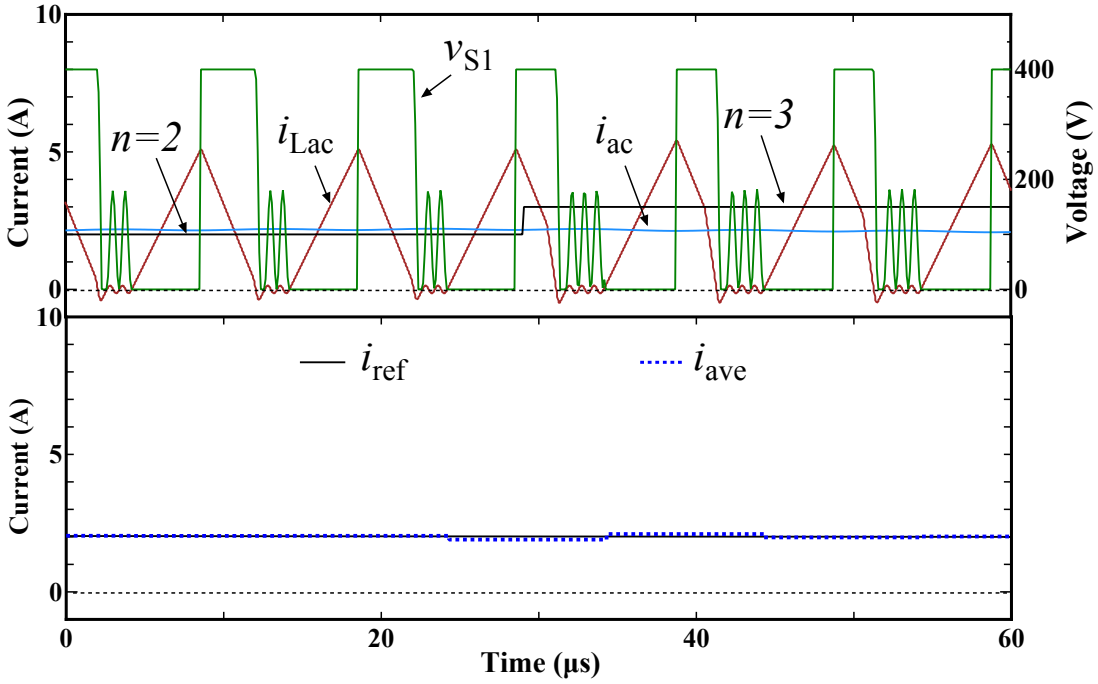

Fig. 4.15 Switching cycle waveforms around the current phase where n was changed from 2 to 3 with the proposed modulation. The drain-source capacitance, C_{ds}, was set at 0.1 nF.

Fig. 4.15 shows the simulation result of switching cycle waveforms around the current phase where n was changed from 2 to 3 with the proposed modulation. The trapezium inductor current, i_{Lac}, with different shapes can be observed before and after the changing

of n, as shown in the upper plot of Fig. 4.15. In addition, the number of oscillation cycles, which can be observed in v_{S1}, changes from 2 to 3 instantaneously. The average values of i_{Lac}, i_{ave}, are calculated in the simulation and shown in the bottom plot of Fig. 4.15. It shows that i_{ave} can be maintained at the value equal to the reference current, i_{ref}, well after the suddenly changing of the current shape. This result proves that the high control degree of freedom can be achieved by the TPCM as discussed in previous sections.

Calculations for Turn-off and Inductor R.M.S. Current

Fig. 4.16 shows a comparison of calculated turn-off currents of i_{Lac} for every switching cycles over half line cycle, rated current operation, with conventional and proposed modulation. The calculation is based on a certain specification that used in the experiment. The conditions and parameters are listed in Table 4.2. It is similar with the results presented in Chapter 3, the turn-off currents are reduced with TPCM being applied. Fig. 4.17 shows a comparison of average turn-off current for half line period. The average turn-off current of TPCM can be reduced by 37.2% in comparison with that of bipolar DCM. The reduction in average turn-off current of proposed modulation is less than that of modulation shown in Chapter 3, since it is not aiming at optimizing inductor peak currents. Nevertheless, the turn-off losses of proposed modulation can be reduced in comparison with that of conventional modulation.

Fig. 4.18 shows a comparison of calculated inductor r.m.s. currents of i_{Lac} for every switching cycles over half line cycle, rated current operation, with conventional and proposed modulation. Fig. 4.19 shows a comparison of inductor r.m.s. current for one line period. The proposed modulation can reduce the inductor r.m.s. current by 4.1% in comparison with the conventional modulation. This result indicates that the conduction losses can be reduced, however, the reduction of conduction losses can be relatively small in comparison with the reduction of turn-off losses.

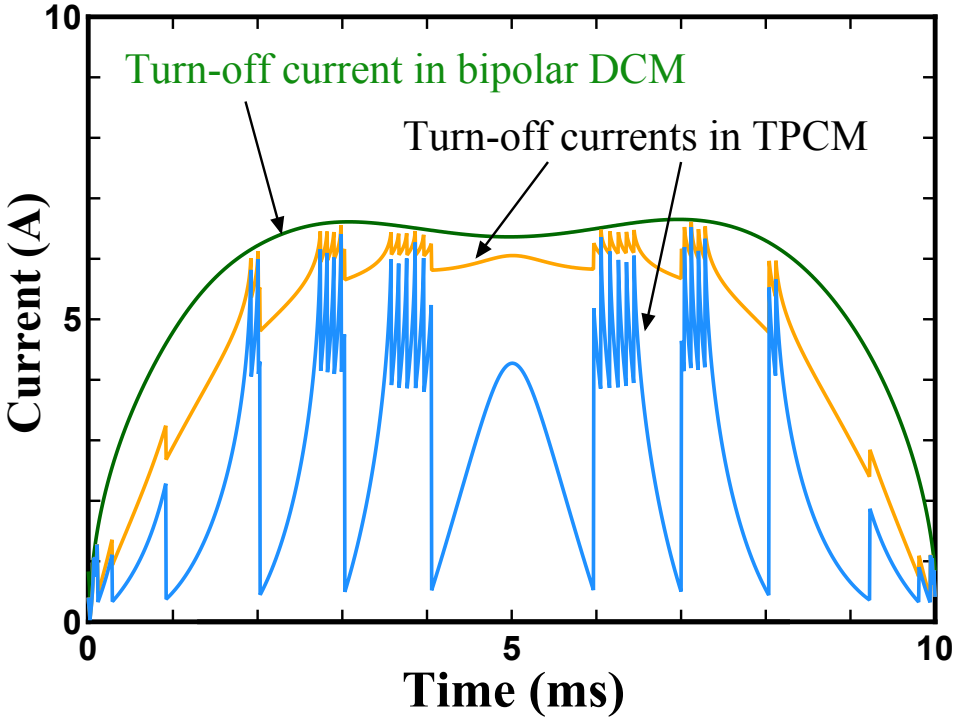

Fig. 4.16 Calculated turn-off currents for every switching cycles over half line period.

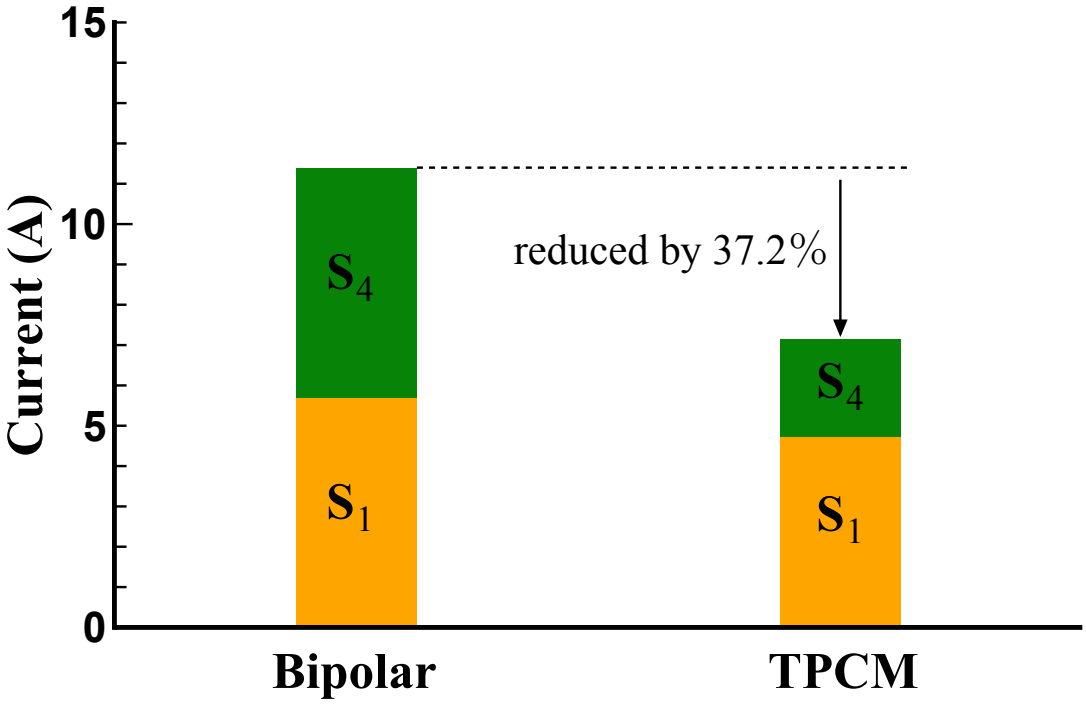

Fig. 4.17 Calculated average turn-off currents for one line period.

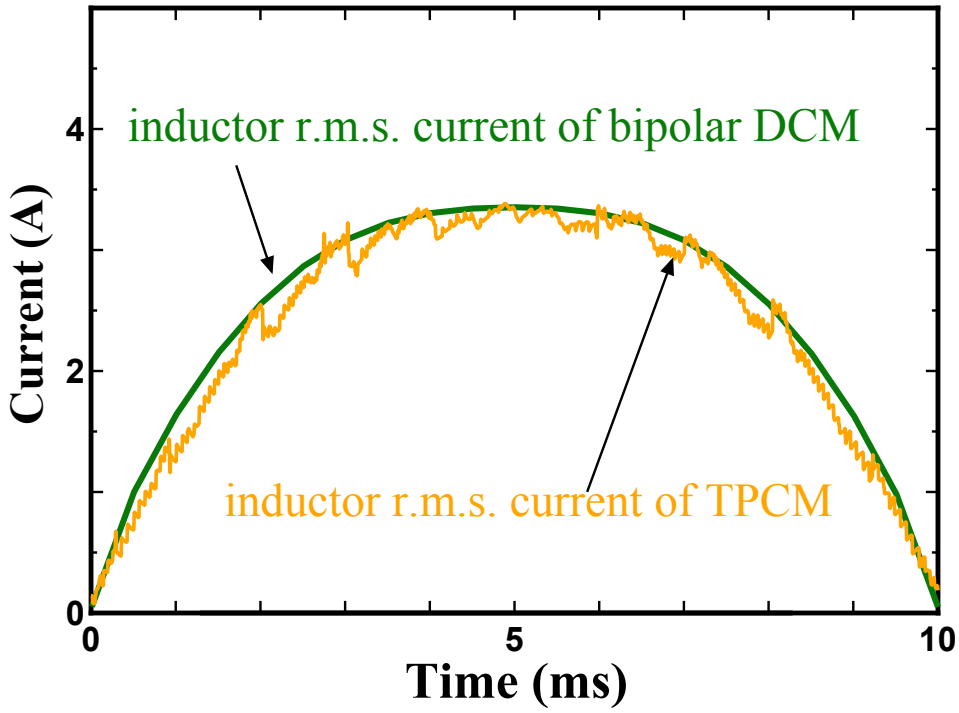

Fig. 4.18 Calculated inductor r.m.s. current for every switching cycles over half line period.

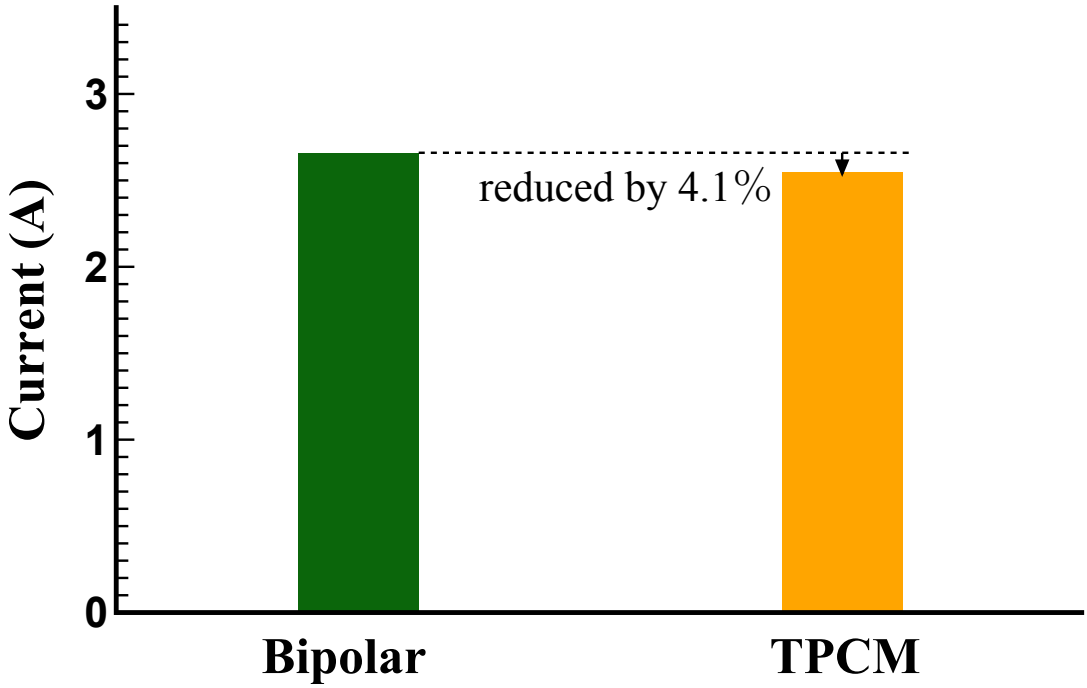

Fig. 4.19 Calculated inductor r.m.s. currents for one line period.

4.3.5 Experimental Verification with SiC-MOSFET

Experimental System and SiC-MOSFET Based Prototype

A laboratory prototype was fabricated to verify the proposed harmonic reduction strategies. The experimental system was the same as that shown in Chapter 3. The experimental conditions were the same as the in the simulation, as shown in Table 4.2. SiC-MOSFETs (SCT3030AL, 650 V, 70 A) that has a relative high current rating therefore parasitic capacitance were intentionally used in order to demonstrate the advantages of proposed modulation. C_{ds} was approximated to be 0.4 nF by a preliminary experiment and according to (4.25), and set for the duty calculations. The estimated C_{ds} was near to the value of the device output capacitance, C_{oss}, shown in the device data-sheet. However, it is not simple to determine the effective capacitance for the oscillation from the data-sheet since C_{oss} usually has a strong voltage dependency. The conventional DCM and proposed TPCM were implemented in the same prototype controlled by a digital signal processor (DSP). A periodic timer interrupt of 20 kHz was used to do all of the computations.

A digital phase locked loop (PLL) was used to generate the current reference, i_{ref} in phase with the line voltage. Current references with unity power factor were set for all the conditions. Two resonant controllers that being tuned at 150 Hz and 250 Hz were used to eliminate the third and fifth harmonics in the experiment.

Waveforms Demonstration and Analysis

Fig. 4.20 and Fig. 4.21 show the experimental waveforms of inverter-side inductor current, i_{Lac}, grid-side inductor current, i_{ac}, and the line voltage, v_{ac}, for rated current operation with conventional and proposed modulation, respectively. In Fig. 4.20, the current control was based on the feed-forward. In Fig. 4.21, the proposed partial feedback control with low-order harmonic compensation was applied to eliminate the low-order harmonics. It is similar to the simulation results, severe distortions can be observed in Fig. 4.20. The distortions was after

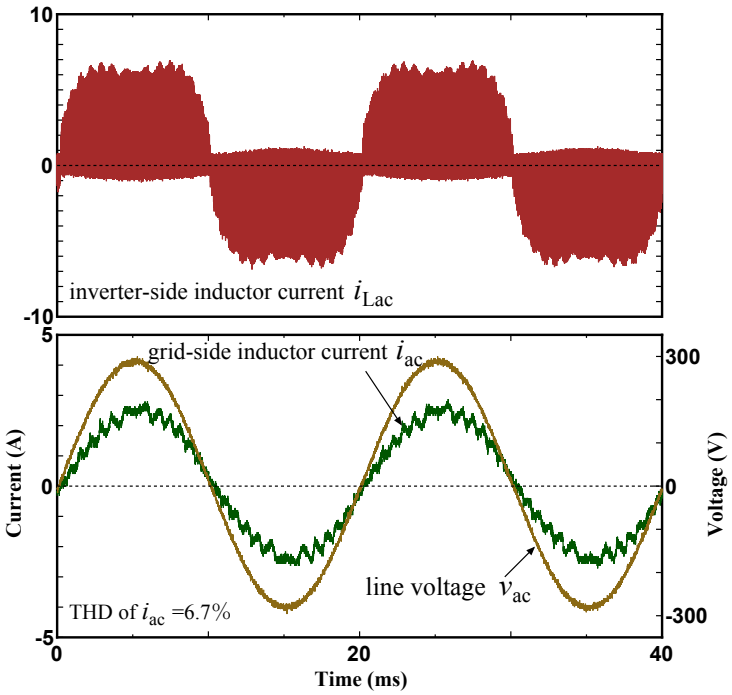

Fig. 4.20 Experimental waveforms of the inverter-side inductor current, i_{Lac}, grid-side inductor current, i_{ac}, and the line voltage, v_{ac}, with conventional modulation and without low-order harmonic compensation. The THD of i_{ac} is 6.7%.

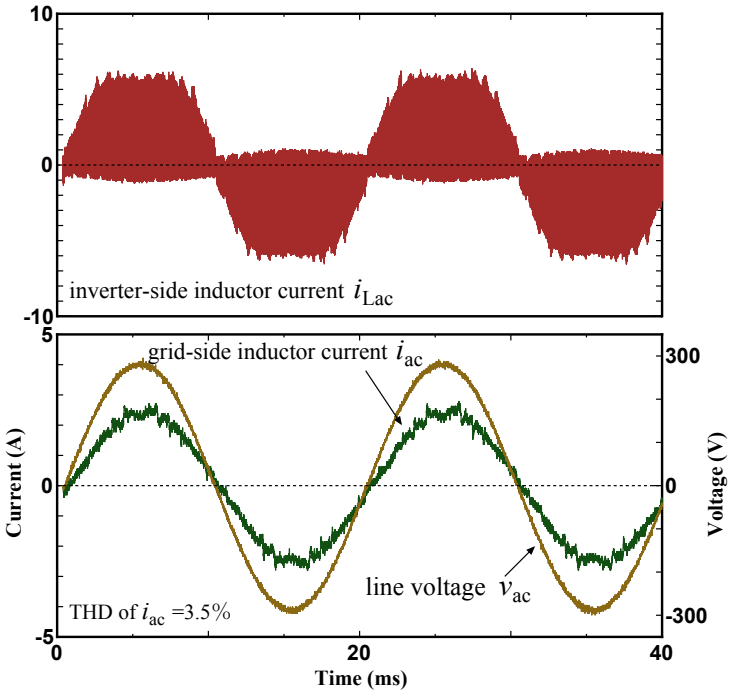

Fig. 4.21 Experimental waveforms of the inverter-side inductor current, i_{Lac}, grid-side inductor current, i_{ac}, and the line voltage, v_{ac}, with proposed modulation and with low-order harmonic compensation. The THD of i_{ac} is 3.5%

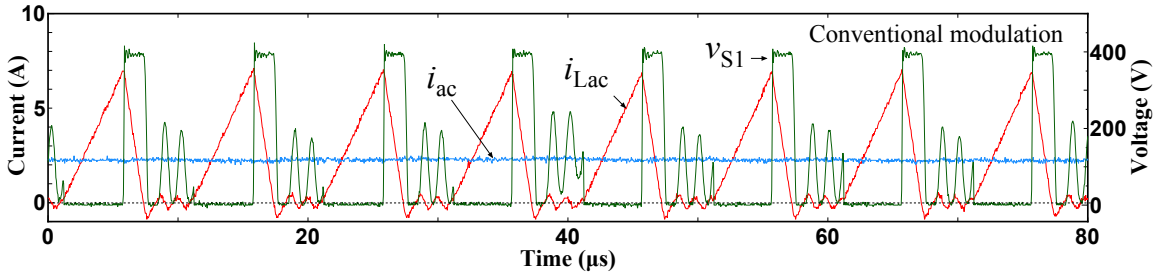

Fig. 4.22 Experimental waveforms of the inverter-side inductor current, i_{Lac}, grid-side inductor current, i_{ac} and the voltage across the device S_1, v_{S1}, in switching cycle view around $wt \approx 135^\circ$ with conventional modulation.

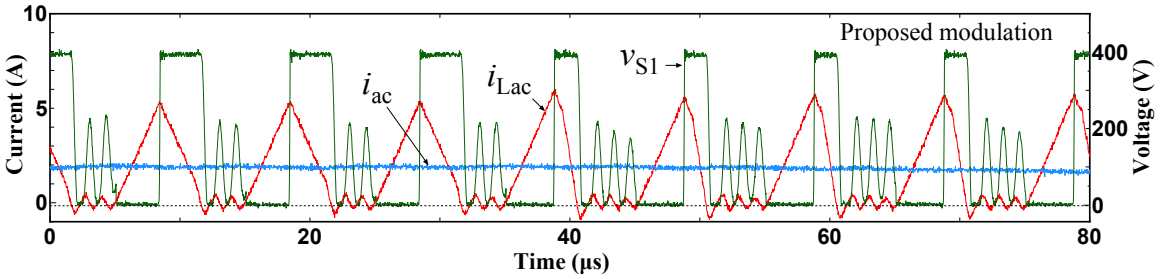

Fig. 4.23 Experimental waveforms of the inverter-side inductor current, i_{Lac}, grid-side inductor current, i_{ac} and the voltage across the device S_1, v_{S1}, in switching cycle view around $wt \approx 135^\circ$ with proposed modulation.

the proposed modulation was implemented to the converter. The THD of i_{ac} was reduced from 6.7% to 3.5% after the proposed modulation and low-order harmonic compensation were applied.

Fig. 4.22 and Fig. 4.23 shows the waveforms in switching cycle view with conventional DCM and proposed TPCM, respectively. Oscillating v_{S1} could be observed in both modulations. However, v_{S1} did not always oscillate to zero or valley at the next turn-on instant with the conventional modulation as can be seen from Fig. 4.22. Consequently, the initial inductor currents were non-uniform.

On the other hand, Fig. 4.23 shows the waveforms with the proposed modulation around the current phase where n was changed from 2 to 3. It was observed that the number of oscillation cycles changed from 2 to 3 instantaneously while the average current was maintained before and after this changing, as same as for the simulation result shown in

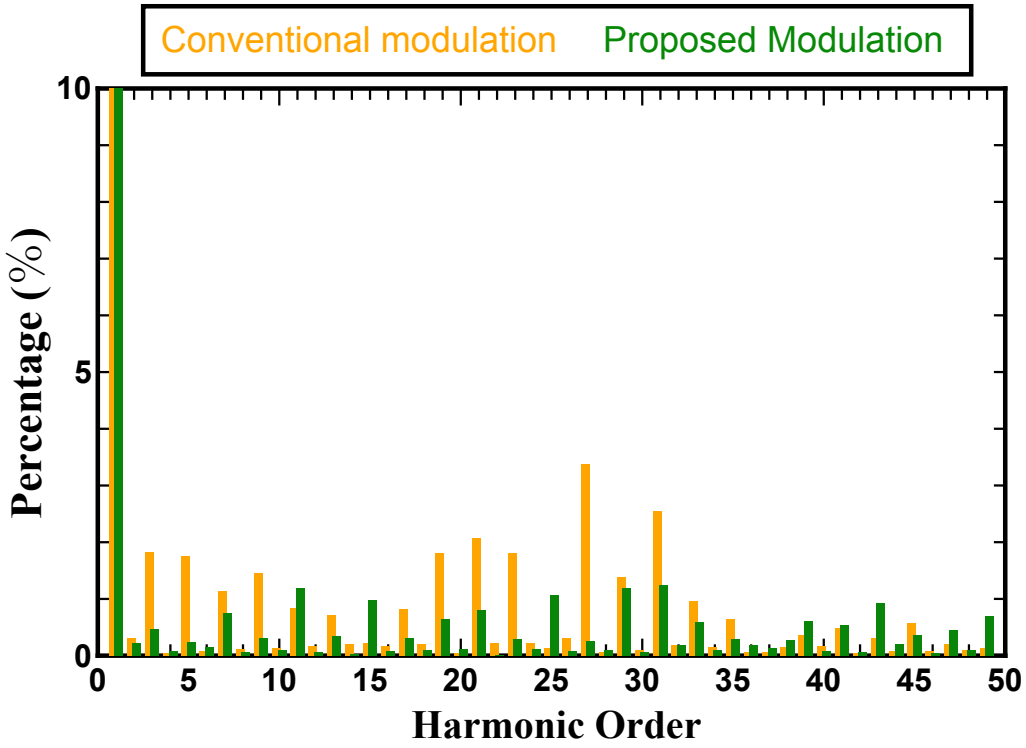

Fig. 4.24 Harmonic components in i_{ac} at the rated current operation.

Section 4.3.4. Consequently, v_{S1} always oscillated to almost zero and the initial inductor currents could be uniform. However, the voltage at the turn-on instant was not always be complete zero. The reason for that can be considered to be existing resistive components in the oscillation current path.

Harmonic Analysis

The harmonic components in i_{ac} with the rated current operations were calculated by means of discrete Fourier transform (DFT), and the results are shown in Fig. 4.24. The high-order harmonics, such as twenty-seventh and thirty-first harmonic components, were found in the conventional modulation and they were reduced after the proposed modulation was applied. At the same time, the high third and fifth harmonic components were also reduced after the low-order harmonic compensation was applied.

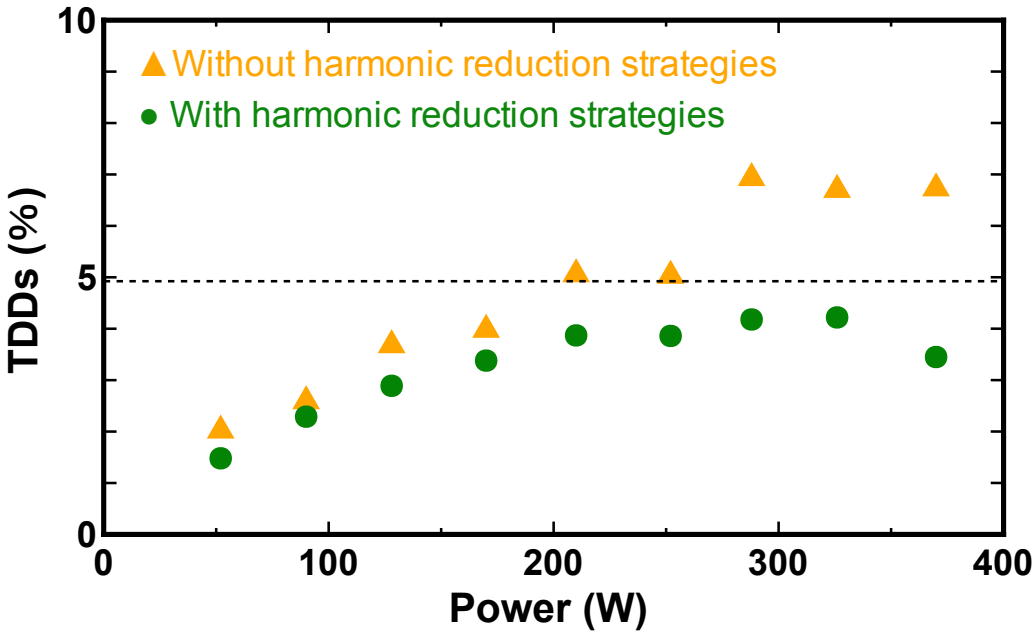

Fig. 4.25 Calculated total harmonic distortions (TDDs) as function of the output power.

The total demand distortions (TDDs) of i_{ac} under different power levels based on the rated current were calculated and the results are shown in Fig. 4.25. The TDD represents the harmonic current distortion in percentage of the maximum demand load current. The definition of TDD is expressed as

$$TDD(h) = \frac{\sqrt{\sum_{h=2}^{49} I_h^2}}{I_{max}}, \tag{4.26}$$

where h denotes the order of harmonic, I_h denotes the harmonic current of h th order in r.m.s., I_{max} denotes the fundamental component of maximum demand current. The calculated results show that the conventional DCM modulation controlled with feed-forward only could not achieve 5% at heavy loads due to the severe current distortions under this experimental condition. On the other hand, the TDDs of i_{ac} were well below 5% over the entire range of the power-level after the proposed strategies of harmonic reduction were applied.

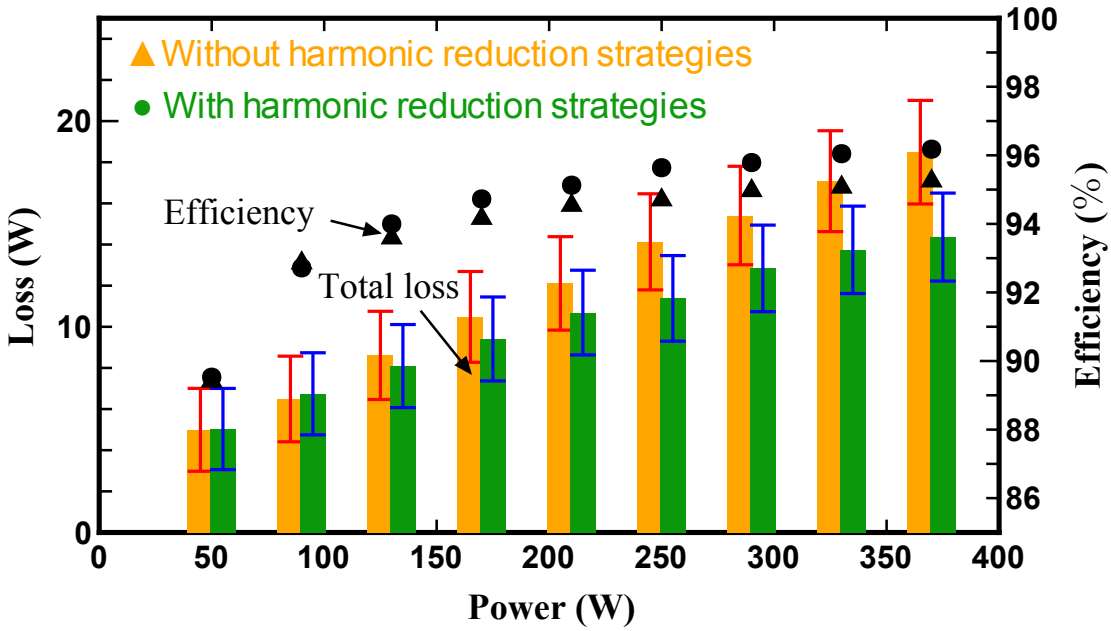

Fig. 4.26 Measured efficiencies and total losses as function of the output power.

Efficiency Analysis

The measured efficiencies and total losses are shown in Fig. 4.26. The measurement was conducted by using a digital power meter (YOKOGAWA WT-1800). The range of measurement for DC input was 600 V/2 A and 300 V/5 A for AC side. The maximum errors of reading and measurement were calculated based on this condition, and the error bars are added.

The efficiencies at heavy loads were improved after the proposed harmonic reduction strategies were applied. Negligible improvements on the total losses reduction can be obtained even the error bars are taken into consideration.

Fig. 4.27 shows the peak values of i_{Lac} with the rated current operations over half line period, which were obtained by processing the measured waveforms. It was similar with the calculated results, the proposed modulation (with harmonic reduction strategies) reduced inductor peak current in comparison with the conventional modulation (without harmonic reduction strategies).

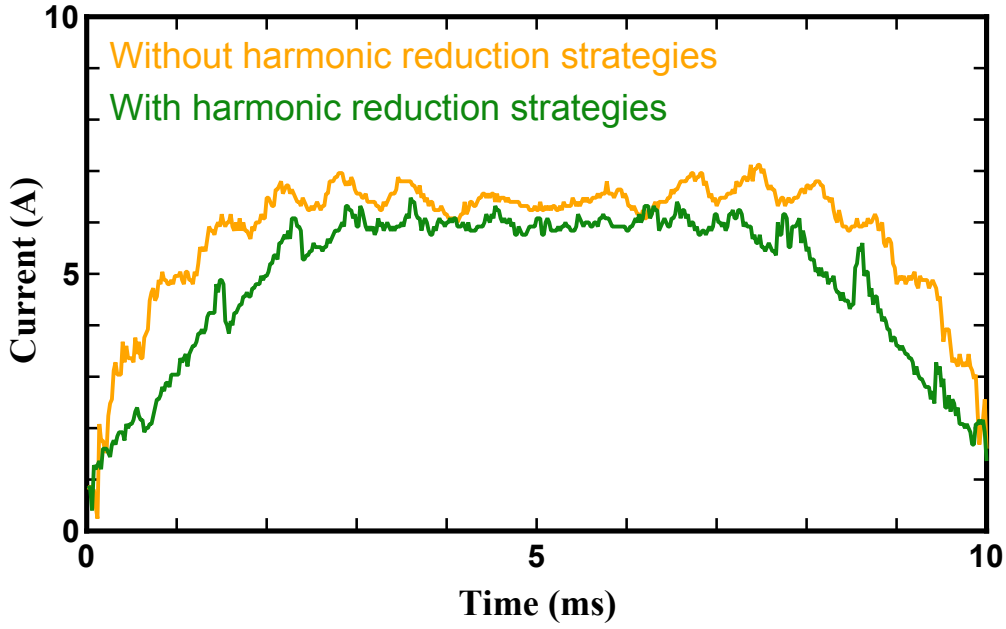

Fig. 4.27 Measured peak values of inverter-side inductor current, i_{Lac}, after low-order harmonic compensation was applied. The peak currents were obtained from measured waveforms with 1 MS/s of acquisition rate.

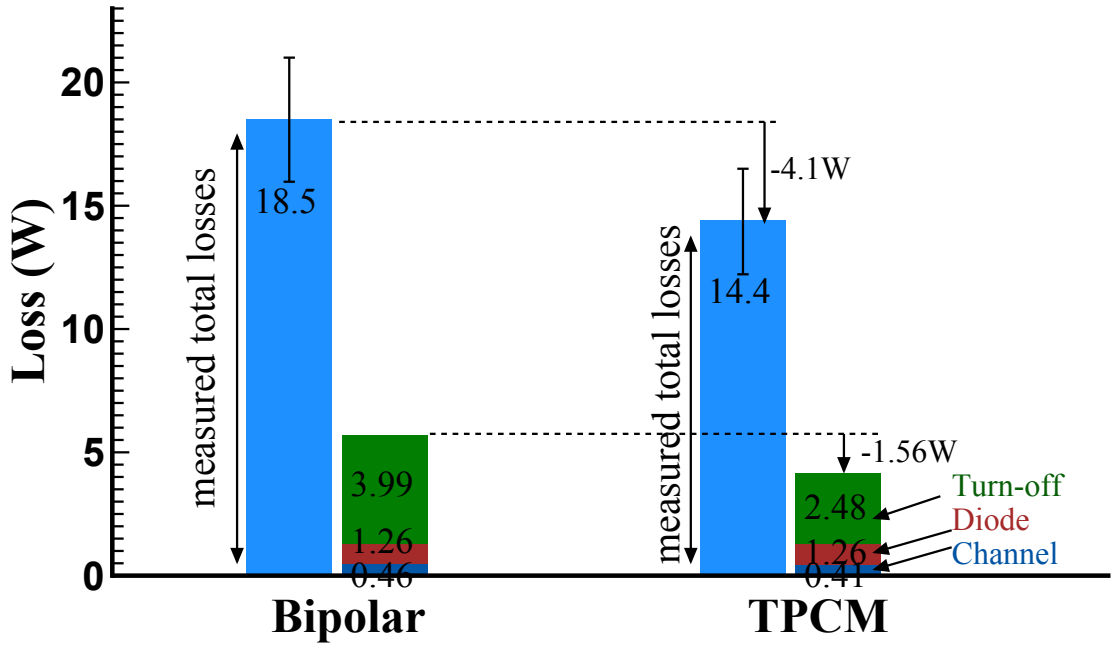

Fig. 4.28 An estimation of loss break-down for conventional and proposed modulations when $I_{\mathrm{ac.set}} = 1.85$ A.

An estimation of loss break-down was conducted for the rated operation and the result is shown in Fig. 4.28. The unknown losses increased in comparison the results shown in Chapter 3, though the conduction losses were significantly reduced. This could be caused by the large parasitic capacitance of semiconductor device, and that resulted in higher turn-on losses. The turn-off losses were reduced with the proposed modulation being applied, as explained in the previous section. The reduction in turn-off losses can be one of the main reasons for the total loss reduction. The proposed modulation can achieve ZVS for turn-on, therefore, the turn-on losses can be reduced. This can also be a reason for the total loss reduction. In addition, the inductor losses can be reduced in the proposed modulation, since the inductor peak current is reduced. However, it is difficult to discuss the unknown losses further when the error bar is taken into consideration.

4.3.6 Experimental Verification with GaN-HEMT

Experimental System and GaN-HEMT Based Prototype

In order to reduce the volume of LCL filter further, the DCM grid-tied inverter is designed to operate at MHz with GaN-HEMT devices being applied. Overview of the laboratory H-bridge prototype is shown in Fig. 4.29. A GaN-HEMT device (GS66504B, 650 V, 15 A) was selected as the switching device, and two half-bridge evaluation boards, which include two GaN-HEMT devices and two gate drivers, were used to form an H-bridge topology. The drain-source capacitance of the GaN-HEMT device was estimated to be 0.1 nF.

The resulting percentage impedance of L_{ac} and L_{f} for the design with $f_{\mathrm{sw}} = 1$ MHz are about 0.0023% and 0.0047%, respectively. The total percentage impedance is drastically reduced in comparison with that of the conventional CCM design, which is generally 2%–5% of the base impedance. Some inductors that are impractical for conventional designs, such as air-core based inductor or chip inductor, can be used due to the extremely low inductance. In [3], a toroidal air-core with Litz wire was considered in order to avoid possible high

Fig. 4.29 Overview of H-bridge prototype with two evaluation boards from GaN Systems.

core loss and to mitigate the skin effect caused by the high frequency discontinuous current for the design of inductors. However, the winging loss, which include skin and proximity effects, can increase since more turns are necessary for an air-core based inductor. In this experiment, the commercial chip inductors (Panasonic: ETQ-P5M2R5YFK, 2.5 μH, 14 A) were applied to form a compact LCL filter, as a new attempt. Fig. 4.30 shows the overview of the LCL filter that used in this prototype. From the point of view of the efficiency improvement, two inductors connected in parallel were used at both lines as the inverter-side inductors to derate the inductor current and avoid too much temperature rising. On the other hand, each inductor on the grid side consisted of one inductor since the current in the grid-side inductor is continuous and sinusoidal with small current ripples. An experiment of operation verification with the MHz operated DCM grid-tied inverter is also conducted. The experimental conditions and circuit parameters are listed in Table 4.3. The experimental

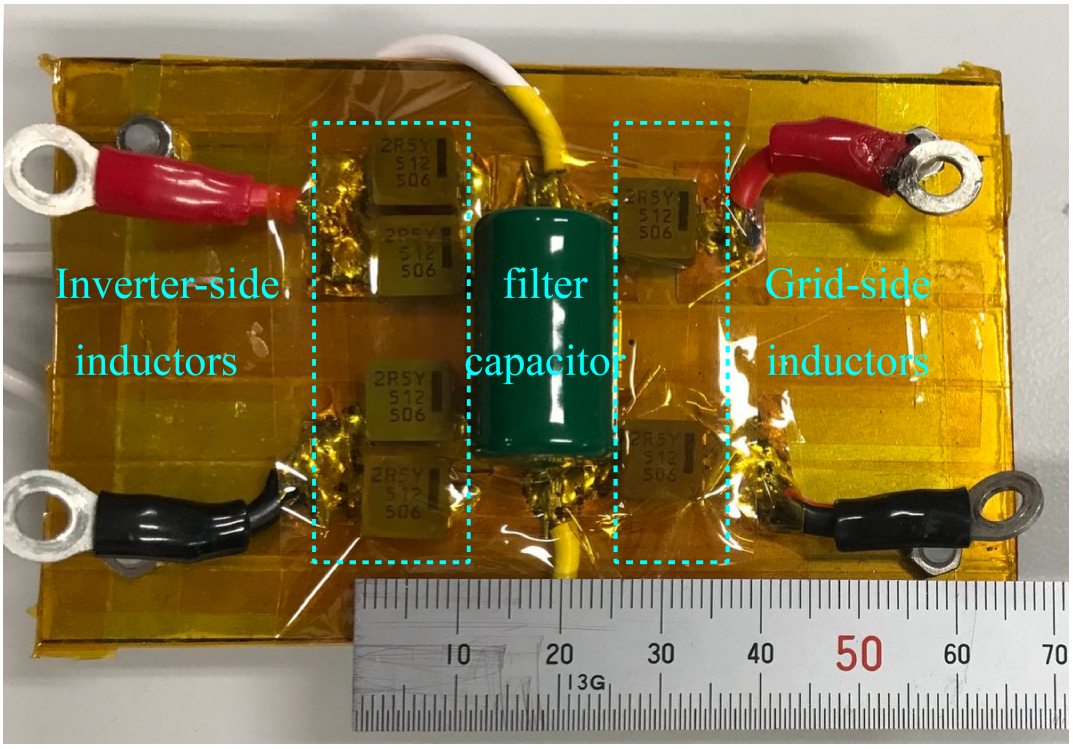

Fig. 4.30 Overview of LCL filter in which commercial chip inductors are applied.

Table 4.3 Parameters and Conditions

Experimental Conditions for GaN-Based Prototype		
DC voltage	V_{dc}	180 V
AC voltage	V_{ac}	100 V
Line frequency	f_{grid}	50 Hz
Rated current	$I_{ac.rated}$	2.25 A
Switching frequency	f_{sw}	1 MHz
Drain-source capacitance	C_{ds}	0.1 nF
Resolution factor	Δn_x	0.1
Minimum value of d_3	$d_{3.min}$	0.01

LCL Filter Design Parameters for GaN-Based Prototype		
Inverter-side inductance	L_{ac}	2.5 μH
Percentage impedance of L_{ac}	$\%X_{Lac}$	0.0023%
Grid-side inductance	L_f	5 μH
Percentage impedance of L_f	$\%X_{Lf}$	0.0047%
Filter capacitance	C_f	0.39 μF

system of the single-phase grid-tied inverter is the same with that shown in Chapter 3. The conventional and proposed control strategy were implemented in the same prototype that being controlled by a DSP controller.

Waveforms Demonstration and Analysis

The experimental waveforms of the conventional DCM and proposed TPCM are shown in Fig. 4.31 and Fig. 4.32, respectively. In Fig. 4.31, the low-order harmonic compensation was not applied so that the converter was controlled with feed-forward only. In Fig. 4.32, the partial feedback control with low-order harmonic compensation was applied. Some distortions could still be observed in i_{ac} around peak current phase. This was caused by the trade-off relationship discussed in Section 4.3.4. The THD of i_{ac} was reduced from 7.3% to 4.5% under maximum current operation after the proposed control strategy was implemented to the converter. The results also demonstrate that the current can be controlled well without any difficulties even under extremely low inductance condition under the model-based control strategy.

Harmonic Analysis

The harmonic components in i_{ac} and calculated total demand distortions (TDDs) based on the maximum current operation are shown in Fig. 4.33 and Fig. 4.34, respectively. The third and fifth order harmonic components were effectively reduced after the low-order compensation method was applied. The high-order harmonics, such as the 25th, the 27th and the 29th, were not effectively reduced. The reason was that integer n was not found during those switching cycles closed to the peak current phase, and uniform turn-on was not achieved, as it was discussed in Section 4.3.4. As a results, the current distortion was obtained, as it can be observed in Fig. 4.32. Nonetheless, the TDDs were below 5% over the entire load ranges after the proposed harmonic reduction strategies were applied.

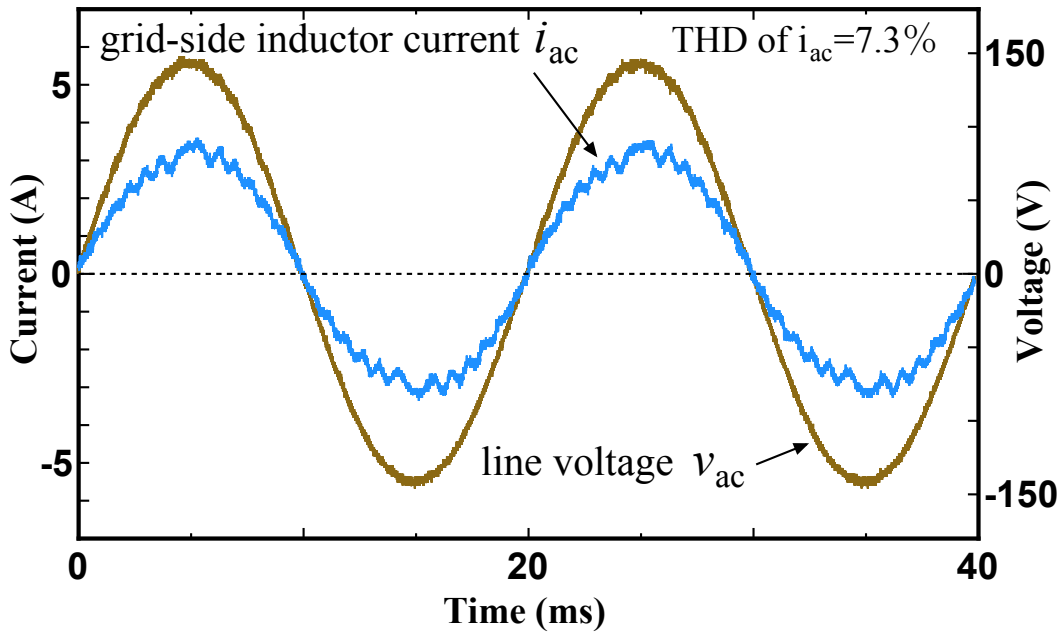

Fig. 4.31 Experimental waveforms of the grid-side inductor current, i_{ac}, and line voltage, v_{ac}, under the maximum current operation, with conventional DCM and without low-order harmonic compensation.

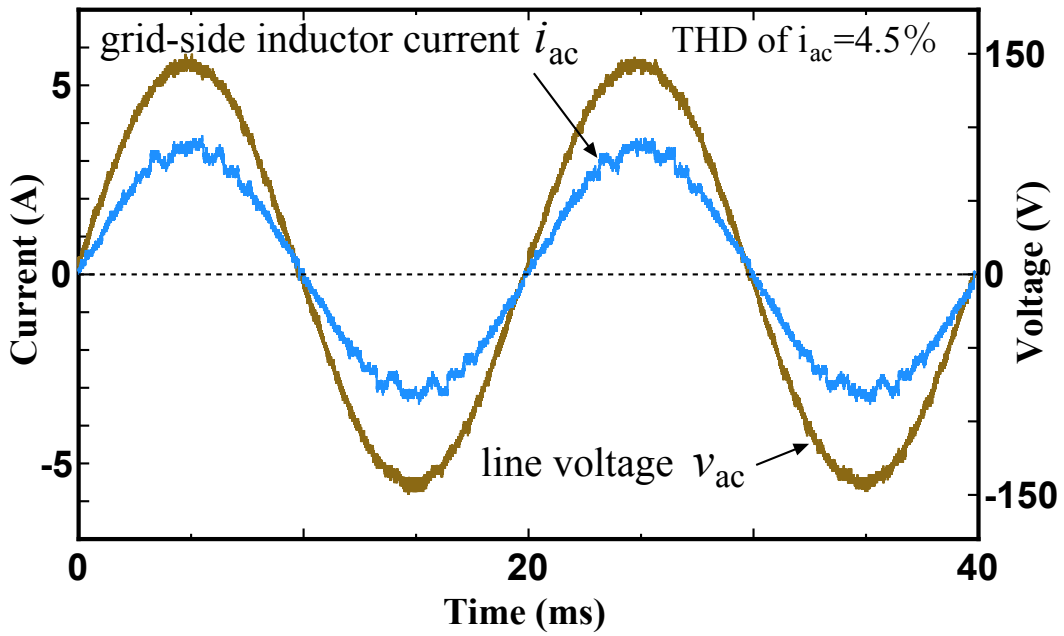

Fig. 4.32 Experimental waveforms of the grid-side inductor current, i_{ac}, and line voltage, v_{ac}, under the maximum current operation, with proposed TPCM and with low-order harmonic compensation.

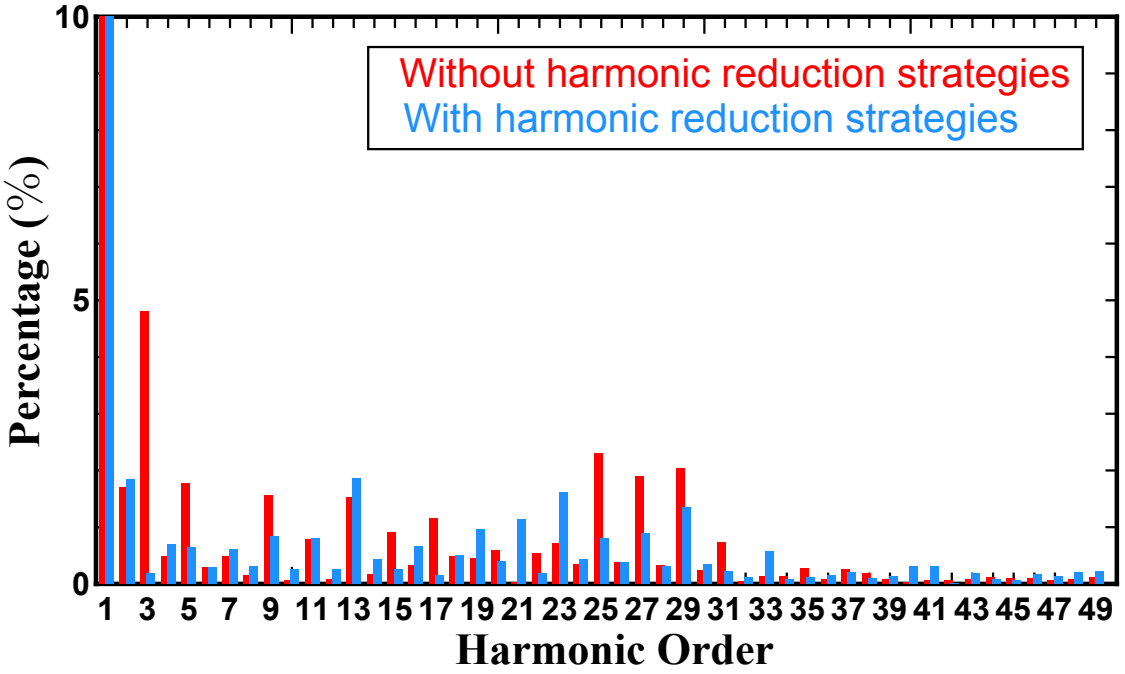

Fig. 4.33 Harmonic components comparison in the case of maximum current operation.

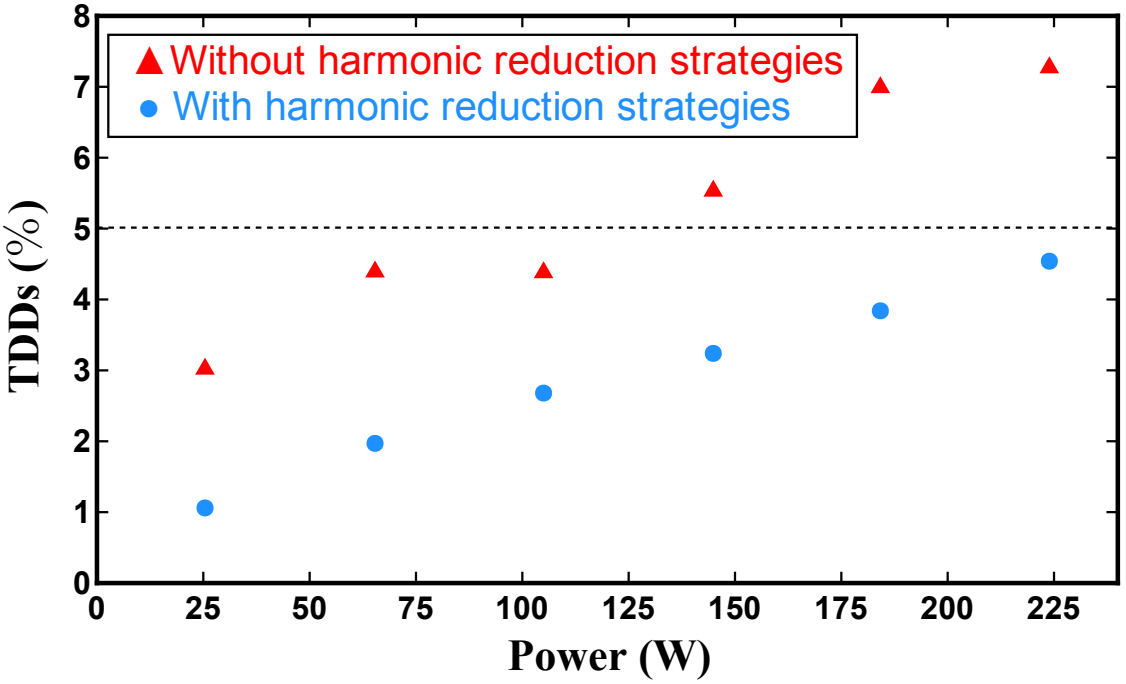

Fig. 4.34 Calculated TDDs under different power levels.

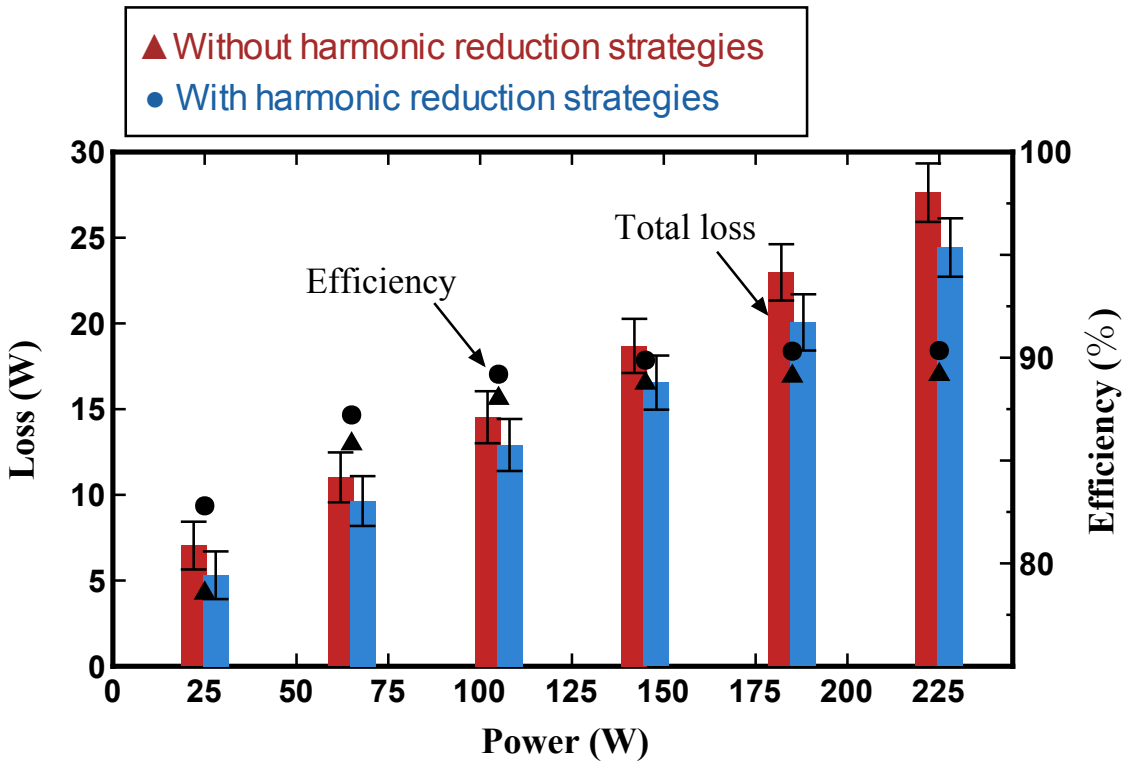

Fig. 4.35 Measured efficiencies and total losses against output power.

The obtained results of a GaN-HEMT based grid-tied inverter are similar with that of a SiC-MOSFETs based grid-tied inverter. In the case of the DCM controlled with feed-forward only, the power quality cannot meet the grid requirements under heavy loads. The switching frequency has to be reduced to at least half of the present one in order to obtain similar performance of TDDs under this experimental conditions. Consequently, the proposed modulation allows further high frequency operation of a DCM grid-tied inverter therefore further volume reduction of inductors.

Efficiency Analysis

The conversion efficiencies and total losses shown in Fig. 4.35 were measured in the experiment. The measurement was conducted by using a digital power meter (YOKOGAWA WT-1800). The range of measurement for DC input was 300 V/2 A and 300 V/5 A for AC side. The maximum errors of reading and measurement were calculated based on this

condition, and the error bars are added. In the case of maximum current operation, the efficiencies without and with the proposed harmonic reduction strategy were 89.2% and 90.4%, respectively. The overall efficiencies were improved with the proposed modulation. One possible reason of this improvement could be caused by the reduced peak currents and turn-off losses in the TPCM. In the case of conventional DCM modulation, the conversion efficiencies of the prototype with chip inductors were almost the same with that with air-core inductors, which was shown in reference [3]. The conduction and reverse conduction loss of the GaN-HEMT devices, and the switching losses were considered to be similar. Although the inner structure of the applied chip inductor was unknown, the winding losses of the air-core shown in [3] were considered to be higher than that of the chip inductors, since more turns were used. Consequently, the core losses of the chip inductors can be a problem.

4.4 Proposed Modulation Based on Variable Frequency

4.4.1 Concept of the Proposed Method

The high-order distortions can be eliminated by achieving an uniform-turn-on behavior for the switches, which means the values of initial current at turn-on being the same. A modulation method that based on the conventional bipolar DCM is proposed to achieve this purpose. The possible current path during one switching cycle operation of the bipolar DCM is shown in Fig. 4.36, where the resonance process has been taken into consideration. The operation principles for the positive gird voltage are briefly described as follows:

Interval 1:

At the beginning of interval 1, S_1, S_4 are turned on simultaneously while S_2, S_3 are kept off. The inverter-side inductor current, i_{Lac}, increases linearly. The interval 1 ends when S_1, S_4 are turned off.

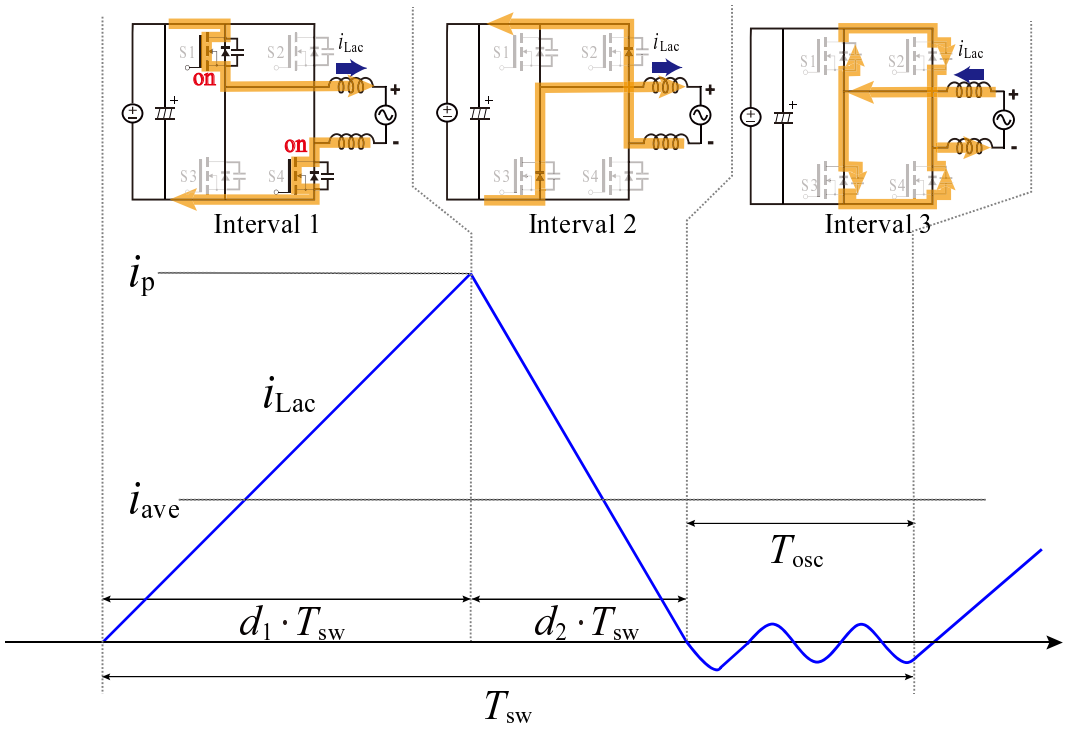

Fig. 4.36 Possible current paths of one switching cycle operation in DCM for positive grid voltage V_{ac}.

Interval 2:

After S_1, S_4 are turned off simultaneously, i_{Lac} decreases through the body diodes of S_2 and S_3. The synchronous rectification can be achieved by turning on S_2 and S_3 during this interval. The interval 2 ends when i_{Lac} reduces to zero current.

Interval 3:

After i_{Lac} reaches at zero, parasitic capacitance of S_1 and S_3 forms a resonant circuit with L_{ac}. The inductor current, i_{Lac}, oscillates around zero and charges and discharges the parasitic capacitance. As a result, the voltages across the switches, v_{S1} and v_{S3}, oscillate during this interval. Parasitic capacitance of S_2 and S_4 also forms a resonant circuit with L_{ac}, and the switch voltages of S_2 and S_4 oscillate as well as v_{S1} and v_{S3}. The interval 3 ends when S_1 and S_4 are turned on again.

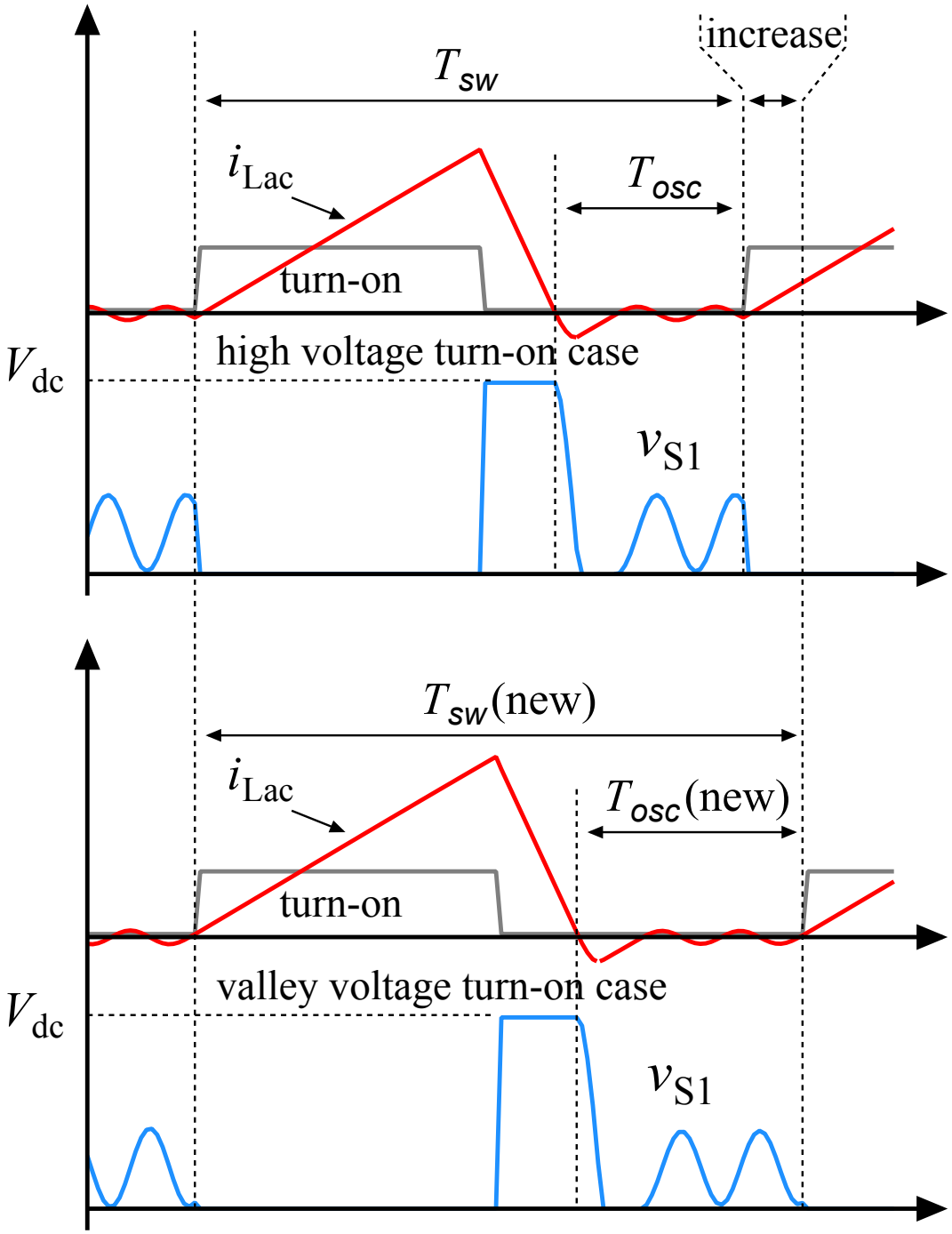

Fig. 4.37 Schematic waveforms with the conventional (top) and proposed modulations (bottom). The switching cycle is extended to achieve the switch voltage, v_{sw}, to be zero at the end of the switching cycle.

The uniform turn-on can be achieved if the inverter-side inductor current, i_{Lac}, always resonates to the same value at the next turn-on instant. To achieve this for any current reference, the length of the switching cycle, T_{sw}, should also be controlled to make i_{Lac} be a constant value at the end of the cycle. for instant, zero as depicted in Fig. 4.37. To make i_{Lac} be zero also achieves v_{S1} being zero at the next turn-on instant, that can be advantageous as known as zero-voltage switching (ZVS). The new switching cycle, T_{sw}, should satisfy the following conditions:

- The average current of i_{Lac} during T_{sw}, i_{ave}, is equal to the given reference current, i_{ref}. i_{Lac} and v_{S1} becomes zero at the end of T_{sw}.

The duty ratios should also be calculated based on this new T_{sw}. It is impractical to realize this kind of control in error-based feedback controls. However, it can be achieved under the calculation-based feed-forward controls with the model considering the oscillation.

4.4.2 Model Derivation for Duty Calculation

Fig. 4.38 shows the key waveform of one switching cycle operation in the DCM. During interval 1, the peak value of i_{Lac}, i_{p}, at t_2 can be calculated as

$$i_{\mathrm{p}} = \frac{V_{\mathrm{dc}} - v_{\mathrm{ac}}}{L_{\mathrm{ac}}} T_{\mathrm{on}}, \tag{4.27}$$

where V_{dc} denotes the DC link voltage, v_{ac} denotes the instantaneous line voltage and being assumed constant in one switching cycle, T_{on} is the turn-on time for the switches and the duration of interval 1, and L_{ac} is the inductance of the inverter-side inductor. According to the voltage-second balance, the relation between diode conduction time, T_{sr}, which is equal to the duration of interval 2, and i_{p} is expressed as

$$-i_{\mathrm{p}} = \frac{-V_{\mathrm{dc}} - v_{\mathrm{ac}}}{L_{\mathrm{ac}}} T_{\mathrm{sr}}. \tag{4.28}$$

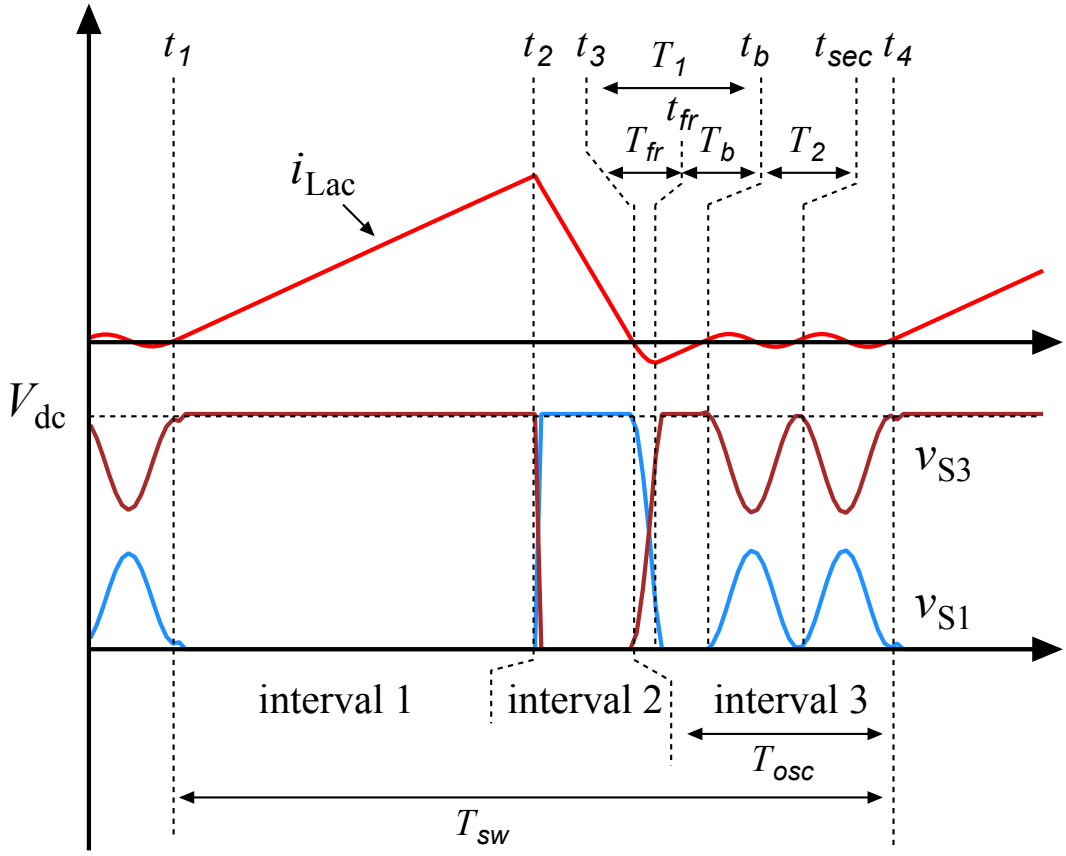

Fig. 4.38 Schematic waveforms during one switching cycle for positive grid voltage in DCM.

By neglecting the small current caused by the resonance during interval 3 and assuming a pure triangular inductor current, the average inductor current during one switching cycle, i_{ave}, can be calculated as

$$i_{\text{ave}} = \frac{S}{T_{\text{sw}}} = \frac{1/2 \cdot i_{\text{p}}(T_{\text{on}} + T_{\text{sr}})}{T_{\text{on}} + T_{\text{sr}} + T_{\text{osc}}} = \frac{1/2 \cdot i_{\text{p}} T_{\text{on}} \dfrac{2V_{\text{dc}}}{V_{\text{dc}} + v_{\text{ac}}}}{T_{\text{on}} \dfrac{2V_{\text{dc}}}{V_{\text{dc}} + v_{\text{ac}}} + T_{\text{osc}}}, \tag{4.29}$$

where S is the area of i_{Lac} in one switching cycle, and i_{Lac} should be equal to i_{ref}. The relation between i_{p} and T_{osc} can be derived by substituting (4.27) to (4.29), which is

$$i_{\text{p}} = i_{\text{ref}} + \sqrt{{i_{\text{ref}}}^2 + \frac{T_{\text{osc}} i_{\text{ref}} ({V_{\text{dc}}}^2 - {v_{\text{ac}}}^2)}{V_{\text{dc}} L_{\text{ac}}}}. \tag{4.30}$$

Then, T_{on} and T_{sr} can be calculated from (4.27), (4.28), and (4.30) as

$$T_{on} = \frac{L_{ac} i_p}{V_{dc} - v_{ac}}, \tag{4.31}$$

$$T_{sr} = \frac{L_{ac} i_p}{V_{dc} + v_{ac}}. \tag{4.32}$$

The switching period, T_{sw}, can be calculated as

$$T_{sw} = T_{on} + T_{sr} + T_{osc} = \frac{2V_{dc} L_{ac} i_p}{{V_{dc}}^2 - {v_{ac}}^2} + T_{osc}. \tag{4.33}$$

It can be observed from (4.31), (4.32), and (4.33) that T_{osc} is the sole variable that can be freely set to determine the duty ratios and the switching cycle to achieve $i_{ave} = i_{ref}$, while the other variables are dependent on the operating conditions. The switching frequency, f_{sw}, can naturally be expressed as

$$f_{sw} = 1/T_{sw}. \tag{4.34}$$

It is similar to the conventional modulation for DCM [4, 3], i_{ave} is controlled directly by duty ratios. The turn-on duty, d_{on}, that is equal to the length of interval 1, can be calculated as

$$d_{on} = \frac{T_{on}}{T_{sw}} = T_{on} f_{sw}. \tag{4.35}$$

The duty for diode conduction, d_{sr}, that is equal to the length of interval 2, can be calculated as

$$d_{sr} = \frac{T_{sr}}{T_{sw}} = T_{sr} f_{sw}. \tag{4.36}$$

d_{on} and d_{sr} can be calculated after determining T_{osc}. d_{sr} can be used to achieve the so-called synchronous rectification.

4.4.3 Model of Resonance During Interval 3

During T_{osc}, there are two types of resonance. The first resonance is referred to as T_1, and one period of the second resonance is referred to as T_2, as shown in Fig. 4.38. T_{osc} can be expressed as

$$T_{\text{osc}} = T_1 + n \times T_2, \tag{4.37}$$

where n is the total number of T_2. The use of integer values of n can always achieve zero current switching therefore the same initial current; eventually the realization of ZVS at the next turn-on instant.

During T_1, the switch voltage, v_{S1} and v_{S4}, resonate to zero first. By assuming that i_{Lac} is zero at t_3, v_{S1} and v_{S4} can be expressed during the resonance as

$$v_{\text{S1}}(t) = v_{\text{S4}}(t) = \frac{1}{2}V_{\text{dc}}(\cos(\sqrt{2}\omega_{\text{r}}(t-t_3))+1) + \frac{1}{2}v_{\text{ac}}(\cos(\sqrt{2}\omega_{\text{r}}(t-t_3))-1), \tag{4.38}$$

where the resonance angular frequency, ω_{r}, can be expressed as

$$\omega_{\text{r}} = \sqrt{\frac{1}{2L_{\text{ac}}C_{\text{ds}}}}, \tag{4.39}$$

where C_{ds} is the estimated equivalent drain-source capacitance of the switch and it is assumed to be the same for all the switches. The bottom voltage of v_{S1} and v_{S4} can be derived by substituting $\cos(\sqrt{2}\omega_{\text{r}}(t-t_3)) = -1$ into (4.8), as follows:

$$v_{\text{S1}} = v_{\text{S4}} = -v_{\text{ac}}. \tag{4.40}$$

The results shown that v_{S1} and v_{S4} can always reach zero during T_1 with the bipolar switching modulation as $-v_{\text{ac}}$ is always negative during the half line cycle with positive grid voltage.

T_{fr} is the time required to discharge v_{S1} and v_{S4} from V_{dc} to zero. T_{fr} can be calculated by solving $v_{S1} = 0$ and it is expressed by

$$T_{fr} = \frac{1}{\sqrt{2}\omega_r} \arccos\left(\frac{|v_{ac}| - V_{dc}}{|v_{ac}| + V_{dc}}\right). \tag{4.41}$$

After v_{S1} and v_{S4} become zero at t_{fr}, i_{Lac} will flow through the body diodes of S_1 and S_4, and the negative voltage is blocked by the body diodes. The block time is referred to as T_b. i_{Lac} during T_b can be expressed as

$$i_{Lac}(t) = \frac{(V_{dc} - v_{ac})}{L_{ac}} \cdot (t - t_{fr}) - \frac{\sqrt{2}(V_{dc} + v_{ac})}{2Z_n} \cdot \sin(\sqrt{2}\omega_r t_{fr}), \tag{4.42}$$

where Z_n is

$$Z_n = \sqrt{\frac{L_{ac}}{2C_{ds}}}. \tag{4.43}$$

When i_{Lac} becomes zero at t_b, the blocked period is ended. T_b can be calculated as

$$T_b = \sqrt{L_{ac}C_{ds}}\left(\frac{V_{dc} + |v_{ac}|}{V_{dc} - |v_{ac}|}\right)\sin(\sqrt{2}\omega_r T_{fr}). \tag{4.44}$$

It should be noted that T_{fr} and T_b are functions of the grid voltage phase, ωt.

In this study, T_2 is assumed to be constant, and approximated by

$$T_2 \approx 2\pi\sqrt{L_{ac}C_{ds}}. \tag{4.45}$$

During T_2, v_{S1} and v_{S4} start from zero and oscillate. If the oscillation is a pure LC oscillation, v_{S1} and v_{S4} during T_2 can be expressed as

$$v_{S1}(t) = v_{S4}(t) = \frac{1}{2}(V_{dc} - v_{ac})(-\cos(\sqrt{2}\omega_r(t - t_b) + 1). \tag{4.46}$$

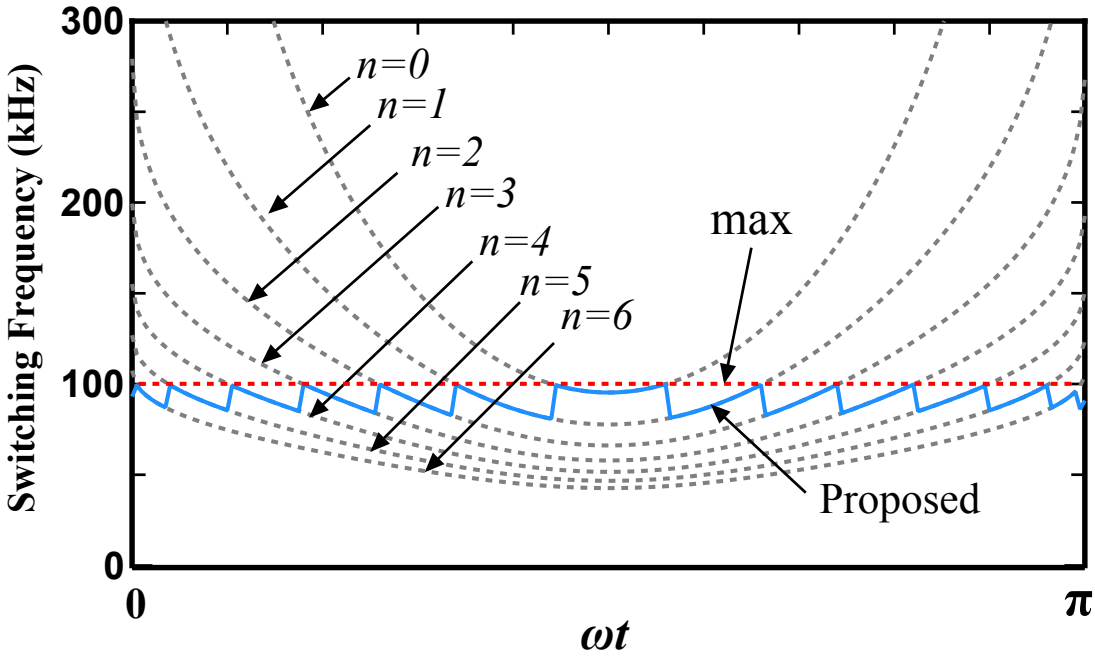

Fig. 4.39 Examples of resulting parameters with the proposed modulation. f_{sw} with different integer numbers for n over half line cycle for the rated current operation.

The valley voltage of v_{S1} and v_{S4} can be derived by substituting $\cos(\sqrt{2}\omega_r(t-t_b)) = 1$ into (4.16), which is

$$v_{S1} = v_{S4} = 0. \tag{4.47}$$

v_{S1} and v_{S4} start from zero and can reach zero again at t_{sec}. Therefore, the initial current can be uniform; and ZVS can be achieved in the next switching cycle by controlling T_{osc} to terminate the switching cycle at this instant.

4.4.4 Design for the Number of Second Resonance

T_{osc} can be determined after selecting integer values for n based on (4.37), then f_{sw} and i_p can be calculated. Fig. 4.39 and Fig. 4.40 show an example of the set of calculated f_{sw} and i_p for the rated sinusoidal current with unity power factor and some different integer numbers

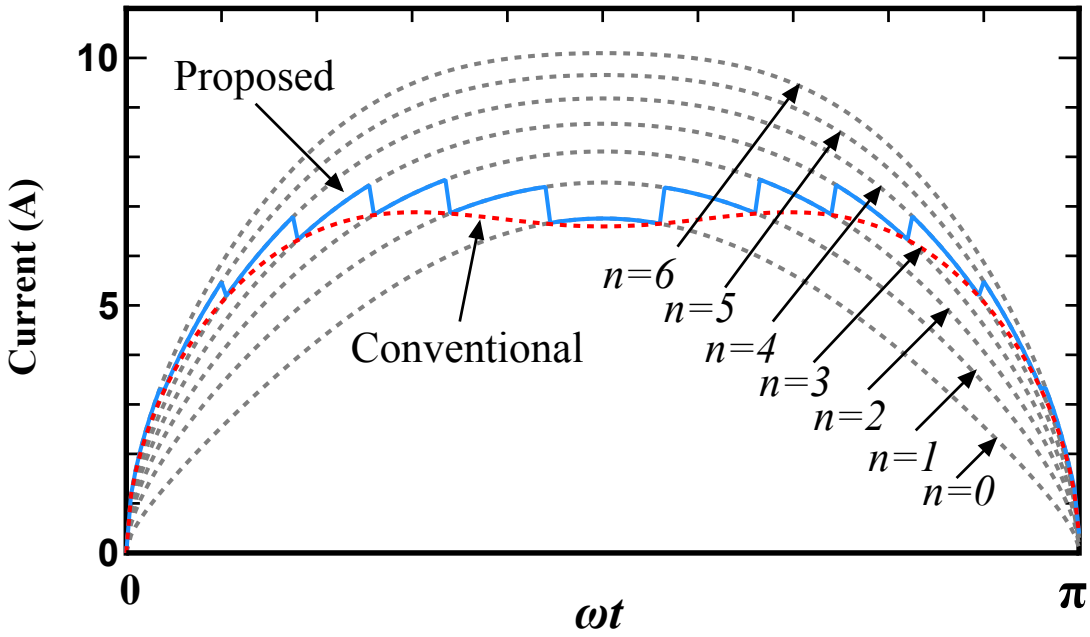

Fig. 4.40 Examples of resulting parameters with the proposed modulation. i_p with different integer numbers for n over half line cycle for the rated current operation.

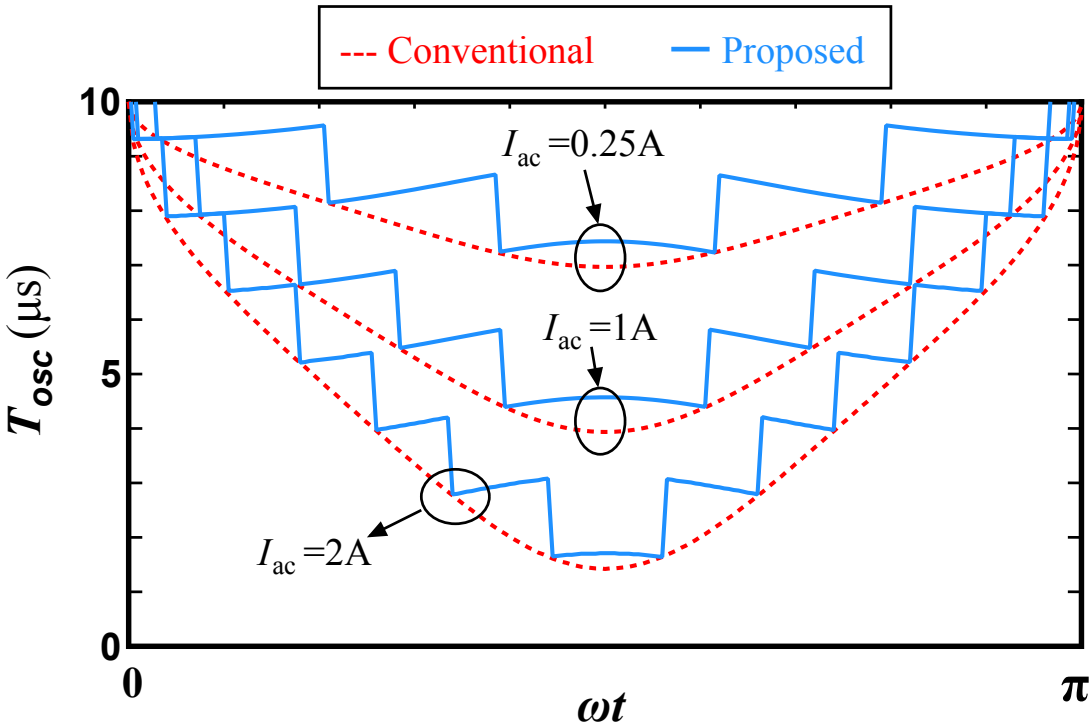

Fig. 4.41 Examples of resulting parameters with the proposed modulation. T_{osc} with different current set-points.

for n, respectively. The calculations are based on a certain specification: $V_{\mathrm{dc}} = 400$ (V), $V_{\mathrm{ac}} = 200$ (V), $I_{\mathrm{ac}} = 2$ (A), $L_{\mathrm{ac}} = 130$ (μH), $C_{\mathrm{ds}} = 0.4$ (nF).

If zero is applied for n, the operation mode becomes BCM and f_{sw} increases significantly when the phase angle is close to 0 or π. However, i_{p} becomes lower than the others. Applying larger integer values for n can reduce f_{sw} significantly; however, i_{p} can become higher. Consequently, fixing n is not a suitable solution regarding the trade-off between f_{sw} and i_{p}.

Selecting an appropriate n can achieve both limiting the switching frequency and obtaining the lowest possible peak current at the same time. n should satisfy the following criteria:

- n should be low as possible to avoid a useless high peak current.
- n should be increased when the resulting switching frequency is higher than the given maximum limitation.

Then, f_{sw} can be determined in accordance with the above design rules for n, as expressed by the blue solid line in Fig. 4.39. f_{sw} has some step changes; however, it is limited to be lower than the given maximum frequency shown by the red dotted line. For the same L_{ac}, f_{sw} should always be lower than that designed for the conventional DCM, so that the DCM operation can always be maintained. However, i_{p} increases in comparison with that in the conventional DCM under the same specification as shown in Fig. 4.40.

T_{osc} with the conventional and proposed modulations, and several current amplitudes are shown in Fig. 4.41. The cascading T_{osc} are obtained after the proposed rules for n are applied.

4.4.5 Simulation Verification and Analysis

Concept Verification

The proposed modulation was verified by a simulation. In order to prove that the proposed modulation does not have the trade-off relationship between f_{sw} and C_{ds} that exists in the

Table 4.4 Specifications for Simulation and Experiments

DC link voltage	V_{dc}	400 V
AC voltage	V_{ac}	200 V
Rated current	$I_{\mathrm{ac.rated}}$	2 A
Inductance of inverter-side inductor	L_{ac}	176-130 μH
Inductance of grid-side inductor	L_{f}	125 μH
Capacitance of filter capacitor	C_{f}	2.2 μF
Maximum switching frequency	$f_{\mathrm{sw(max)}}$	100 kHz

TPCM, widely different values of C_{ds} were evaluated. The same conditions and parameters as those listed in Table 4.4 were used for both modulations in the simulations. The rared current was set at 2 A. For each value of C_{ds}, L_{ac} was calculated to just satisfy $n = 0$ at the peak current phase to make a fair comparison.

The top plots of Fig. 4.42, Fig. 4.43, Fig. 4.44 and Fig. 4.45 show the waveforms with the conventional modulation with the rated current and unity power factor operations. The corresponding middle and bottom plots show the waveforms with the proposed DCM modulation, and the resulting f_{sw} and n. It can be observed that i_{ac} was distorted with the conventional DCM modulation; moreover, the distortion became severe with the increase in C_{ds}. In contrast, clean sinusoidal waveforms of i_{ac} were obtained with the proposed modulation, even with a comparatively large value for C_{ds}.

With the increase in C_{ds}, the peak current of i_{Lac} became higher and the variations of switching frequency became wider. The large value for C_{ds} results in an increase of T_2; therefore, the extension of T_{osc} to find the integer solution for n can be longer. The increase in T_{osc} naturally leads to the increases in T_{sw} and the peak current. Those results indicate that the switching frequency and the peak current are affected by the value of C_{ds}; however, C_{ds} does not affect the current distortion.

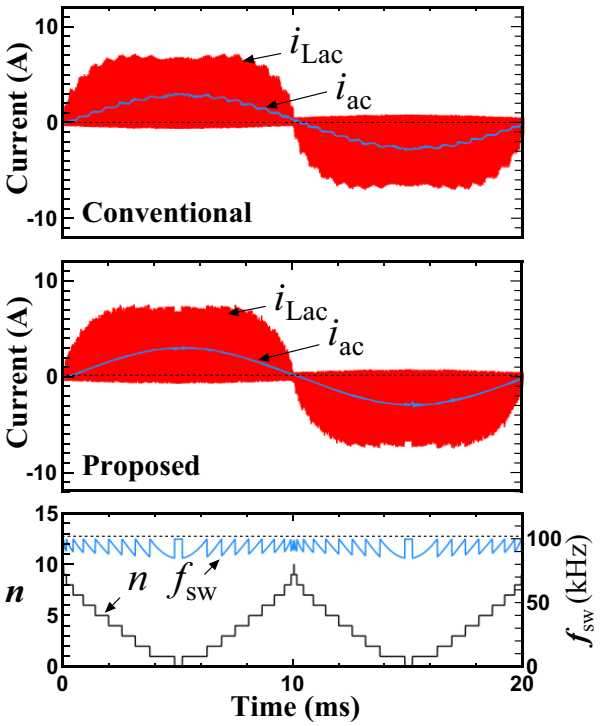

Fig. 4.42 Results obtained by time-domain simulations with the conventional and proposed DCM modulations with $L_{ac} = 135\ \mu$H, $C_{ds} = 0.2$ nF.

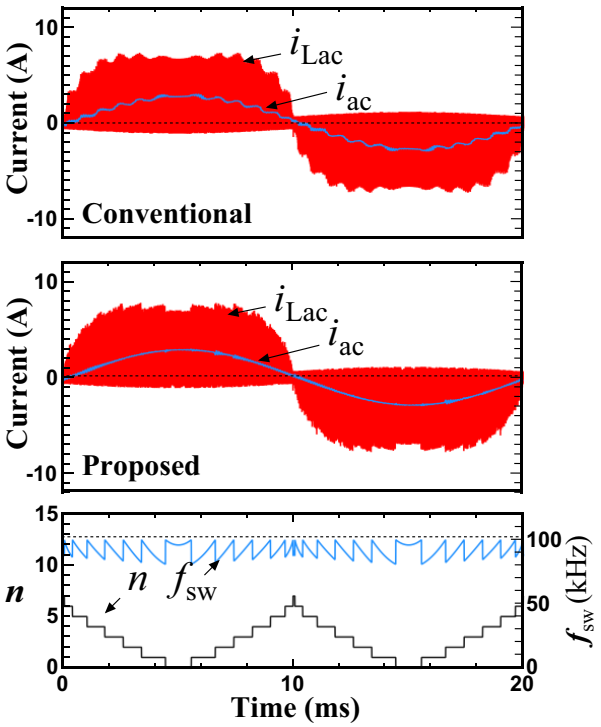

Fig. 4.43 Results obtained by time-domain simulations with the conventional and proposed DCM modulations with $L_{ac} = 130\ \mu$H, $C_{ds} = 0.4$ nF.

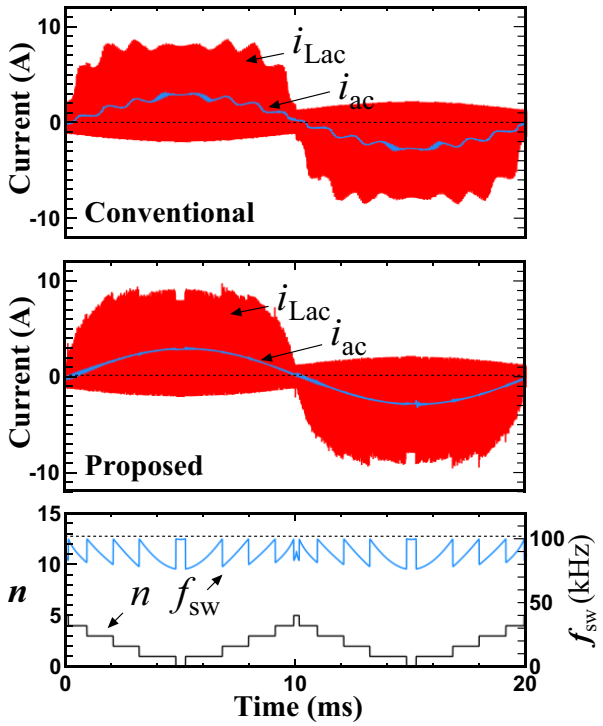

Fig. 4.44 Results obtained by time-domain simulations with the conventional and proposed DCM modulations with $L_{ac} = 100\ \mu$H, $C_{ds} = 1$ nF.

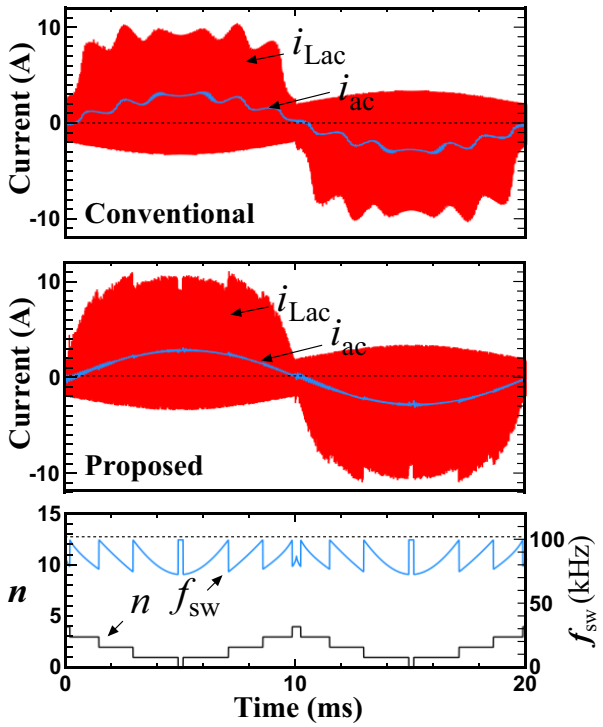

Fig. 4.45 Results obtained by time-domain simulations with the conventional and proposed DCM modulations with$L_{ac} = 80\ \mu$H, $C_{ds} = 2$ nF.

Fig. 4.46, Fig. 4.47, Fig. 4.48 and Fig. 4.49 show the results with the proposed DCM modulation under reduced power levels with $L_{ac} = 130$ (μH) and $C_{ds} = 0.4$ (nF). The results demonstrate that the minimum values of f_{sw} can not be reduced further even under low-power levels. Consequently, the maximum range of the switching frequency can be determined under the rated current operation for a given design.

The upper plots in Fig. 4.50 show the switching cycle waveforms of i_{Lac}, and the switch voltage, v_{S1}, with the conventional modulation in the case of $C_{ds} = 0.4$ (nF). An oscillating v_{S1} could be observed in the duration of the zero-current period. v_{S1} was not zero at most of the turn-on instants. The bottom plots in Fig. 4.50 show the waveforms with the proposed modulation at the time when n was changed from 3 to 2.

The resonance was terminated at the end of the switching cycle with zero voltage in all the switching cycles. Therefore, the switches always turned on with almost zero voltage and current. The results clearly demonstrate the concept of the proposed modulation and the reasons why the current distortion can be improved. Fig. 4.51 shows the switching cycle waveforms for a low-power operation where the current set-point, $I_{ac.set}$, was set at 0.25 A. It can be observed that the zero-current and zero-voltage at turn-on instants could still be achieved with the proposed modulation. It confirms that there is no lower limit of the current amplitude to achieve the zero-current and zero-voltage turn-on.

Trade-off Between Peak Current and Parasitic Capacitance

Fig. 4.52 shows the minimum values of the varying switching frequency, $f_{sw.min}$, normalized by the upper frequency, $f_{sw.max}$, under the rated current operation as function of C_{ds}. Fig. 4.53 shows the increased maximum peak inductor current, $i_{p.max}$, normalized by the value of $i_{p.max}$ when C_{ds} was zero, $i_{p.base}$, under the rated current operation as function of C_{ds}.

It can be observed that $i_{p.max}$ became high along with the increase in C_{ds} and the increased amount became high for higher $f_{sw.max}$. The results indicate that a comparatively large

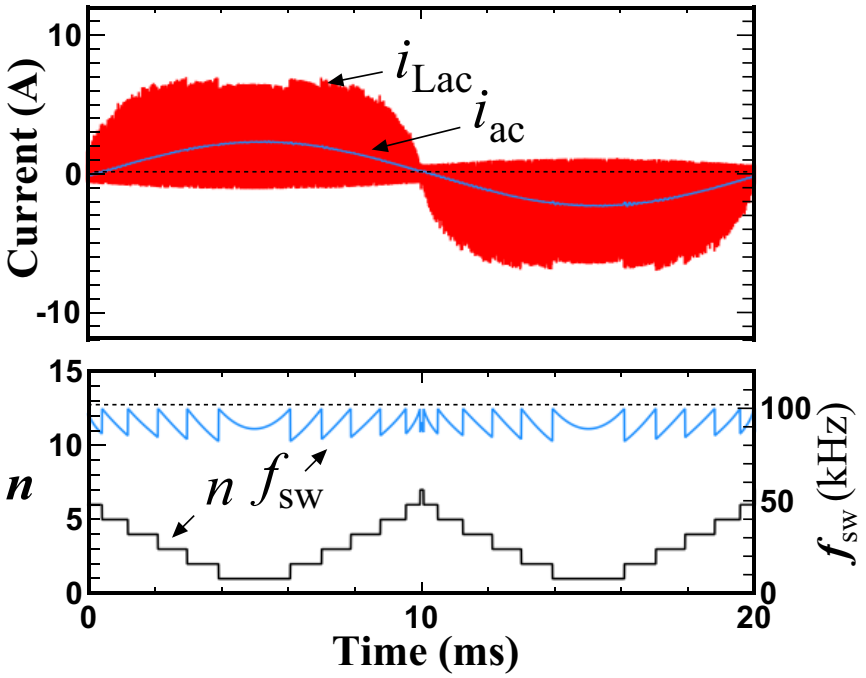

Fig. 4.46 Results obtained by time-domain simulations with the conventional and proposed DCM modulations with $L_{ac} = 130$ (μH), $C_{ds} = 0.4$ (nF) when I_{ac} is set to be 1.6 A.

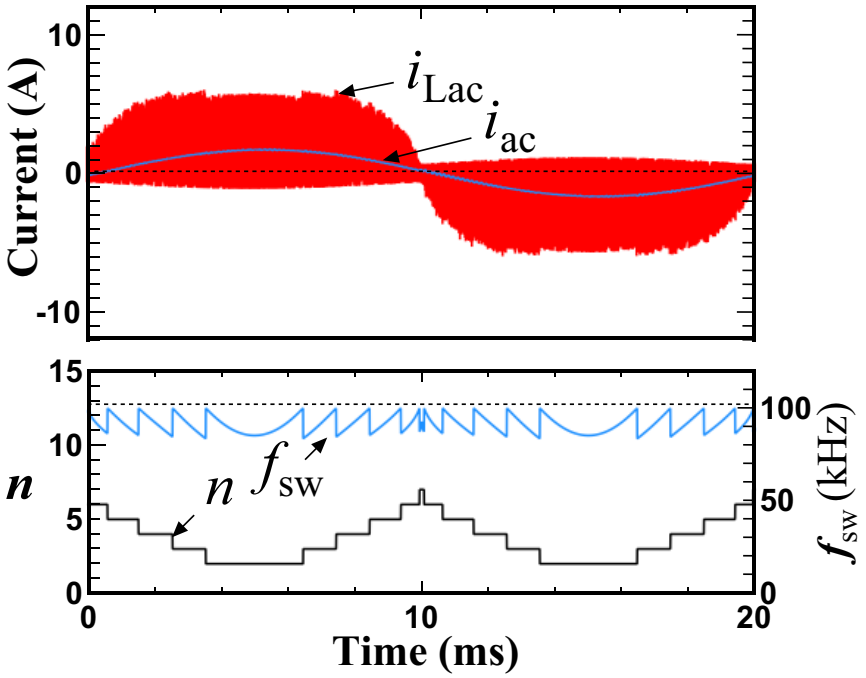

Fig. 4.47 Results obtained by time-domain simulations with the conventional and proposed DCM modulations with $L_{ac} = 130$ (μH), $C_{ds} = 0.4$ (nF) when I_{ac} is set to be 1.2 A.

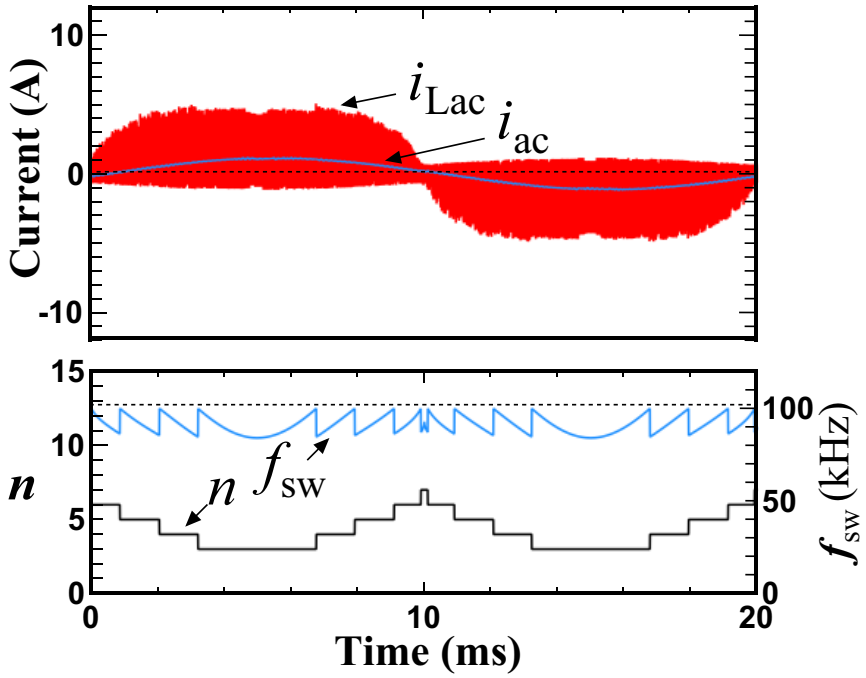

Fig. 4.48 Results obtained by time-domain simulations with the conventional and proposed DCM modulations with $L_{\mathrm{ac}} = 130$ (μH), $C_{\mathrm{ds}} = 0.4$ (nF) when I_{ac} is set to be 0.8 A.

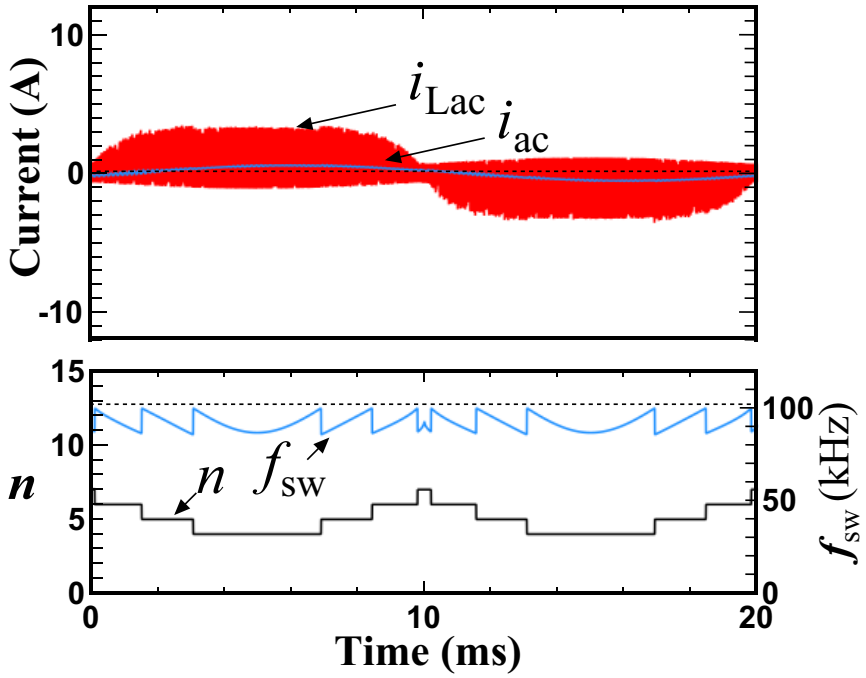

Fig. 4.49 Results obtained by time-domain simulations with the conventional and proposed DCM modulations with$L_{\mathrm{ac}} = 130$ (μH), $C_{\mathrm{ds}} = 0.4$ (nF) when I_{ac} is set to be 0.4 A.

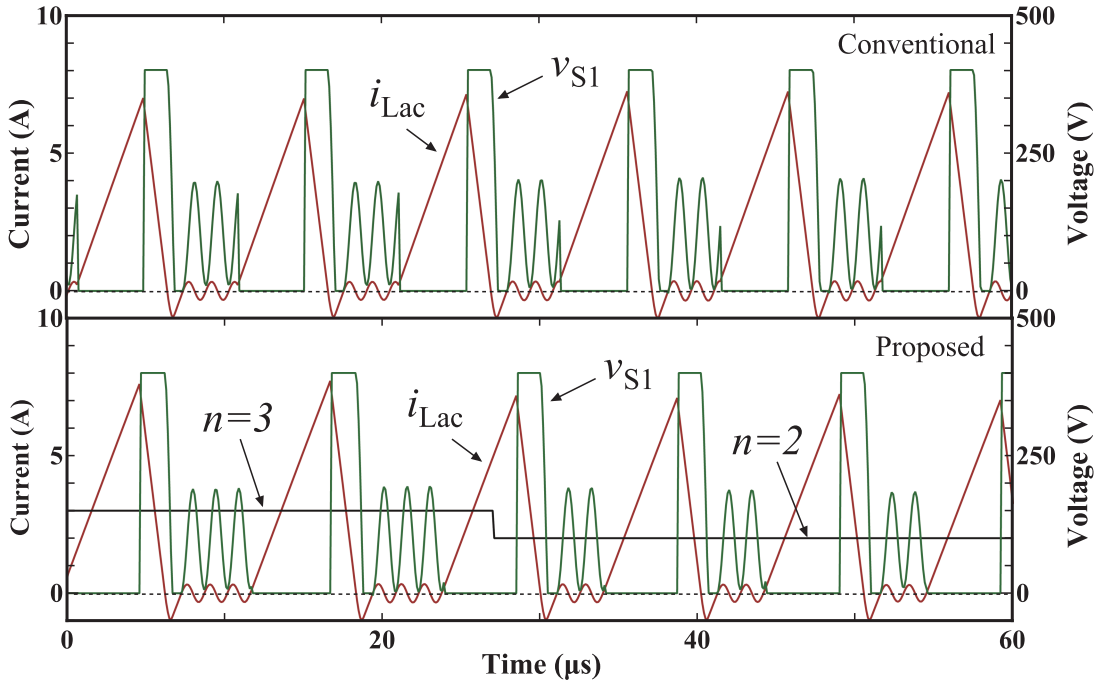

Fig. 4.50 Switching cycle waveforms obtained by time-domain simulations under rated current operation with the conventional and proposed DCM modulations around the current phase where n was changed from 3 to 2.

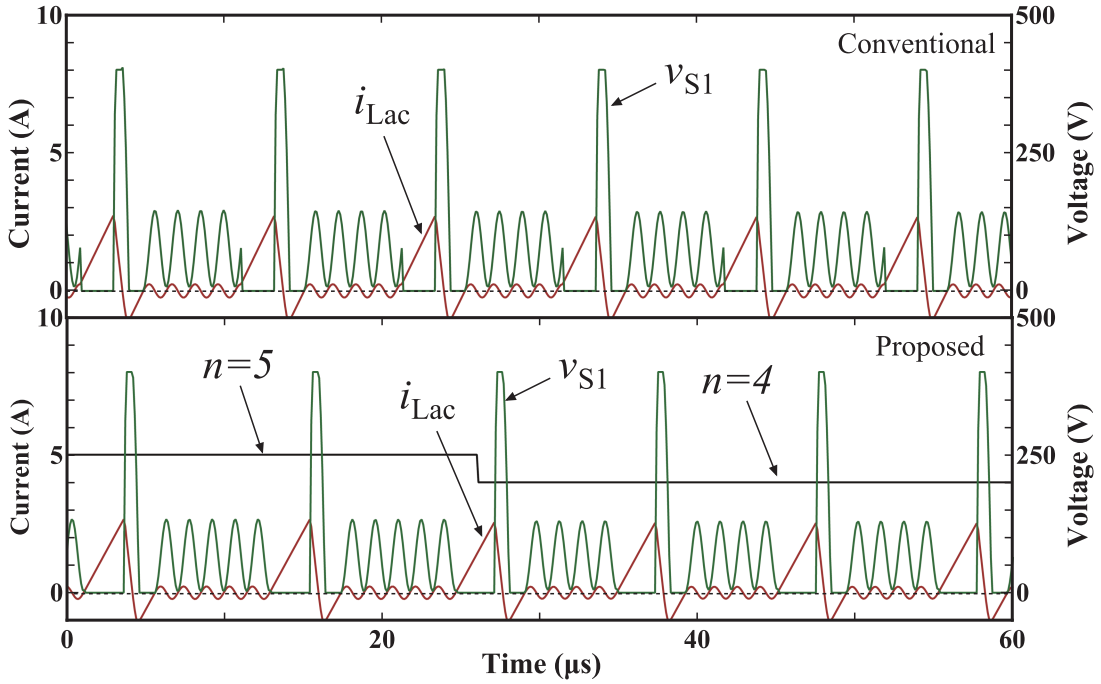

Fig. 4.51 Switching cycle waveforms obtained by time-domain simulations under low-power operation with the conventional and proposed DCM modulations around the current phase where n was changed from 5 to 4.

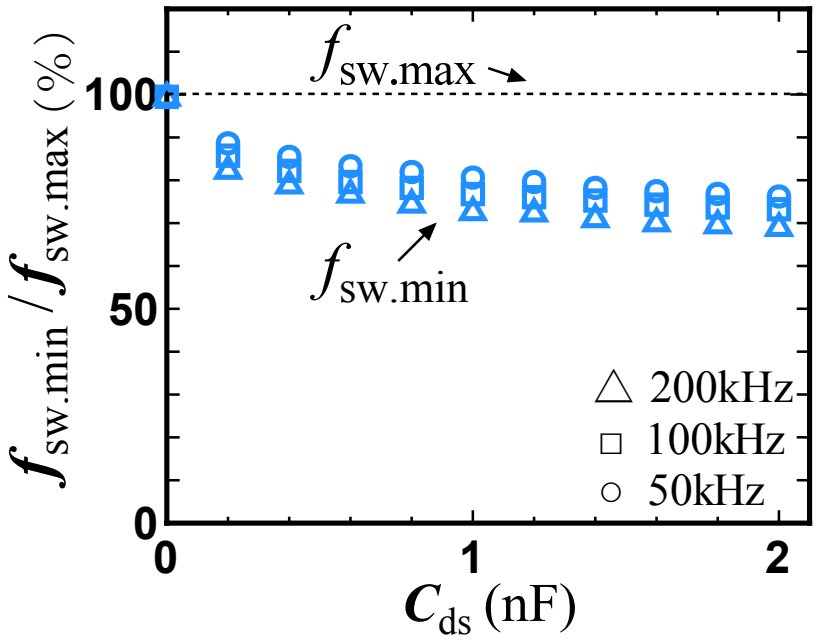

Fig. 4.52 The ratios of $f_{sw.min}$ to $f_{sw.max}$ under the rated current operation as function of C_{ds}

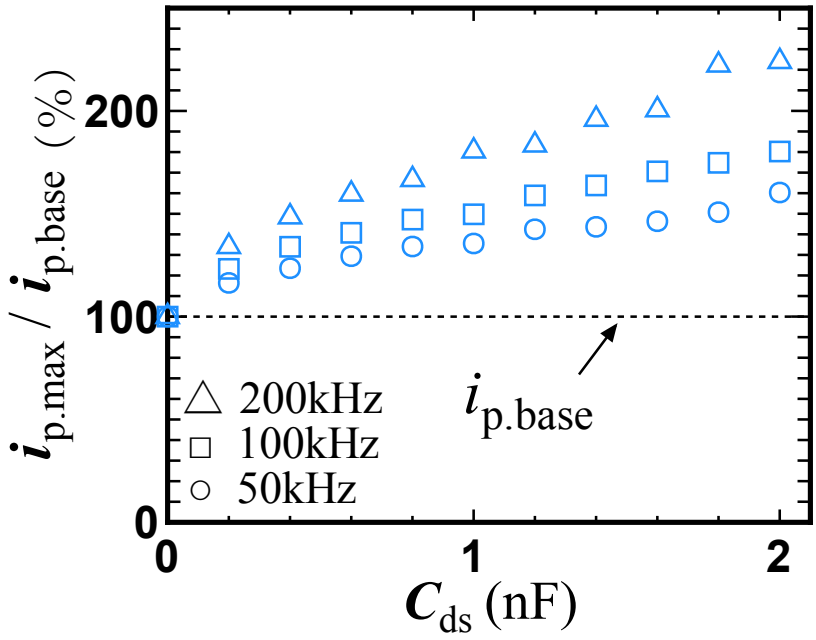

Fig. 4.53 The ratios of $i_{p.max}$ to $i_{p.base}$ under the rated current operation as function of C_{ds}

parasitic capacitance for a given switching frequency results in the increase in the inductor peak current. The trade-off between the conduction loss and parasitic capacitance of power semiconductor devices still affect the system design, even though it does not limit the capability to correct the current waveform.

Calculations for Turn-off and Inductor R.M.S. Current

Fig. 4.54 shows a comparison of calculated turn-off currents of i_{Lac} for every switching cycles over half line cycle with conventional and proposed modulation. The calculation is based on a certain specification that used in the experiment. The conditions and parameters are listed in Table 4.4 ($I_{\mathrm{ac.set}} = 1.85$ A and $L_{\mathrm{ac}} = 130\ \mu$H are considered in order to make a comparison with previous modulation with TPCM). It is different from the modulation with TPCM, the switches are turned off at the same currents and the turn-off currents are increased with the proposed modulation being applied. This is caused by the reduced switching frequency, as discussed in previous sections. Fig. 4.55 shows a comparison of average turn-off current for half line period. The average turn-off current of proposed modulation increases by 5.3% in comparison with that of conventional modulation.

Fig. 4.56 shows a comparison of calculated inductor r.m.s. currents of i_{Lac} for every switching cycles over half line cycle with conventional and proposed modulation. Fig. 4.57 shows a comparison of inductor r.m.s. current for one line period. The proposed modulation also increases the inductor r.m.s. current by 4.1% in comparison with the conventional modulation. This result indicates that the conduction losses can be slightly increased.

Analysis on Transient Response

The transient performance under the proposed DCM modulation was analyzed by using the same simulation software. Fig. 4.58 shows the transient response for a step-up change of the current reference from 20% to 100% at $\omega t = 90^{\circ}$. In the simulations, the capacitor

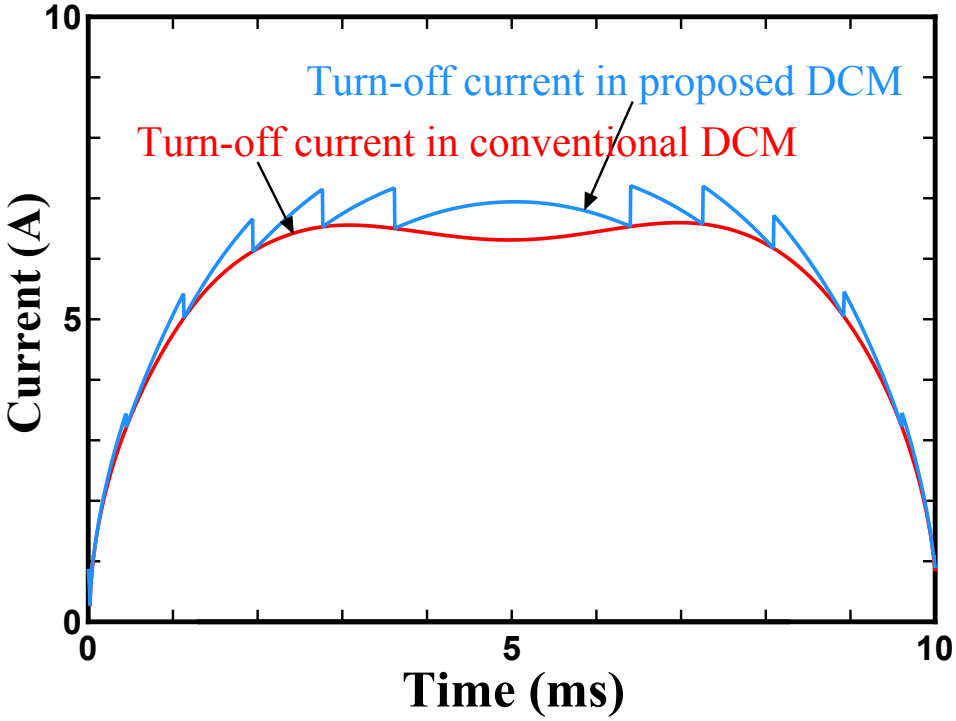

Fig. 4.54 Calculated turn-off currents for every switching cycles over half line period.

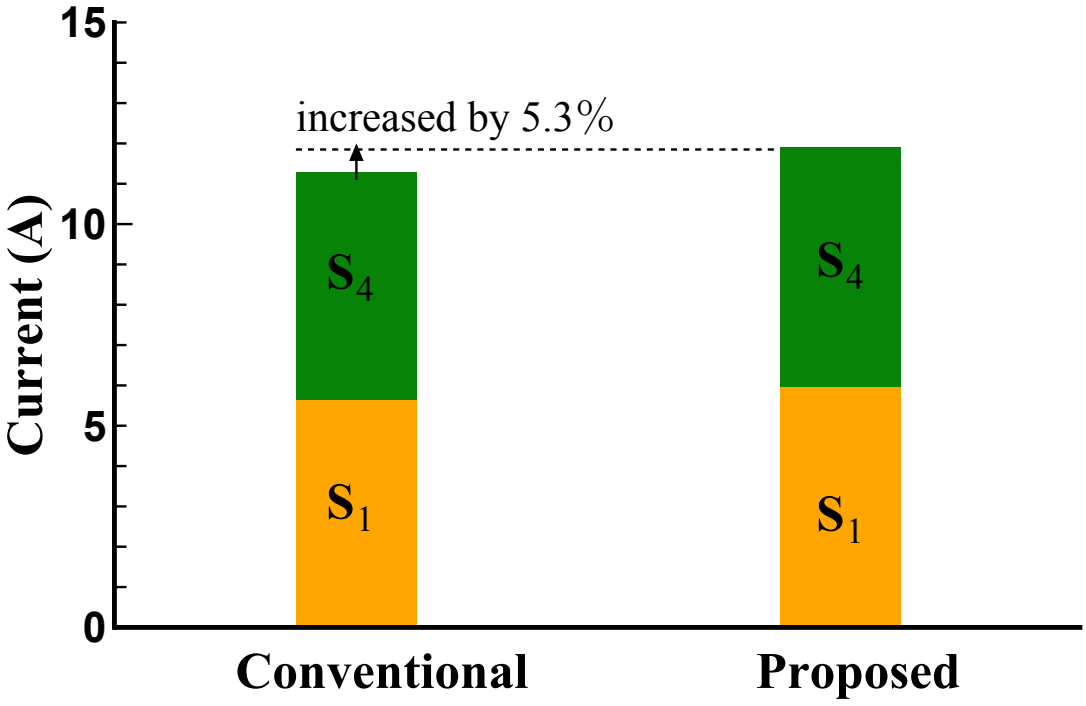

Fig. 4.55 Calculated average turn-off currents for one line period.

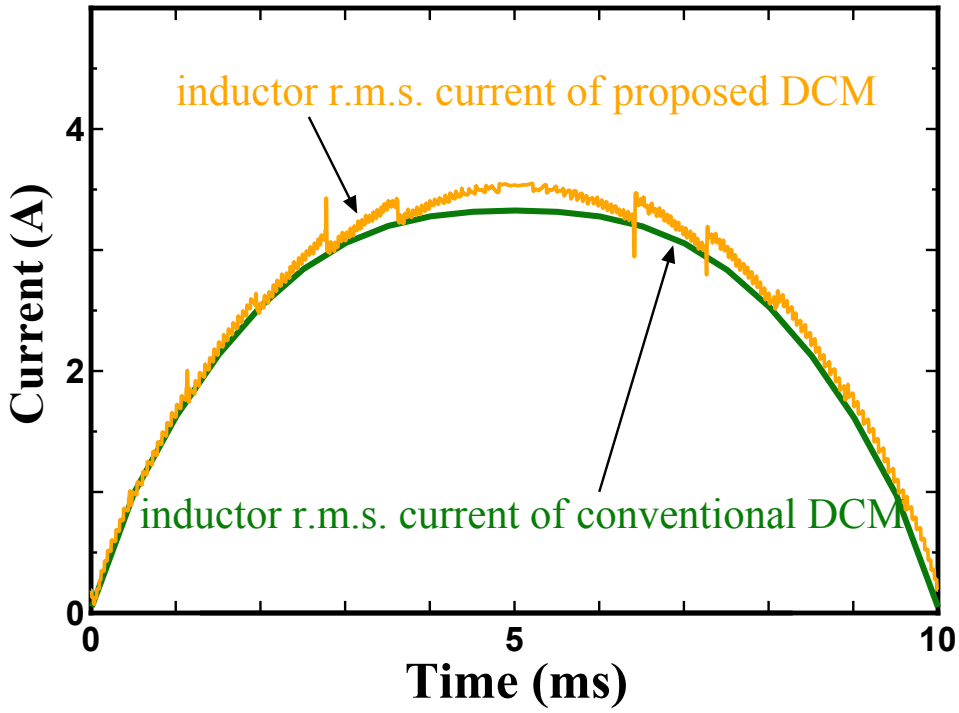

Fig. 4.56 Calculated inductor r.m.s. current for every switching cycles over half line period.

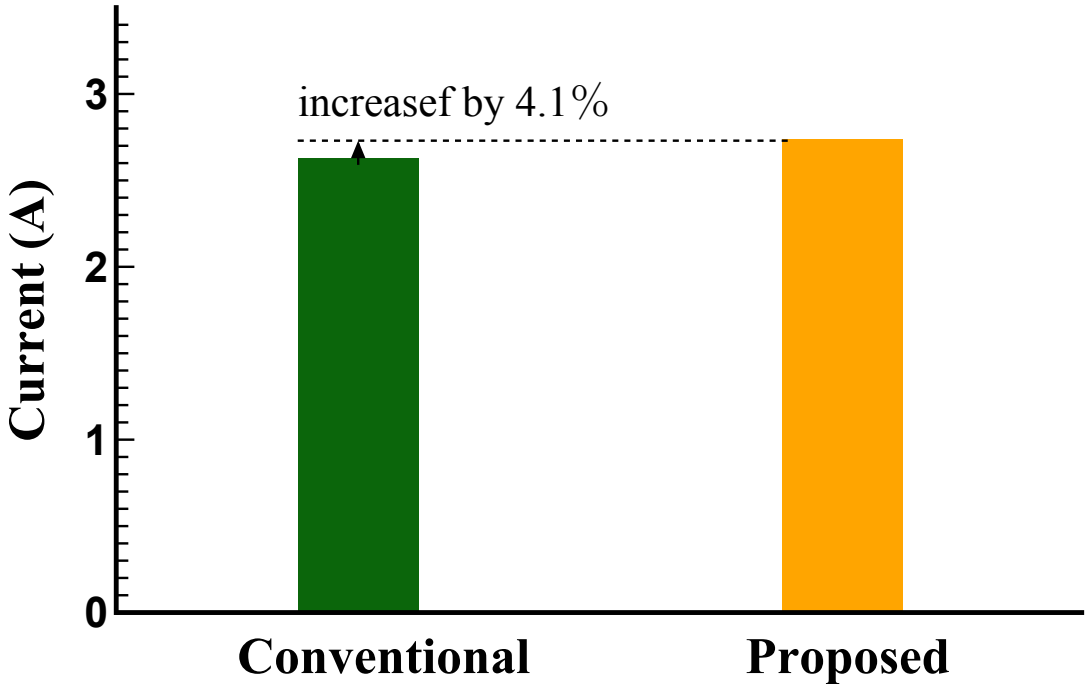

Fig. 4.57 Calculated inductor r.m.s. currents for one line period.

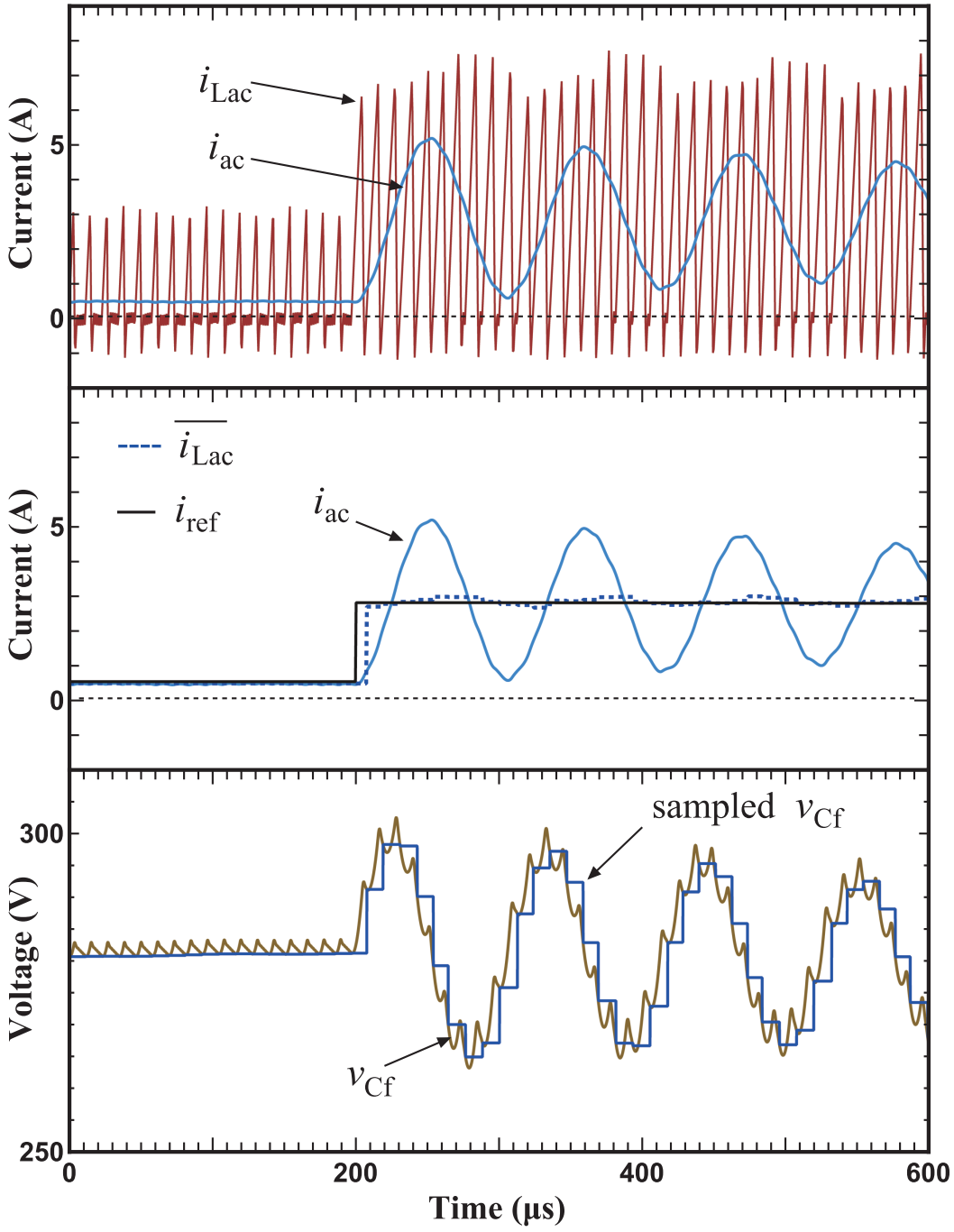

Fig. 4.58 Simulation results of the transient response for a step-up changing of the current reference.

voltage, v_{cf}, was sampled at the beginning of every switching cycle, and used for the duty calculations as v_{ac} for the switching cycle. The average value of i_{Lac} over one switching cycle, i_{ave}, was calculated from the measured waveform of i_{Lac}. It should be noted that i_{ave} shown in Fig. 4.58 is delayed by one switching cycle due to the calculation.

It can be observed from Fig. 4.58 that i_{ave} could respond in step to the change of i_{ref} without remarkable overshoot or oscillation, even though the peak of i_{Lac} was oscillating. The result confirms that the dynamic response of i_{ave} under the feed-forward control is sufficiently quick. However, a slight oscillation of i_{ave}, which can be caused by the differences between v_{cf} and sampled v_{Cf}, was observed.

On the other hand, i_{ac} cannot respond as quickly as i_{Lac}, since it is not directly controlled by the feed-forward controller. An undesired oscillation of i_{ac} was observed after the step change. It is confirmed that the frequency of this oscillation was close to the resonance frequency of the LC low-pass filter composed by L_f and C_f. In addition, it was also observed that the oscillation decayed after several ten switching cycles by parasitic resistance of the components. The result indicates that the oscillation will not cause severe problems in low-power converters. However, further investigation is still needed for this phenomena.

Analysis on EMI Generation

In order to investigate the EMI generation caused by the proposed modulation in comparison with the conventional DCM modulation, and to discuss the required effort for filtering it, the conducted emission was analyzed by time-domain simulations using the same software. Two high-pass filters, which emulate a line impedance stabilization network (LISN) for the frequency range between 150 kHz and 30 MHz, were connected between the inverter (after the harmonic filter) and an AC source as shown in Fig. 4.59.

The voltages across 50 Ω resistors, v_{LISN1} and v_{LISN2}, were measured. The difference voltage between v_{LISN1} and v_{LISN2} is considered to be the differential-mode (DM) conducted

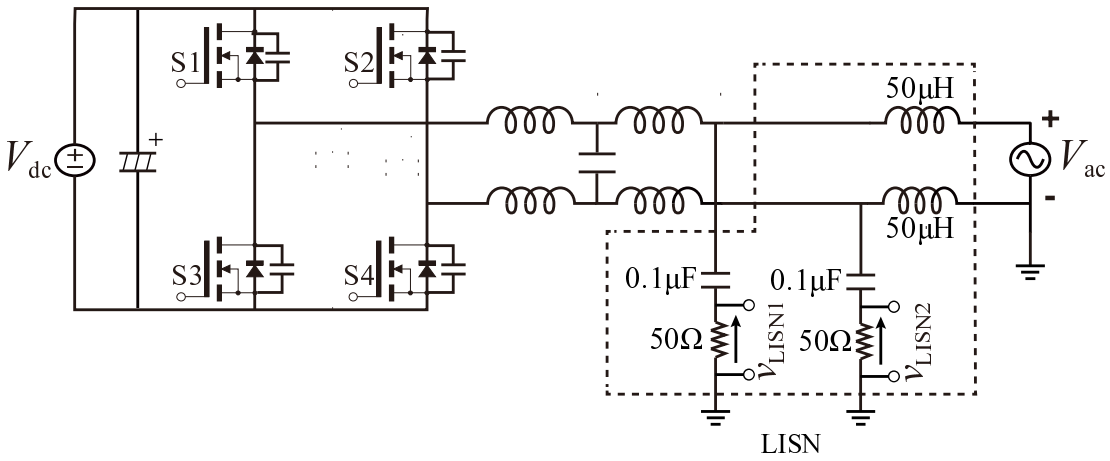

Fig. 4.59 Schematic view of the EMI noise measurement setup conducted in the simulation.

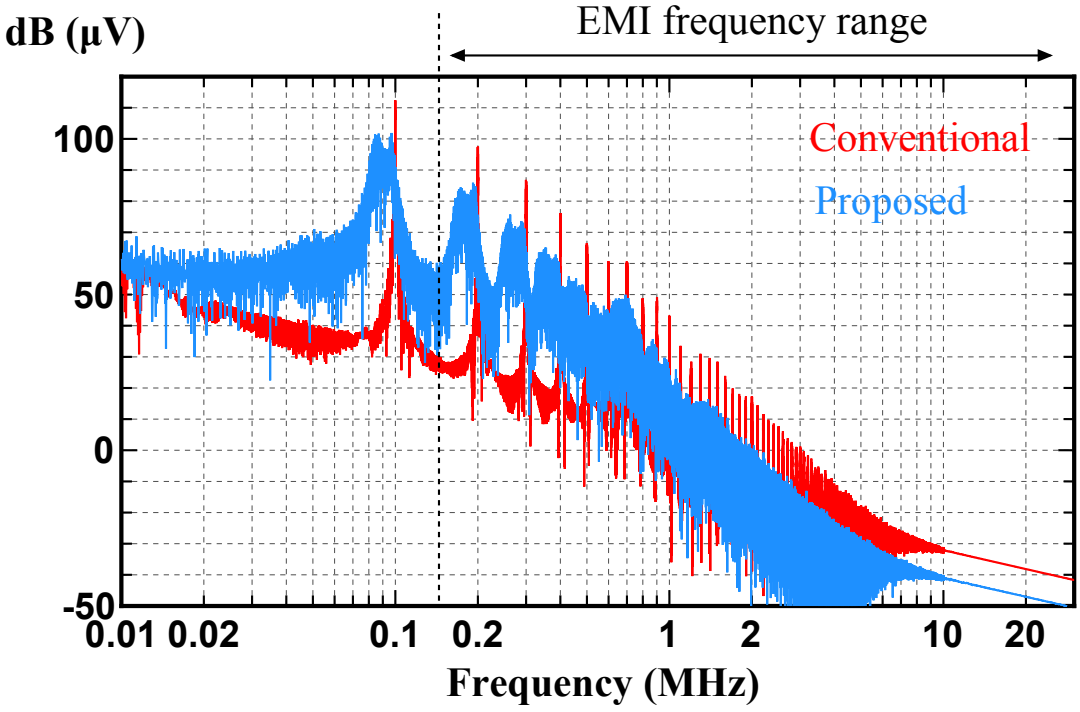

Fig. 4.60 Comparison of the spectrum of DM voltage between conventional and proposed DCM.

emission. On the other hand, the sum (average) of v_{LISN1} and v_{LISN2} represents the common-mode (CM) conducted emission. Both the conventional and proposed DCM modulations employ a bipolar switching scheme. Therefore, the CM voltage can theoretically be zero if the switching of the paired switches is perfectly simultaneous and parasitic components are symmetric. Consequently, only the DM conducted emission was analyzed in the simulation.

The simulation time step was set at 1 ns in order to support the results up to 30 MHz. $C_{\mathrm{ds}} = 0.4$ (nF) for the switching devices was considered. The switching frequency was fixed at 100 kHz for the conventional DCM modulation. The range of the switching frequency for the proposed DCM modulation was same with that shown in Fig. 4.43. The frequency spectrum of the DM voltage over a line cycle was calculated through fast Fourier transform (FFT). Fig. 4.60 shows the calculated results. The EMI frequencies are in the range of 150 kHz to 30 MHz. For the conventional DCM modulation, peaks clearly appeared at integral multiples of the switching frequency and their side-bands were narrow. On the other hand, for the proposed DCM modulation, the spectrum spread over a wider range of frequencies due to the variable switching frequency operation. It can be observed that the peaks were reduced in comparison to those with the conventional DCM; therefore, the requirement of attenuation for the peak components can be less. However, the widely spreading frequency spectrum can increase the difficulties of designing the EMI filter in comparison with that designed for specified peak frequencies.

4.4.6 Experimental Verification

Experimental Setup

In this experiment, the same SiC-MOSFET based prototype as that shown in Section 4.3.5 was used. To reduce the conduction loss, switching devices with relatively low on-resistance are preferred. However, such devices have a relatively large output capacitance, which results in a severe current distortion with the conventional DCM modulation in a sufficiently high

switching frequency. The distortion can be eliminated by the proposed DCM modulation, even with the relatively large parasitic capacitance as discussed in Section 4.4.5. SiC-MOSFETs (SCT3030AL, 650 V, 70 A), which have a relatively high current rating, were intentionally used to demonstrate the advantage of proposed frequency variation modulation. The same circuit parameters and conditions listed in Table 4.4 were also used for the experiments. The percentage impedance of the inverter-side inductor and grid-side inductor are 0.041% and 0.039%, respectively. In comparison with the that used in CCM control, which is usually 2%-5% of base impedance, the total percentage impedance is about 0.08% only.

The maximum switching frequency, $f_{\mathrm{sw(max)}}$ was set at 100 kHz and used for the conventional DCM modulation. In the conventional DCM modulation, the switching frequency is fixed. Therefore, the carrier counter, TBCTR, in the PWM peripheral module or a field programmable gate array (FPGA) is always reset at a fixed specified value, TBPRD, which corresponds to the switching frequency. TBPRD can be calculated as $\mathrm{TBPRD} = f_{\mathrm{clock}}/f_{\mathrm{sw}}$, where f_{clock} is the clock frequency of the digital controller. The gate signals are generated by comparing TBCTR with a register value, CMPA, that corresponds to the time duty ratio, d_{on}, as $\mathrm{CMPA} = d_{\mathrm{on}} \times \mathrm{TBPRD}$. In the proposed DCM modulation, the switching frequency has some variations; therefore, both the TBPRD and CMPA should be updated every control cycle.

The system structure of the fabricated single-phase grid-tied inverter is shown in Fig. 4.61. The specifications of the DSP and FPGA used in the experiments are listed in Table 4.5. In this prototype, the computations of CMPA and TBPRD were conducted in a digital signal processor (DSP) using a periodic timer interrupt of 20 kHz, and the calculated results were sent to the FPGA to generate the gate signals. The calculation results were kept constant during one control cycle, which was longer than the switching cycle. This implementation was needed due to the longer calculation time than the switching cycle in this setup. It

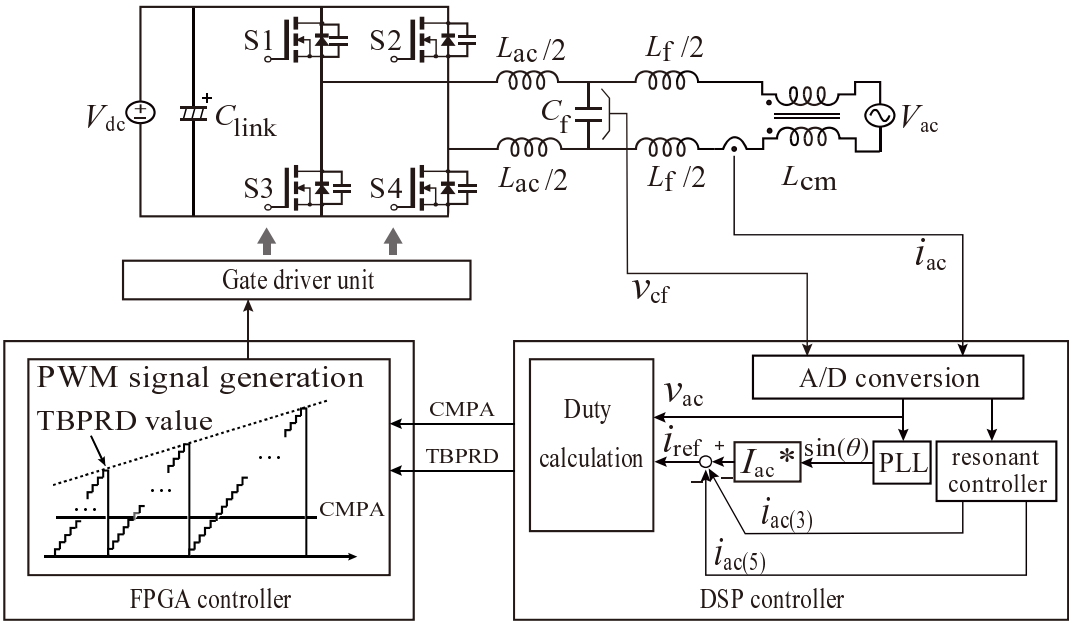

Fig. 4.61 Simplified structure of the fabricated single phase grid-tied inverter system.

Table 4.5 Specifications of the Digital Controllers

	Model	Clock Speed	
DSP	TMS320F28377S	$f_{clock.DSP}$	200 MHz
FPGA	XC6SLX45	$f_{clock.FPGA}$	100 MHz

can cause harmonic distortion of the frequencies higher than 20 kHz. However, the total harmonic distortion (THD), which is usually defined by the components lower than 49th order, is not affected. The DC voltage was supplied from a DC power source, the AC voltage was supplied from a linear AC voltage source with power dissipating resistors connected in parallel. A current sensor was connected with the grid-side inductor in series to perform an over-current-protection and a low-order harmonic compensation. The instantaneous filter capacitor voltage, v_{cf}, was sensed and used as v_{ac} for the duty computations. A sinusoidal current reference, which was in-phase with v_{cf}, was given as i_{ref} so that the unity power factor was almost achieved.

Practical Implementation

n can be found in accordance with the design rules discussed in Section 4.4.4. However, n is required to be examined from 0 in every control cycle. The computation time increases when the current phase angle is close to zero and π. In this prototype, a simple way was used to find the appropriate n, that is, to obtain n as

$$n = \lceil \frac{T_{\mathrm{osc(conv)}} - T_1}{T_2} \rceil, \tag{4.48}$$

where $T_{\mathrm{osc(conv)}}$ is the calculated zero current period with the conventional DCM modulation, as depicted in Fig. 4.41 with the red dotted line. The minimum integer values of n to satisfy the design rules can be easily found by means of a ceiling function.

$T_{\mathrm{osc(conv)}}$ can be expressed as

$$T_{\mathrm{osc(conv)}} = \frac{1 - d_{\mathrm{on(conv)}} - d_{\mathrm{sr(conv)}}}{f_{\mathrm{sw(conv)}}}, \tag{4.49}$$

where $f_{\mathrm{sw(conv)}}$ is the designed switching frequency with the conventional DCM, which is equal to $f_{\mathrm{sw(max)}}$ for this purpose; $d_{\mathrm{on(conv)}}$ and $d_{\mathrm{sr(conv)}}$ are the duty ratios for turn-on and diode conduction with the conventional DCM, respectively. $d_{\mathrm{on(conv)}}$ and $d_{\mathrm{sr(conv)}}$ can be calculated [4] as

$$d_{\mathrm{on(conv)}} = \sqrt{\frac{|i_{\mathrm{ref}}| L_{\mathrm{ac}} f_{\mathrm{sw(conv)}} (V_{\mathrm{dc}} + |v_{\mathrm{ac}}|)}{V_{\mathrm{dc}} (V_{\mathrm{dc}} - |v_{\mathrm{ac}}|)}}, \tag{4.50}$$

$$d_{\mathrm{sr(conv)}} = \sqrt{\frac{|i_{\mathrm{ref}}| L_{\mathrm{ac}} f_{\mathrm{sw(conv)}} (V_{\mathrm{dc}} - |v_{\mathrm{ac}}|)}{V_{\mathrm{dc}} (V_{\mathrm{dc}} + |v_{\mathrm{ac}}|)}}. \tag{4.51}$$

Before the implementation of the proposed modulation, T_2 was measured through a preliminary operation with the conventional DCM; and the equivalent value of the drain-source capacitance, C_{ds}, was approximated on the basis of (4.25). Then the resonant angular

frequency during T_1, ω_r, was calculated by using the values of C_{ds} and L_{ac} on the basis of (4.39). Consequently, the sequence of calculation to get n, TBPRD and CMPA are listed as follows:

1. Calculating the duty ratios, $d_{on(conv)}$, $d_{sr(conv)}$, and zero current period, $T_{osc(conv)}$, in the conventional DCM on the basis of (4.50), (4.51), (4.49), respectively.

2. Calculating n on the basis of (4.48), where T_1 is the sum of T_{fr} and T_b, which are calculated on the bases of (4.41) and (4.44).

3. Calculating the zero current period, T_{osc}, on the basis of (4.37).

4. Calculating the peak inductor current, i_p, on the basis of (4.30).

5. Calculating the time for turn-on, T_{on}, and turn-off, T_{off}, on the basis of (4.31) and (4.32), respectively.

6. Calculating the switching period, T_{sw}, and switching frequency, f_{sw}, on the basis of (4.33) and (4.34), respectively; and calculating TBPRD.

7. Calculating the duty ratio for turn-on, d_{on}, on the basis of (4.35); and calculating CMPA.

Waveforms Demonstration and Analysis

The experimental waveforms with the conventional and proposed modulations under the rated current operations are shown in Fig. 4.62 and Fig. 4.63, respectively. These results are similar to those of the simulation in that i_{ac} was seriously distorted when the conventional DCM was adopted. The total harmonic distortion (THD) of i_{ac} was 8.8%. Meanwhile, the distortion was obviously reduced by applying the proposed modulation, and the THD of i_{ac} was reduced to 1.0%.

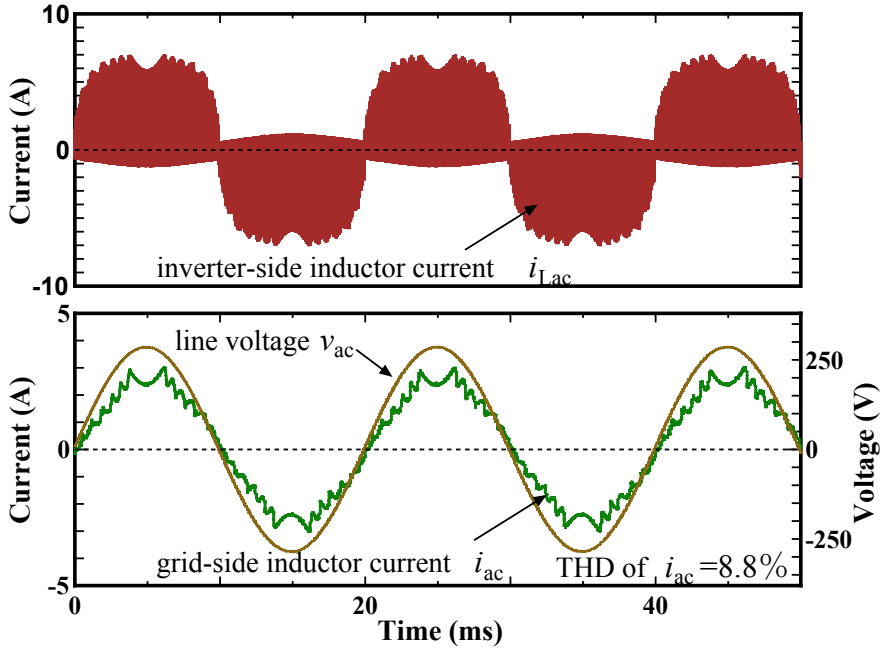

Fig. 4.62 Experimental waveforms of the inverter-side inductor current, i_{Lac}, grid-side inductor current, i_{ac}, and the line voltage, v_{ac}, with the conventional modulation and low-order harmonic compensation for rated current operation.

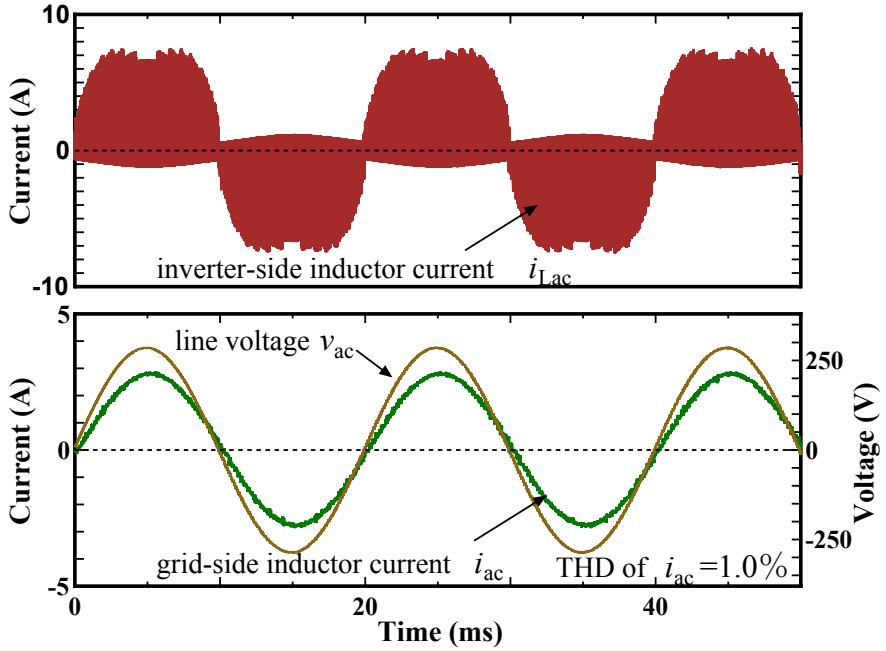

Fig. 4.63 Experimental waveforms of the inverter-side inductor current, i_{Lac}, grid-side inductor current, i_{ac}, and the line voltage, v_{ac}, with the proposed modulation and low-order harmonic compensation for rated current operation.

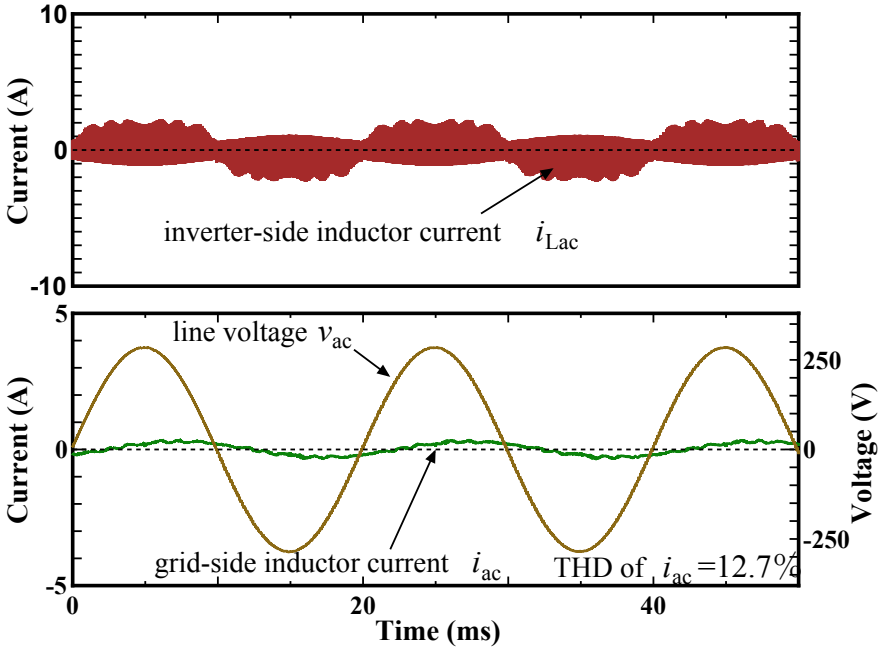

Fig. 4.64 Experimental waveforms of the inverter-side inductor current, i_{Lac}, grid-side inductor current, i_{ac}, and the line voltage, v_{ac}, with the conventional modulation and low-order harmonic compensation for low current operation.

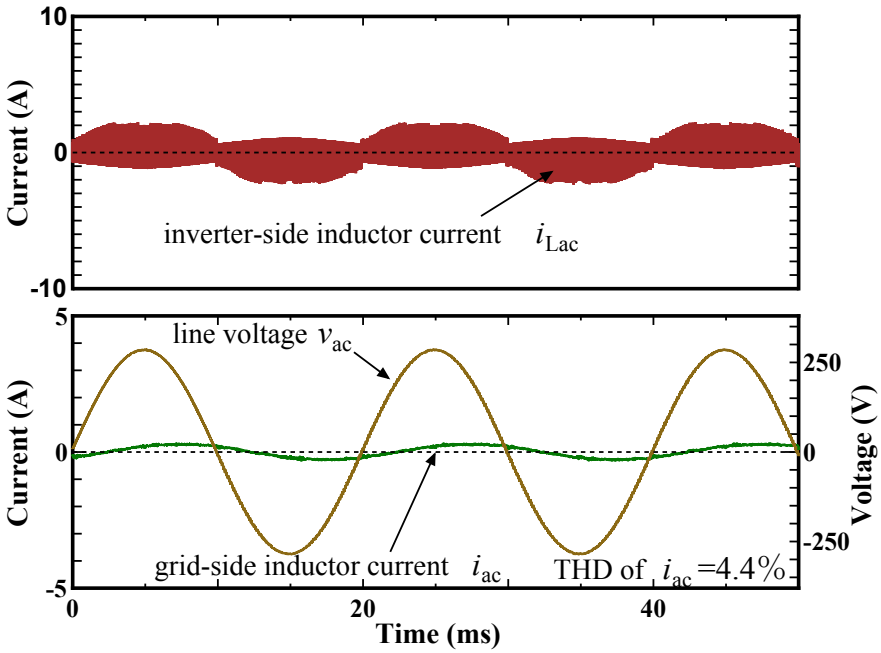

Fig. 4.65 Experimental waveforms of the inverter-side inductor current, i_{Lac}, grid-side inductor current, i_{ac}, and the line voltage, v_{ac}, with the proposed modulation and low-order harmonic compensation for low current operation.

Fig. 4.64 and Fig. 4.65 demonstrate the waveforms under low-power operations. The current distortion could still be observed in i_{ac} with the conventional modulation. The THD of i_{ac} was reduced from 12.7% to 4.4% after the proposed modulation was adopted. Low THD of i_{ac} was achieved even in the low-power operation. It should be noted that lagging currents caused by the filter capacitors were observed in the low-power operations.

Harmonic Analysis

The harmonic components in i_{ac} were calculated by means of a discrete Fourier transform (DFT) and the results are shown in Fig. 4.66. The harmonic components were reduced effectively in almost all the orders after the proposed DCM modulation was adopted.

The THDs and total demand distortions (TDDs) of i_{ac} for rated current operation are calculated from the experimental waveforms. The results are shown in Fig. 4.67. For the conventional modulation, the THDs were higher than 5% in the entire operating power range, although the TDDs at light loads were less than 5%. Both the THDs and TDDs were less than 5% in the entire operating power range with the proposed modulations. For conventional DCM modulation, the switching frequency has to be reduced to at least one-fourth of the present one to obtain the similar performance of THDs and TDDs under this experimental condition. Consequently, further volume reduction for a DCM grid-tied inverter can be achieved with the proposed modulation.

Demonstration of Switching Cycles Waveforms

Fig. 4.68 demonstrates the switching cycle waveforms with both modulations. With the conventional DCM, the switch voltage, v_{S1}, could not resonate to zero at most of the turn-on instants, and v_{S1} at the turn-on instants varied. Therefore, it can be considered that the uniform turn-on was not achieved, and that is the reason why the current distortion was observed in i_{ac}. Fig. 4.69 demonstrates the waveforms with the proposed DCM around the

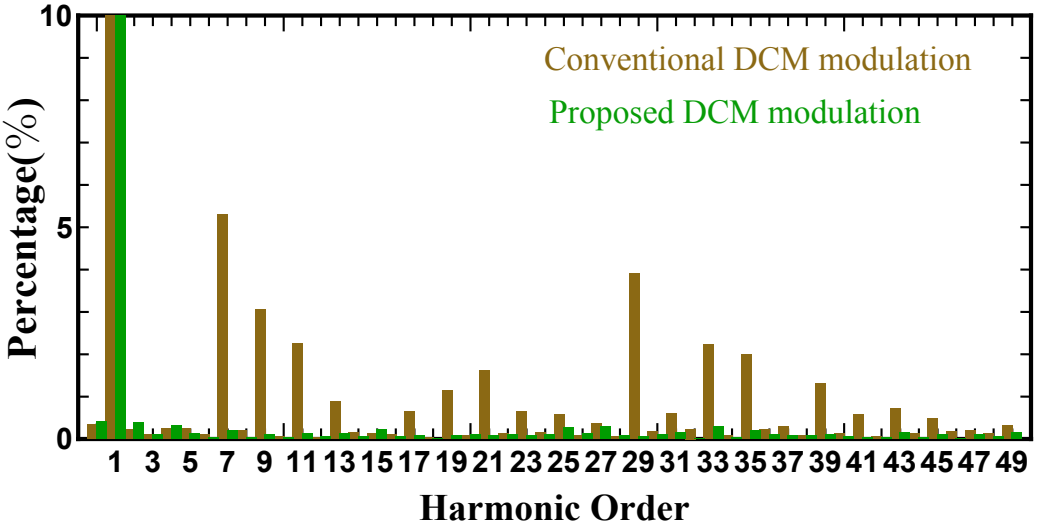

Fig. 4.66 Harmonic components in i_{ac} at the rated current operation.

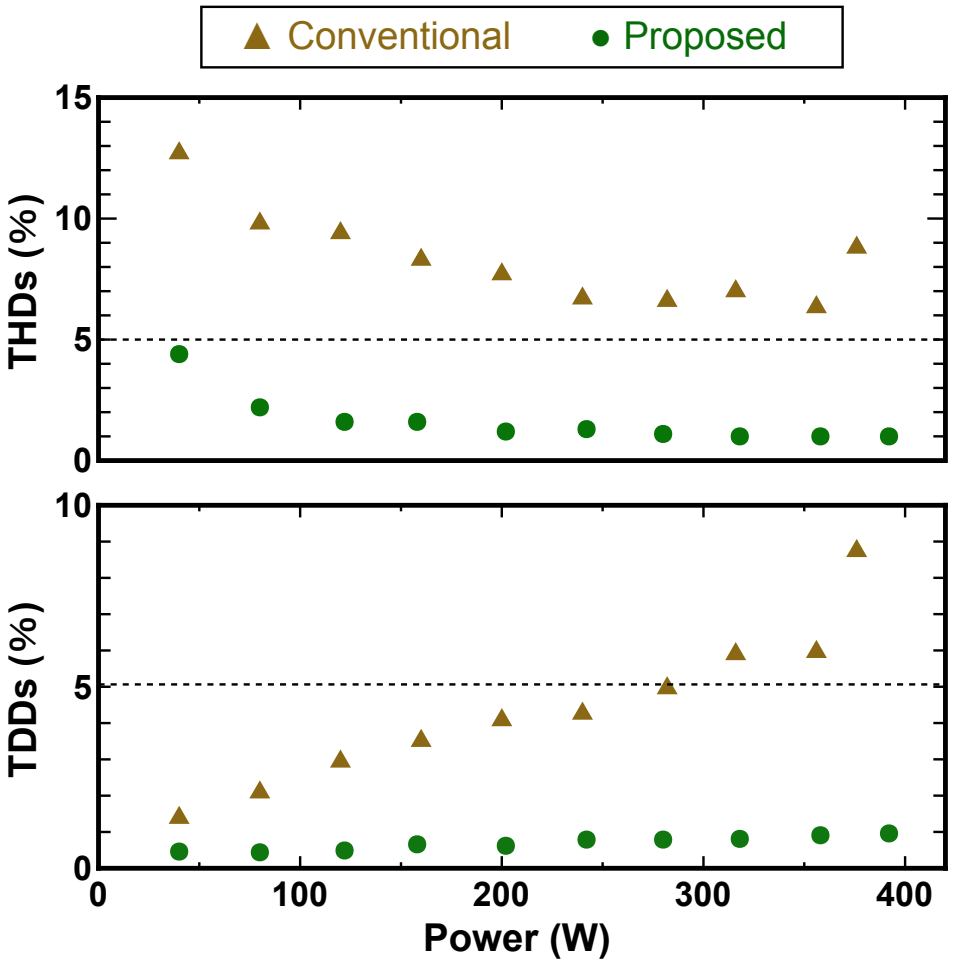

Fig. 4.67 Measured TDDs as function of the output power.

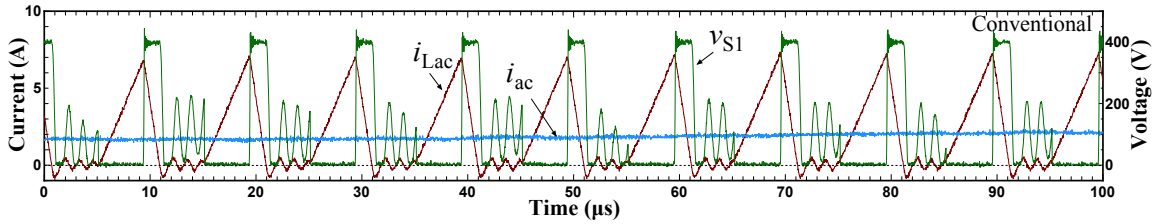

Fig. 4.68 Switching cycle waveforms of inverter-side inductor current, i_{Lac}, and switch voltage, v_{S1}, with conventional DCM modulation.

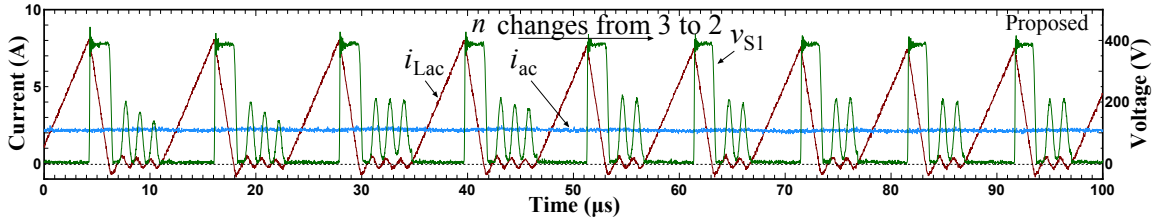

Fig. 4.69 Switching cycle waveforms of inverter-side inductor current, i_{Lac}, and switch voltage, v_{S1}, with proposed DCM modulation around the current phase where n was changed from 3 to 2.

current phase where n was changed from 3 to 2. It was confirmed that the switching cycles were controlled properly, and the switch was turned on at valleys of v_{S1} in all the switching cycles. The changing switching frequency could be observed around 100 μs. It was also confirmed that the transient of n could be performed safely. v_{S1} could not completely resonate to zero in some switching cycles. This could be caused by the resistive components in the oscillation current path. Nevertheless, uniform turn-on was still achieved and v_{S1} could resonate to low values in comparison with the result with the conventional DCM modulation.

Demonstration of Current Response

Fig. 4.70 and Fig. 4.71 show the line cycle and switching cycle view of the response of the currents for a step-up change of the current reference, respectively. Fig. 4.72 and Fig. 4.73 show the line cycle and switching cycle view of response of the currents for a step-down change of the current reference, respectively. Those were similar with the simulation results shown in Section 4.4.5. There were almost no overshoot observed in i_{Lac} after the step

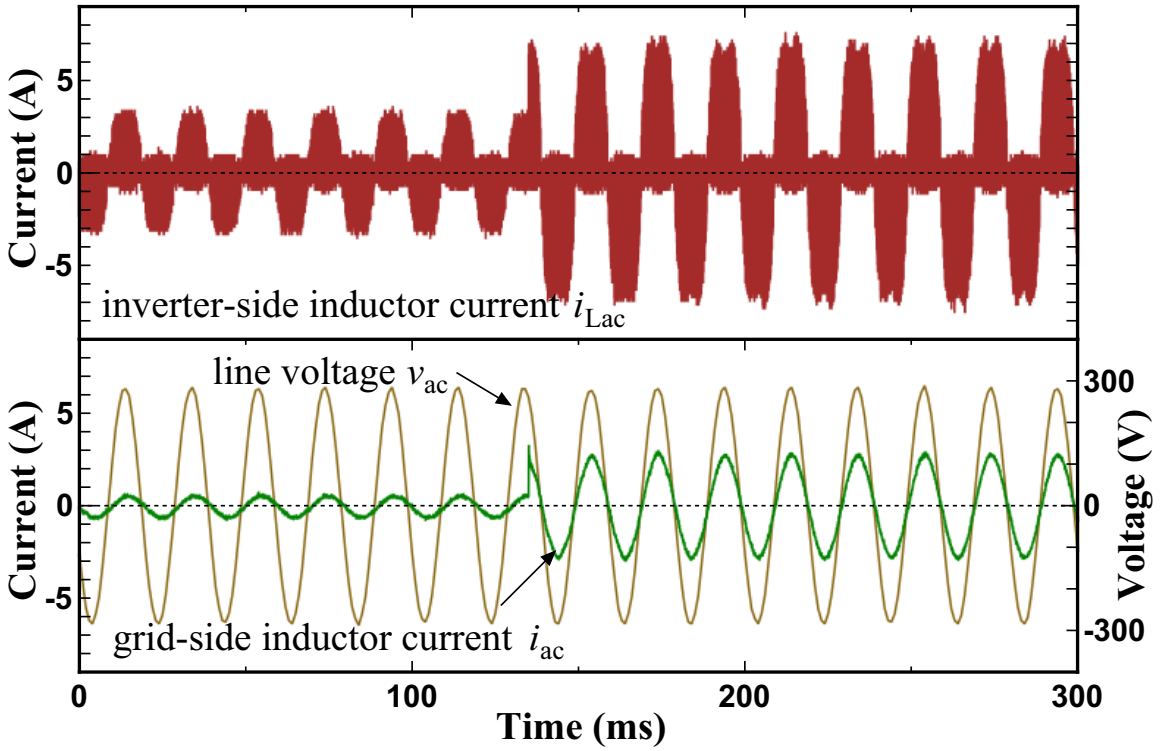

Fig. 4.70 Experimental waveforms of current response to the step-up change of reference current from 20% to 100% in line cycles view.

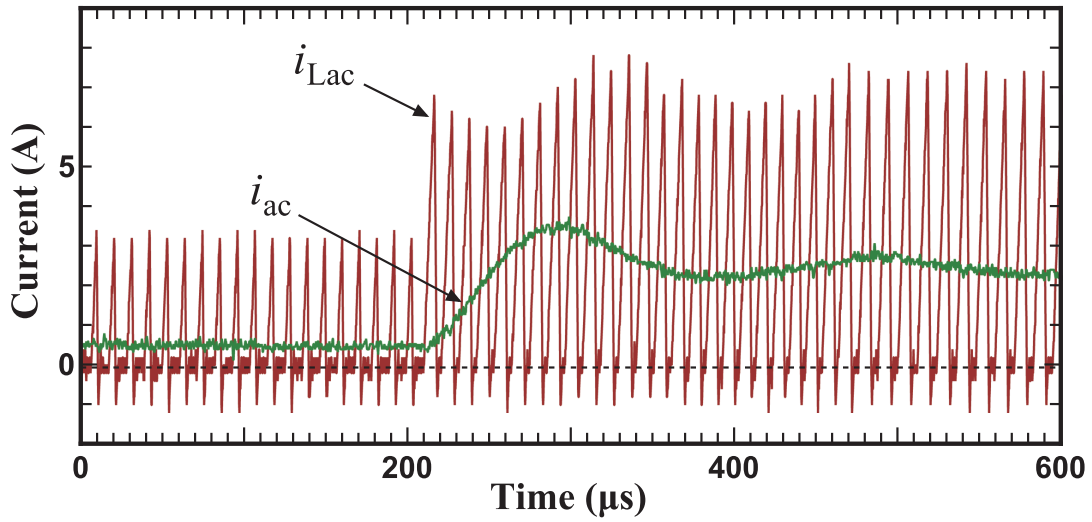

Fig. 4.71 Experimental waveforms of current response to the step-up change of reference current from 20% to 100% in switching cycles view.

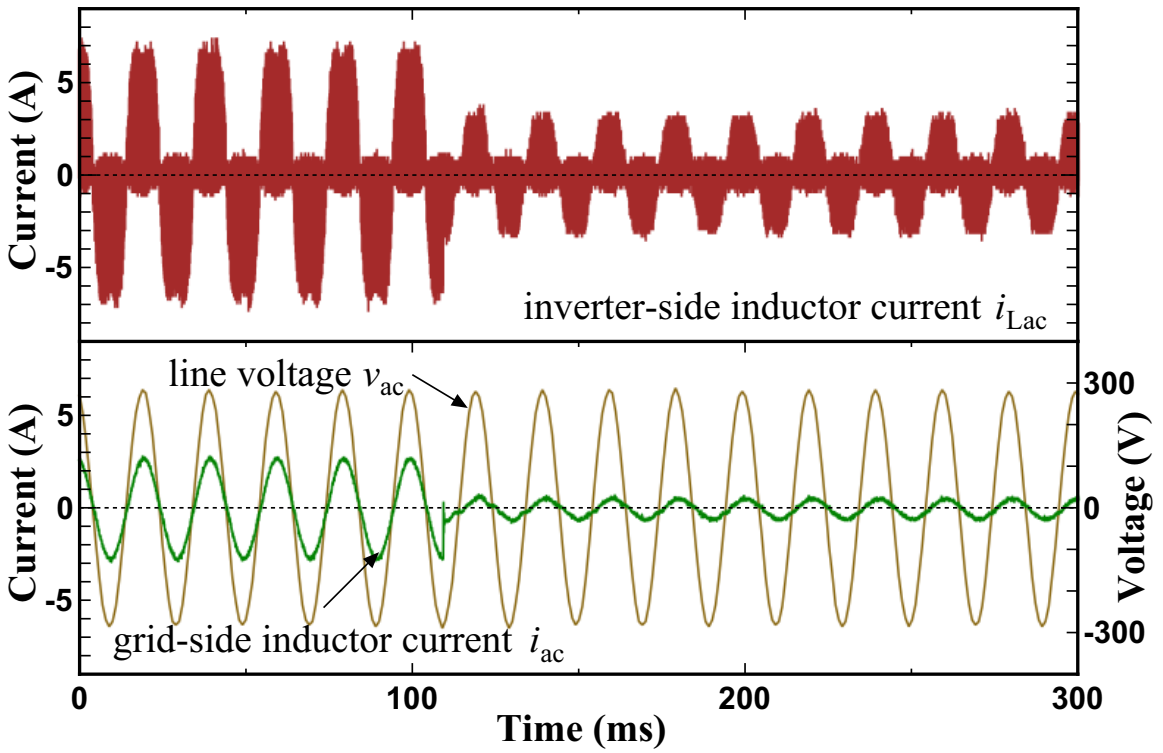

Fig. 4.72 Experimental waveforms of current response to the step-down change of reference current from 100% to 20% in line cycles view.

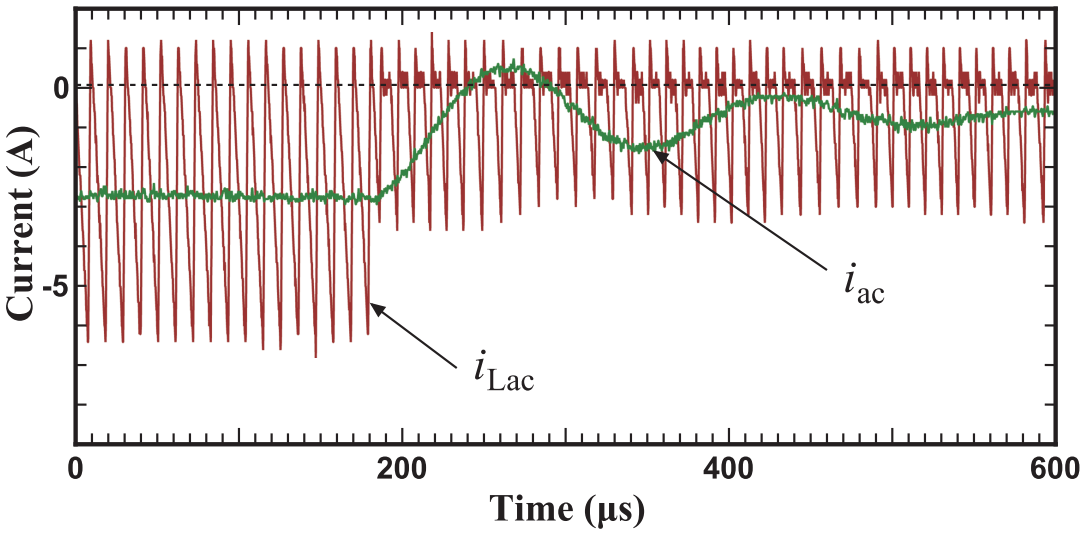

Fig. 4.73 Experimental waveforms of current response to the step-down change of reference current from 100% to 20% in switching cycles view.

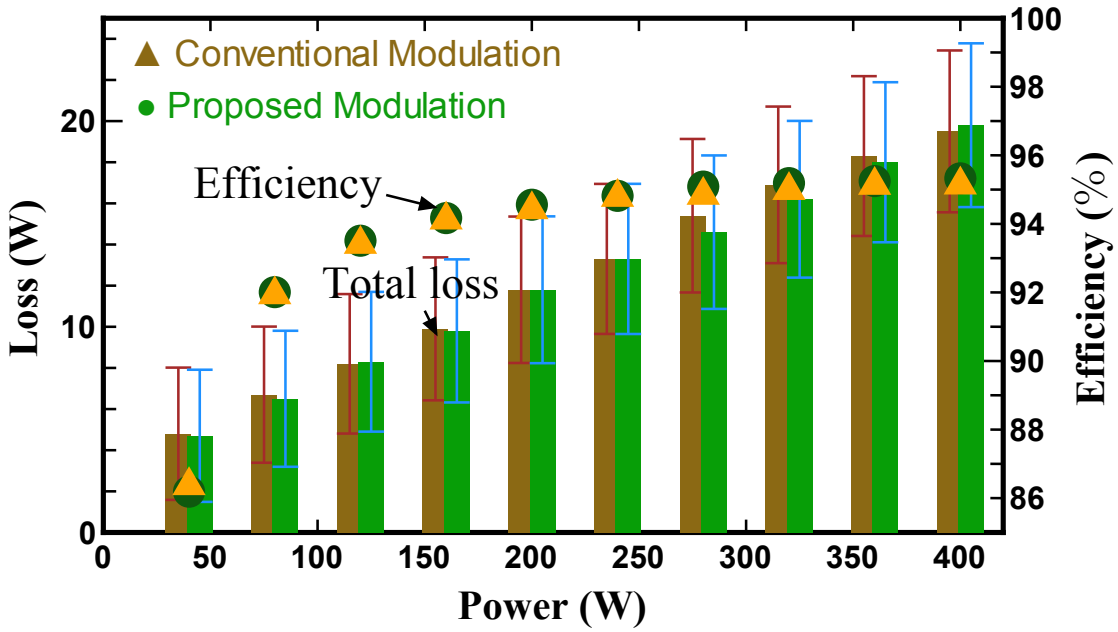

Fig. 4.74 Measured efficiencies and total losses as function of the output power.

changes; on the other hand, i_{ac} could not respond as fast as i_{Lac}. In the experiments, it was observed that the oscillation of i_{ac} decayed soon after the step change. The fact indicates that the parasitic resistance in the fabricated converter was sufficiently high to avoid the problems caused by the oscillation.

Efficiency Analysis

The efficiencies and total losses are shown in Fig. 4.74. The measurement was conducted by using a digital power meter (YOKOGAWA WT-1600). The range of measurement for DC input was 600 V/2 A and 300 V/5 A for AC side. The maximum errors of reading and measurement were calculated based on this condition, and the error bars are added. Almost the same efficiencies between the two modulations were obtained. Fig. 4.75 shows an estimation of loss break-down when $I_{ac.set} = 1.85$ A (in order to make a comparison with previous modulation with TPCM). It was similar with the results shown in Section 4.3.5, the unknown losses were high, and this could be caused by the large parasitic capacitance of semiconductor device. The conduction and turn-off losses in the proposed modulation

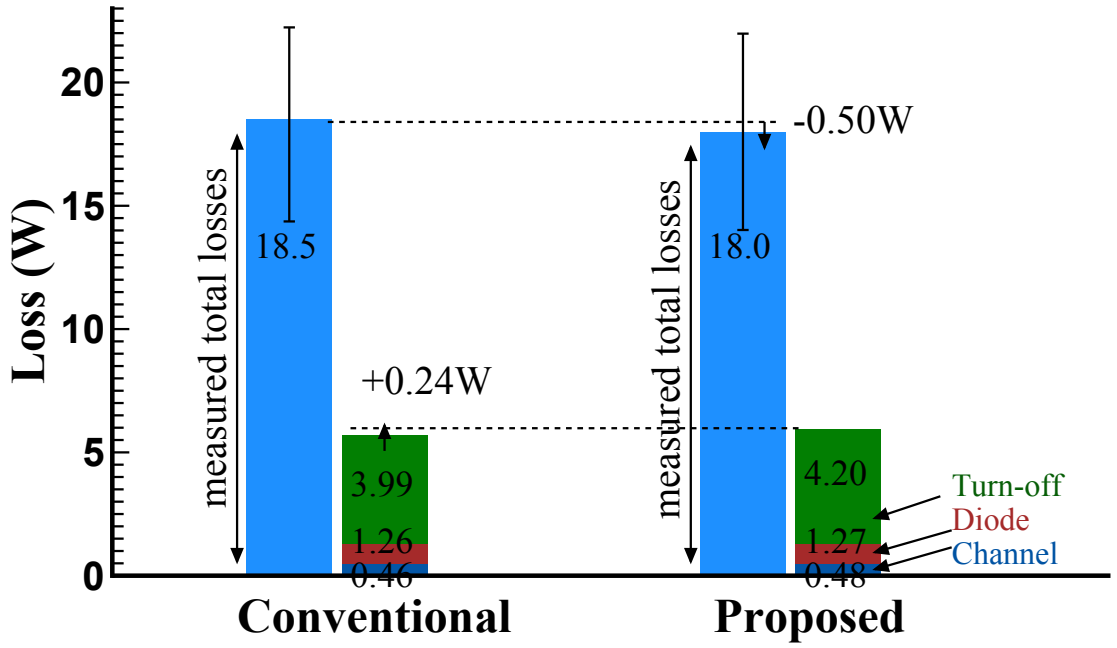

Fig. 4.75 An estimation of loss break-down for conventional and proposed modulations when $I_{\text{ac.set}} = 1.85$ A.

increased slightly in comparison with those in the conventional modulation. This can be caused by the increased inductor peak current, as discussed in previous sections. In addition, the inductor losses can also be increased due to the increased inductor peak current. The proposed modulation can achieve ZVS turn-on. Therefore, the reduction in total losses could be caused by the effect of ZVS turn-on. However, it is not obvious since the conduction losses, turn-off losses and inductor losses are increased. Nevertheless, it is difficult to discuss the effect of ZVS further since the difference in between two modulations are relatively small in comparison with the error bar.

4.5 Conclusion

With wide band-gap semiconductor devices, grid-tied inverters can be operated at relatively high frequencies to achieve the volume reduction of passive components. The DCM can be considered as a promising design for low-power grid-tied inverters for the purpose of

further reduction of the inductor volume. The model-based control can be applied and it is advantageous to the control of the grid-tied inverters operated in the DCM with further high switching frequency, because the highly rippled and high-frequency inductor current is not required to be sensed. However, the conventional DCM modulation cannot achieve the uniform turn-on; therefore, it can generate high-order harmonic distortions in the output current. The high-order distortion is caused by the resonance between inductor and parasitic capacitors of switching devices. Two modulations together with an improved DCM model that considers the resonance are proposed to reduce the high-order harmonic distortions.

The first modulation is based on the TPCM with constant frequency. Different combination of duty ratios can be used to change the length of resonance current period. Therefore, the uniform turn-on for the corresponding switches can be achieved. The use of TPCM can reduce the peak inductor current and turn-off losses, however, it has an upper limit of the switching frequency to improve the current distortion effectively for given device parasitic capacitance.

The second modulation is based on conventional DCM with variable frequency. The proposed method can always achieve the uniform turn-on for the switches by expanding the switching periods, and that leads to the reduction of the harmonic distortion. This method can remove the trade-off relationship between switching frequency and parasitic capacitance. However, the increased peak inductor current can still affect the converter design.

In general, semiconductor devices with low on-state resistance, which can easily be achieved by increasing the chip area, can improve the efficiencies; however, a trade-off between the parasitic output capacitance and the on-state resistance exists. In the conventional DCM operated with the feed-forward current control, the trade-off relationship limits the maximum switching frequency due to the generated current harmonics. This trade-off can be eliminated by the proposed modulations shown in this chapter. Higher switching frequency for a given device can be selected, or the conduction loss can be reduced by selecting high-

current devices while the switching frequency is maintained high. Therefore, improvement in the trade-off between loss and power density can be expected.

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Chapter 5

Conclusion

5.1 Summary of Dissertation

The photovoltaic system have received more and more attentions in recent years due to the increasing demand for clean energies. The operation of such systems do not generate pollution and greenhouse gas emissions, therefore they can be considered as one of the promising power generation systems that to replace the conventional ones. With the continuous increasing of residential market of PV applications, demands for grid-tied inverter with relatively low power ratings has been rapidly increased. A new concept of low-power grid-tied inverters, which is referred to as AC module or micro-inverter, has been proposed and gained more and more attentions. For such an inverter, the reduction on the manufacturing cost is of importance in order to be mass produced. The techniques of minimizing the grid-tied inductors play an important role in micro-inverters.

Generally, high frequency operation can be used to reduce the volumes of inductors. However, the use of conventional power devices, such as Si-IGBTs, Si-MOSFETs or Si-SJ-MOSFETs can degrade the performance of inverter, particularly under high frequency operations. With the development of WBG power devices, higher performance can be achieved by adopting such devices, even under higher switching frequencies. However,

control of a grid-tied inverter under extremely low inductance can be a challenge with conventional CCM design. To address this problem, the converter can be designed to operate in BCM or DCM.

In Chapter 2, the current control strategies of grid-tied inverters operating in CCM, BCM and DCM are reviewed and compared. The hysteresis control and linear control are the well established strategies for CCM grid-tied inverter. The hysteresis current features simple control and implementation. However, the wide variation and high switching frequencies make it not suitable for low-power applications. The linear PI control is a feedback control strategy that based on the errors. However, the current control can be highly difficult under extremely low inductance conditions. Therefore, the low inductance cannot be achieved with such control strategy.

On the other hand, the number of researches on BCM control for low-power grid-tied inverters have been increased in recent years. For BCM control, the current control strategies are usually based on hysteresis control or model-based control. The low inductance can be used since the control is not error based. However, the current controls of BCM rely on the detection of current of inverter-side inductor, which can be a challenge especially under high frequency operations. Further more, the wide variation of switching frequencies can also result in too much turn-off and inductor losses at low-power levels. Consequently, the BCM is also not the best choice for high frequency designed inverters.

For DCM, the linear control and model-based control can be applied to as the current control. It is pointed out that the DCM design with model-based control is the most advantageous and suitable one for grid-tied inverters, for the purpose of high frequency operation. By applying such control strategy, the extremely low inductance can be used and the current detection for inverter-side inductor is no longer required. However, the current distortions can be generated with an imperfect model being used. The model-based controller unable

to correct the control errors, since is based on the feed-forward control. This makes the model-based control sometime impractical for grid-tied applications.

In order to eliminate the current distortions, several approaches are proposed. A partial feedback control is introduced to the model-based controlled DCM inverter. The concept is to feed back the errors that exist between the output and reference current to the model-based controller. An application of this partial feedback control regarding to the elimination of low-order harmonics is presented and discussed. Through this kind of partial feedback control, the low-order harmonics in the output current can be eliminated adaptively.

In Chapter 3, a hybrid switching scheme that combines the scheme of conventional bipolar DCM and asymmetry unipolar DCM is proposed. The proposed switching scheme is named as TPCM in accordance with the shape of inductor current. The TPCM features high control degree of freedom. This allows the operation mode of converter to be shifted freely from bipolar DCM to asymmetry unipolar DCM, and vice versa. A modulation is also proposed to reduce the peak inductor current and address problem of zero-crossing distortion. The operation mode is controlled to be bipolar DCM around zero-crossing areas in order to avoid the zero-crossing distortion; and the operation mode during other switching cycles is controlled to be asymmetry unipolar DCM. The experimental results demonstrate that the proposed modulation has higher efficiencies than the bipolar DCM, meanwhile, without zero-crossing distortion in comparison with the asymmetry unipolar DCM.

Chapter 4 discusses the effect of resonance caused by the parasitic capacitance of switching device on the output current. The impacts of this resonance can no loner be neglected when a DCM grid-tied inverter is operated at high frequencies. The conventional DCM modulation suffers from the current distortions due to the problem of resonance. For a given switching device, the switching frequency has to be reduced to maintain a relatively low distortion of output current. However, this is in conflict with the volume reduction of inductors. To address this problem, an improved model that considers the resonance is

analyzed; and two modulations based on this model are proposed to achieve the uniform turn-on and reduce the high-order harmonic distortions.

The first modulation is based on the TPCM with constant switching frequency being applied. The length of the resonant current period is controlled to achieve uniform turn-on by means of different combinations of duty ratios. The proposed modulation is verified by experiment with a SiC-MOSFET based prototype and a GaN-HEMT based prototype. The experimental results confirms the effectiveness of harmonic reduction with the proposed methods. The TDDs of output current can maintain below 5% even with large parasitic capacitance of switching device being applied. The efficiency of converter at rated power operation is also improved almost by 1% with the proposed modulation. It is shown that the design of switching frequency with proposed modulation can be increased to a higher level in comparison with that with conventional one. However, an upper limitation of switching frequency still exists and it affects the further volume reduction of inductors.

The second modulation is based on conventional DCM with variable switching frequency. The switching period is controlled to terminate the oscillating current. By doing this, the trade-off between switching frequency and parasitic capacitance can be totally removed. However, the trade-off between peak inductor current and parasitic capacitance can still influence the system design. The superior performance on harmonic reduction of the proposed method is verified by both simulation and experiment analysis. The THD of output current is reduced from 8.8% to 1.0% at rated power operation and from 12.7% to 4.4% at low-power operation. Both THD and TDD of output current can maintain below 5% without worsening the efficiencies under this design specification.

5.2 Achievements and Contributions

With WBG devices, high frequency operation becomes possible and it is preferred for the purpose of inductor volume reduction. To reduce the volume of inductor further, the DCM design can be a good candidate. The model-based feed-forward control can be advantageous for DCM in comparison with the conventional feedback control. However, the drawback is that the harmonic distortion cannot be eliminated. This drawback makes the DCM impractical for grid-tied inverter applications since the harmonics should meet the grid standards. In this dissertation, problems of DCM grid-tied inverters operating at high frequency, which are the method of current control, the reduction of harmonic distortion and the achievement of soft-switching, are studied, and the solution to the corresponding problems are proposed.

In can be concluded that the converter cannot be designed to operate at high switching frequency with conventional model-based controls, such as average current control, variable peak current control or dual-mode control, in order to avoid current distortions, particularly the high-order harmonic distortions. Consequently, volume reduction of grid-connected inductors can be restricted due to this reason. The high-order harmonic distortions can be avoided if the peak values of inverter-side inductor current are well controlled (i.e. in this case, the peak inductor currents are not affected by the non-uniform turn-on and so do the average current). Therefore, the design possibilities can be expanded with peak current control being applied, e.g. constant peak current control. However, the requirement of detecting the triangular inductor current can be a challenge, as discussed in previous sections. The detection of inductor current can be sensitive to switching noises and delay problems. Consequently, the designed switching frequencies (therefore volume reduction) also has an upper limitation.

Another shortcoming of a grid-tied inverter with DCM design is the higher peak current and resulted higher conduction losses in comparison with that in the grid-tied inverter with conventional CCM design. In order to reduce the conduction losses and improve the converter

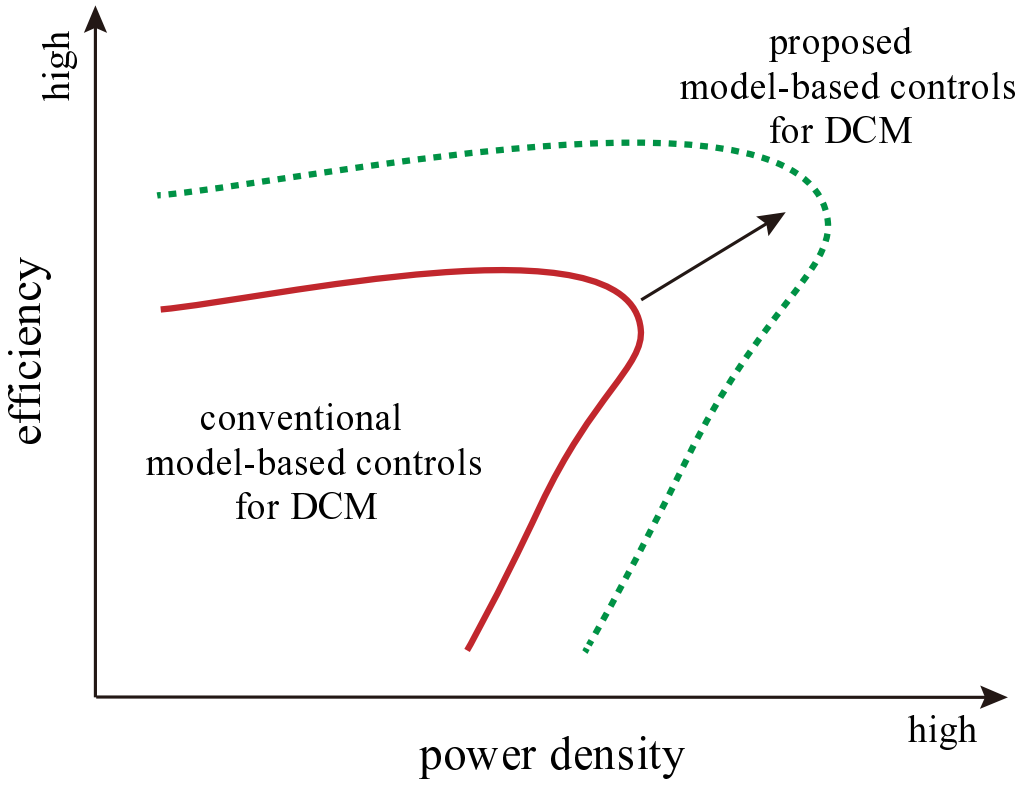

Fig. 5.1 Pareto fronts with respective to efficiency and power density of a DCM grid-tied inverter with conventional and proposed model-based control strategies.

efficiencies, devices with lower on-stare resistance are preferred. However, the trade-off relationship between the device on-state resistance and parasitic output capacitor is the factor that limits the use of such devices, because the turn-on losses and total harmonic distortions can be even worse. This trade-off relationship also limits the design and efficiency improvement for the DCM grid-tied inverter. Consequently, the design possibilities can be narrow if the conventional control methods are adopted as the control strategy for low-power DCM grid-tied inverters.

Fig. 5.1 depicts an image of improvements that can be obtained by adopting the proposed model-based controls. The improvements are evaluated in terms of efficiency and power density, and it is also known as Pareto fronts. When the DCM grid-tied inverters are designed with conventional controls, the switching frequency should be low and the switching devices with relatively high on-resistance should be selected, in order to keep relatively low harmonic

distortions. The distortion problems can be addressed by means of different modulations being proposed. Therefore, design possibilities are wider than that with conventional DCM controls. By adopting the modulation methods proposed in this dissertation, the control of a DCM grid-tied inverter without sensing the high frequency current can be realized, the harmonic problems can be addressed even under higher switching frequency conditions and the trade-off relationship can be expanded or even removed. This contribution allows a DCM grid-tied inverter to be designed with high switching frequencies, so that the realization of a reduced volume of inductor can be achieved. Further more, the designs of DCM grid-tied inverters can be more flexible, so that the realization of a more efficient converter can be achieved. Therefore, the Pareto fronts are possible to be moved from the solid-line curve (when conventional controls are adopted) to the dash-line curve (when the proposed controls are adopted).

This dissertation offers an insight into the control methods for high frequency DCM grid-tied inverters. With the control and modulations proposed in this dissertation, the use of high frequency DCM for low-power grid-tied inverter applications becomes practical. With WBG devices and the proposed DCM controls, the converter can be designed with higher switching frequencies, higher efficiencies and lower harmonic distortion in comparison with the conventional one. Therefore, the realization of a grid-tied inverter with higher power density, efficiency becomes possible.

5.3 New Insights and Future Works

This dissertations discusses the model-based controls for DCM grid-tied inverters to achieve reduction of harmonic distortions. The effectiveness of the proposed methods are validated by experimental results. It is shown that the harmonic distortions are no longer problems with the proposed controls being applied to the DCM grid-tied inverters. However, some works are still required to be further elaborated in order to meet other requirements given by the grid requirement.

5.3.1 Non-Unity Power Factor Operations

The proposed modulations and experimental verification shown in this dissertation are based on unity power factor operation. Recently, grid-tied inverters with reactive injection abilities are required. One problem of the DCM can be the peak inductor current that being increased under non-unity power factor operation. This can cause saturation of the inductor core. In order to avoid saturation, the inductor should be designed with a larger volume.

In this dissertation, a modulation with TPCM to achieve peak current reduction is shown in Chapter 3; a modulation with TPCM and a modulation with bipolar DCM for the purpose of harmonic reduction are shown in Chapter 4. It is possible to combine the three individual concepts together, e.g. TPCM with variable frequency operation or DCM with peak current control and variable frequency. It is also interesting to use the proposed method or the combination of proposed concepts to realize optimal operation under non-unity power factor operation.

5.3.2 Capability of Low Voltage Ride Through

This dissertation discusses about model-based controls for DCM grid-tied inverters. In the model-based control, it is suggested to measure the DC-link voltage and grid-voltage and used

their values for duty calculation in order to address the problem of low-order harmonics. By measuring the grid voltage, it is possible to provide the capability of low voltage ride through (LVRT), if the control frequency is synchronized with the switching frequency. However, One drawback of the model-based control is the relatively long computation times in comparison with that of classic CCM controls. The capability of LVRT may not be satisfied if the required computation times are longer than one switching period with the increasing of switching frequency. The LVRT capability requires the grid-tied inverter to operate continuously when the voltage of electrical grid drops. However, over current protection can be triggered if a suddenly drop of grid voltage occurs, particularly in the case of the control frequency being much lower than the switching frequency (e.g. MHz operation). Consequently, the grid-tied inverter can be forced to stop, which is conflict to the requirement of LVRT capability. In order to address this problem, the duty should be corrected as fast as possible to prevent the current from overshooting.

Appendix A

Experimental Verification of Low-order Harmonic Compensation

The experimental verification of low-order harmonic compensation using partial feedback control is presented in this Chapter. The simplified structure of the system of a single-phase grid-tied inverter with model-based control is shown in Fig. A.1. In this experiment, the DC voltage was supplied from a DC power source. The AC voltage was supplied from an AC power source with parallel connected linear resistor. The capacitor voltage was measured and the values are used in the duty calculation as the AC reference. The experimental conditions and circuit parameters are the same as that shown in Chapter 3 and are listed in Table A.1. In this experiment, the conventional bipolar switching scheme and its modulation for DCM was considered. Two resonant controllers that being tuned at 3ω and 5ω were used to eliminate the high third and fifth order harmonics. The current reference was generated and synchronized in phase with the line voltage through a digital phase-locked-loop (PLL). All of the programs were implemented in a digital signal processor (DSP) (TMS320F28377S 200MHz).

The experimental waveforms of grid-side inductor current, i_{ac}, and line voltage, v_{ac}, under rated current operation, without and with partial feedback control are shown in Fig. A.2

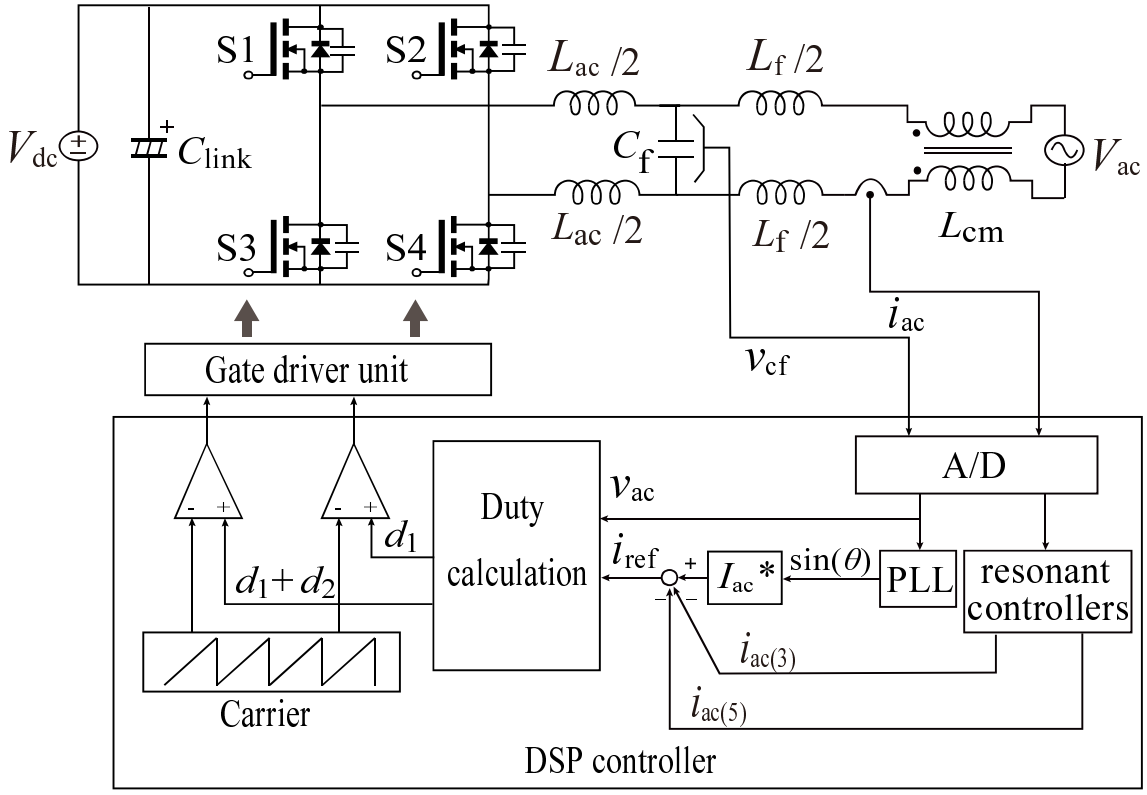

Fig. A.1 Simplified structure of the fabricated single phase grid-tied inverter system.

Table A.1 Circuit Parameters and Conditions

DC link voltage	V_{dc}	400 V
AC voltage	V_{ac}	200 V
Rated current	$I_{ac.rated}$	2.4 A
Switching frequency	f_{sw}	100 kHz
Digital controller	DSP	TMS320F28377S
Switching device	SiC-MOSFET	SCT2160KE

LCL Filter Design		
Inverter-side inductance	L_{ac}	119 μH
Percentage impedance of L_{ac}	$\%X_{Lac}$	0.045%
Grid-side inductance	L_f	125 μH
Percentage impedance of L_f	$\%X_{Lf}$	0.047%
Capacitance of filter capacitor	C_f	2.2 μF

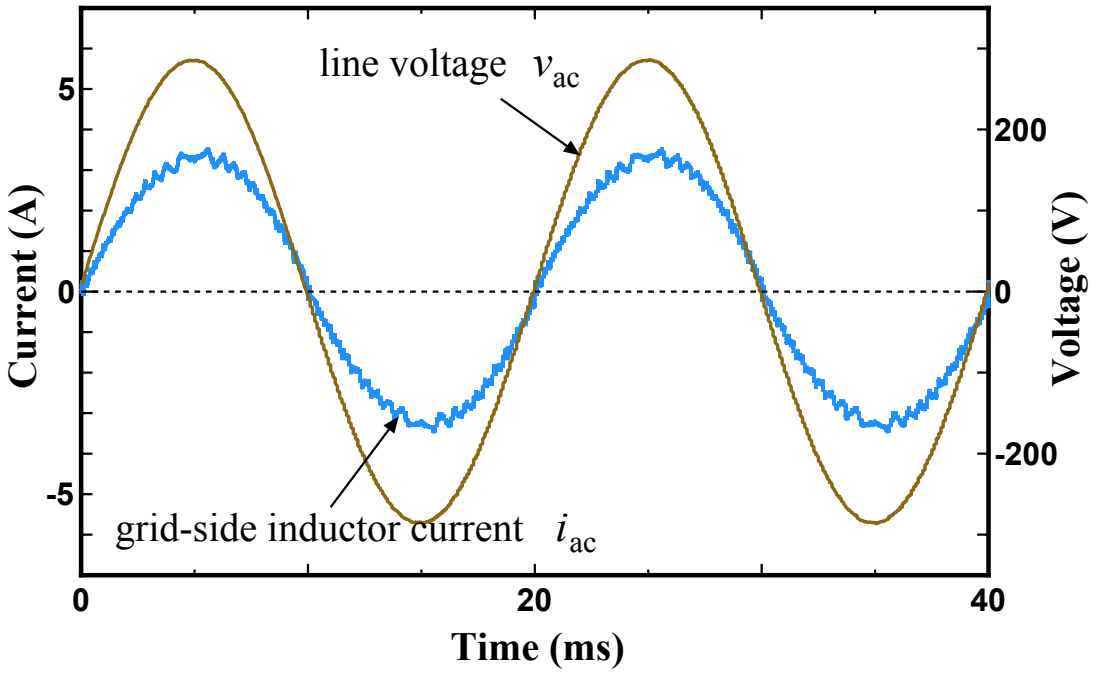

Fig. A.2 Experimental waveforms of grid-side inductor current, i_{ac}, and line voltage, v_{ac}, under rated current operation without partial feedback control.

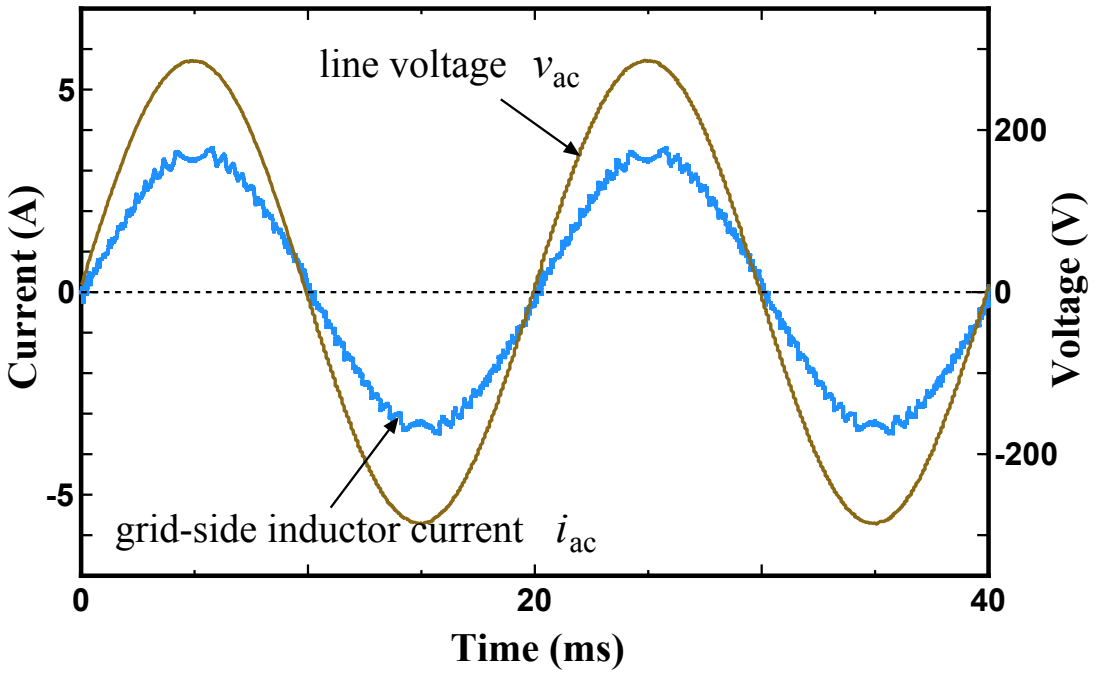

Fig. A.3 Experimental waveforms of grid-side inductor current, i_{ac}, and line voltage, v_{ac}, under rated current operation with partial feedback control.

and Fig. A.3, respectively. The harmonic components in the gird-side inductor current, i_{ac}, were calculated by means of discrete Fourier transform (DFT). The calculated results of harmonic components are shown in Fig. A.4. It was obtained that third and fifth harmonics were high with conventional control structure and they were effectively eliminated after the partial feedback control was applied. The THD of i_{ac} was reduced from 4.8% to 3.0%. The effectiveness of the low-order harmonic compensation was verified by this experiment.

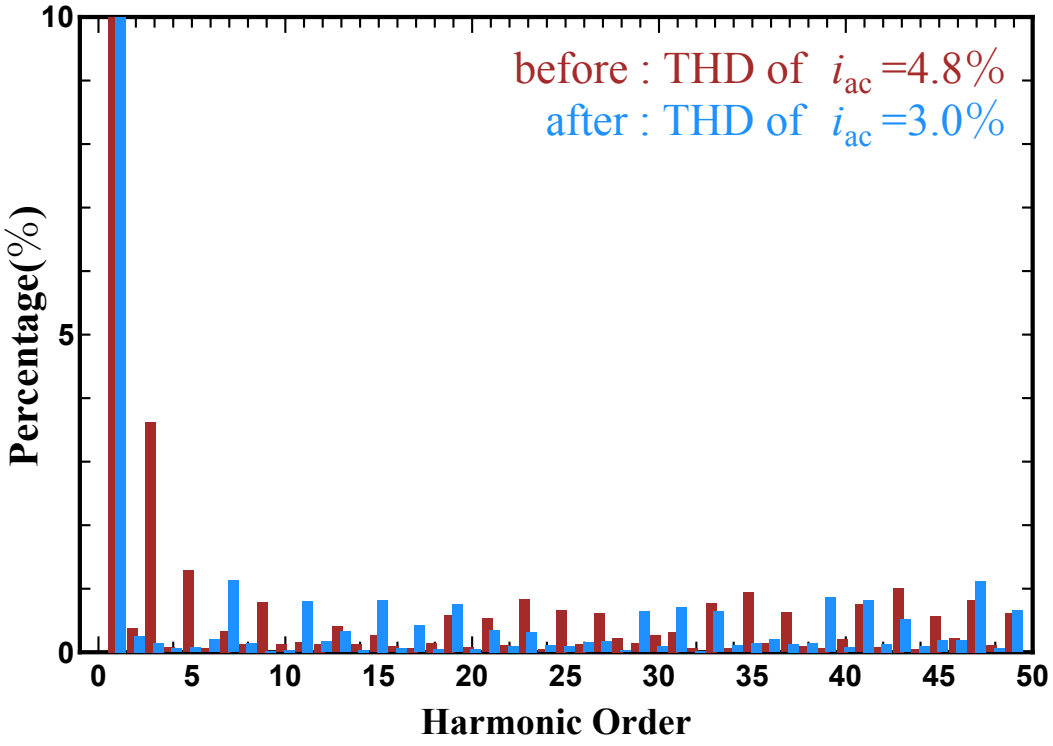

Fig. A.4 Harmonic components comparison for rated current case.