Silicon Nanostructures and their Application in Radial Junction Solar Cells

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Abstract

In recent years, to solve the problem of the traditional c-Si solar cell, many novel structures and materials have been investigated. Si nanostructures have shown potential for solar cell applications due to the unique optical, electrical and extraordinary surface-area-to-volume properties. Several methods have been reported to form different nanostructures, such as nanowires, nanopillars, nanopencils, and nanotips.

There are two key strengths of nanostructures. First, the nanostructure effectively enhances light absorption. Absorption losses for traditional solar cells are divided into reflection and transmission losses. Thus, an antireflection layer and a thick substrate are needed for the conventional bulk c-Si solar cell, which increases device fabrication costs (extra materials). However, the nanostructured solar cell's light-trapping effect extremely increases the absorption. Second, the radial p-n junctions in the nanostructure provide a short carrier collection path which especially benefits rapid charge separation and efficient carrier collection. These two major benefits of nanostructured solar cells suggest exciting possibilities for low costs and good efficiency. Despite the advantages of Si nanostructure solar cells, industrialization is still at an early stage due to high surface recombination over large areas, a need for better morphology control, rudimentary fabrication methods and relatively low efficiencies. There is still a lot of work needed to do, but rapid improvements in recent years certainly indicates potential in the future.

The purpose of this thesis is to find new phenomena and novel ways to enhance the advantages of silicon nanostructures for solar cell application in simple and feasible paths.

We first investigated the fabrication and optimization of different Si nanostructures, as well as their applications for next-generation solar cell devices. We hoped to achieve a higher short-circuit current-density by optimization of the Si nanostructures morphologies for better anti-reflection property. A novel metal electrode method using a micro-grid pattern has also been developed for lower reflection and better carrier collection.

Moreover, we attempted to find some new phenomena and novel ways of using quantum dots for photovoltaic devices. Quantum dots are able to absorb the high energy photons in the low wavelength range due to quantum confinement, which makes it possible to overcome the Shockley–Queisser limit of the traditional solar cell. Because a non-radiative energy transfer process occurs between the quantum dots and Si nanostructure surface, the energy transfer rate is much higher than through the radiative energy transfer, based on our group's previous work. Thus, non-radiative energy transfer of the quantum dots become an extra and fast energy transfer channel to increase the light-generated

carriers for a solar cell device.

Finally, we investigated the hybrid heterojunction solar cell devices combined with the contractive polymer of PEDOT: PSS and Si nanostructure. It has the potential to become a low cost and high-performance device due to its low energy-intensive fabrication process. In addition, high energy transfer efficient Si nanocrystal quantum dots were studied by changing the passivation ligand in the quantum dot surface. This was successfully applied to a photovoltaic device to achieve a higher short-circuit current density.

All these studies are helping to pursue additional insight and solutions to society's current energy problems by overcoming the limitations of traditional solar cells by nanoscale structures.

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Chapter 1. Introduction

1.1 Background

When the 'Industrial Revolution' occurred, human beings achieved rapid development of science and technology. [1,2] It is primarily by the large-scale using of non-renewable fossil fuels such as oil, coal, and natural gases. However, resource depletion is now a potential threat to human society, because of the mass consumption of fossil fuels. The reserve-production ratio indicates it is possible that coal and oil will deplete in about 120 and 50 years, respectively. In view of future increases in energy consumption, this prospect is increasingly serious. [3] In addition, carbon dioxide (CO_2) and other greenhouse gas concentrations have been steadily increasing due to the mass consumption of fossil fuels. [4,5] As a result, the rapid growth in emissions of greenhouse gases has led to an increase in global average surface air temperatures. Therefore, it is necessary to look for new types of energy production. Non-fossil fuel energy sources (solar, wind, nuclear, etc.) are attracting more and more attention as potential methods of slowing or halting global warming, of which solar energy has seen the fastest development in recent years. [6–8] As an attention-getting candidate solar energy which includes some outstanding merits such as no gas emission, endless and environment-friendly.

The solar cell is a device that utilizes the photovoltaic effect of semiconductors to convert solar energy directly into electricity. [9,10] At present, the rising expectations of suppressing greenhouse gas emissions have led to solar cells attracting a lot of attention culminating in solar cell systems increasing in terms of investment and growth, with the photovoltaic installations having expanded a 97 GW in 2017. [11]

1.2 Basic theory of solar cells

A solar cell is an electronic device that directly converts sunlight into electricity by the photovoltaic effect. Sunlight irradiated on the solar cell to produce both current and voltage to output the electrical energy [12,13]. The process is indicated in Figure 1.1, which first requires the material can absorb the sunlight and raises an electron to a higher energy state. Secondly, the movement of the high energy electrons from the solar cell to an external circuit. Finally, the electron then dissipates its energy in the external circuit and back to the solar cell. There are varieties of materials that can potentially meet the requirements of the conversion of solar energy, but in practice, almost all photovoltaic energy conversion using semiconductor materials in the form of a p-n junction.
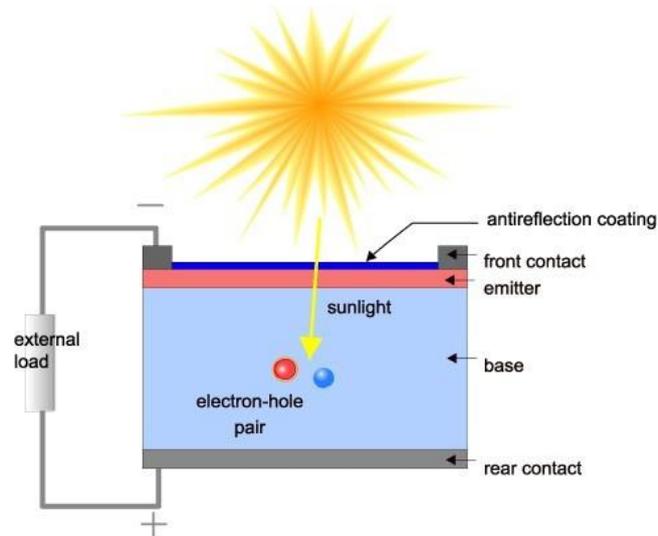
Figure 1.1 Schematic of a solar cell device in a cross-sectional view.

[Source: http://pveducation.org/pvcdrom/solar-cell-structure]

Generating a current in the solar cell, known as "photo-generated current", includes two main processes, shown in Figure 1.2 of the band diagram under short circuit conditions[14,15].

The first process is the creation of electron-hole pairs by the absorption of the incident photons. Electron-hole pairs are generated in the solar cell on the condition when an incident photon has higher energy than the bandgap. However, in general, the electrons (p-type material) and holes (n-type material) are meta-stable, and these will only exist for the time equal to the lifetime of minority carriers before they recombine. If the carrier recombines, the generated electron-hole pairs by light will be lost and don't obtain any current or power.

The second process, the collection of these carriers through the p-n junction, prevents this recombination with a p-n junction spatial separation of the electron and the hole. The carriers are separated by the action of the electric field at the p-n junction. When the photo-generated minority carriers reach the p-n junction, it is about the connection by the electric field at the junction where there is now a majority carriers' stroke. If the emitter and the base of the solar cell are connected to each other (when the solar cell is short-circuited), the photo-generated carriers flow through the external circuit.
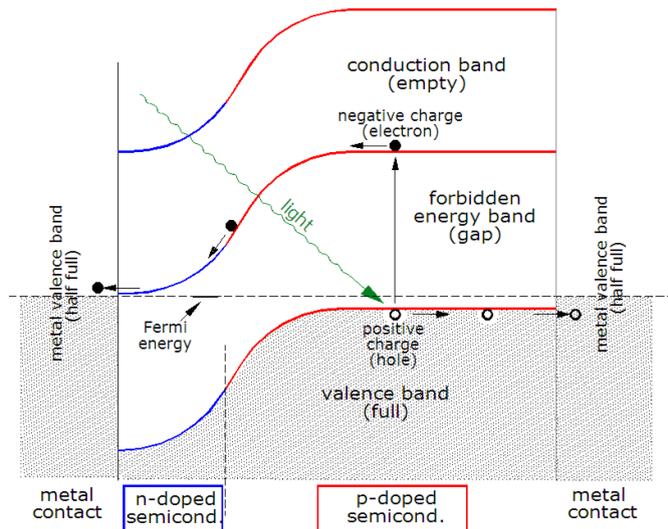
Figure 1.2 Band diagram of a silicon solar cell, under short circuit conditions.[15]

When sunlight illuminates into the solar cell, it generates a photo-current. The total current in the circuit can be described as below:

$$J = J_L - J_0 \left[\exp\left(\frac{qV}{nKT} \right) - 1 \right] \qquad \text{1-1}$$

J_L is the photo-generated current, J_0 is the junction saturation current, q is electron unit charge, n is the ideality factor, k is Boltzmann constant and T is the junction temperature (degrees Kelvin). The J-V curve of a solar cell in Figure 1.3 indicates that it is the superposition of the J-V curve of the solar cell diode in the dark with the photo-generated current. [10] Illuminating a cell adds to the normal "dark" currents in the diode.
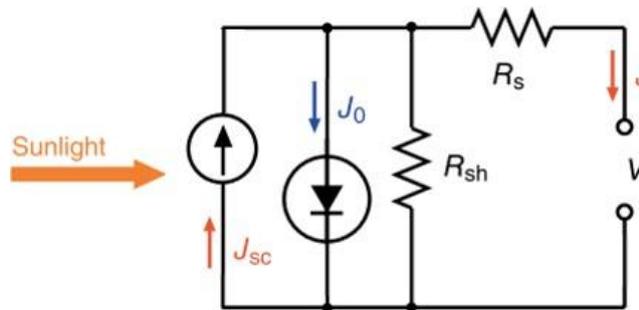
Figure 1.3 Electronic circuit of the solar cell system. [12]
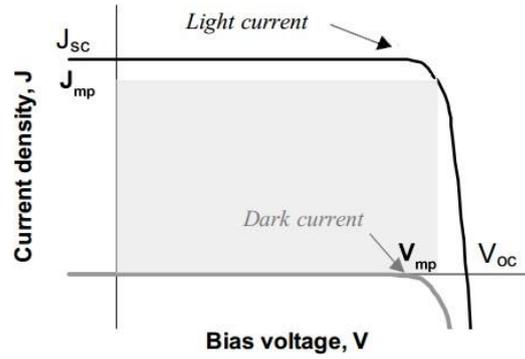
Figure 1.4 J-V curve of the solar cell in dark and light conditions. [12]

If the load has a large endless and opened resistance, the open-circuit voltage V_{OC} is a voltage between the terminals of the solar cell under standard illumination conditions. In this situation, when the current is zero, the open-circuit voltage can be estimated as

$$V_{OC} \approx \frac{nKT}{q} \ln \frac{J_L}{J_0} \qquad \text{1-2}$$

If the load has a zero resistance, short-circuit current J_{SC} is a current of the solar cell under standard illumination conditions. In this case, when the voltage is zero, the short-circuit current J_{SC} equal to the photo-generated current.

$$J_{SC} = J_L \qquad \text{1-3}$$

Because of the Power $P = JV$. The maximum output is determined by the condition

$$P_{MAX} = J_{MP} V_{MP} \qquad \text{1-4}$$

The fill factor is defined as:

$$\text{FF} = \frac{P_{max}}{J_{SC} V_{OC}} = \frac{J_{MP} V_{MP}}{J_{SC} V_{OC}} \qquad \text{1-5}$$

FF is a coefficient indicating whether the angular extent characteristic curve of the solar cell, which means that it is an excellent solar cell when it close to 1.

The first significant factor of the solar cell is the energy convention efficiency. It is described as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\text{FF} \times J_{SC} \times V_{OC}}{P_{in}} \qquad \text{1-6}$$

The input power is from the sunlight, and output is the electricity generated by the solar cell. Thus, high efficiency is pursued, by achieving high FF, J_{SC} and V_{OC}.

1.3 The varieties of solar cells

The solar cell is a power device that utilizes the photovoltaic effect of the semiconductor to converts solar energy directly into electricity.[16–22] Currently, the most widely used Si solar cells were first invented at Bell Labs in 1954. This device was called the Bell Solar Battery. The energy conversion efficiency of this time was 6%.[23,24] In the 1960s, Si solar cell main had been used limited for the satellite power.[25] However, in the wake of the oil crisis of 1974, developed Si solar cells as power had been started in earnest.[26] When it comes to the 1980s, solar cells began to apply to consumer equipment and remote location powers widely.[19,27]

There is a wide variety of applications in solar power, such as artificial satellites, street lights, emergency power, and portable power. At present, rising expectations of suppressing carbon dioxide emissions. This is about 60% greenhouse gas due to carbon dioxide emission, which may be the cause of global warming problems, about 80% of them are because of the consumption of fossil fuels. [7,28]

Bulk solar cell

In the bulk type solar cell, there are single-crystal Si solar cell and the polycrystalline Si solar cell crystal Si-based and III-V compound semiconductors such as GaAs or InP. [27,29–31]

Single-crystal Si solar cell is capable of large minority carrier's diffusion length, which benefits to produce a high-efficiency solar cell. In contrast, the polycrystalline Si solar cell is lower conversion efficiency than the single-crystal Si solar cell while it is advantageous in the inexpensive production than single-crystal Si solar cell.[32–35]

Also, the III-V compound solar cell is attracting attention as a material system with a very high conversion efficiency of 30-40%. However, due to the high substrate and process costs, it is mainly used in space applications.[36,37]

Thin-Film solar cells

The thin-film solar cell, the thickness of a semiconductor layer in the solar cell, is about several μm.[38–41] The feature of the thin-film solar cell, since the light absorption coefficient of the material is large, as compared to the bulk type solar cell, the light absorption layer can be thin, and that it is possible to reduce the material cost. These thin-film solar cells are positioned attention as the third-generation solar cell, and currently, research has been actively conducted. At present, bulk crystal silicon (c-Si) solar cells still dominate the market due to their high efficiency and develop the technology. However, two major problems limit its future usage: first, Si is an indirect bandgap material which prevents effective absorption of sunlight, so the optical properties of c-Si are relatively poor. It is necessary to a sufficient thickness (several hundred μm) of the semiconductor layer for light absorption, which has been the problem of the Si raw materials shortage. The high cost of thick Si wafers limits its cost-competitiveness, creating a need for an alternative type of thinner Si wafer with a significantly lower cost. Second, solar cells based on a monocrystalline Si single junction structure realized the highest photovoltaic conversion efficiency of around 25%,[42] which is very close to the Shockley-Queisser limit (30%). Therefore, the efficiency improvement rate of bulk c-Si solar cells has slowed down in

recent years, and it can be expected that further development will be more difficult. New structures or new materials are must be pursued to solve these two problems.[43]

In the thin-film solar cell, a-Si thin-film solar cells, CdTe and some other II-VI compound semiconductors, organic thin-film solar cells, and nanostructure solar cells.

The a-Si solar cells, the optical and electrical properties are very different from the crystalline Si solar cells. [44,45] The light absorption coefficient of the a-Si is larger than the crystalline Si, and it is possible to absorb enough light, even film. For the short diffusion length of the minority carrier, it is difficult to hope such high conversion efficiency as a crystalline Si solar cell.

II-VI compound semiconductor system such as CdTe is likely to manufacture high-efficiency solar cells, but using harmful Cd as raw material, it is a problem that on the massive load of the environment. [46,47]

An organic thin-film solar cell is what using the organic semiconductor or conductive organic polymers, for light absorption and charge transport to generate electricity by the photovoltaic effect. [48,49]

Nanostructure solar cell is generally based on silicon nanostructures, which already have some researches in solar cell applications. [50–53] It shows a future potential because of its unique optical, electrical properties of the nanostructure.

1.4 Silicon nanostructure solar cell

1.4.1 Advantages of silicon nanostructure

In recent years, to solve the problem of the traditional c-Si solar cell, many novel structures and materials have been investigated. Si nanostructures have shown potential for solar cell applications due to the unique optical, electrical, and extraordinary surface-area-to-volume properties. [51,53–56] The schematics of silicon radial p-n junction arrays and a single enlarged junction are shown in Figure 1.5. There are two key strengths of nanostructures: first, the nanostructure effectively enhances light absorption. Absorption losses for traditional solar cells divide into reflection and transmission losses. Thus an antireflection layer and a thick substrate are needed for the conventional bulk c-Si solar cell increasing device fabrication costs (extra materials). [57–62] However, the nanostructured solar cell's light-trapping effect extremely increases the absorption. Second, the radial p-n junctions in the nanostructure provide a short carrier collection path, which especially benefits rapid charge separation and efficient carrier collection.[63–65] The two major benefits of nanostructured solar cells suggest exciting possibilities for low costs and good efficiency. Despite the advantages of Si nanostructure solar cells, industrialization is still at an early stage due to high surface recombination by large areas, needing better morphology control, rudimentary fabrication methods, and relatively low efficiency. There is still a lot of work needed to do, but rapid improvements in recent years certainly indicate potential in the future. [66–68]
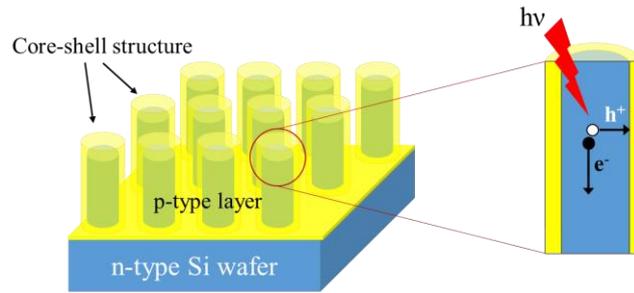
Figure 1.5 The schematics of silicon radial p-n junction arrays and a single enlarged junction.

1.4.2 Experimental of silicon nanostructure solar cell

Nanostructure fabrication methods

Fabrication of nanostructure with controllable diameter, length, and electronic properties is essential to its applications. Significant progress has been made in the development of facile and controlled methods for nanostructure fabrication in recent years.

In principle, there are two major fabrication methods to form the nanostructure. i.e.,

✦ Bottom-up methods

✦ Top-down methods

The most common **bottom-up method** is the Vapor-liquid solid (VLS) growth method, which usually uses gold as a catalyst. [69] However, the Au is a problem for following solar cell device fabrication and removing of Au is difficult. Thus, top-down fabrication is attracting more attention for future industrialization.

The **top-down methods** fabricate nanostructure by reduction of bulk Si material via an etching process.[70–74] Generally, Si nanostructure fabrication methods are divided into wet etching and dry etching methods. Here, the wet etching is using $AgNO_3$/HF solution to etch Si substrate. While the dry etching is using the plasma to dissolve the Si and form nanostructure. Each method has its advantages and disadvantages. The wet etching does not require a high vacuum chamber; its fabrication processes are simple and fast. But Ag particles are hard to remove completely, and the nanostructure morphology is not easy to control. For the dry etching, various factors (gas flow, plasma power, pattern shape) can be adjusted to control the nanostructure morphology easily. However, the lithography process for making pattern mask and high vacuum of plasma etching is limit the large-scale fabrication.
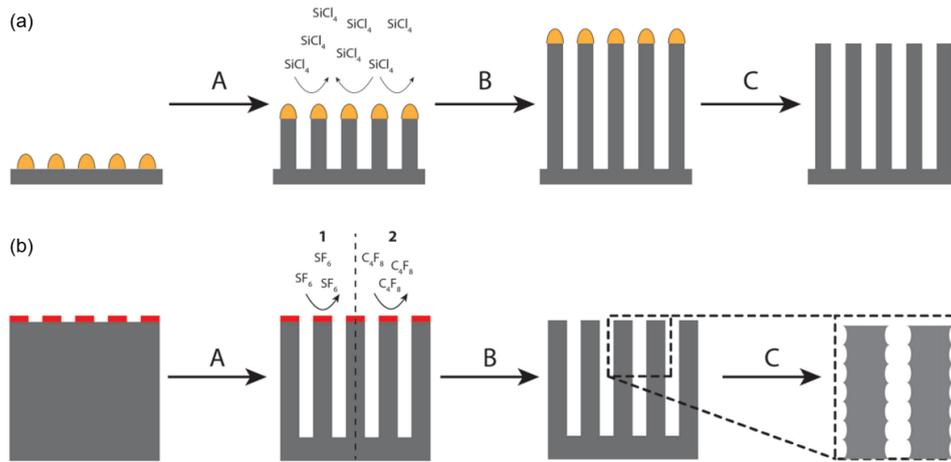
Figure 1.6 Schematic of (a) a VLS-growth method and (b) a dry etching method. [68]

CVD shell formation

The CVD process utilized for the p- and n-type doping of silicon, on either flat or structured surfaces. [64] Although there are several elements (B, P, Sb, As, Ga) that can be used for the introduction of p- and n-type dopants in silicon, only boron and phosphorus will be discussed here, as they are most commonly used. The standard process for any doping method is divided into two steps: first, the dopant atoms are introduced at the surface of the Si substrate via the formation of a layer (usually an oxide layer), followed by a drive-in step during which dopant diffusion into silicon takes place.

One classic method to deposit boron- or phosphorus-containing layers, is low-pressure CVD (LPCVD). The layer thickness and dopant concentration of the grown layer are controlled by the pressure and the gas inlets. For this process, the pressure of typically about 10^{-5} Pa is often used, corresponding to gas flows that are significantly low. Depending on the application, different gas mixtures are supplied, for example, PH_3 and SiH_4 for in situ phosphorus doping of silicon, yielding a phosphorus-doped shell.

Device structure and J-V measurement of nanostructure solar cell

Figure 1.8 shows the schematic of a nanostructured solar cell. After the core-shell fabrication by etching methods and CVD shell formation, some optional steps can be done, such as thermal annealing, ITO layer deposition, and n^+ layer diffusion. Finally, front and rear metal electrodes were deposited by sputter to form the device.
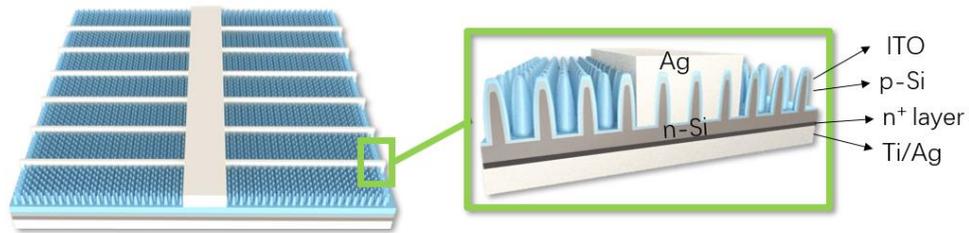
Figure 1.8 Device structure schematic of a nanostructured solar cell.[75]

J-V measurement is the most vital measurement for solar cell performance. As explained before, the efficiency of the solar cell can be simply described as below:

$$\text{Efficiency} = \frac{\text{Output Energy}}{\text{Input Energy}} \qquad 1\text{-}7$$

Here, the output energy is the detected electricity power, and input energy is the constant power of a solar simulation, the setup is shown in Figure 1.9. A copper stage touches the rear electrode, and a pin touches the front electrode. In this thesis, the solar cell device size is 0.7 cm * 0.7 cm.
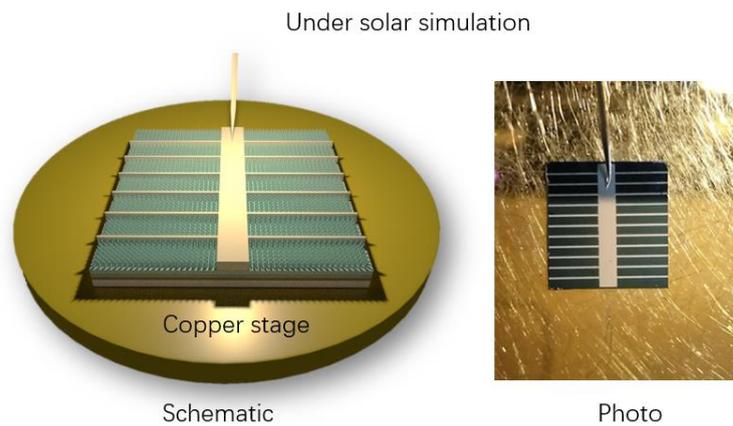
Figure 1.9 Schematic and photo of the setup of J-V measurement.

1.4.3 Roadmap of nanostructure researches
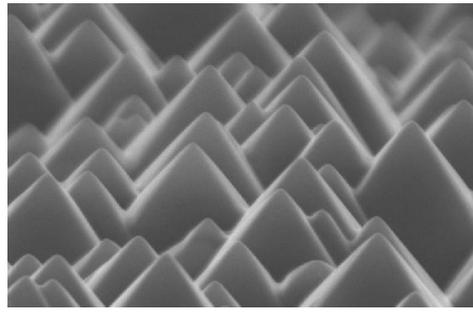
Figure 1.10 Texture etching of the silicon surface.[76]

In 1979, William L. Bailey first reported texture etching of the silicon surface. [76] This textured surface was used to reduce surface reflection. The pyramids are nanometer to micrometer scale and efficient for the anti-reflection property. But it still needs a thicker substrate and not suitable for the further thin-film device.
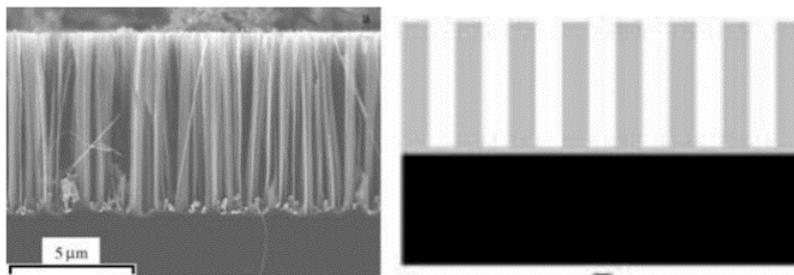
Figure 1.11 silicon nanowires array only as an efficient antireflection layer.[77]

In 2005, Kuiqing Peng fabricated silicon nanowires array as an efficient antireflection layer for photovoltaic devices to further reduce the reflection and use thinner substrate, nanowires structure was developed. But the mechanism of absorption does not have essential differences.[77]
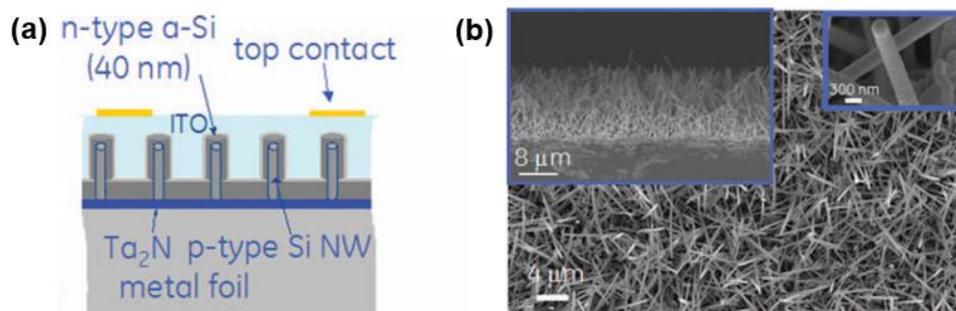
Figure 1.12 Photovoltaic devices based on CVD-VLS-grown SiNWs arrays.[53]

L. Tsakalakos at 2007 fabricated photovoltaic devices based on VLS-growth SiNWs arrays core-shell structure, for shortening the carriers collection length. [53] But the metal catalyst is hard to remove and limit the performance.
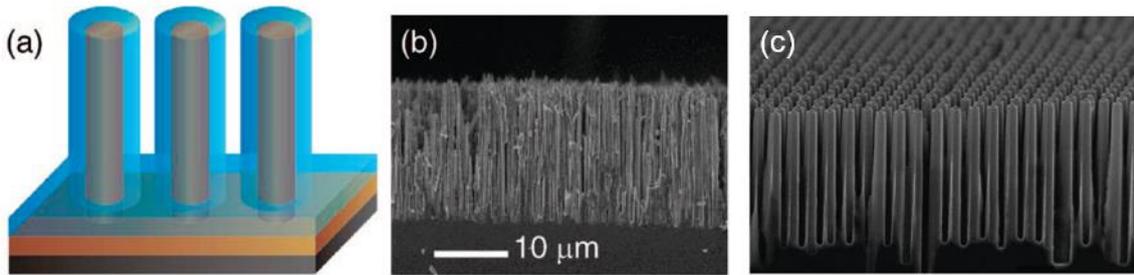
Figure 1.13 Fabricated radial p-n Junction solar cell based on wet and dry etching methods.[51,62]

E.C. Garnett, (at 2008, 2010) fabricated radial p-n junction solar cells based on wet etching method and dry etching method, respectively. [51,62] Both two methods can reach low reflection, and no catalyst was used. But their low reflection relies on the very long length nanowires (over 10μm). It reduces the J_{SC} of the solar cell device due to surface recombination. Thus, the efficiency of this device is low for industry use. (normal close to 15%)
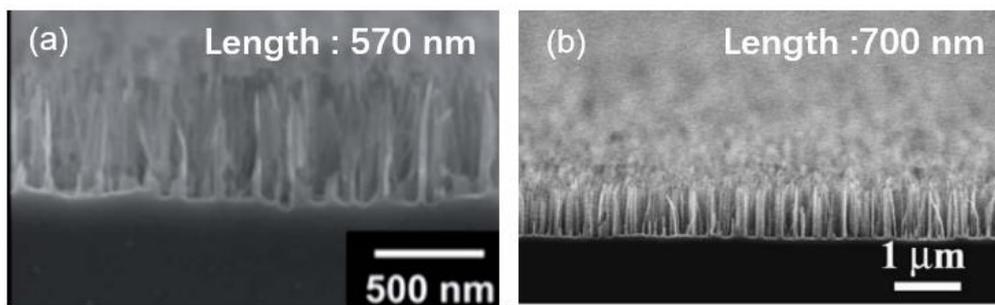
Figure 1.14 Short length nanowires for hybrid heterojunction and Si homojunction radial solar cells.[61,63]

In previous researches of our group, Keisuke Sato in 2014 investigated nanowires length for hybrid radial heterojunction solar cells. Mrinal Dutta in 2015 investigated nanowires length for Si homojunction solar cells. [61,63] Both two works found that the nanowires over 1μm can achieve low reflection, but they are not good for solar cells because of the high surface carrier's recombination. A 500-700 nm length nanowire can obtain the best balance.

1.5 Purpose

We investigate the fabrication and optimization of different Si nanostructures, as well as their applications for next-generation solar cell devices. Based on previous researches, we hope to achieve a high-performance (efficiency close to 15%) Si nanostructure solar cell device by some simple and feasible paths. Moreover, we try to find some new phenomena and novel ways to enhance the **advantages of silicon nanostructures** for photovoltaic usage. All these attempts are pursuing additional insight into the energy problem by the nanoscale solution.

In detail, my major purpose is to achieve **higher J_{SC}** for better solar cell efficiency; The J_{sc} is due to the generation and collection of light-generated carriers. Mainly affected by below reason:

- **The optical properties** (include **absorption** and **reflection**) of the solar cell
- **The collection probability** of the solar cell

Thus, in the following chapters, kinds of methods and phenomena were investigated and optimized to achieve this purpose.

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Chapter 2.   Nanostructure morphologies optimization

2.1 Silicon nanowire solar cell

In this section, we first introduce the silicon nanowires(SiNWs) which fabricated by the metal-catalyzed electroless etching (MCEE) methods. [1–5] It is already proposed as low-cost and simple fabrication processes due to its possibility to obtain quite high-efficiency SiNW solar cells at a standard pressure of the atmosphere and room temperature.[6,7]

As we introduce in Chapter 1, in the nanostructure, a photon may travel up to $4n^2$ times further than without light trapping, and hence increase its chances of being absorbed. Longer path-length that the light can travel more times in the array between nanostructure scattering events. Thus, increase the length of the nanowire is a standard way to reduce reflection by enhanced light trapping effect. Our group's previous work found reflection (400 -1000 nm wavelength) lower than 5% need at least 2000 nm.[8,9] However, longer nanowires, due to their high surface area to volume ratio, tend to decrease the minority-carrier lifetime, and the deep valleys between SiNW arrays the electrode deposited on the silicon surface cannot be continuous, both these two factors reduced device efficiency.[10,11] Previous studies have led us to optimize the nanowire length to around 500-700 nm.[3,9] Alternatively, a higher nanowire array density enhances light absorption for the same nanowire length.[8,12] Here, we report a UV/Ozone pre-oxidation treatments before the MCEE process with which we succeeded in achieving higher SiNW arrays density and better uniformity.

2.1.1 Experimental of silicon nanowire solar cell

Fabrication process

The schematic images of fabrication processes (nanostructure and device) are shown in Figure 2.1(a)(b). The SiNWs were first fabricated on 280 µm n-type monocrystalline silicon (100) wafer by metal-catalyzed electroless etching (MCEE) methods. After nanostructure formation, the sample was epitaxially grown a B-doped p-type Si shell layer to make p-n junctions by CVD. The SEM images were indicated in Figure 2.1(c). Then rapid thermal annealing (RTA) was performed at 950 ˚C in an N_2 environment for 3 min by ULVAC QHC furnace. An n^+ layer was created by spin-coating a phosphorus-containing solution (OCDP-59210) for the back-surface field (BSF). Then it was concurrently prebaked at 450 ˚C for 30 min and annealed at 850 ˚C in N_2 flow for 45 min.[13–17] At last, an ITO layer was deposited on the surface to advance the carriers transport. Front and back electrode contacts are finger grid Ag pattern and full-cover Ti/Ag which deposited by sputter.
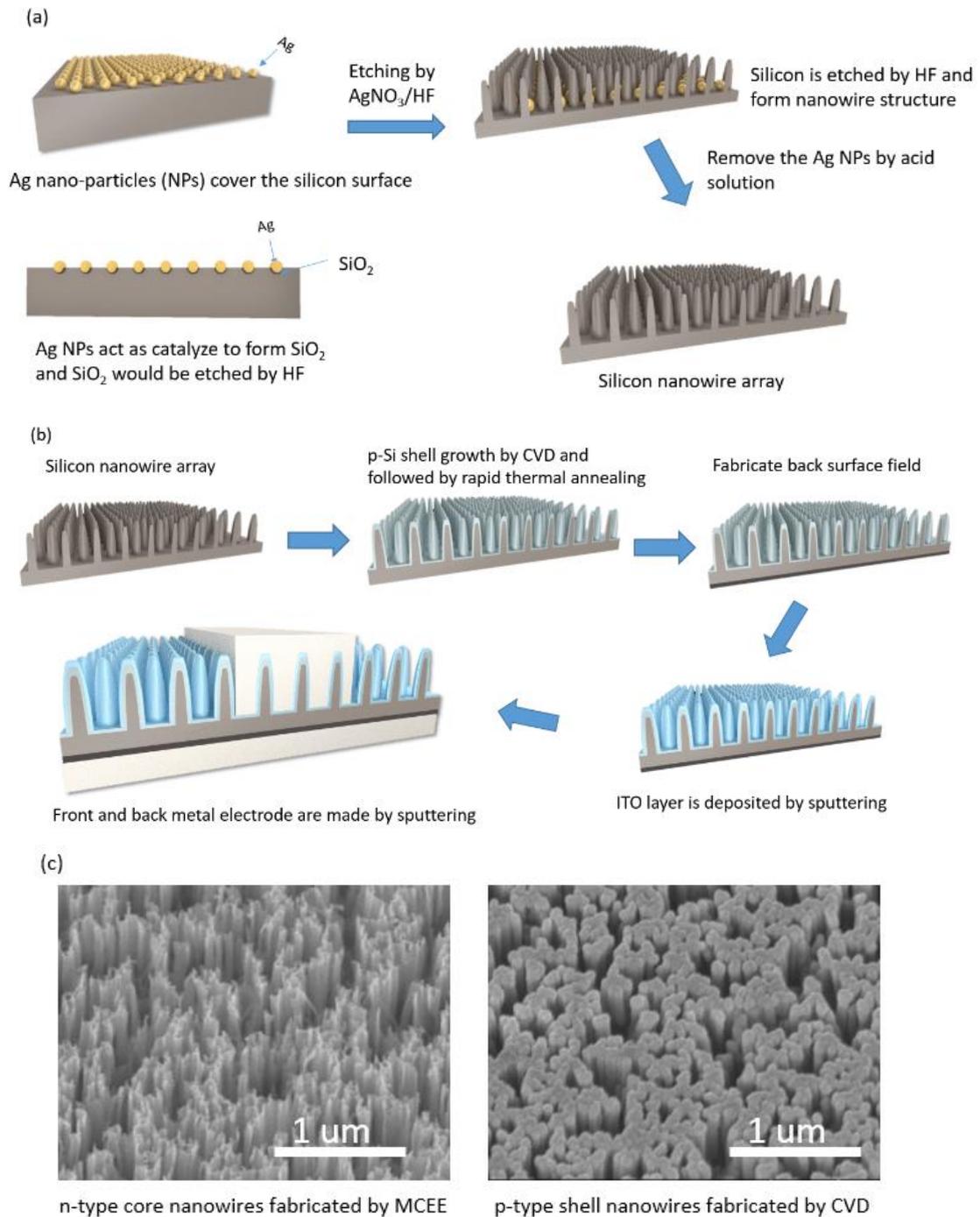
Figure 2.1: (a) Schematic of the brief fabrication process silicon nanowires by MCEE. (b) Schematic of solar cell devices fabrication from nanowires substrate. (c) SEM images of the core nanowires and core-shell nanowires in 30-degree tilted top-view.[18]

UV/Ozone pre-oxidation methods

Pre-oxidation treatments were applied before the MCEE process. It is using UV/ozone to oxidize the silicon wafer and form a thin SiO_2 layer on the surface. The UV/ozone treatment was done at 200 °C for 20 min under a 20 mW UV irradiation and 10 mTorr O_2 pressure atmosphere.

Characterizations

The nanostructure characterization was detected by a high-resolution field-emission scanning electron microscope (FESEM, Hitachi S-8000). UV-Vis-NIR reflectance spectra (wavelength range of 220 - 2000 nm) were measured by an NIR spectrophotometer (Jasco V-670). Current density-voltage measurements were performed under illumination with a 1 sun air mass (AM) 1.5 G Xenon lamp solar simulator by a Keithley 2400 source meter. It was calibrated using a Sharp single-crystalline silicon solar cell (BS-500).

2.1.2 UV/Ozone treatments for silicon nanowire solar cell

The oxidation of silicon can be carried out by different liquid chemicals, such as perchloric acid ($HClO_4$), potassium dichromate ($K_2Cr_2O_7$) or potassium permanganate ($KMnO_4$). But the liquid reaction process for silicon oxidation is hard to control. For achieving high-quality thin SiO_2 layers, gas oxidation is a more suitable technique. Ozone is more reactive than normal oxygen gas because the oxidation potential of ozone is higher than oxygen. Moreover, the reactants after oxidation by ozone are not problematic and are easily prepared by an ozone generator which is widely used in the semiconductor industry. Here, we generated the ozone by introducing oxygen under UV irradiation.

To check the effect of UV/Ozone pre-oxidation treatments before the MCEE process, we fabricated samples without pre-oxidation treatment and using UV/Ozone pre-oxidation methods for the silicon wafer after using HF remove the native oxide layer. Nanowires were then fabricated typically using 5-min MCEE process.

Top-view SEM images of these samples are shown in Figure 2.2 (a) without pre-oxidation, (d) UV/Ozone pre-oxidation treatment. The fraction was calculated of silicon nanowires (SiNWs areas/ total areas) in these samples. Silicon nanowire fractional volume density is the nanowire/air filling ratio as considered in this work. The results showed the fraction of nanowires to have increased by 15% after pre-oxidation treatment. The density of nanowires is, therefore, higher in the UV/Ozone pre-oxidation samples than in the without-oxidation samples.

Figure 2.2 (b), (c) shows cross-sectional SEM images of the samples and their respective length distributions. The morphologies are quite different in the samples: first, the sample without oxidation shows that most of the nanowires remain vertical and have close to the same length, but some of the nanowires are bent at the top. The length of the nanowire ranges around 600 - 680 nm, in which about 98% measuring 650 $\pm$ 30 nm. The sample with UV/ozone oxidation is shown in Figure 2.3 (e) and (f), it indicates excellent nanowire morphology with vertical and uniform structures. Around 90% of nanowires' length is in a narrow range of 570 $\pm$ 30 nm. The relative lower length is due to the SiO_2 layer, which slows down the etching process.

(a)

Fraction: ~35%

(b)

(c)

(d)

Fraction: ~50%

(e)

(f)
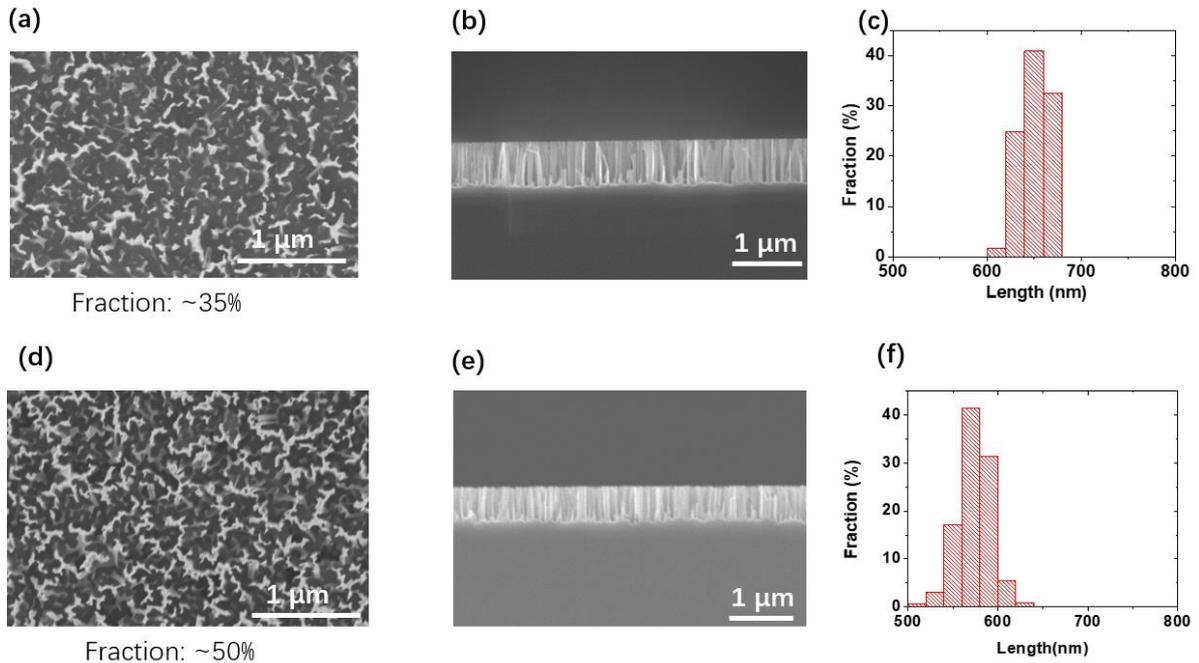
Figure 2.2 Top-view, cross-section view of SEM images and length distribution of two samples: (a), (b), (c) without pre-oxidation, (d), (e), (f) with UV/ozone pre-oxidation treatments.

These oxidation process fabricated a thin SiO_2 layer on the surface of the silicon substrate, which affects the following MCEE process subsequently. The schematic diagrams of the mechanism and SEM images for the two methods are shown in Figure 2.3: (a), (b), (c) without pre-oxidation, (c), (d), (e) with UV/ozone pre-oxidation treatments. In the sample without oxidation, an Ag nucleus first generated when the Ag^+ ions in the solution attract an electron from the silicon wafer. Then, electron transfer occurred between the Ag nanoparticle; at the same time, Ag^+ ions are deposited around the Ag nuclei. Both two factors make the Ag particle become very large, and finally generating a flake-like particle. The large Ag particle makes the space between SiNWs enlarged, and the density will be reduced.

In the sample with UV/ozone treatment, uniformly form a thin SiO_2 layer was generated by the controllable gas oxidation process, as seen in Figure 2.3 (c). This thin SiO_2 layer stops the electron transfer in the silicon surface. Thus, the nucleation of Ag NPs was suppressed. Then the thin SiO_2 layer is dissolved by the HF solution, and small Ag NPs are formed. The SiNWs can keep close, and density was increased.[8,12]
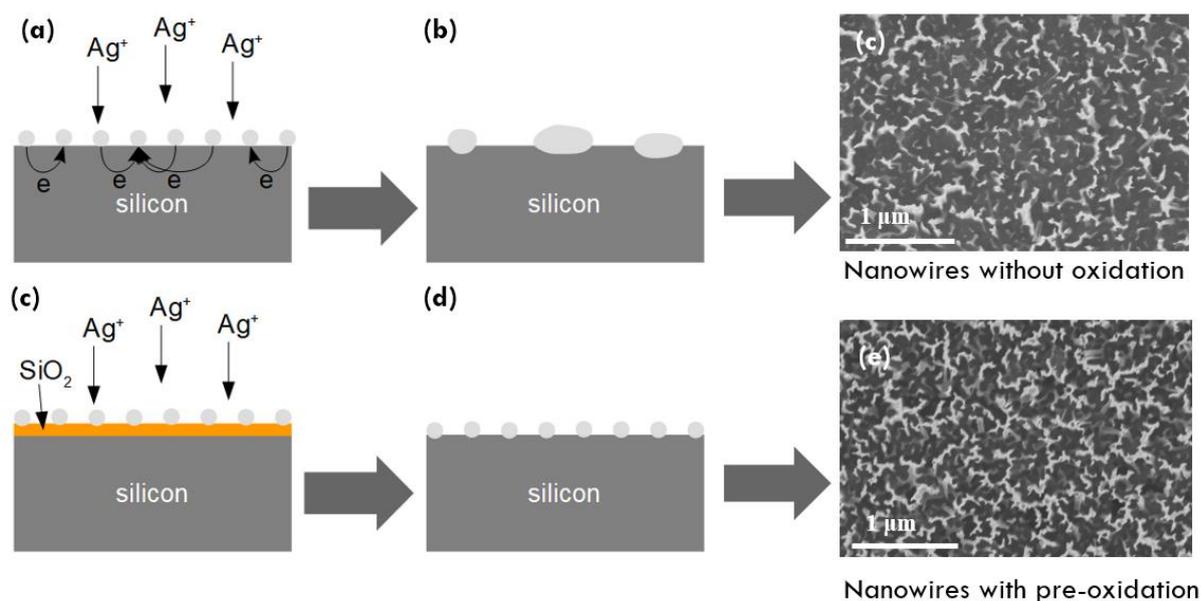
Figure 2.3 Schematic diagrams of the MCEE process and the SEM images in top vies (a, b, c: the sample without oxidation, c, d, e: the sample with pre-oxidation by UV/ozone).

One of the reasons why uses nanostructure is the better anti-reflection property, which will significantly influence structural changes. As we described before, the spectrum of sunlight ranges from 200 - 2500 nm. But for the Si material, most of the absorbable energy is in the visible spectrum and the near-infrared portion (400 - 1000 nm) due to its bandgap. Light absorption in this range is, therefore, the key to Si material solar cells. UV-Vis-NIR spectra measurement is a convenient and commonly-used method to analyze the anti-reflection properties of nanowire structures. The results for different samples are shown in Figure 2.4, in addition to that for a silicon planar wafer used as a reference (black line) to show the anti-reflection property of SiNWs. The spectral measurements reveal that the average reflectance of the silicon planar wafer was very high, at greater than 40% in the 300 - 1000 nm range. But due to the light trapping effect of nanowires, obviously lower reflectance of nanowire samples was found. Moreover, in the sample without oxidation (red line), the reflectance increased from 10% to 20% over the 300 - 1200 nm range. While the sample with UV/ozone pre-oxidation (blue line), reflectance maintains at a shallow level (less 5%). This is a noticeable enhancement of light anti-reflection property in this region. It indicates that the UV/ozone treatment can obtain sufficiently low reflectance with shorter and uniform nanowire. Also, in Table 2.1, we can find that the density of SiNWs increases, the light-trapping effect can be enhanced, and the reflection can be reduced significantly.
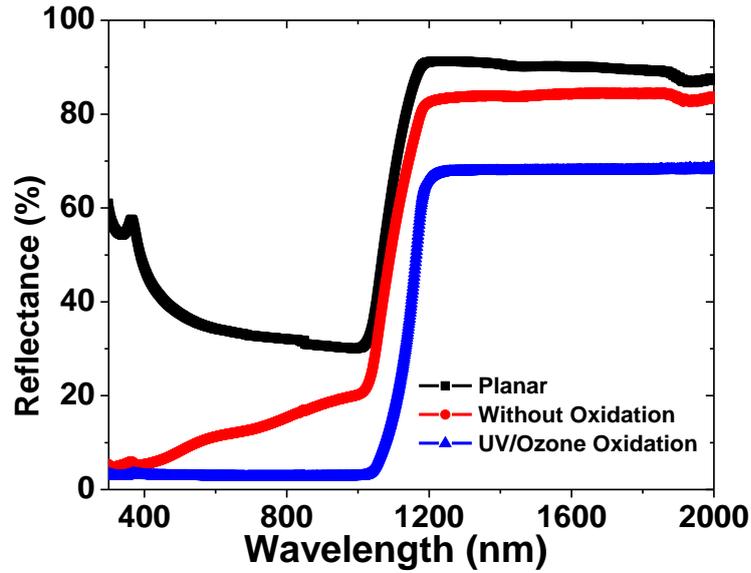
Figure 2.4: The spectra of the samples: the wavelength ranging from 300 - 2000 nm, measured by the UV-Vis-NIR spectroscopy.

Table 2.1 The filling ratio and reflectance of the samples with and without UV/Ozone pre-oxidation.

	Filling ratio	Reflectance (400 nm – 1000 nm)
Without pre-oxidation	~35%	5 ~ 20%
With pre-oxidation	~50%	~3%

The above results show that UV/Ozone pre-oxidation leads to higher density nanowires and better anti-reflection. Thus, we continued to fabricate solar cell devices with and without pre-oxidation based on the above results. These solar cell devices were fabricated using simple processes without BSF or RTA treatments to prevent interference from other factors.

Figure. 2.5 shows current density-voltage curves measured in 1 sun for the samples without oxidation and with UV/Ozone samples. The solar cell properties are shown in Table 2.2. It is clear that the UV/Ozone sample showed better performance than the sample without oxidation. The significant improvement comes from the improvement short circuit current density (J_{SC}), increasing from 19.57 to 22.09 mA/cm^2. It helps the solar cell efficiency (η) achieved from 4.8% to 5.6%. This J_{SC} improvement can be described by below formula:

$$J_{SC} = q \int_{\lambda_1}^{\lambda_2} F(\lambda)\big(1 - R(\lambda)\big)Q(\lambda)d\lambda$$

2-1

Photon flux $F(\lambda)$ is calculated from the AM 1.5 solar energy spectrum. Internal quantum efficiency $Q(\lambda)$ is major affected by surface recombination and diffusion length. $R(\lambda)$ is the reflectance. Thus, based on the spectrum of reflectance of the incident light from 400 nm to 1100 nm. $R(\lambda)$ reduced ~14%, it would contribute to the increasing of J_{SC} according to the formula.

In the practical device, 2.52 mA/cm^2 (12.8%) improvement of J_{SC} was achieved in the pre-oxidation samples. It close to the reflection contribution but little lower, it may be a reduction in the $Q(\lambda)$, because nanowires density increasing also increase the surface recombination. The improvements of J_{SC} in oxidation samples revealed that the enhanced light absorption is able to generate higher photo-current. In other words, higher nanowires density strongly enhanced solar cell performances. These results also demonstrate that UV/Ozone treatment is better than Piranha oxidation and is possibly a useful way to improve the silicon nanowire solar cell performance. Increase the light-trapping effect for low light reflection in short nanowire length and achieve higher J_{SC}.
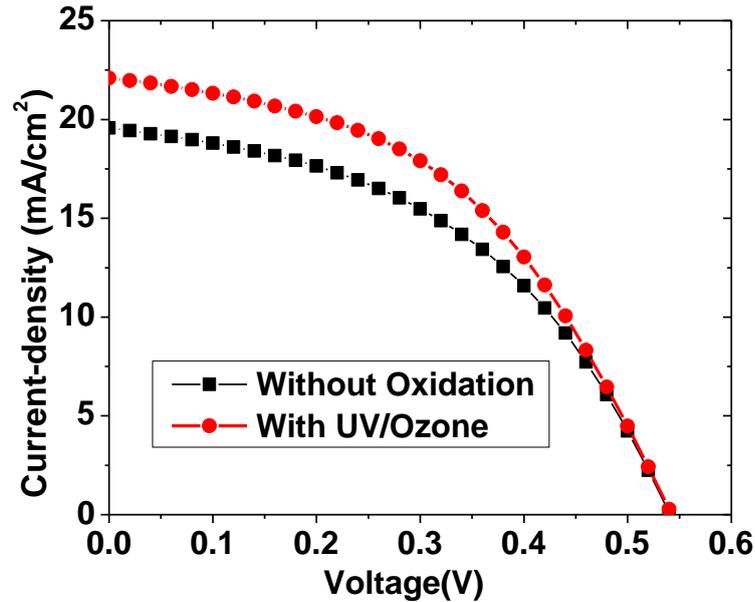
Figure 2.5 Current density-voltage curves of samples without oxidation and with pre-oxidation by UV/ozone.

Table 2.2. Parameters of the solar cell devices without oxidation and UV/ozone pre-oxidation.

	Jsc (mA/cm^2)	V_{OC} (V)	FF	η (%)
Without oxidation	19.57	0.54	0.46	4.8
With UV/ozone	22.09	0.54	0.47	5.6

2.1.3 Optimization of the silicon nanowire length
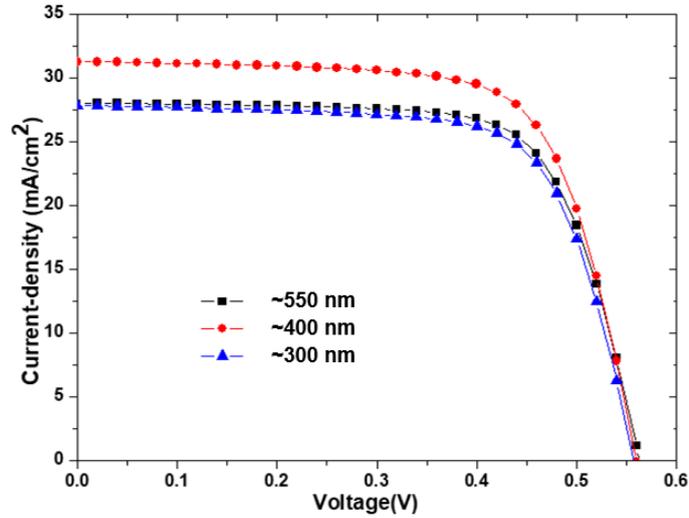
Figure 2.5 Current density-voltage curves of samples in different nanowire length.

Table 2.3. Parameters of the solar cell devices in different nanowire length.

Nanowire length (nm)	J_{SC} (mA/cm^2)	V_{OC} (V)	FF	η (%)
~550	27.84	0.56	0.70	10.9
~400	31.28	0.56	0.71	12.4
~300	28.01	0.56	0.71	11.2

In our previous works, the optimized condition of the solar cell was 5 min MCEE with 700 nm-length nanowire, which represented the right balance between light anti-reflection and surface states. Here, due to shallow reflection with the UV/ozone treatment in a relatively short length of 550 nm. It is necessary to optimize the conditions for this new structure. We are, therefore attempting to reduce the MCEE process time to decrease nanowire length and reduce surface states. We fabricated three samples of different length:550, 400, 300 nm, all these samples are etched after UV/Ozone pre-oxidation treatment. The J-V curves of solar cell devices with different SiNWs length are shown in Figure 2.5. The corresponding parameters of the solar cell, including V_{OC}, J_{SC}, FF, and efficiency, are indicated in Table 2.5. When SiNWs lengths reduce to 400 nm, J_{SC} increased from 27.84 to 31.28 mA/cm^2. This is due to decreasing recombination of photo-generated carriers, caused by fewer surface states and interfacial dangling bond defects in the shorter 400 nm SiNWs, which has a decreased surface area. This J_{SC} enhancement leading to the device efficiency increased to 12.4%. However, further decreased of SiNWs length from 400 nm to 300 nm is not work as before, the J_{SC} decreases from 31.28 to 28.01 mA/cm^2. This is because of the reduction of the total active p-n junction area detracts from the benefits of less recombination. Ultimately, the 400 nm length sample showed the best performance, with a UV/ozone pre-oxidation treatment.

2.2 Silicon nanopillar solar cell

In this section, we fabricated ordered silicon nanopillars using a combination of nanoimprint lithography and Bosch etching methods. Then, grow the p-Si shell to form a radial p-n junction by using chemical vapor deposition. Our previous research shows that ordered nanopillar solar cells have achieved excellent performance due to the back surface field (BSF) treatment and rapid thermal annealing (RTA)[19]. But the solar cell performance still suffers from a low current-density and fill factor because of the relatively low reflectance and poor electrode contact caused by the ordered nanopillar array structure and large electrode spacing, respectively. Here, indium tin oxide (ITO) was investigated to improve carrier transfer between the nanopillars and the metal contact. The reason is due to the high electrical conductivity and optical transparency of ITO. Finally, shorter nanopillars were used to reduce surface recombination.

2.2.1 Experimental

Fabrication process

The process to fabricate ordered silicon nanopillars is shown in Figure 2.6(a) and starts with a 280 μm-thick n-type monocrystalline silicon (100) substrate wafer. Nanoimprint lithography process is performed by first coating photoresist layer on the silicon substrate. Then, a transparent quartz mold is pressed onto the surface coated photoresist layer and irradiated with UV light to form a nanohole structure. Next, the residue is cleaned off after the mold is removed. A 30nm Cr layer is deposited onto the surface, and the photoresist is removed, leaving behind an ordered array of Cr. The followed Bosch process uses SF_6 & C_4F_8 plasma to etch silicon material and forms nanostructures. [20] The flow rates of SF_6 and C_4F_8 were both 35 sccm, under 0.75 Pa chamber pressure and 100W RF power. Finally, an ordered silicon nanopillar array was obtained after removing the Cr.

The fabrication process of solar cell device based on silicon nanopillars is shown schematically in Figure 2.6(b). Nanopillar samples were placed in a CVD chamber to fabricate solar cell p-n junctions by epitaxially growing a B-doped p-type Si shell layer. Then rapid thermal annealing (RTA) was performed at 950 ˚C in an N_2 environment for 3 min by ULVAC QHC furnace. An n^+ layer was created by spin-coating a phosphorus-containing solution (OCDP-59210) for the back-surface field (BSF). Then it was concurrently prebaked at 450 ˚C for 30 min and annealed at 850 ˚C in N_2 flow for 45 min.[13–17] At last, an ITO layer was deposited on the surface to advance the carriers transport. Front and back electrode contacts are finger grid Ag pattern and full-cover Ti/Ag which deposited by sputter.

Characterization

The nanostructure characterization was detected by a high-resolution field-emission scanning electron microscope (FESEM, Hitachi S-8000). UV-Vis-NIR reflectance spectra (wavelength range of 220 - 2000 nm) were measured by an NIR spectrophotometer (Jasco V-670). Current density-voltage measurements were performed under illumination with a 1 sun air mass (AM) 1.5 G Xenon lamp solar simulator by a Keithley 2400 source meter. It was calibrated using a Sharp single-crystalline silicon solar cell (BS-500).
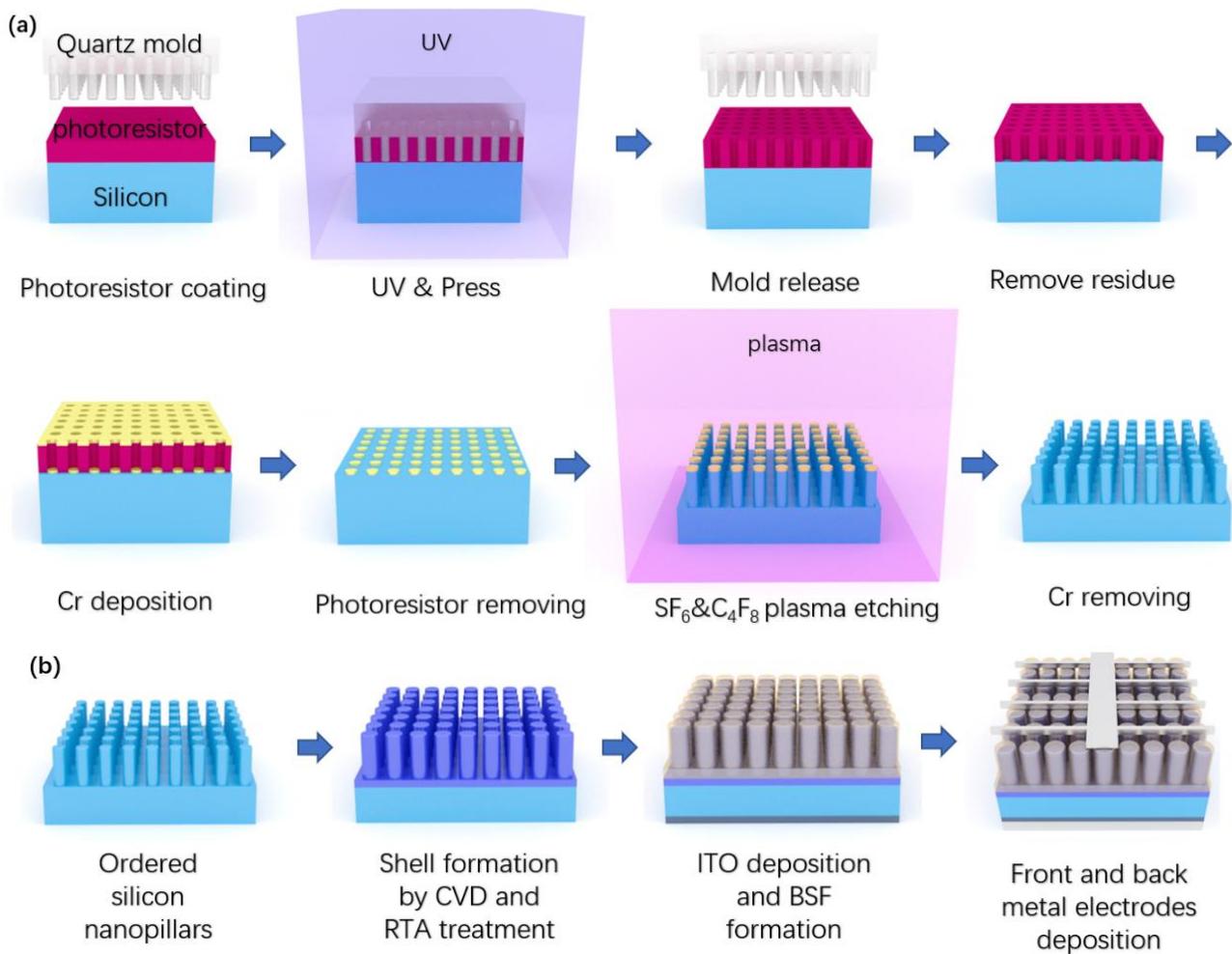
Figure 2.6. Schematic diagram of (a)silicon nanopillars formation process and (b) device fabrication process.[21]

2.2.2 Basic properties of the silicon nanopillars
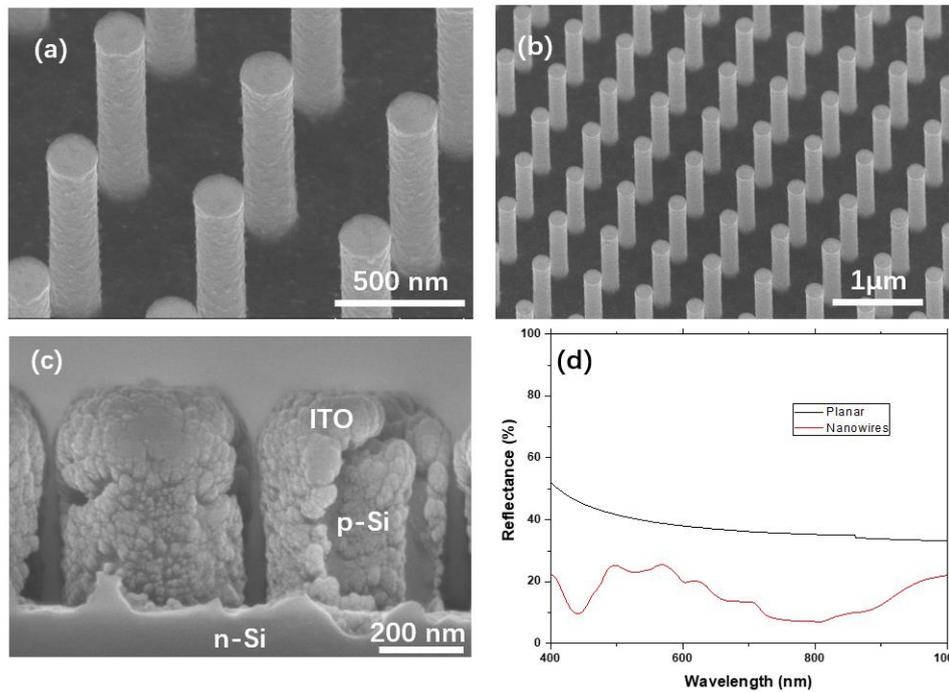
Figure 2.7. (a) Zoomed in SEM images of ordered silicon nanopillars and (b) overview SEM images of the nanopillar array tilted at 30º. (c) SEM image in the cross-section view of the ordered silicon nanopillars deposited with p-Si shell and ITO layer. (d)Reflectance spectrum from 400 to 1000 nm for planar wafers and nanopillars, measured by UV-vis-NIR spectroscopy. [21]

The SEM image in Figure 2.7(a) clearly shows the nanopillars formed by the Bosch etching process, and the dimensions of each nanopillar 1080 nm long and 200 nm in diameter. Because of how controllable and reliable the nanoimprint lithography and Bosch etching process are, that the nanopillars show very high uniformity and good order, as shown in Figure 2.7(b). Figure 2.7(c) shows the nanopillars (540 nm) deposited with p-Si shell and ITO layer. Then, a UV-Vis-NIR spectral measurement was taken to investigate the light-absorbing properties of the nanopillars. Same with the previous nanowire solar cell, the light absorption in the visible-to-NIR range (400 - 1000 nm) is vital due to it is the primary energy absorbed range for silicon[22]. In Figure 2.7(d), the reflectance of a planar Si wafer (black line) was taken as a reference and had a very high value of around 40%. On the other hand, the reflectance of the nanopillar sample (red line) maintained a low level, which is only 10% - 20% due to light scattering by the nanopillar structure.

2.2.3 Effect of ITO layer coating on silicon nanopillars
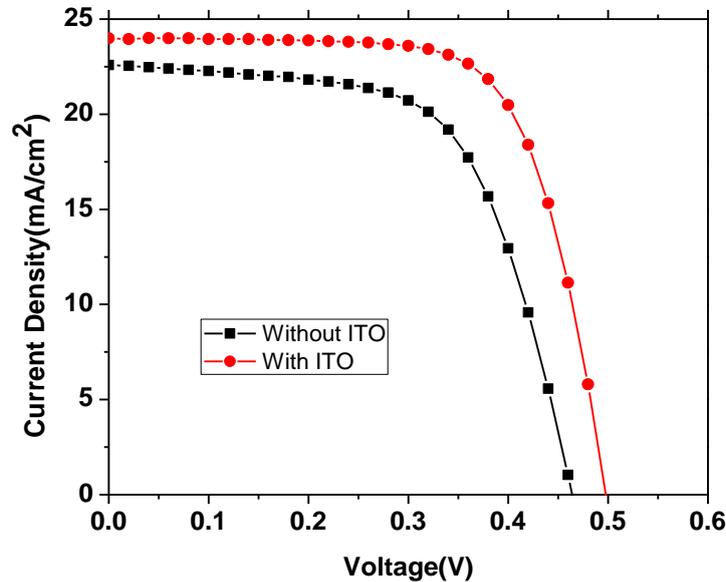
Figure 2.8. J-V curves of the solar cell device with and without the ITO layer. [21]

Table 2.3. Solar cell parameters of devices with and without the ITO layer.

	J_{SC} (mA/cm^2)	V_{OC}(V)	FF	η(%)
Without ITO	22.58	0.46	0.62	6.5
With ITO	24.00	0.50	0.69	8.3

To improve photocarrier collection efficiency as a transparent electrode and an anti-reflection layer, we deposited the ITO films on the entire front surface of the device by sputter. First, ITO thickness is needed to be considered, because it is a trade-off between conductivity and transmittance of the front surface. Thus, the film thickness with optimal transparency often differs from the desired film thickness of the electrodes. When considering conductivity on its own, using very thick ITO films is the best approach for the device. However, thick ITO films can lead to higher parasitic absorption in both the UV and NIR regions. This will reduce the incident light intensity for the p-n junction. Moreover, another thing is that deposit ITO on the nanostructure is different from a planar coating, due to the space between nanostructure. Correspond to our experiment and some reference; we found that a ~120 nm ITO layer is the critical value at which has to do a balance of resistivity and transparency for our nanostructure solar cell device. [23]

The results are shown in Figure 2.8 and Table 2.3, after applying the ITO layer on the nanopillar solar cell, the short-circuit current density (J_{SC}) was obtained an excellent enhancement. This is due to the silicon

nanopillars absorb more lights and generate a higher photocurrent by the anti-reflection property of ITO. Also, the entire surface coated of ITO is better at carrier collection, and reduction of surface recombination, the open-circuit voltage (V_{OC}) increased from 0.46 V to 0.50 V. Moreover, the fill factor (FF) was significantly improved from 0.62 to 0.69 due to the improved conductivity by better electrode contact and the surface passivation accomplish by the ITO layer. Thus, with the apparent improvement of the three parameters, the total PCE of the solar cell device was calculated as 8.3%, a significant change to the device without an ITO layer whose PCE was only 6.5%.

2.2.4 Optimization of Si nanopillar length
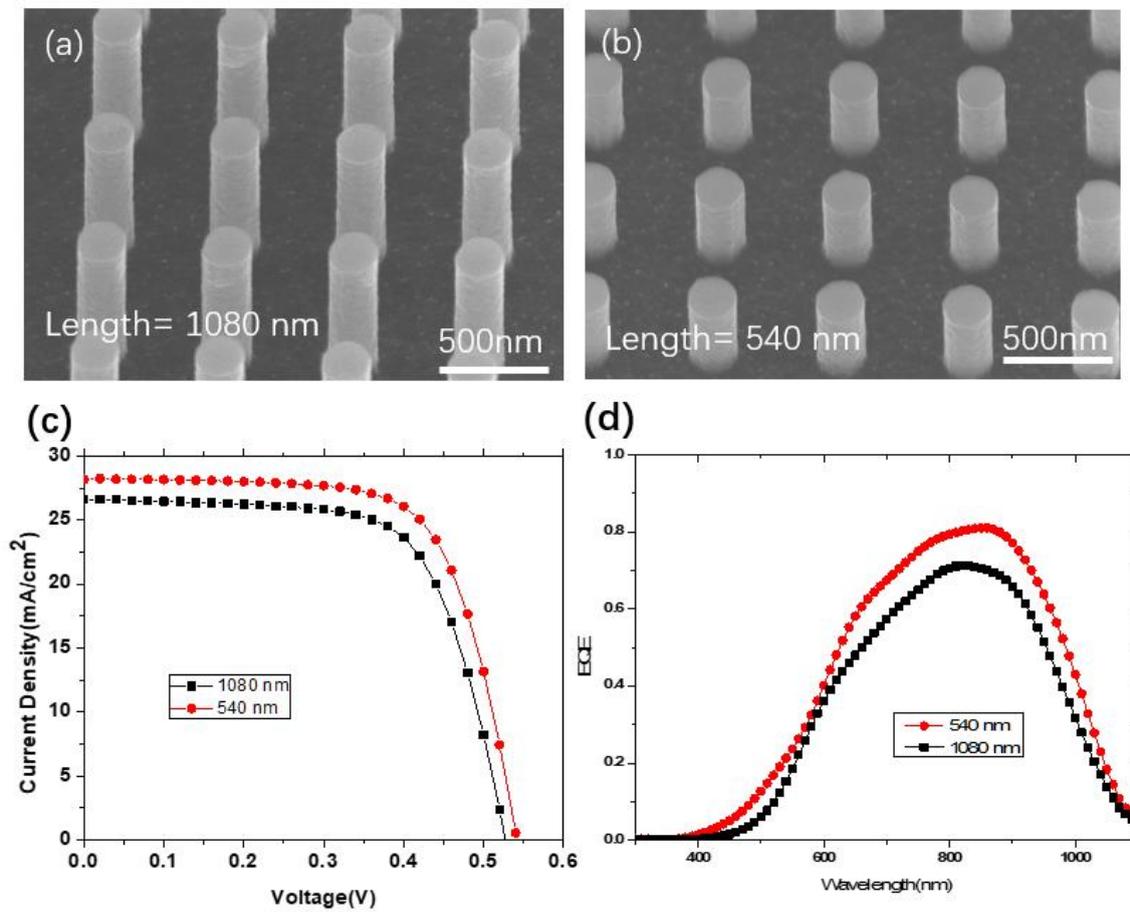
Figure 2.9. (a)(b) The 30° tilted view SEM images of 1080 nm and 540 nm tall ordered silicon nanopillars. (c) J-V curves and (d) EQE spectra of SiNW solar cell devices. [21]

Table 2.4. The parameters of solar cell device in 1080 nm and 540 nm

Nanopillar length	J_{SC} (mA/cm^2)	V_{OC}(V)	FF	η(%)
1080 nm	26.58	0.53	0.68	9.5
540 nm	28.18	0.54	0.69	10.5

In the previous section, we investigate the trade-off between light absorption and nanowires surface states. Therefore, an optimized length of nanopillar is vital for maximizing device efficiency. Same as the nanowires, longer nanopillar also enhances light absorption but increases surface states. In this section, the surface light absorption was enhanced using ITO. Therefore, we consider shortening the nanopillar length for fewer surface states. Ordered nanopillars in 540 nm length were fabricated, as shown in Figure 2.9(b) and comparing with the 1080 nm one Figure 2.9(a). Here, only the length of the nanopillar was reduced. Else parameters such as the shape, diameter, and periodicity were kept the same. The J-V curves of these solar cell devices and the corresponding solar cell properties are shown in Figure 2.9(c) and Table 2.4. We found that in the 540 nm length nanopillar sample, the J_{SC} increased from 26.58 to 28.18 mA/cm^2. Also, the EQE spectra in Figure 2.9 (d) have a clearly increasing of the 540 nm sample. This EQE increasing is corresponding to the improvement of J_{SC}. Both improvements are due to the reduction of surface recombination, causing by the reducing surface area in the shorter length nanopillar sample with decreasing surface defects and dangling bonds.[24] It allows photo-generated carriers to travel more efficiently without recombination. Finally, the improvement of J_{SC} results in a higher PCE of 10.5%.

2.3 Silicon nanopencil solar cell

In this section, we investigated a novel method that combines colloidal lithography and plasma reactive ion etching (ICP-RIE) techniques to form silicon nanopencil structures. This nanopencil structure shows outstanding broad-band absorption and light trapping properties due to the asymmetric structure. Moreover, due to its potential for large-area and low-cost fabrication process, colloidal lithography is ideal for industrial mass-production, which is challenging to be realized by the conventional photolithography technique[25–27]. The vertical and horizontal etching rates are adjusted by the fabrication parameters such as etching time, nanoparticle diameter, power bias volume, gas flow rate, and so on. Thus, the shape, pitch, height, and diameter of nanopencil are controllable during the process.

2.3.1 Experimental of silicon nanopencil solar cell

Fabrication of silicon nanopencils

The silicon nanopencil structures were prepared based on 525 or 280 µm thickness n-type Si (100) wafers and 500nm diameter sphere-shaped colloidal silica particles. The fabrication process includes colloidal lithography and ICP-RIE. First, immerse silica particles into aminopropyltriethoxysilane or allyltrimethoxysilane to make a hydrophobic surface. After that, the silicon wafer was placed in a mixture with 80% chloroform and 20% ethanol of a Langmuir Blodgett trough. The silica particles were dispersed on the surface of the mixture, and a monolayer of silica particles was formed at the interface of air-water by self-assembly. Then, the silica particles monolayer can be transferred to the wafer surface when withdrawn from the silicon substrate upwards from the sub-phase water. Next, the ICP-RIE process was performed by CHF_3/Cl_2 gases under a 1.0 Pa pressure by using an ICP dry etcher (Tokyo Electron ME-510 I). The silica particles were gradually etching during the process, and make the top more and more tapered, finally generated a vertical nanopencil structure.

Fabrication of solar cell device

Nanopencil array samples were placed in a CVD chamber to fabricate solar cell p-n junctions by epitaxially growing a B-doped p-type Si shell layer. Then rapid thermal annealing (RTA) was performed at 950 ˚C in an N_2 environment for 3 min by ULVAC QHC furnace. An n^+ layer was created by spin-coating a phosphorus-containing solution (OCDP-59210) for the back-surface field (BSF). Then it was concurrently prebaked at 450 ˚C for 30 min and annealed at 850 ˚C in N_2 flow for 45 min.[13–17] At last, an ITO layer was deposited on the surface to advance the carriers transport. Front and back electrode contacts are finger grid Ag pattern and full-cover Ti/Ag which deposited by sputter.

Characterizations

The nanostructure characterization was detected by a high-resolution field-emission scanning electron microscope (FESEM, Hitachi S-8000). UV-Vis-NIR reflectance spectra (wavelength range of 220 - 2000 nm) were measured by an NIR spectrophotometer (Jasco V-670). Current density-voltage measurements were

performed under illumination with a 1 sun air mass (AM) 1.5 G Xenon lamp solar simulator by a Keithley 2400 source meter. It was calibrated using a Sharp single-crystalline silicon solar cell (BS-500).

2.3.2 Basic properties of silicon nanopencil solar cell
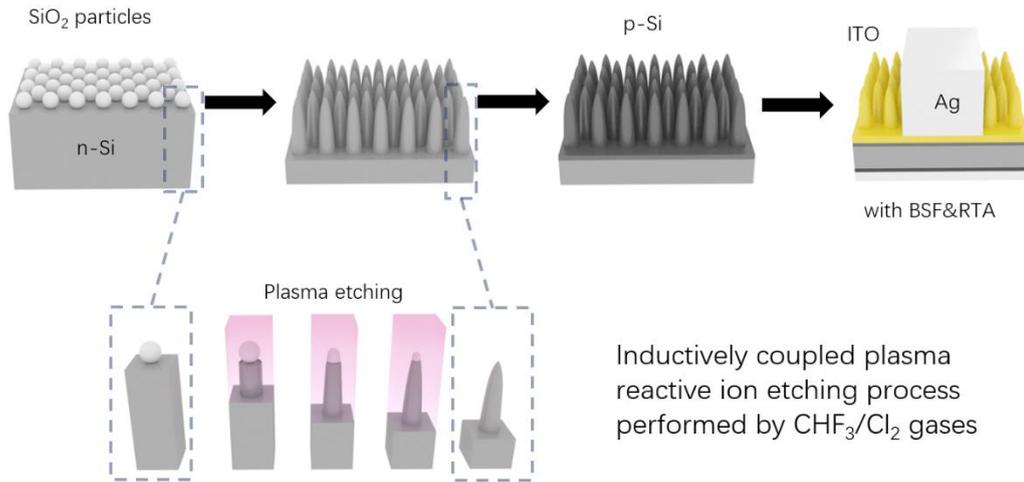
Figure 2.10 Schematic of the fabrication process of the silicon-nanopencil solar cells, from left to right: Silica-particle monolayer covering the silicon wafer surface; Silicon nanopencil arrays; p-type silicon shell formation by CVD; Formation of ITO, BSF and metal electrode layers to form the solar cell device. The bottom schematic is the formation process of the tapered structure of nanopencil by ICP-RIE. [28]
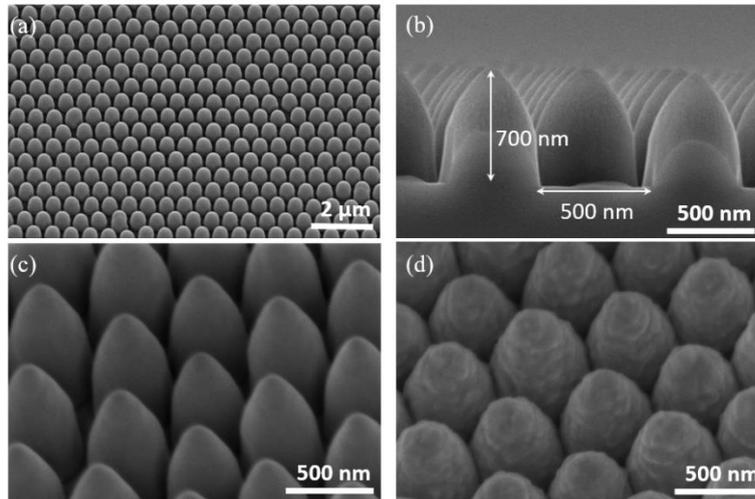
Figure 2.11 (a) 15 degree-tilted top view of nanopencils SEM image. (b) A cross-sectional view of the SEM image with the nanopencil parameters shown. (c) 30 degree-tilted view of nanopencils before and (d) after CVD p-Si shell coating. [28]

The schematic of Si nanopencils and its solar cell device fabrication processes are shown in Figure 2.10. Here, we combined the colloidal lithography and ICP-RIE process to fabricate it; the whole process is in Figure 2.10(a). An explanation schematic of the ICP-RIE process is indicated in Figure 2.10(b). The details of

the experiments are described in the above part. Further, the SEM images of nanopencils in different views are shown in Figure 2.11. It is obvious that the nanopencils show very high uniformity and an excellent staggered array, suggesting that both methods of colloidal lithography and ICP-RIE are controllable and reliable. The cross-sectional view in Figure 2.11(b) clearly shows the pencil shape of each nanopencil that the top is tapered off and their parameters which have a height of 700 nm and a pitch of 500 nm. Figures 2.11 (c) and (d) show outlook of the nanopencils structures in a 30-degree tilted, before and after p-Si shell formation. We can find that after shell formation, their surfaces became slightly roughened due to the polycrystalline nature and CVD process. The fully covered surfaces make their diameter has increased to around 600 nm.

2.3.3 Refractive-index change from the nanopencil structure
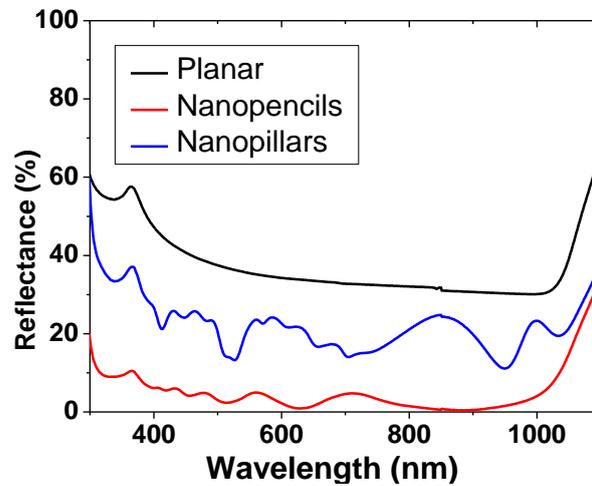
Figure 2.12 Reflectance of the nanopencils comparing with nanopillars and planar wafer. [28]
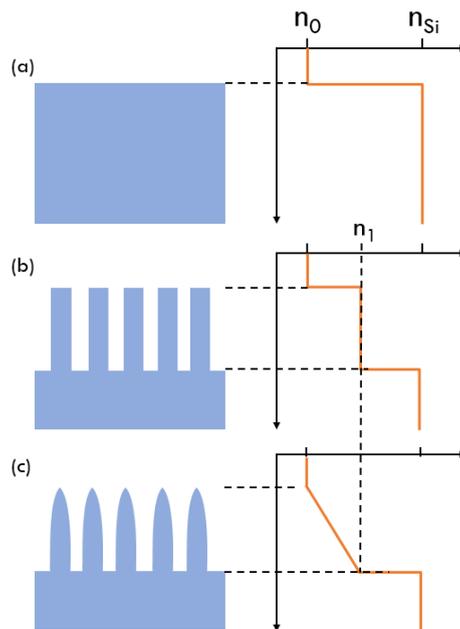
Figure 2.13 Mechanism of refractive-index change in different structures: planar wafer, nanopillars, and nanopencils.

As we described before, the UV-Vis-NIR spectral measurement is a useful and commonly used tool for investigating the light-absorbing properties of the nanostructure. The light absorption in the visible-to-NIR range (400 - 1000 nm) is vital for solar cells due to it is the most absorbable energy range. Here, to check the influence of optical properties with different structures, we measured three samples, include two dry etching nanostructures of the nanopencils, the nanopillars, and a reference of planar Si wafer. The spectrum is shown in Figure 2.12 and mechanism schematics of reflection change in Figure 2.13. The reference planar Si wafer (black line) has a very high average reflectance of around 40%. In Figure 2.13 (a), refractive-index n directly changes from n_0 to n_{Si}, which causes a considerable light reflection. The reflectance of the nanopillars sample (blue line) was low due to the light-trapping effect and the intermediate refractive-index of the nanostructure, as shown in Figure 2.13 (b). The nanostructure can be considered as an interface layer that its effective refractive index n_1 is a value between the n_0 and n_{Si}, leading to the reflection decreasing. While the reflectance of nanopencils (red line) remains at a lower level comparing with nanopillars, showing the advantage of the tapered nanopencil structure.[29] As shown in Figure 2.13 (c), it is due to the tapered tips of the nanopencils, which gives the graded change of refractive-index from n_0 to n_1. [30] Thus, the incident light is hard to be reflected. The density of nanopillars and nanopencils is also different because the lithography methods are different. This can affect their anti-reflection properties. First, it is hard to fabricate high-density nanopillar arrays due to the limitation of the quartz mold using for the nano-imprint lithography method. Because it is difficult and expensive to make a quartz mold with very small interspaces. On the other hand, high-density nanopencil arrays can be obtained by using the colloidal lithography method. This is due to that the colloidal lithography is using close-interspace SiO_2 nanoparticles as a colloidal mask. The effort of the graded change of refractive-index and the high-density are leading an excellent anti-reflection property in the nanopencils.
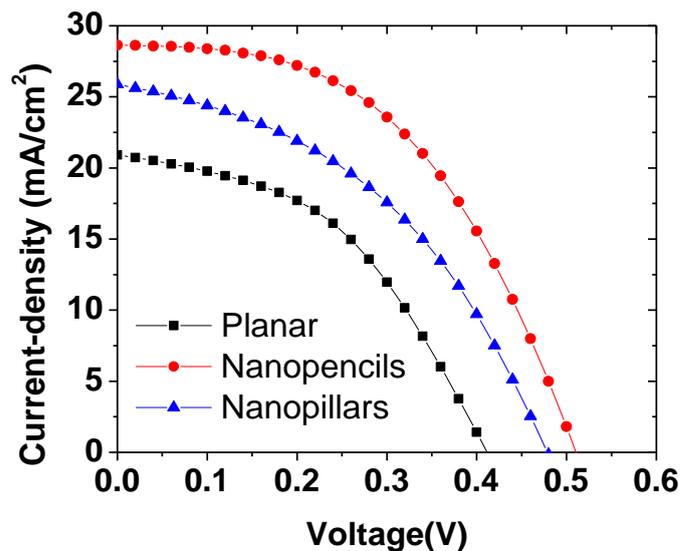
Figure 2.14 Current-Density/Voltage curves of the devices: planar wafer, nanopillars, and nanopencils. [28]

Table 2.5 Parameters of the devices: planar wafer, nanopillars, and nanopencils.

	J_{SC} (mA/cm^2)	V_{OC} (V)	FF	η(%)
Planar	20.91	0.41	0.45	3.9
Nanopillars	25.89	0.48	0.43	5.3
Nanopencils	28.64	0.51	0.49	7.2

J-V curves of device performances were measured using an AM 1.5 G solar simulator with 100 mW/cm^2 illumination, as shown in Figure 2.14. The corresponding measured properties are listed in Table 2.5. Due to high light absorption and large p-n junction area is resulting from the high surface-to-volume ratio of the nanostructures, which can, therefore, generate more photocurrent. Thus, the solar cells which based on the nanostructure of nanopillars and nanopencils show marked improvements in J_{SC}. Also, in the nanostructure, the short carrier collection lengths of nanoscale junctions further increase the collection efficiency and reduce carrier recombination, resulting in an enhanced V_{OC}. Finally, the conversion efficiency of the solar cell increased.

Moreover, the conversion efficiency of nanopillars samples shows lower than that of nanopencils sample, because of the relatively worse anti-reflection properties according to the 400-1000 nm region of the nanopillars sample, resulting in a lower current-density than the nanopencils sample. It's can be described by below formula:

$$J_{SC} = q \int_{\lambda_1}^{\lambda_2} F(\lambda)\big(1 - R(\lambda)\big)Q(\lambda)d\lambda$$

<div align="right">2-1</div>

Based on the spectrum of reflectance of the incident light from 400 nm to 1100 nm. The calculation result shows it is a ~15% improvement of J_{SC} has been obtained by reflection. In the practical device, 2.75 mA/cm^2 (11%) improvement of J_{SC} was achieved. The relative lower value may be due to that all surfaces of the nanopencils are etched, but the top of nanopillar is not. In the ICP-RIE process, the surfaces of the nanopencil structures are damaged by the plasma and led to high roughness with many surface states. These surface states act as recombination centers for photo-generated carriers, which reduce the $Q(\lambda)$, and the J_{SC} is not increasing as expected.

2.3.4 CPE treatment for silicon nanopencil solar cell

So, many methods have been investigated to reduce this problem of the surface states, including the passivation via the formation of an intrinsic Si layer, [31,32] hydrogen termination, [33,34] thin SiO$_2$,[35] and even the formation of a fluorinated alkyne-derived layer.[36] We report here a simple method called

chemical polish etching (CPE) treatment to smooth the nanopencil surfaces and reduce the number of surface states. The main advantage of CPE treatment is simple and cost reductions, due to it can be done at room temperature and in the ambient atmosphere.
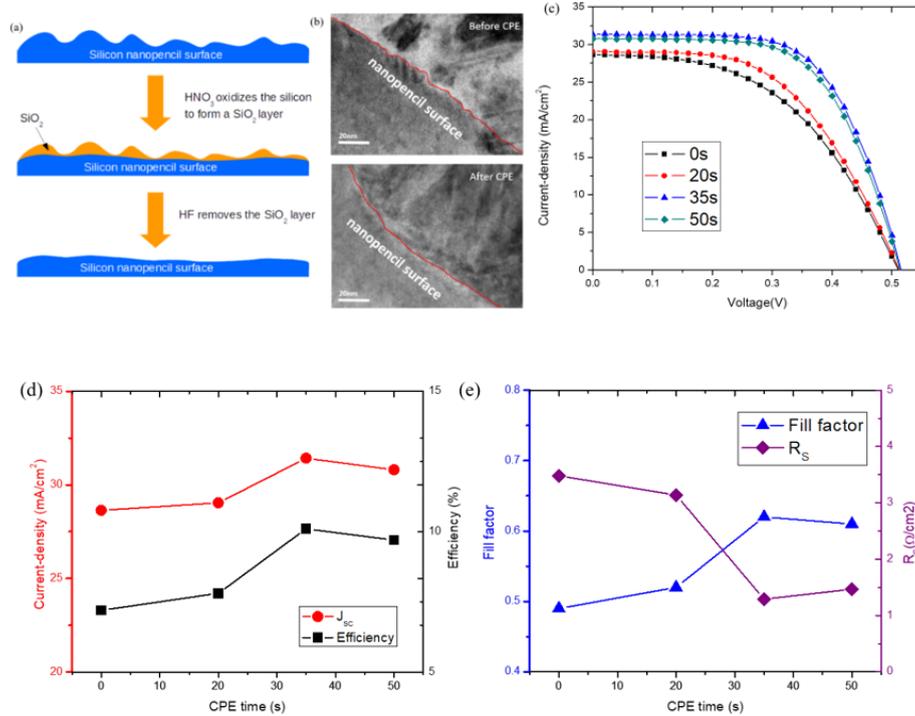
Figure 2.15 (a)Schematics of the SiNP surface before and after CPE treatment. (b) TEM images of the SiNP surface before and after CPE treatment. (c) J-V curves of solar cell device for SiNPs with different time CPE treatment. (d) Current density and efficiency are plotted as a function of CPE time. (e) Fill factors and series resistance are plotted as a function of CPE time. [28]

Table 2.6 Performance of solar cell devices, SiNPs are on different time CPE treatment.

CPE time (s)	J_{SC} (mA/cm^2)	V_{OC} (V)	FF	R_S (Ω/cm^2)	η (%)
0	28.64	0.51	0.49	3.48	7.2
20	29.04	0.51	0.52	3.14	7.8
35	31.43	0.52	0.62	1.29	10.1
50	30.81	0.51	0.61	1.47	9.7

The mechanism of CPE treatment is shown in Figure 2.15(a). The original surface of nanopencil is rough due to the damage from the plasma process. Then, the CPE treatment is based on the HF/HNO$_3$ mix solution. The HNO$_3$ solution is an oxidant that forms SiO$_2$ on the nanopencil surfaces, and HF is an etchant that simultaneously removes the SiO$_2$ layer. Rough surfaces are etched faster than smooth surfaces due to their larger contact area with the HNO$_3$ and HF. Thus, nanopencil samples were immersed in the solution and leading to a smooth surface. In Figure 2.15(b), TEM images give the evidence, that before the CPE treatment,

a rough surface is clearly observed as a marked red line. Then, a smooth surface is obtained after the CPE treatment, and the surface defect has been removed.

Also, optimization of the CPE treatment in various etching time was investigated; the corresponding J-V curves of the devices are in Figure 2.15(c). The estimated properties are listed in Table 2.6. First, the 20s of CPE (red line) was done, minor improvements of J_{SC}, V_{OC}, and FF were found, and the overall increase in efficiency is, therefore, only 0.5 %. This is because of CPE treatment in the 20s is too short to sufficient remove amounts of the surface states. Thus, the CPE time was increased to 35 s (blue line) to reduce surface states further. It obtains a significant improvement in efficiency to 10.1 %, due to the significant enhancement in J_{SC}, which increased to 31.43 mA/cm^2. However, when further increased the CPE time to 50s (cyan line), the performance did not improve as expected, and J_{SC} fell: this was due to a reduction in the total surface area and effective p-n junction areas by extended etching. The trend of J_{SC} and efficiency in different CPE etching time are in Figure 2.15(d), it is evident that the reduction of the surface states by CPE treatment increases carrier lifetime, resulting in the larger current-density and higher efficiency. A 35s etching time of CPE treatment is the optimized condition.

Furthermore, in Table 2.6, we found that the series resistance (R_s) reduced by a smooth surface created by CPE treatment, and the fill factor (FF) increased at the same time. A trend of R_S and FF in different etching times of CPE treatment is indicated in Figure 2.15(e). Here, ΔFF_S, the reduction in fill factor can be described by below formula, is given by[37]

$$\Delta FF_s = -\frac{J_{SC}}{V_{OC}} \times R_s \times FF_{ideal} \qquad 2\text{-}2$$

and FF$_{ideal}$ can be estimated by[38]

$$FF_{ideal} = \frac{v_{OC} - \ln(v_{OC}+0.72)}{v_{OC}+1} \qquad 2\text{-}3$$

where V_{OC} is defined as a "normalized V_{OC}", the ideal factor n is assumed to be 1, q is the absolute value of electron charge; k is Boltzmann's constant; and T is absolute temperature (K).

$$v_{OC} = \frac{q}{nkT} V_{OC} \qquad 2\text{-}4$$

Thus, base on the above three formulas, we estimated the ΔFF_S. In the sample without CPE treatment, J_{SC} is 28.64 mA/cm^2, and V_{OC} is 0.51 V. With an R_S of 3.48 Ω/cm^2, we can calculate that the ΔFF_S is 0.157. In the optimized sample with 35s CPE treatment, a 31.43 mA/cm^2 J_{SC} and 0.52V V_{OC} were obtained. The R_S falls to 1.29 Ω/cm^2; the ΔFF_S is calculated to be 0.063. The difference in ΔFF_S in these two samples is around 0.09, which means improvement of FF can be achieved with a reduction of R_S by the CPE treatment. In the real device, a 0.13 increasing in FF was found. It indicates that the reduced R_S is the primary reason for the increased FF, which corresponds to Figure 3(e). These significant improvements in device performance by introducing CPE treatment and optimizing the CPE treatment conditions, demonstrating that CPE treatment effectively

reduces the surface states and decrease carrier recombination. CPE treatment, therefore, is a useful process of nanopencils for solar cells device.

2.3.5 Optimization of the morphology and wafer thickness

After we achieved the smooth surface of nanopencil, with fewer surface states, by the CPE treatment, we think to optimize the morphology of nanopencil further. In the previous section of the silicon nanowire solar cells, we have described some efforts to increase light absorption and junction area by using high nanowire density. Then we reduced surface states by shortening the nanowire length to limit the surface area. It is because that the correct balance between effective junction area and surface state over a large surface area is vital for the solar cell device performance. Here, the structure and alignment of nanopencil need to be further optimized by varying their parameters of height and pitch.
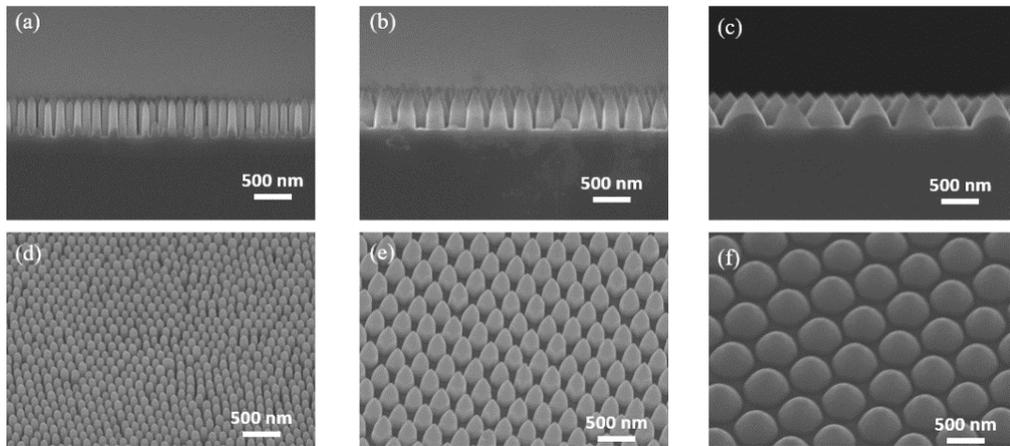
Figure 2.16 SEM images of different pitch nanopencils, (a), (b), (c) cross-sectional views of 120 nm, 300 nm, 600 nm pitch samples; (d), (e), (f) 30º tilted views of 120 nm, 300 nm, 600 nm pitch samples. [28]
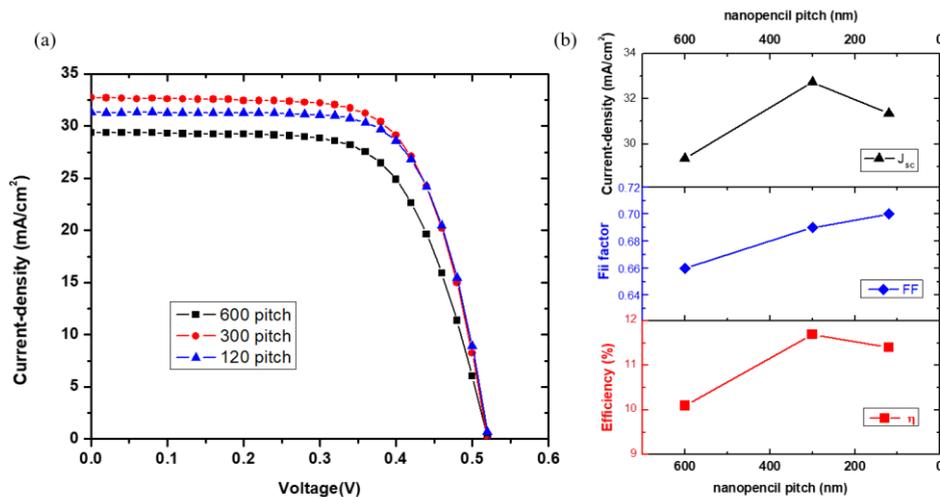
Figure 2.17. (a) J-V curves of nanopencil solar cells with the same height and different pitch. (b) Current-density, fill factors and efficiency are plotted as a function of nanopencil pitch. [28]

Table 2.7 Performance of solar cell devices based on the different pitches nanopencil.

Pitch	height	J_{SC} (mA/cm²)	V_{OC} (V)	FF	R_S (Ω/cm²)	η(%)
600	500	29.36	0.52	0.66	0.97	10.1
300	500	32.73	0.52	0.69	0.64	11.7
120	500	31.34	0.52	0.70	0.59	11.4

Three samples of different nanopencil lengths were prepared, with the same height of 500 nm and different pitches of 120, 300, 600 nm each, all these samples are after the surface state reduction by CPE treatment. The SEM images were shown in Figure 2.16: (a), (b), (c) are the cross-sectional views of samples with 120 nm, 300 nm, 600 nm pitch; (d), (e), (f) are the 30º tilted views of samples with 120 nm, 300 nm, 600 nm pitch. All these samples were subjected to CPE treatment. These SEM images indicate the outlook of nanopencils with different morphology. Large space between nanopencils was found in the 600 nm pitch sample while the nanopencil close to each other in the 120 nm pitch sample. A 300 nm pitch sample is in the medium state between the above two samples.

To check the influence of morphology on solar cell performance, we continue to fabricate the device. Figure 2.17(a) is the J-V curves of solar cells with 120 nm, 300nm, 600 nm pitch, and Table 2.7 shows the estimated parameters. A clear trend can be found in Figure 2.17(b) in which current density, fill factors, and efficiency is plotted as a function of nanopencil pitches. We first found that when the nanopencil pitch decreased from 600 to 300 nm, a higher FF and J_{SC} were obtained; therefore, it achieved higher efficiency. This improvement of J_{SC} is due to the increase in the effective junction area, which can generate more charge-carrier and separate them. The increasing of FF is from the decreased R_S for the same reason as before. It caused by the better continuous of surface electrical metal contact in a closed space between the nanopencils. Furthermore, when the pitch of nanopencils keeps decreasing to 120 nm, FF improves as before, which means the decreasing of R_S still works. But the reduction of J_{SC} limits the total efficiency lower than the sample with 300 nm pitch. This is because of the surface states increasing from the higher area counteracts the beneficial effects of the increasing effective junction area. Thus, a solar cell with nanopencils in 300 pitch shows a better performance with 11.7% efficiency due to the optimized balance between effective junction area and surface states.
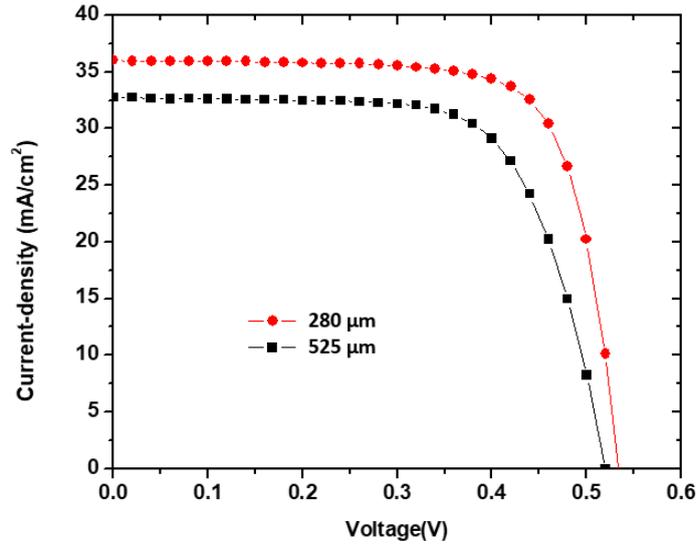
Figure 2.18 J-V curves of SiNP solar cells with different wafer thickness. [28]

Table 2.8. Performance of the silicon nanopencil solar cell devices, based on different wafer thickness.

Wafer thickness (μm)	J_{SC} (mA/cm^2)	V_{OC} (V)	FF	η(%)	R_S (Ω/cm^2)
280	36.00	0.53	0.75	14.3	0.32
525	32.73	0.52	0.69	11.7	0.63

In traditional silicon solar cells, it needs enough thickness of the bulk material to absorb the light. This is because of the Si material is an indirect bandgap semiconductor that is hard to absorb photons. As we introduce before, one of the most vital advantages of nanopencil solar cells is an excellent anti-reflection property, which makes it possible to use thinner silicon wafers. Here, to check the influence of different wafer thickness, we investigated nanopencil solar cells based on silicon wafers of 280 μm and 525 μm thick. Thus, the solar cell samples with different thicknesses were fabricated, the J-V curves are shown in Figure 2.18, and parameters are shown in Table 2.8. We can clear found very significant improvements J_{SC} was obtained, increasing from 32.73 mA/cm^2 to 36.00 mA/cm^2. This improvement of J_{SC} is mainly because of the reduction of the bulk carriers' recombination or the increase of the carriers' lifetime by using the thinner wafer. Therefore, the carriers can be more effectively collected and then generate a higher current circuit.

Moreover, significant improvements were also observed in FF. As we discussed in the previous parts of CPE treatment, the FF value is highly related to the series resistance of the device (R_S), which includes the R_S of the substrate, R_S of the surface, R_S of the contacts and other R_S.[37]

$$R_S(total) = R_S(substrate) + R_S(surface) + R_S(contact) + R_S(others) \qquad \text{2-5}$$

The R_S of the substrate, therefore, depends on the bulk resistivity (ρ) of the wafer and its thickness (T_W). Because the ρ is the same in the silicon wafer, R_S of the substrate is only changed by the wafer thickness.

$$R_S(substrate) = \rho \times T_W \qquad \text{2-6}$$

In the devices of 280-μm sample, the total R_S is only 0.32 Ω/cm^2: this falls 50.7% with the 525-μm sample (0.63 Ω/cm^2). The ratio of the total R_S decrease is very close to the wafer thickness reduction ratio of 525 μm to 280 μm (53.3%). Thus, the reduction of total R_S can be chiefly attributed to the decrease by the R_S of the substrate with a thinner wafer. Therefore, we can conclude nanopencil solar cell based on a thinner wafer effectively enhances efficiency by increased J_{SC} and FF.

2.4 Summary

In this chapter, the nanostructure morphologies were investigated. There are three different methods were used to fabricate the nanostructures included of nanowires (formed by MCEE), nanopillars (formed by NIL and dry etching) and nanopencils (formed by CL and dry etching). All these nanostructures have outstanding anti-reflection properties compared with the planar wafer.

1. The better anti-reflection property of the three nanostructures (nanowires, nanopillars and nanopencils) give a good improvement of J_{SC} in silicon nanostructures homojunction solar cell devices.

2. Pre-oxidation treatment was introduced to silicon nanowires by the UV/Ozone. It successful increased nanowires density, and obtained better anti-reflection property due to its enhanced light-trapping effect.

3. A silicon nanopencils structure was developed. It gives a graded-refractive-index and higher density, resulting in a better anti-reflection compared with the silicon nanopillars structure.

4. The shapes and morphologies of three nanostructure were optimized for better solar cell efficiency.

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Chapter 3.   A novel design of front metal electrodes

A vital solution to reduce the optical loss is to minimize shading loss by decreasing the area of front electrodes in solar cells. Many studies have been made using conventional bus/finger bar electrodes. Because the metal reflects the incident light, it gives an optical loss (normally called "shading loss") of the device. In general, 10%-20% of the total area is metal electrodes in commercial solar cell devices. These shading losses reduce device performance. In this study, micro-grid electrodes were investigated to decrease shading loss and improve carrier transfer by taking advantage of the short distance between the metal lines. [1–6] More efficient photocarrier collection with the micro-grid electrodes gives a higher photocurrent output, resulting in an improvement of J_{sc}.

3.1 Mechanism of the micro-grid electrodes
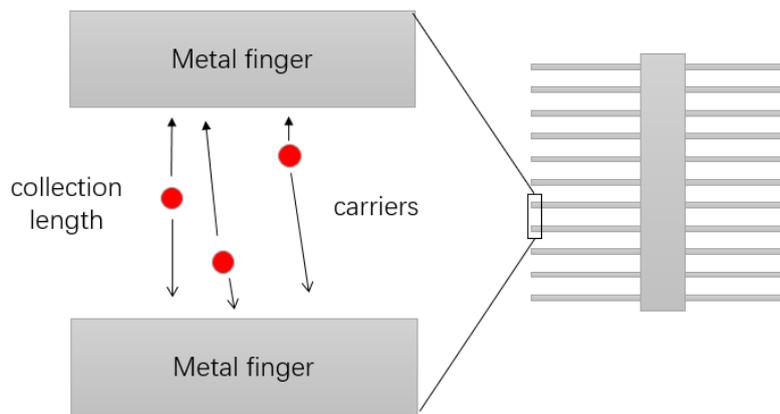
Figure 3.1 Schematics of carriers' collection process in the metal electrodes

A schematic of conventional electrodes, as shown in Figure 3.1. In the photovoltaic process, the photo-generated carriers need to be collected as soon as possible. The distance of carriers to the metal finger called "carriers collection length", which shorter is better due to carrier recombination occur during the collection process. But on the other hand, reducing the distance of metal fingers, the total metal area on the surface will increase. Thus, the active areas decrease, which also not beneficial to solar cell device efficiency.

Thus, to solve this trade-off, we used a micro-grid to make front electrodes consisting of a mesh pattern with a width of 5 μm and a spacing of 400 μm. The corresponding schematic illustrations of fabrication processes are shown in Figure 3.2. The first advantage of micro-grid electrodes comparing with conventional electrodes are the minimization of shading loss by decreasing the top electrode area. Compared to our conventional bus/finger bar electrodes, which cover more than 10% of the top area, micro-grid electrodes decrease this to 5%, improving current density.
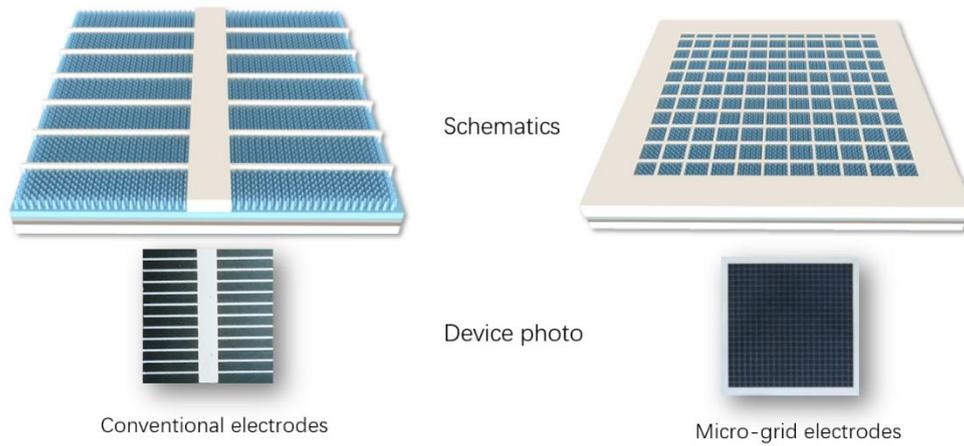
Figure 3.2 Schematics and photos of conventional electrodes and micro-grid electrodes.[7]

Another is that carriers can be collected more efficiently than in conventional electrodes. [8] As shown in Figure 3.3, it reduces the carrier recombination chance; therefore, the power loss. Because of the shorter carrier path and uniformly distributed micro-grid electrodes, photocarriers can be effectively collected before recombination.
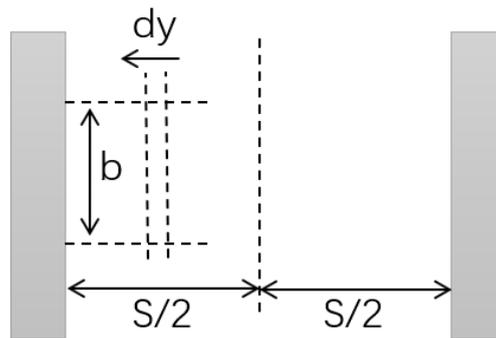
Figure 3.3 Schematic of the power loss between the metal fingers

The power loss can be described as below:

$$P_{loss} = \int I(y)^2 dR = \int_0^{S/2} \frac{J^2 b^2 y^2 \rho dy}{b} = \frac{J^2 b \rho S^3}{24}$$

3-1

J is the current-density; ρ is the sheet resistivity, b is the distance along the finger; S is the distance between two grid fingers. Thus, after calculation, it shows that the micro-grid electrodes can reduce more than 50% of the power loss.

Moreover, for the nanostructure solar cell, micro-grid electrodes would be more effective than a planar solar cell. The schematics were shown in Figure 3.4. Because of the large surface area of the nanostructure device. When we applied the micro-grid electrodes to reduce the top metal area, the nanostructure device

would be able to obtain a more effective junction area due to its 3D structure and large surface area. This feature helps nanostructure devices benefit more than the planar device.
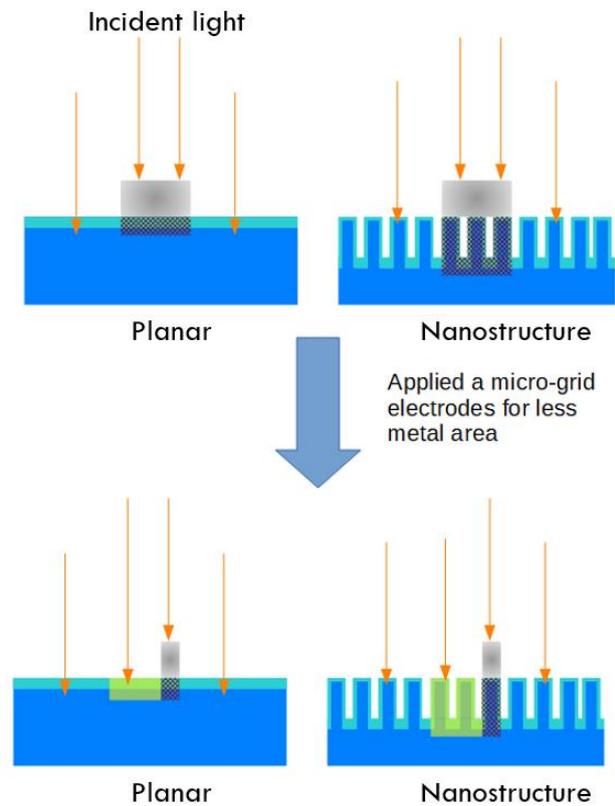
Figure 3.4 The schematics of planar and nanostructures by using micro-grid electrodes. [7]
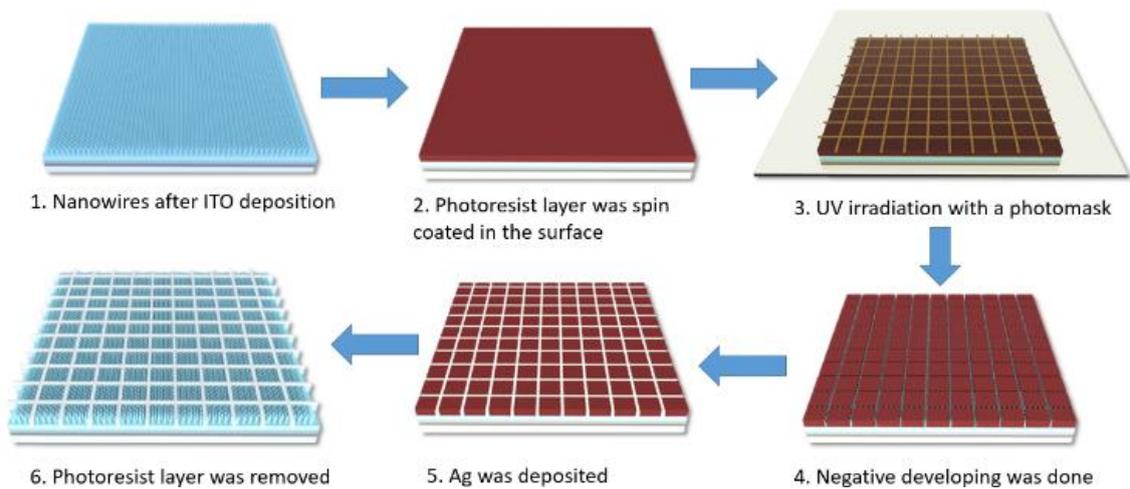
Figure 3.5 Schematic illustration of micro-grid electrodes fabrication processes. [7]

The schematics illustrations of the photolithography process for micro-grid electrodes fabrication were shown in Figure 3.5. First, a photoresist layer was spun on the surface of the silicon substrate after grow the p-Si shell and the ITO deposition. Next, the sample was irradiated under a UV lamp through a micro-grid pattern photomask. Then, the sample was negative-developed to remove the unirradiated part. Finally, Ag was deposited at the front surface by sputter, and the photoresist layer was removed by acetone to finish the micro-grid electrodes.

3.2 Micro-grid electrodes for different nanostructure solar cells

3.2.1 Wet etching-nanowires based solar cell

In the silicon solar cell device, because the incident light cannot be transmitted to the back surface, we assume that all the incident light is either absorbed or reflected. [7] Moreover, the incident light cannot transmit the front metal electrodes. Thus a portion of the incident light will be reflected. So that the total optical loss increases and the absorbable incident light of the p-n junction are reduced. In Figure 3.6, the reflectance spectra of UV-vis-NIR was shown to investigate the light reflection changes from conventional electrodes to micro-grid electrodes. It is obvious that the reflectance spectra of the two electrodes demonstrated very similar profiles but different absolute values, indicating that the improvement due to the reduction of optical loss. This is due to the metal areas of micro-grid electrodes are smaller than those of conventional electrodes. Therefore, in silicon nanowire solar cells, the micro-grid electrodes have better anti-reflection property than the conventional electrodes, as their less optic loss.
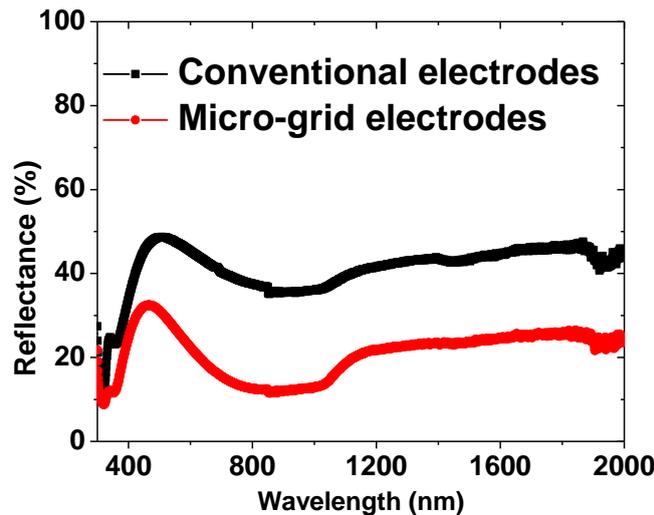
Figure 3.6 Reflectance spectrum of silicon nanowire solar cells with conventional and micro-grid electrodes. [7]

Silicon nanowire solar cells with conventional and micro-grid electrodes were fabricated, J-V curves of devices are shown in Figure 3.7. The parameters include V_{OC}, J_{SC}, FF, and efficiency, as indicated in Table

3.1. We found that the J_{SC} is the main difference in the parameters between the conventional-electrodes solar cell and the micro-grid-electrodes solar cell, which increased by almost 18% from 23.66 to 27.84 mA/cm^2. It is due to the use of micro-grid electrodes, which both reduce the optical loss by less metal area and power loss by shorter fingers space. There is no loss in FF or V_{OC} despite a reduction of the total metal electrodes area. The significant improvement of J_{SC} (4.18 mA/cm^2) helps the device efficiency increased by 1.5%.
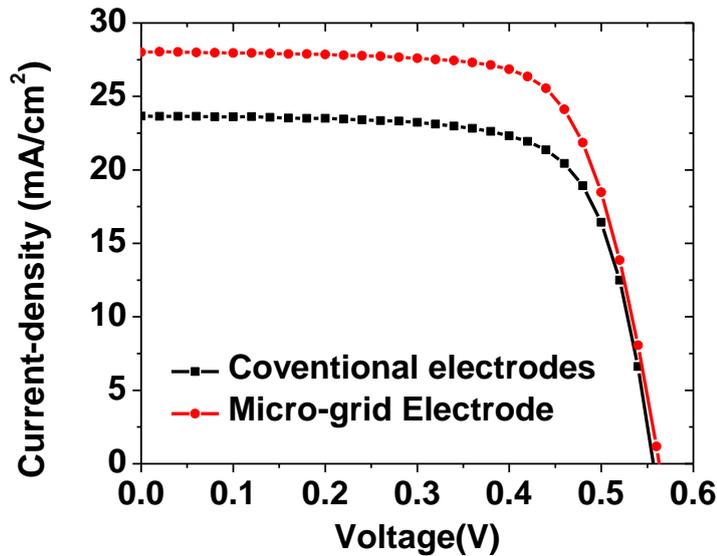
Figure 3.7 J-V curves of devices in conventional and micro-grid electrodes. [7]

Table 3.1 Parameters of the solar cells of conventional and micro-grid electrodes.

Electrodes	J_{SC} (mA/cm^2)	Voc (V)	FF	η (%)
Conventional	23.66	0.56	0.72	9.4
Micro-grid	27.84	0.56	0.70	10.9

3.2.2 Dry etching-nanopillars based solar cells

In silicon nanopillar solar cell fabricated by dry etching, we also applied micro-grid electrodes to enhance efficiency. The silicon nanopillar solar cells with conventional and micro-grid electrodes were fabricated, the J-V curves are shown in Figure 3.8. The corresponding parameters include V_{OC}, J_{SC}, FF, and efficiency, which are summarized in Table 3.2. Same with the nanowire solar cell, after introducing the micro-grid electrodes, the J_{SC} increased from 24.00 to 26.58 mA/cm^2 due to the reduced optical loss. These enhancements raised the total solar cell efficiency to 9.5%, showing that micro-grid electrodes also can obtain better properties than conventional electrodes for silicon nanopillar solar cell.
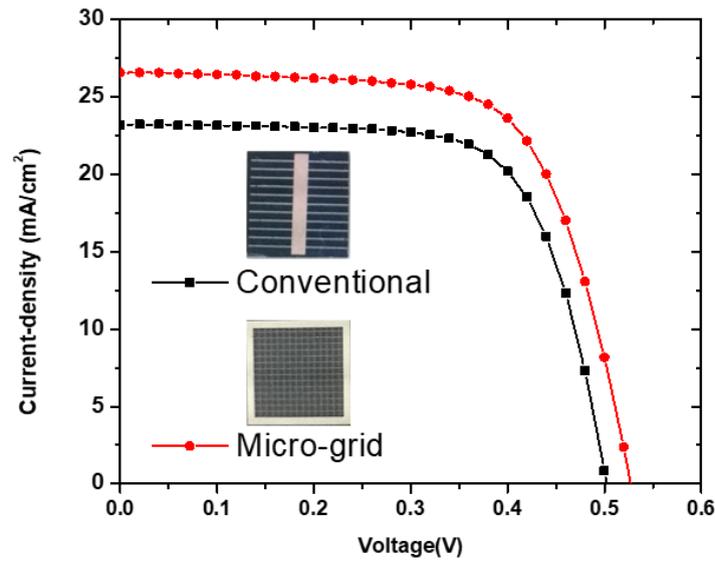
Figure 3.8 J-V curves of the solar cell device with conventional and micro-grid electrodes (inset: the device photos).[8]

Table 3.2 The parameters of solar cell device with conventional and micro-grid electrodes

Electrodes	J_{SC} (mA/cm^2)	V_{OC}(V)	FF	η(%)
Conventional	24.00	0.50	0.69	8.3
Micro-grid	26.58	0.53	0.68	9.5

3.3 Optimization of different patterns for micro-grid electrodes

After we successfully applied the micro-grid electrodes into nanostructure solar cell device. Another part can be further discussed, which is the micro-grid pattern. Because the advantage of micro-grid electrodes is the reduction of the metal area. Thus, we hope to tile the surface with the least metal. This can be solved by the honeycomb conjecture, as shown in Figure 3.9. [10,11] It states the bees build their house in a hexagonal pattern because it is using the least materials for the same areas. It means a regular hexagonal grid or honeycomb structure is the best way to divide a surface with the least total perimeter. Therefore, if we fabricate the micro-grid in a hexagonal pattern, it will further reduce the total surface metal areas.
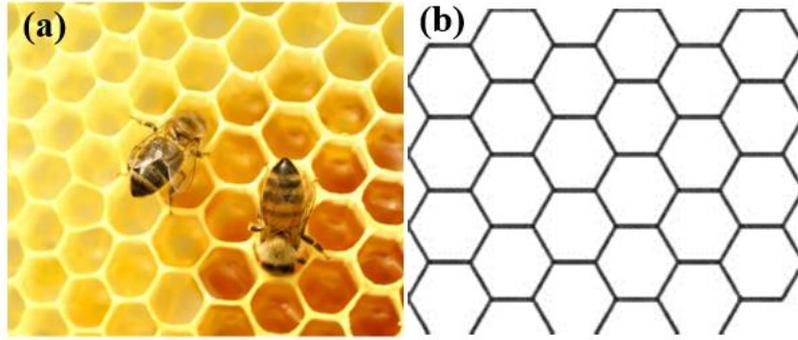
Figure 3.9 The honeycomb photo and a schematic of the hexagonal grid

Therefore, we designed three different patterns of the micro-grid electrodes; there are shown in Figure 3.10: (a) is the square grid the same as previous, (b) is a reference triangle grid and (c) is the hexagonal grid. The parameters were designed by the rule that all the longest distance to the center is the same ($200\sqrt{2}$ µm) so that the carrier collection length is very close in three patterns samples.
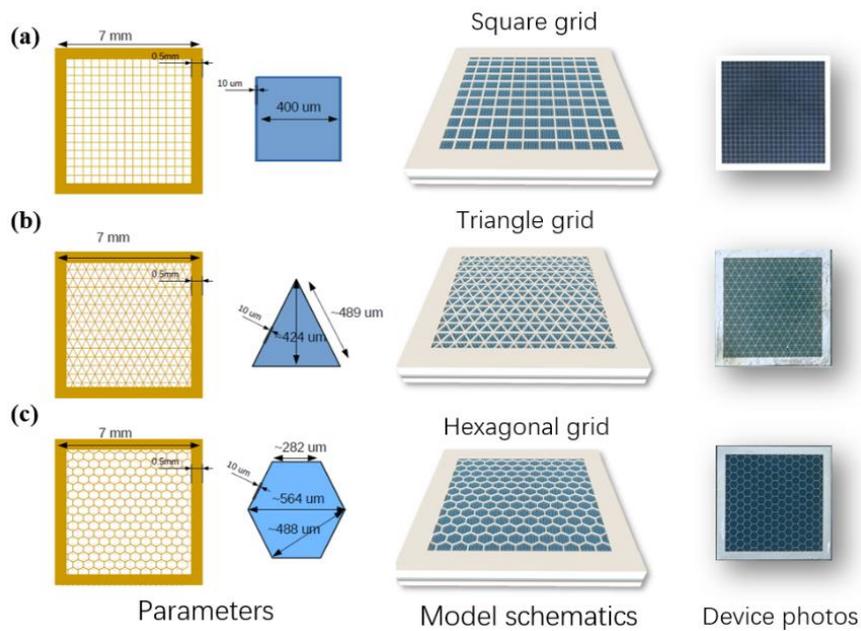
Figure 3.10 The parameters, model schematics, and photos of three patterns of micro-grid electrodes.

The three solar cell devices of the different micro-grid pattern were measured, and the J-V curves were shown in Figure 3.11, and corresponding parameters are in Table 3.3. We can find that from the square grid change to the hexagonal grid, the J_{SC} has increased from 31.28 to 31.80 mA/cm^2, while it decreased to 28.92 mA/cm^2 in the triangle grid. It clearly indicated the benefit of less metal area in the hexagonal grid that more active area was obtained. Meanwhile, FF of three patterns also shown a similar trend; it may be due to the contact resistance reduction of less metal.
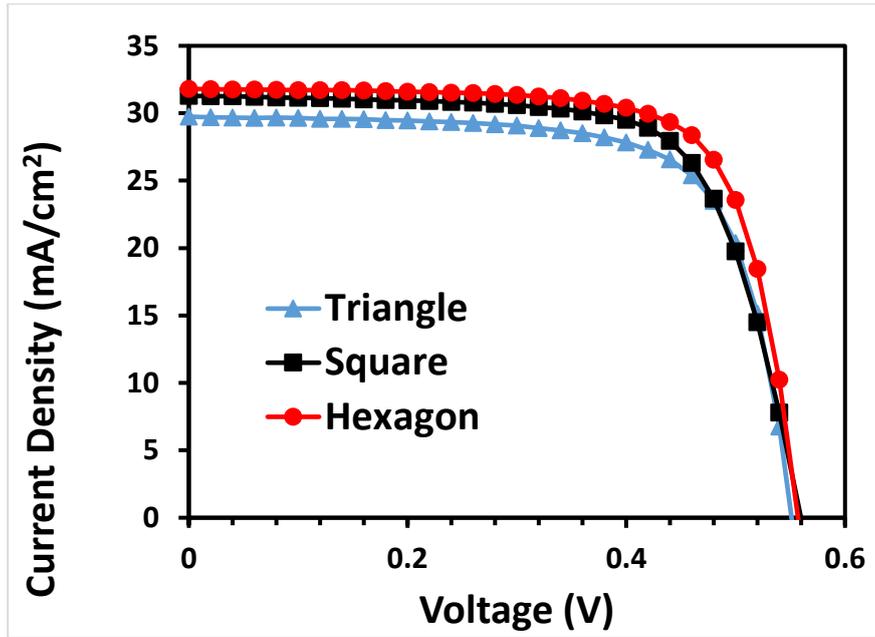
Figure 3.11 The J-V curves of three patterns of micro-grid electrodes samples.

Table 3.3 Parameters of micro-grid electrodes samples with three grid patterns.

Patterns	J_{SC} (mA/cm²)	V_{OC} (V)	FF	η(%)
Triangle	28.92	0.55	0.69	11.0
Square	31.28	0.56	0.71	12.4
Hexagon	31.80	0.56	0.73	13.0

To more obviously described the relation between the metal area ratio and the J_{SC}, a figure is shown in Figure 3.12. The value of the metal area ratio comparing with J_{SC} was listed in Table 3.4. It includes the change of J_{SC} and metal area ratio value in three pattern samples. From the triangle sample to square sample, the metal area ratio reduced a lot of 32%, so that a significant J_{SC} increase was obtained from 28.92 to 31.28 mA/cm², which increased around 8%. When it changed from square sample to hexagon sample, the metal area ratio only reduced approximately 13%, thus J_{SC} also only increase by 1.6% from 31.28 to 31.80 mA/cm². It can be clearly concluded that the reduction of the metal area ratio is highly linked with the increase of J_{SC} in the solar cell, due to it is the only variable factor in the samples. It is evident that we achieved to obtain higher J_{SC} through the better optical property by reduction of shading loss in the surface using a different pattern of micro-grid electrodes. In conclude, the hexagon is the most suitable pattern for micro-grid electrodes.
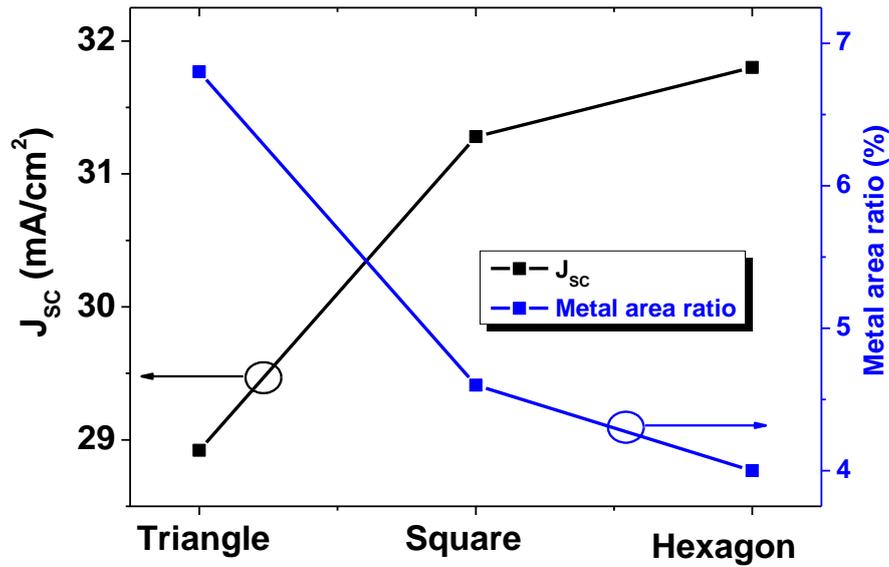
Figure 3.12 The metal area ratio and J_{SC} trend in three patterns of micro-grid electrodes samples.

Table 3.4 Parameters of micro-grid electrodes samples with three grid patterns.

Patterns	J_{SC} (mA/cm^2)	Metal area ratio
Triangle	28.92	~6.8%
Square	31.28	~4.6%
Hexagon	31.80	~4%

3.4 Summary

In this chapter, we focus on investigating the surface electrode for Si nanostructure solar cells. We aim at reducing the optical loss by minimizing shading loss of the surface, which can be obtained by reducing the area of front electrodes. We also hope to keep a good collection of the carriers at the same time.

1. We established a novel structure of micro-grid electrodes by using the lithography process. It effectively increases the active area by reduction of metal area and shortens the carrier collection length by a close distance of metal fingers. Both two advantages give an enhancement of the J_{SC} in the solar cell device.

2. A hexagonal pattern was developed of the micro-grid electrodes. It further reduced the shading loss of metal for achieving higher active areas, resulting in higher J_{SC} and solar cell efficiency.

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Chapter 4.   Effect of silicon quantum dots: Energy transfer

As we described in Chapter 1, the J_{SC} of the solar cell is related to the generation and collection of light-generated carriers. It is mainly affected by two reasons: the optical properties (includes absorption and reflection) and the collection probability. In the previous two chapters, lots of works were done to achieve the better property of the light anti-reflection. However, some problems of light absorption also limit J_{SC}.

4.1 The unique property of Si QDs for enhancing light absorption
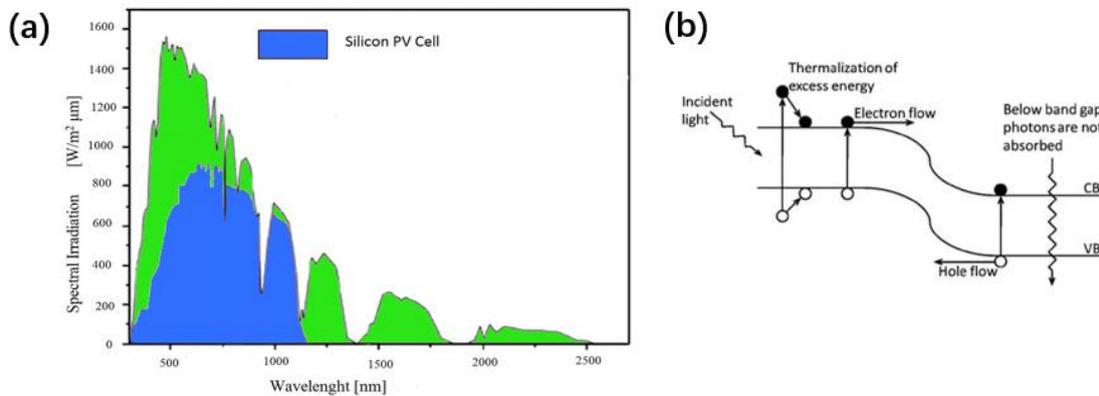
Figure 4.1 (a) The solar spectrum and absorption spectrum of a typical silicon solar cell, (b) Shockley–Queisser limit of the solar cells. [1,2]

One of the problems is the absorption spectra of the silicon bulk material. In Figure 4.1(a), it shows that the spectral distribution of sunlight (AM 1.5G) range from 280–2500 nm.[3] But the absorption spectra of Si solar cells only utilize a relatively small fraction of the solar photons, which is mainly in 400 to 1100 nm range. Thus, there are still an amount of energy of sunlight can't be absorbed by Si solar cell, including the light wavelength lower than 400 nm or higher than 1100 nm.

Figure 4.1(b) shows the reasons for the absorption wavelength range in bulk Si materials, which normally called Shockley–Queisser limit.[2,4–6] It is attributed to that the material responds to a narrow range of photons whose energy is matching the bandgap of the material. In principle, only the photons whose energy higher than the bandgap can be absorbed, but the excess energy is also not effectively used and released as heat. During the conversion process from incident solar energy to electricity in silicon-based solar cell, it is approximately 50% of energy are lost, due to the thermalization of photons whose energy is exceeding the bandgap and non-absorption of photons whose energy is less than the bandgap.
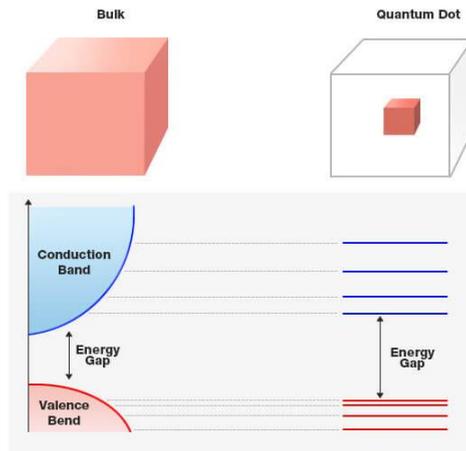
Figure 4.2 Energy gap distribution in the bulk and quantum dot materials.[7]

Therefore, much research was done to solve this problem, for example, by using up-conversion and down-conversion materials.[8–11] These materials can convert the light to a lower or higher wavelength. However, these materials are basically based on rare earth elements that limit its usage. Moreover, the conversion efficiency are also not enough.

Recently, quantum dots research has a huge increase in various applications and devices.[12–16] One of its features is the splitting of energy levels, and it leads to a lot of unique properties. Due to the number of overlapping energy levels decreases, it is resulting in a large width between the band. Thus, the energy gap is enlarged in the quantum dots. Thus, the QDs can absorb the high energy photons of the low wavelength range. This property makes it possible to be used for the solar cells to absorb the energy that bulk silicon can't. The major advantages of Si QDs are abundant in silicon materials and no toxic (not like CdSe or PbS QDs).[17,18] Therefore, our purpose in this chapter is enlarging the absorption spectrum and improving the J_{SC} of Si solar cell by the Si QDs.

4.2 Experimental of surface passivated Si QDs
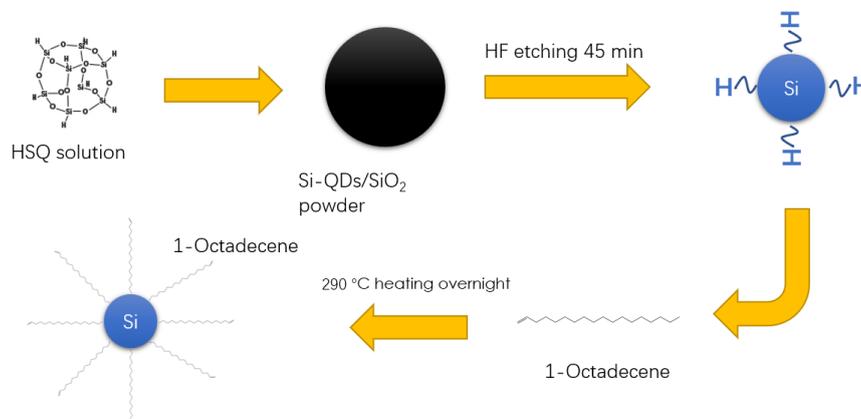
Figure 4.3 The schematic process of Si QDs from an HSQ solution

The schematic process is shown in Figure 4.3. The fabrication process can be divided into two steps: (1) Si QDs/SiO$_2$ powders and (2) surface passivated Si QDs. [19,20] The photo records of the procs were indicated in Figures 4.4 and 4.5.

(1) Experiments are started with an H-Si-O material called hydrogen silsesquioxane (HSQ), which was purchased from Dow Chemical and used as received. The HSQ was dissolved in an organic solvent. First, the solvent was removed using a rotary evaporator in a water bath at 40 °C under 75 Pa. After around 1 hour, the solvent was gone and left a gel of HSQ. This gel was then dried under vacuum overnight. The resultant white solid, as shown in Figure 4.4, was placed in a quartz crucible and transferred in an inert atmosphere to a high-temperature furnace. The thermal annealing was done at 1100 °C for 1h in an atmosphere of 95% Ar and 5% H$_2$. A dark brown solid was obtained after annealing and cooling to room temperature, which is the Si QDs/SiO$_2$ mixtures. These mixtures were then mechanically ground by a mortar and pestle, and finally, they were yielded into a fine powder.

(2) In a typic experiment, 200 mg of Si QDs/SiO$_2$ powder was added to a mixture of 2 mL of deionized (DI) water and 2 mL of ethanol with 1 min sonication mix. Then 2 mL of HF was added, and the mixture solution was stirred for 30 min to achieve the acidic etching of the SiO$_2$ matrix and a gradual decrease in the size of the core Si. Next, hydride-terminated Si QDs were separated with excess toluene, and the supernatant extra solution was decanted. After, the product was transferred into a round-bottomed flask and dried under a dry Ar flow to obtain a powder of Si QDs. 10 mL of 1-octadecene solution was added and degassed for 1 h by Ar bubbling. The reaction was carried out at 290 °C overnight in Ar ambient to passivate the surface of hydrogen-terminated Si QDs by the 1-octadecene. After, the resulting transparent light-yellow solution was purified with a 1:1 ratio mixture of ethanol and methanol to remove the excess 1-octadecene. Finally, 5 mL of toluene was added to obtain 1-octadecene passivated Si QDs solution.

HSQ after evaporation   Annealing to generate Si-QDs/SiO$_2$ Yield the mixture in mortar
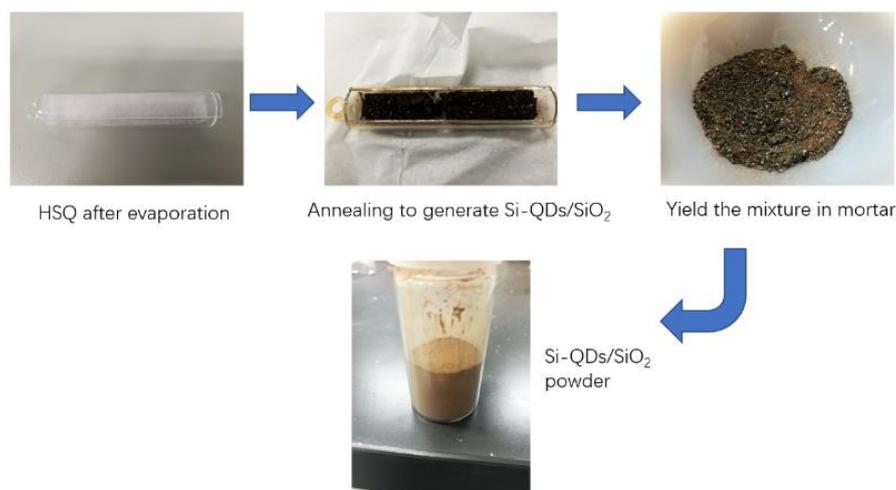
Si-QDs/SiO$_2$ powder

Figure 4.4 Photo records of the Si QDs/SiO$_2$ powder fabrication process.
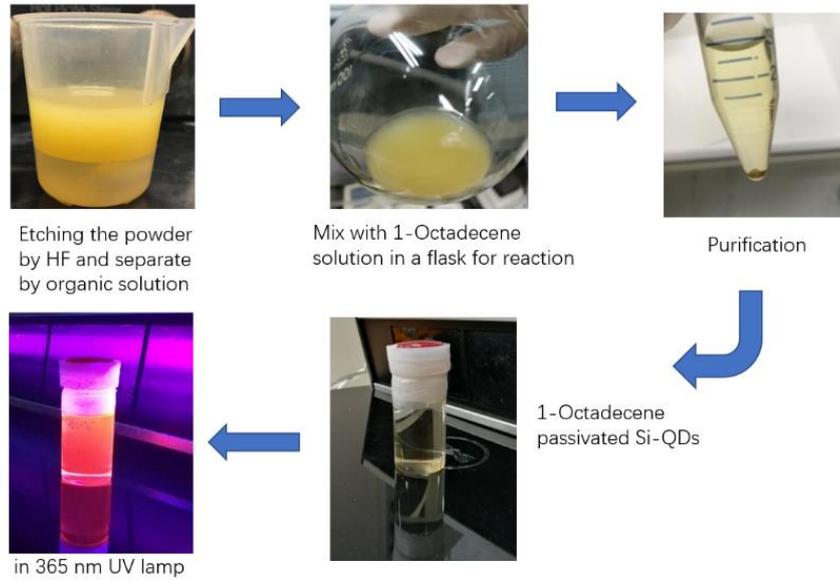
Figure 4.5 Photo records of the surface passivated process on Si QDs
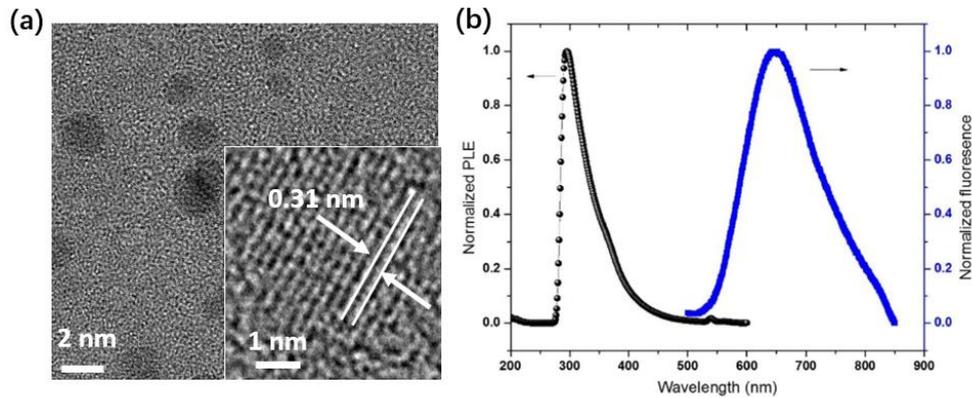
Figure 4.6 (a) TEM and HRTEM (inset) images, (b) PLE (left) and fluorescence (right) spectra. [21]

The transmission electron microscopy (TEM) was done of the 1-octadecene passivated Si QDs which assembled on a carbon film-covered Cu grid. The TEM images in Figure 4.6(a) show that the average diameter of the nanoparticles is 3~4 nm. In the inset image of the high-resolution TEM, the crystal fringes clearly show an interplanar lattice spacing of 0.31 nm, corresponding to the Si (111). Both these properties prove that Si nanoparticles can be seen as quantum dots. The fluorescence spectrum in Figure 4.6(b) of the Si QDs shows an emission peak around 650 nm under a 300 nm wavelength excitation light. It is corresponding with the orange color of the emission light under a UV lamp irradiation in Figure 4.5. All evidence shows the successful fabrication of Si QDs and its unique optical property of light absorption in the UV wavelength.

4.3 Energy transfer process from Si QDs to solar cell
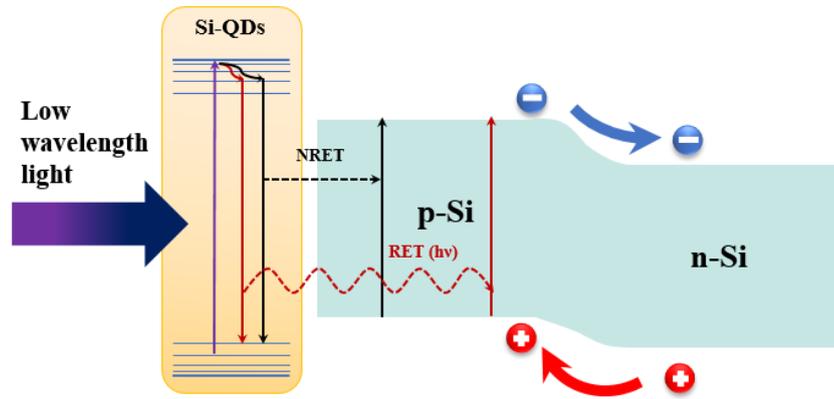
Figure 4.7 Energy band diagram of the energy transfer process from the Si QDs to Si p-n junction.

Our purpose is to enlarge the absorption spectrum and improve the J_{SC} of Si solar cell by the Si QDs. The mechanism is shown in Figure 4.7 of the energy band diagram in the energy transfer process. First, the Si QDs absorb the energy of low wavelength light photons. Then, this part energy was transferred to the bulk Si layer (no carriers transfer) via the resonance dipole-dipole reaction (Non-radiative energy transfer, NRET), and the radiative decay of photons (radiative energy transfer, RET).[22–25] So that, excess electron-hole pairs are generating at the p-n junction area, resulting in higher carrier separation and extraction via Si core-shell nanostructure.

Moreover, nanostructures can show increased absorption via energy transfer from Si QDs than the planar structure. Because of the larger surface area compared with planar samples, this energy transfer can substantially affect absorption.
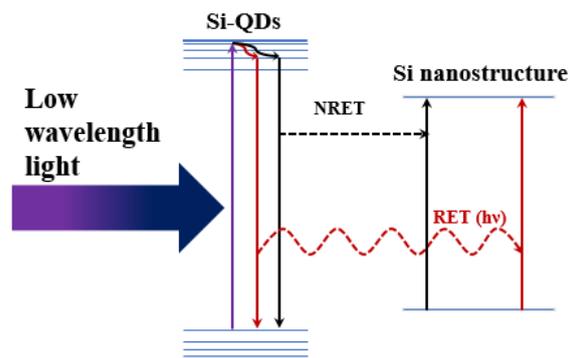
Figure 4.8 Mechanism of the RET and NRET process.

The RET process in Figure 4.8 is from the emission of a donor and re-absorption by an acceptor. Here, the donor is Si QDs, which absorb the light of UV range and emit a 650 nm wavelength light. The emission light was then absorbed by accepter, which is Si nanostructure.

The NRET also called Förster resonance energy transfer (FRET) which first observed by Förster, which showed the direct dipole-dipole resonance interaction between molecules. Studies of excitation transfer between colloidal quantum nanostructures and epitaxial nanostructures were started in recent years. The NRET is near-field communication, which normally worked within 10 nm, and it is a highly distance-dependent phenomenon. [26–28]
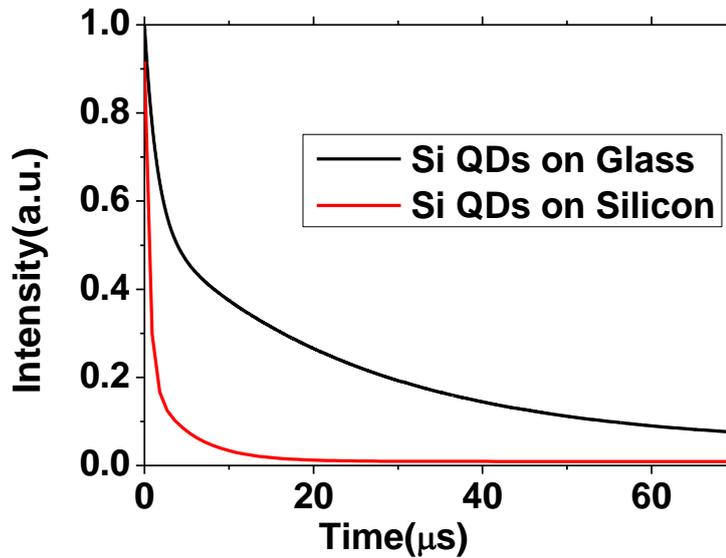
Figure 4.9 PL lifetime decay of the Si QDs coating on glass and silicon nanostructure surface.

In order to observe and compare the difference of the RET and NRET process from Si QDs to Si core-shell nanostructure, time-dependent photoluminescence decay of the Si QDs coating on glass and silicon nanostructure surface were measured. Figure 4.9 is the PL decay curves, it clearly indicates two different curves, which means different energy transfer processes occurred in the two samples. The fitting results show the PL lifetime is 24.8 µs of the Si QDs on glass, while it is only 5.81 µs of the Si QDs on the silicon. This is because of the Si QDs on glass is mainly affected by the RET. But a NRET process is active as another transfer channel from Si QDs to Si surface, resulting in the reduction of PL lifetime.

Therefore, the difference between the two energy transfer process can be attributed to their decay rate. For the Si QDs on the glass, photon emission by the RET is the significant decay. Thus, it can be described as:[23]

$$(\tau_{RET})^{-1} = \text{QE} \, (\tau_{glass})^{-1} \qquad\qquad \text{4-1}$$

$(\tau_{RET})^{-1}$ is the RET decay rate, QE is the quantum efficiency and $(\tau_{glass})^{-1}$ is the total decay rate of the Si QDs on the glass. For the Si QDs on the silicon, there is another energy transfer channel to the silicon surface. The decay rate $(\tau_{silicon})^{-1}$ can be calculated by:

$$(\tau_{silicon})^{-1} = (\tau_{glass})^{-1} + (\tau_{ET})^{-1} \qquad\qquad 4\text{-}2$$

$$(\tau_{ET})^{-1} = (\tau_{RET})^{-1} + (\tau_{NRET})^{-1} \qquad\qquad 4\text{-}3$$

$(\tau_{ET})^{-1}$, $(\tau_{RET})^{-1}$ and $(\tau_{NRET})^{-1}$ are the total energy transfer rate, the RET rate and NRET rate of Si QDs.

After the calculation of the above formulas, the results are shown below in Table 4.1. We found that the NRET rate is around 1.55 times faster than the RET rate from Si QDs transfer energy to the Si core-shell nanostructure, which has also been reported by our group. [23] This indicates that for applying Si QDs to the solar cell, the NRET process is more effective than the RET process. Therefore, the NRET is the dominant part in the energy transfer process.

Table 4.1 Energy transfer rate of RET and NRET.

$\tau_{(RET)}{}^{-1}$	$\tau_{(NRET)}{}^{-1}$	$\tau_{(NRET)}{}^{-1}/\tau_{(RET)}{}^{-1}$
$(19.37\mu s)^{-1}$	$(12.48\mu s)^{-1}$	~1.55

4.4 Application of Si QDs to homojunction solar cell devices

4.4.1 Device performance for Si QDs coating
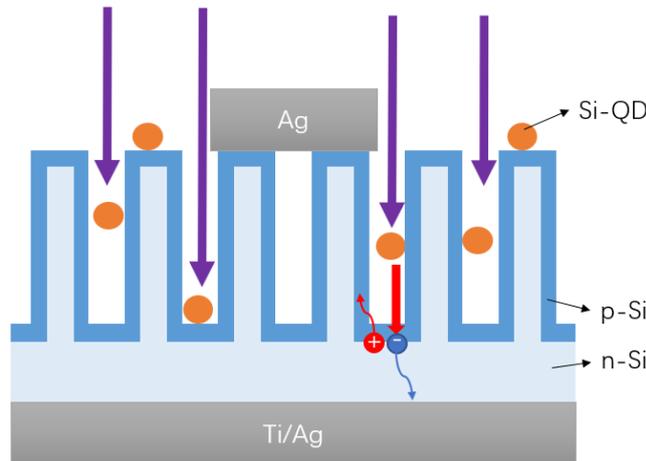
Figure 4.10 Schematic of coating the Si QDs on the Si nanostructure solar cell

A schematic of the coating the Si QDs was shown in Figure 4.19. The Si QDs were coated on a fabricated Si nanostructure solar cell surface by spin coater. Same as the mechanism in Figure 4.7, the Si QDs absorb the photon energy of incident light in the low wavelength range. Then, the energy is transferred to the Si core-

shell nanostructure layer through the RET and NRET. Thus, there are more photocarriers can be generated and separated, which benefit the solar cell performance.
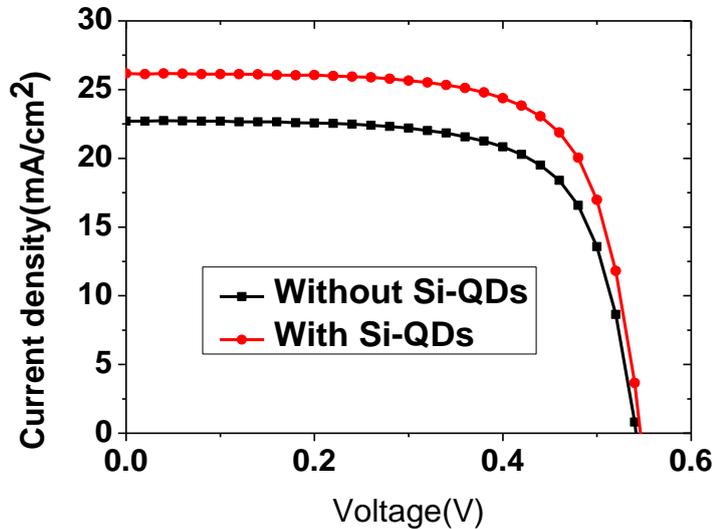
Figure 4.11 J-V curves of the Si nanostructure solar cell with and without Si QDs.

Table 4.2 Performance of the Si nanostructure solar cell with and without Si QDs.

	J_{SC} (mA/cm^2)	V_{OC} (V)	FF	η(%)
Without Si QDs	22.71	0.54	0.70	8.6
With Si QDs	26.42	0.55	0.71	10.2

The device performance of Si nanostructure solar cells with and without coating the Si QDs are indicated in Figure 4.11. The J_{SC}, V_{OC}, FF, and efficiency are list in Table 4.2, respectively. It obviously indicates a considerable improvement after introducing Si QDs, which mainly contributed by the large J_{SC} enhancement of 3.7 mA/cm^2. The solar cell efficiency obtained a 1.6% increasing. It shows the increased photo-carriers generation as a benefit of energy transfer by the Si QDs, due to the enhanced absorption of low wavelength light.

Stability of the Si QDs

Moreover, because our Si QDs are passivated by 1-octadecene and dissolved in the toluene, its stability is better than the original hydrogen-terminated Si QDs. To clearly indicate this property, the solar cell device performance was measured in a long period after coating Si QDs. Here, it is described as the degradation process of Si QDs.
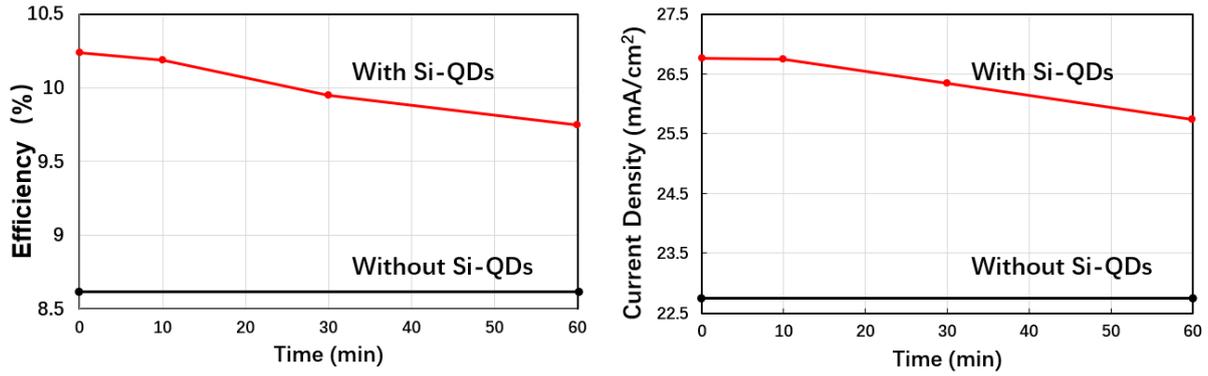
Figure 4.11 The efficiency and J_{SC} change in 60 min of the device with and without Si QDs.

Figure 4.11 is the change of efficiency and J_{SC} in 60 min. We found in the first 10 min, both efficiency and $J_{SC\ did}$ not have a significant degradation. When the time increase, degradation is also keeping increase. Finally, it reduces ~0.5% of efficiency and ~1 mA/cm^2 of J_{SC} after 60 min. This degradation may cause by the oxidation of some bonds in Si QDs surface, which is not completely passivated by the 1-octadecene. However, the enhancement of Si QDs is still evident compared with the samples without Si QDs.
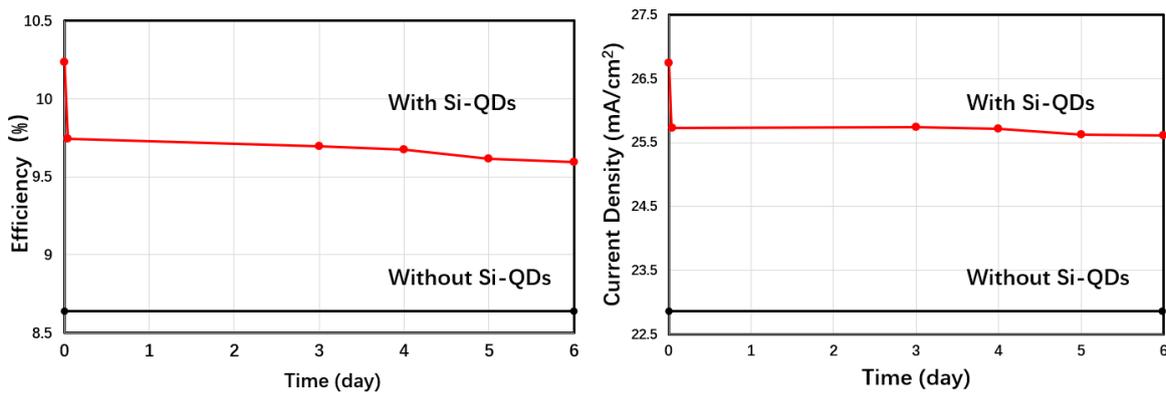
Figure 4.12 The efficiency and J_{SC} change in 6 days of the device with and without Si QDs.

Then, a long time of 6 days is also measured in Figure 4.12. After the fast fall in 60 min, both efficiency and J_{SC} keep at a high level in the last 6 days. It is possible because the major un-passivated bonds of Si QDs are oxide in a short time, and the other parts can keep in excellent stability in a long time. It still shows a better performance than the samples without Si QDs.

4.4.2 Investigation of different sized Si QDs
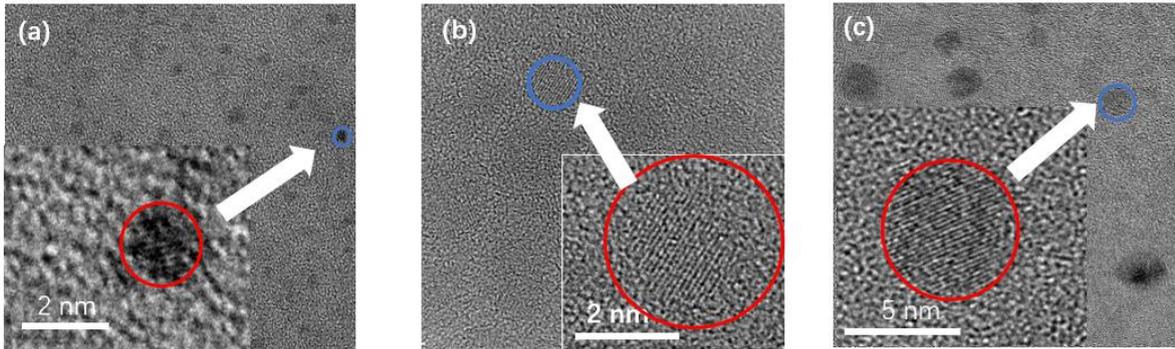
Figure 4.13 TEM images of different size Si QDs, the respective diameter is: (a) 2 nm, (b) 3~4 nm, and (c) 5~6 nm.

To check the influence of the size of Si QDs, we fabricated 3 types of Si QDs with different sizes. The diameter of Si QDs was controlled in the etching process that longer etching time leads to a smaller size. The TEM was measured of these Si QDs which assembled on a carbon film-covered Cu grid. The TEM images in Figure 4.13 shows that the respective diameter of Si QDs is 2 nm, 3~4 nm, and 5~6 nm. In the inset image of the high-resolution TEM, the crystal fringes also clearly show an interplanar lattice spacing of 0.31 nm, corresponding to the Si (111).
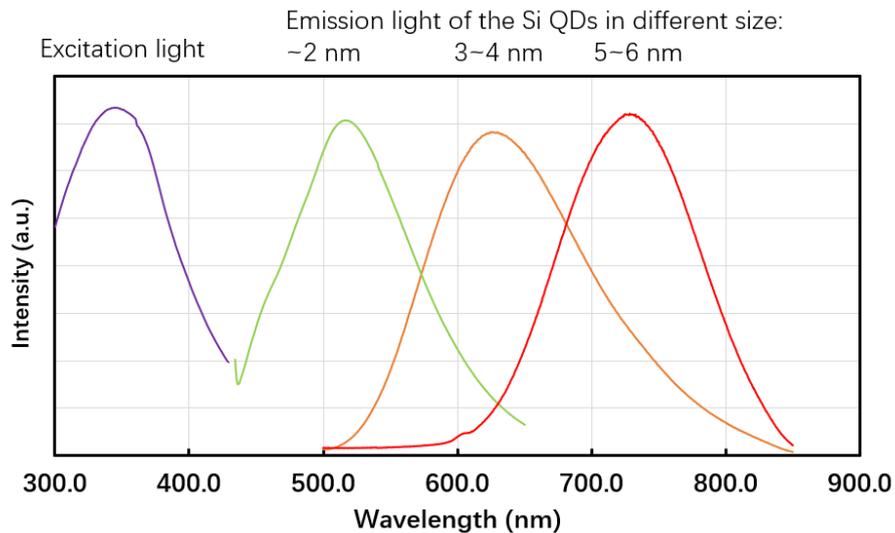
Figure 4.14 Spectra of excitation light and corresponding emission light of different size Si QDs.

Figure 4.14 shows the fluorescence spectra of the different size Si QDs under a 350 nm wavelength excitation light. The emission light is different in the three Si QDs that it is 500nm wavelength green light of the 2 nm Si QDs, 620 nm wavelength orange light of the 3~4 nm Si QDs and 720 nm wavelength red light of the 5~6 nm Si QDs. The different fluorescence light of the Si QDs in a different size is due to the effect of quantum confinement which is stronger in a smaller size.[25–27]
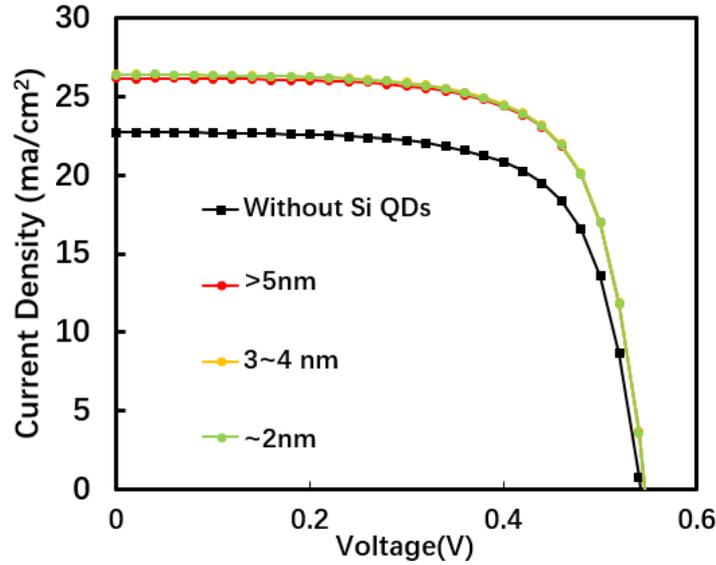
Figure 4.15 J-V curves of the solar cell coated by Si QDs with different sizes.

We also fabricated the device and coated the Si QDs to check the enhancement of different size Si QDs. The J-V curves of the solar cells are indicated in Figure 4.15. The results show the curves are only a little different and increasing of J_{SC} after coating the different size Si QDs is very close. The reason why similar results are obtained is still not clear and needed to solve in future research.

4.5 Optimization of the device structure for ITO coating

In Chapter 2, we discussed the effect of the ITO layer for nanostructure solar cell that it can help the photocarrier collection efficiency as a transparent electrode. Here, the device structure needs to be further investigated for the application of Si QDs.
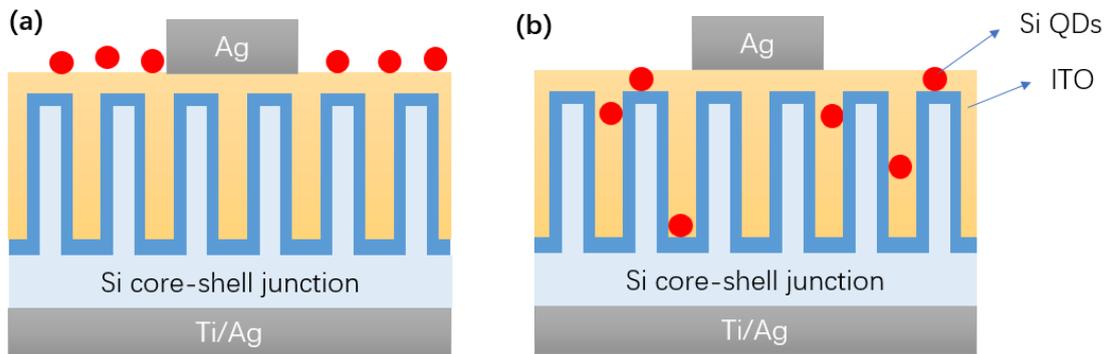
Figure 4.16 Schematic of the device structure ITO deposition and Si QDs coating: (a) Si QDs/ITO/ Si core-shell and (b) ITO/Si QDs/ Si core-shell.

Two different device structures are indicated in Figure 4.16, (a) is coating the ITO first and then the Si QDs; (b) is the opposite that coating the Si QDs first and then ITO.

The devices performance is measured and list in Table 4.3. We found in the (a) structure, J_{SC} has an improvement of 2.35 mA/cm^2 and efficiency is increased by 0.9%. They are lower than the improvement of the device without ITO at above section 4.4.1, which has a considerable J_{SC} enhancement of 3.7 mA/cm^2 and a 1.6% increasing of the solar cell efficiency. This lower improvement in (a) structure is because the NRET is a near-communication process which normally works in a very short distance. However, the ITO layer is too thick(120nm) so that the NRET effect is very weak in this device structure. On the other hand, in the (b) structure, it does not have any improvement, but all the paraments are reduced. It is due to the Si QDs are degraded by plasma during the ITO deposit process. Also, the dissolved solution is not completely dry, which is harmful to the contact of the electrodes.

Table 4.3 Solar cell performance of different device structures.

	J_{SC} (mA/cm^2)	V_{OC} (V)	FF	η(%)
With ITO and without Si QDs	25.82	0.55	0.73	10.4
(a) Si QDs/ITO/ Si core-shell	28.17	0.55	0.73	11.3
(b) ITO/Si QDs/ Si core-shell	24.74	0.54	0.35	4.7
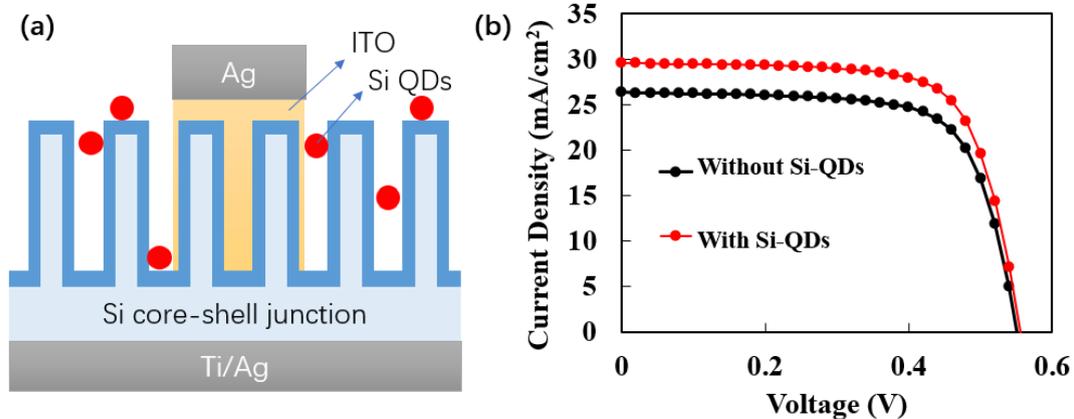
Figure 4.17 (a)Schematic of the device structure of the ITO only deposited under the metal area. (b) J-V curves of the special structure device with and without Si QDs.

Table 4.4 Solar cell performance of the special structure device with and without Si QDs.

	J_{SC} (mA/cm^2)	V_{OC} (V)	FF	η(%)
Without Si QDs	26.38	0.55	0.71	10.3
With Si QDs	29.59	0.56	0.72	11.8

To solve the problem, we fabricate a special device structure that only deposits the ITO layer on the metal area. After that, the Si QDs are coated on the device. The schematic of the device structure is shown in Figure 4.17(a). The device performance of solar cells with and without coating, the Si QDs are indicated in Figure 4.18(b). The respective parameters of J_{SC}, V_{OC}, FF, and efficiency are list in Table 4.4. The J_{SC} gives an increase of 3.21 mA/cm^2. It shows that the effect of Si QDs energy transfer is not reduced, and contact is improved by the transparent ITO electrode.

Introduce the micro-grid electrodes
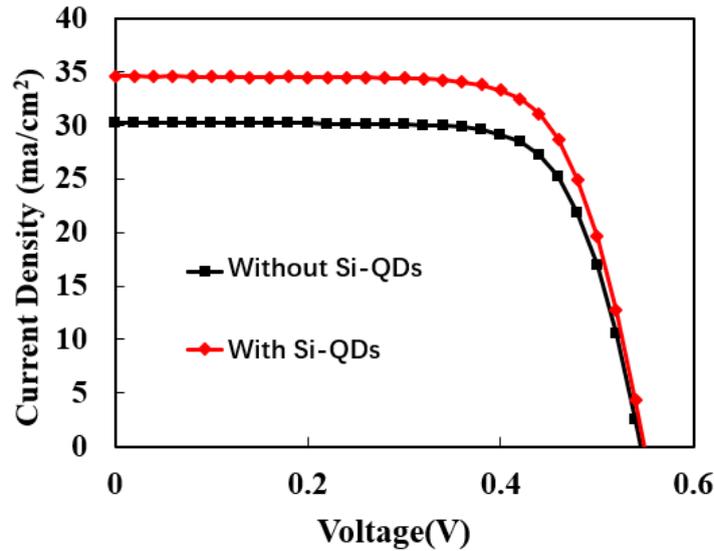
Figure 4.18 J-V curves of the micro-grid electrodes device with and without Si QDs.

Table 4.5 Solar cell performance of the micro-grid electrodes device with and without Si QDs.

	J_{SC} (mA/cm^2)	V_{OC} (V)	FF	η(%)
Without Si QDs	30.26	0.55	0.73	12.0
With Si QDs	34.59	0.55	0.72	13.7

Moreover, we apply the Si QDs to the device based on the micro-grid electrodes. The device performance of solar cells with and without coating the Si QDs are indicated in Figure 4.18. The respective parameters of J_{SC}, V_{OC}, FF, and efficiency are list in Table 4.5. Same as the last chapter, the basic efficiency increased to 12% by using the micro-grid electrodes. A further improvement was obtained after combing with Si-QDs. The J_{SC} has an increase of 4.33 mA/cm^2, resulting in the higher efficiency of 13.7%.

4.6 Summary

In this chapter, we discussed the fabrication of Si QDs and its application SiNW solar cell. The purpose is to broaden the absorption spectra, because the normal Si solar cells only utilize a relatively small fraction of sunlight in 400 to 1100 nm range. Because of the quantum confinement effect, Si QDs could absorb high energy photons in the low wavelength range and transfer it to SiNW solar cell through the energy transfer channel, resulting in more photo carriers.

1. The Si-QDs were fabricated based on HSQ solution and the surface was passivated by 1-octadecene. Results of the TEM and fluorescence spectra clearly indicates the morphology and optical property of the Si QDs.

2. A large improvement of J_{SC} was obtained after coating the Si-QDs on the surface of the silicon nanowire solar cell. It is due to the enlarged absorption spectrum by the energy transfer effect of the Si QDs.

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Chapter 5.   Hybrid heterojunction Si nanostructure solar cell

In the previous chapters, we discuss a lot of the silicon nanostructure homojunction solar cell devices. All of these devices are growing a p-type Si shell on the n-type Si nanostructure core to form the p-n junction. It requires an energy-intensive fabrication process, which is including the high-temperature thermal annealing and high-vacuum chemical deposition processes. [1–4] However, we also hope to find a cheaper and easier fabrication process for the industry produce. A hybrid heterojunction structure of the device is a potential candidate by using the polymer/Si. Because the process is no need a high vacuum and high temperatures. In the past few years, a steady increase in efficiency has been obtained for polymer/Si hybrid heterojunction solar cells. [5–10] This heterojunction construction has high potential, due to it combine the broadband optical absorption capability of the Si nanostructures and the simple and low-cost production processes of the solution-based polymer. [7,11]

5.1 The basics of the hybrid device

Among the various conducting polymers, a cheap and solution-processed poly (3,4-ethylenedioxy-thiophene): poly (styrene sulfonate) (PEDOT: PSS) was under intense investigation due to its high transparency and conductivity. Moreover, PEDOT: PSS can also serve as a passivation and antireflection layer. [12–16] Thus, considerable progress has been made of PEDOT: PSS/Si hybrid solar cells. In Figure 5.1(a), it shows the schematics of the energy band diagram. PEDOT: PSS of highest occupied molecular orbital (HOMO) energy level is around 5.1 eV, which is similar to the valence band energy of n-Si. Thus, the depletion region was generated, PEDOT: PSS layer is the formation of a heterojunction with n-type Si as a hole-transporting pathway. Figure 5.1(b) is the molecular structure of PEDOT and PSS.
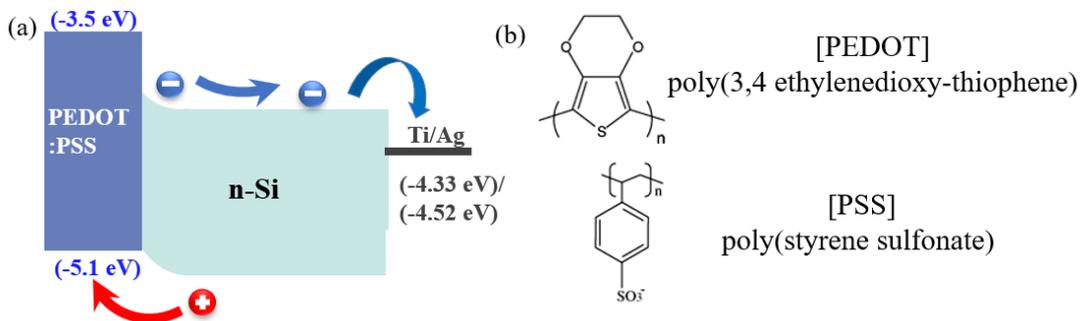
Figure 5.1 (a) Energy band diagram of PEDOT: PSS and Si heterojunction. (b) The molecular structure of PEDOT and PSS. [11]
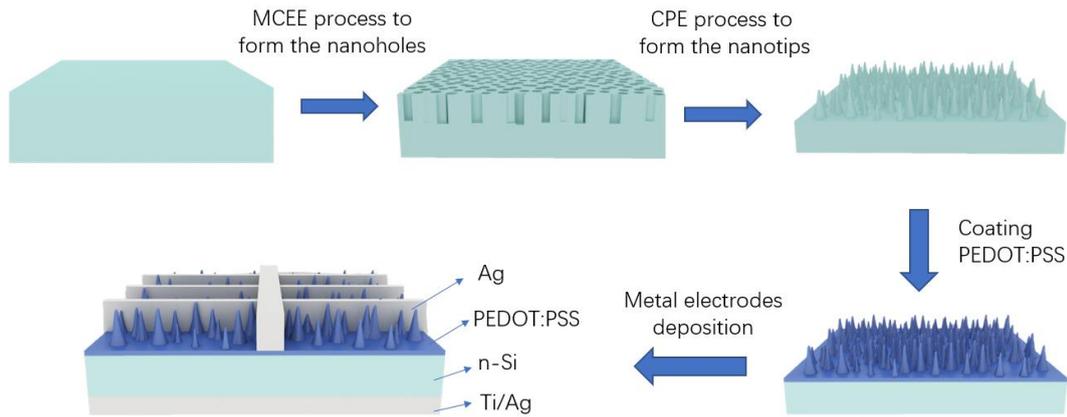
Figure 5.2 Schematics of the fabrication process from the silicon substrate to the hybrid solar cell device

Here, unlike the previous MCEE process for nanowires fabrication, we use the MCEE method combined with chemical polish etching (CPE) to form Si nanotips for the fabrication of hybrid solar cell device. The reason why not use nanowires structure is that the space of nanowires is too short for the PEDOT：PSS to enter. [17,18] Because of the surface tension between the nanowires, so that it can't make good contact for the heterojunction and many interface defects will be generated.

Schematics of the fabrication process are shown in Figure 5.2. First, we use the AgNO$_3$/HF solution and an extra step of HF/H$_2$O$_2$ to fabricate a nanoholes structure from an n-type Si substrate. Then a CPE treatment was used to change the nanostructure by the strong oxidizing ability of HNO$_3$/HF. The Si nanotips were then fabricated and coated with PEDOT: PSS by the spin coating. After thermal annealing to dry the solvent of PEDOT：PSS, a hybrid heterojunction of PEDOT: PSS/Si was formed. Finally, front and rear metal electrodes of Ag and Ti/Ag were deposited to finish the solar cell device fabrication.
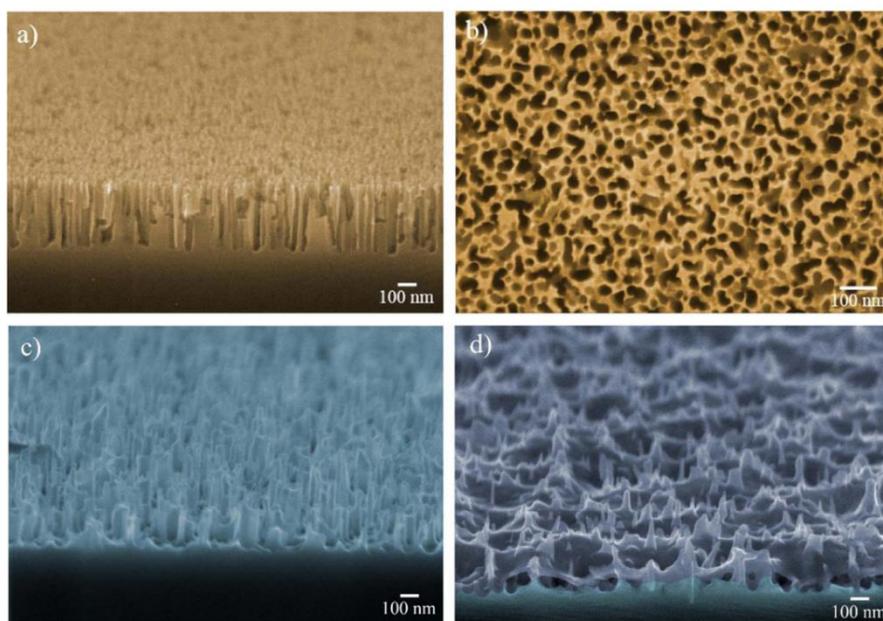
Figure 5.3 SEM images of (a) cross-sectional view of the nanoholes, (b) top-view of the nanoholes (c) cross-sectional view of silicon nanotips as-fabricated and (d) after PEDOT: PSS coated.[17]

The SEM images are shown in Figure 5.3(a) to (c) of the high-density Si nanoholes and tapered Si nanotips formed by the CPE treatment. Figure 5.3(a) shows a cross-sectional view SEM image of high-density nanoholes. These nanoholes have an average diameter of 30-50 nm and a high density, as shown in the top-view SEM image of Figure 5.3(b). The nanoholes are fabricated by a two steps MCEE process: firstly, an electroless metal deposition of $HF/AgNO_3$ solution and secondly a vertical etching step in HF/H_2O_2 solution. Figure 5.3(c) shows SEM images in the cross-sectional view of modified Si nanotips after CPE treatment. It is clear that the density and depth of the nanostructures were reduced and the gaps between the nanostructures were widened. The CPE treatment is also discussed in Chapter 2, which consists of HNO_3 and HF; the HNO_3 assists the formation of the oxide layer of Si nanostructure and HF helps to remove the oxide layer. It is used to eliminate metal contamination, reduce surface defects and improve surface morphology. Here, the nanoholes structure was changed their morphology into nanotips. We can, therefore, control the surface morphology of nanotips by adjusting the solution concentration and the CPE time to make it suitable for the coating of PEDOT：PSS. In Figure 5.3(d), it is the SEM images in the cross-sectional view of CPE-treated nanotips after the coating of PEDOT: PSS. It indicates that the surface of silicon nanostructures was fully infiltrated and covered with PEDOT: PSS. There is less gap in the interface. The large PEDOT: PSS/Si heterojunction area boosts charge collection efficiency by shortening the minority carrier diffusion paths.
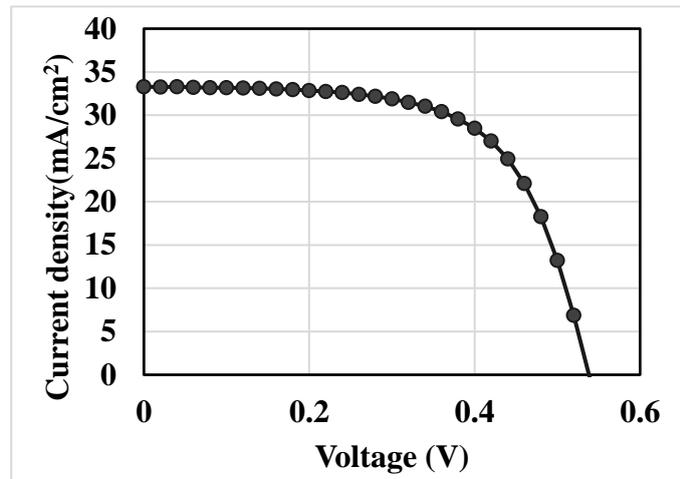
Figure 5.4 J-V curve of the hybrid heterojunction solar cell device.

Table 5.1 Performance of the hybrid heterojunction solar cell device.

J_{SC} (mA/cm^2)	V_{OC}(V)	FF	Efficiency (%)
34.32	0.54	0.60	11.1

The J-V curve and performance of the hybrid silicon solar cell device are indicated in Figure 5.4 and Table 5.1. The solar cell exhibits an efficiency of 11.1% with a J_{SC} of 34.32 mA/cm^2, V_{OC} of 0.54 and FF of 0.60. The high efficiency of a basic device shows the good proper of PEDOT: PSS and Si nanostructure. It

also suggests the high potential of the hybrid heterojunction solar cell device for achieving high performance and low cost by using PEDOT：PSS and Si nanostructure.

5.2 Application of Si QDs to the hybrid device
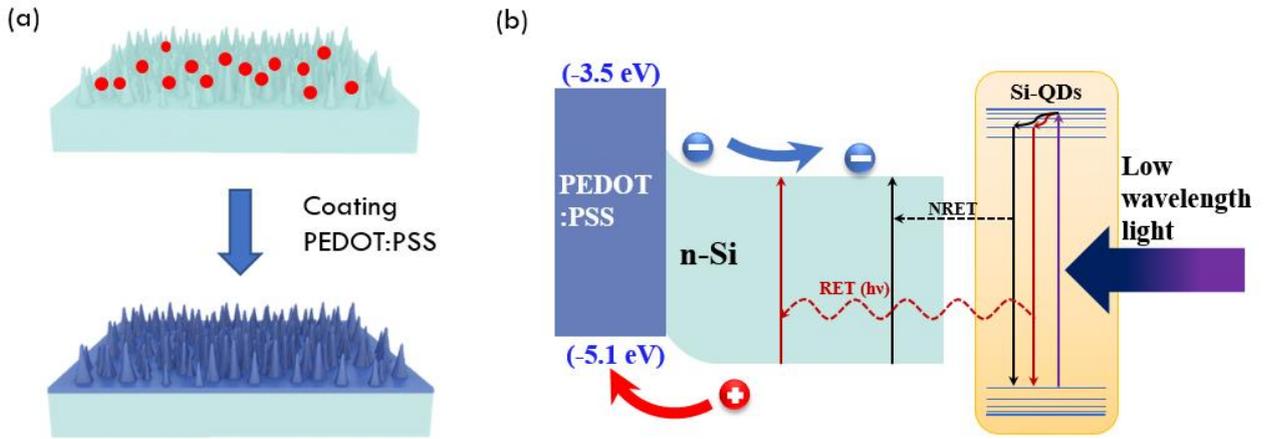
Figure 5.5 (a) Schematics of the process for Si QDs coating on the Si nanotips. (b) Energy band diagram of PEDOT: PSS and Si heterojunction, after coating the Si QDs.

Moreover, we investigate the application of Si QDs to this hybrid solar cell device. The schematics of the process are indicated in Figure 5.5(a). Unlike the Si QDs coating on the surface of p-type Si in Chapter 4. Here, we are coating the Si QDs before coating the PEDOT：PSS. This is because the coating of PEDOT：PSS is doing in the standard atmosphere and room temperature. [19–22] There are not harmful to the Si QDs effect in the continuous process. The energy band diagram of PEDOT: PSS/ Si heterojunction and Si QDs are shown in Figure 5.5(b). It illustrates that Si QDs absorb light (especially the low wavelength light) and transfer energy to the Si layer by NRET and RET process. This effect of Si QDs can help to generate more hole-electron pairs from the transferred energy.
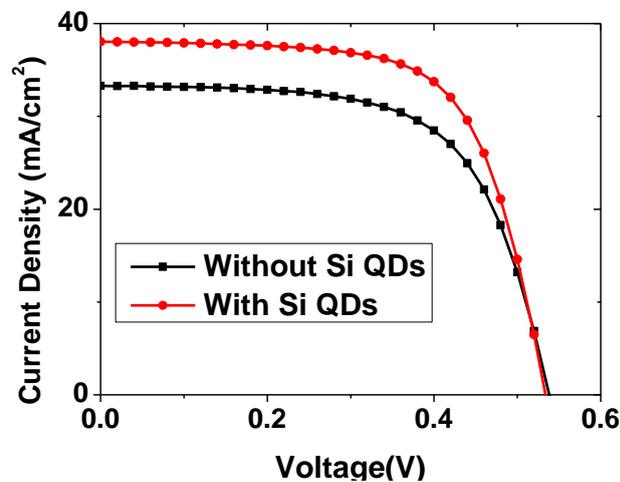
Figure 5.6 J-V curve of the hybrid silicon solar cell device with and without the Si QDs coating.

Table 5.2 Performance of the hybrid silicon solar cell device with and without the Si QDs coating.

	J_{SC} (mA/cm^2)	V_{OC} (V)	FF	η(%)
Without Si QDs	34.32	0.54	0.60	11.1
With Si QDs	37.98	0.54	0.62	12.7

Solar cell devices are fabricated to check the effect of Si QDs in the hybrid heterojunction solar cell. In Figure 5.6 and Table 5.2, it indicates the J-V curves and performance of the device with and without Si QDs coating. The device with Si QDs shows a higher J_{SC} of 37.98 mA/cm^2, leading to the highest PCE of 12.7%. It is because that more photons being absorbed by the Si QDs and thus many more charge carriers are created by energy transfer from the Si QDs to the underlying silicon layer. The generated charge carriers are effectively separated with the help of organic polymer PEDOT: PSS and Si nanotips. The FF improvement is due to that the Si QDs with the passivated ligand can be considered as a hydrophilic layer. It can help a better cover of PEDOT: PSS and reduce the series resistance.

5.3 Advantages for the hybrid structure by the Si QDs effect
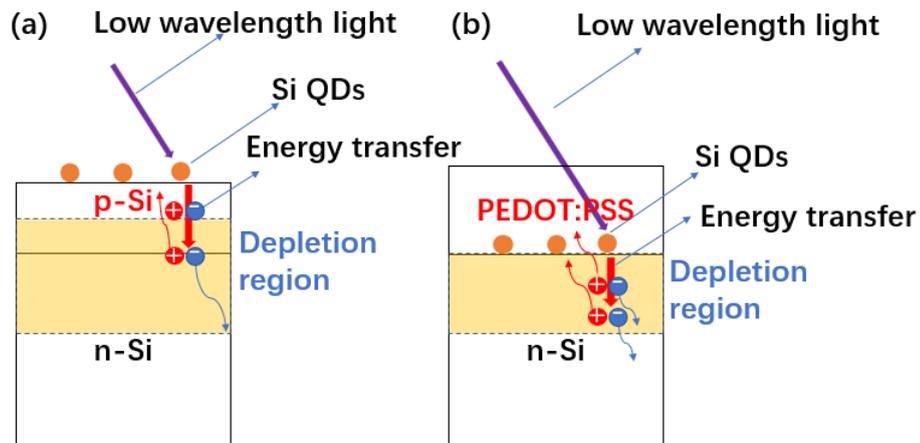
Figure 5.7 Schematics diagram of difference in energy transfer of Si QD at (a) p-Si/n-Si homojunction and (b) PEDOT: PSS/n-Si heterojunction structure. (c)The J_{SC} improvement of these two structures.
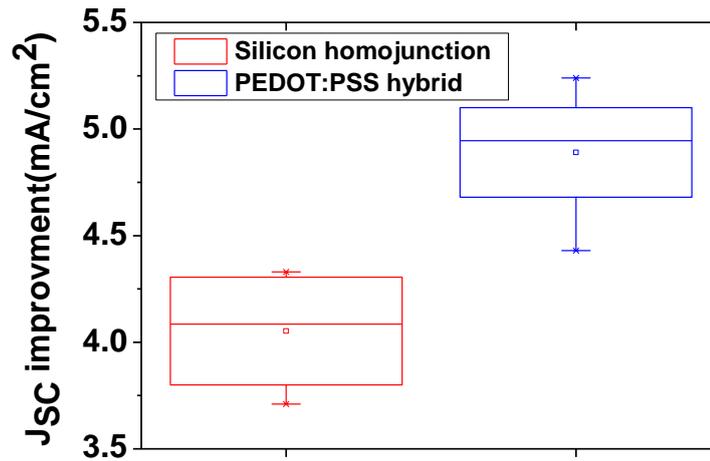
Figure 5.8 The J_{SC} improvement in the Si homojunction device and PEDOT：PSS hybrid device.

To more clearly understand the difference of Si QDs effect in the hybrid device. Schematic comparison between the energy transfer processes of the homojunction Si device and hybrid device are indicated in Figures 5.7(a) and (b) that the Si QDs was coated between the PEDOT: PSS and Si layer on a hybrid device. Figure 5.7(a) shows there is some distance between the p-Si surface layer and the depletion region. This distance leads to some energy can't transfer to the depletion region. Thus, some photo-carriers can't be separated resulting in a reduction of photocurrent. However, in the hybrid heterojunction structure of Figure 5.7(b), due to the depletion region being generated in the n-Si layer, coating the Si QDs on the n-Si surface layer is beneficial. This allows contact with the depletion region such that almost all of the energy can be transferred to generate and separate the photo-carriers. This suggests a heterojunction structure is more effective than the previous homojunction Si solar cell because the Si QDs are closer to the depletion region. The Si QDs absorb the light and then transfer the energy to the depletion region where the photo-carriers can be separated.

The J_{SC} improvement of solar cell devices in these two structures is shown in Figure 5.8. It is clear that a greater J_{SC} improvement was obtained in the hybrid structure sample (around 5 mA/cm^2) than the homojunction sample (around 4.1 mA/cm^2). It is due to more energy being transferred to the depletion region as explained above. In the homojunction, some of the electron-hole pairs are generated out of the depletion region which can't separate and generate the current. In the hybrid structure, almost all the electron-hole pairs are generated in the depletion region. Thus, more photo-current can be created in a hybrid device. In conclusion, both the mechanism and experiment results prove that Si QDs are more effective in the hybrid device.

5.4 Optimization of the Si QDs surface passivation

5.4.1 The effect of distance for the NRET effect
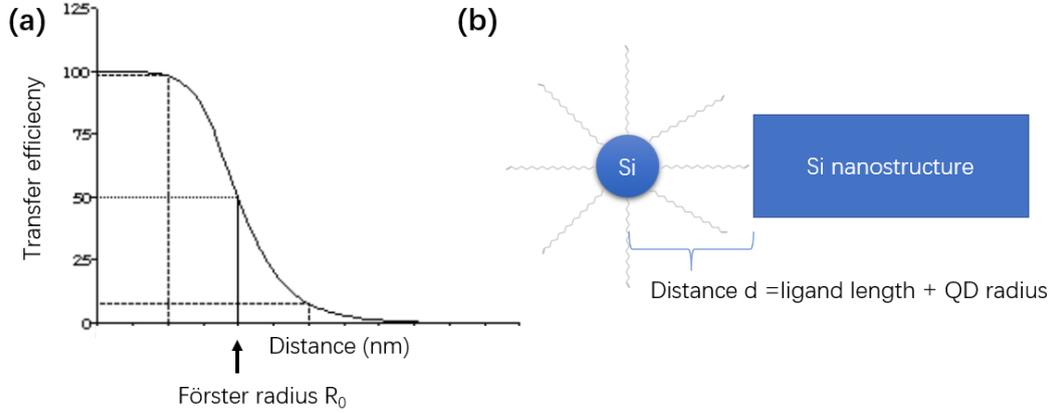
Figure 5.9 (a) The attenuation curves of transfer efficiency (NRET) along with the increase of distance. (b)Schematic of the distance between Si QDs and Si nanostructures.[23]

In Chapter 4, we discuss the basic properties of the Si QDs. Here, we try to investigate and optimize the surface passivation ligand of the Si QDs. Figure 5.9 (a) is the attenuation curves of transfer efficiency (NRET) along with the increase of distance. It is obvious that the transfer efficiency keeps at a high level (close to 100%) in short distance and then quickly attenuates when distance increases. The Förster radius (R_0) is the distance when the transfer efficiency equals to 50%. It can be calculated by [24]

$$(\tau_{NRET})^{-1} = (R_0/d)^4 (\tau_{RET})^{-1} \qquad \text{5-1}$$

Here, the distance (d) is ligand length plus the radius of Si QDs as shown in Figure 5.9(b), and $(\tau_{RET})^{-1}$ and $(\tau_{NRET})^{-1}$ is the RET and NRET rate. We can, therefore, obtain the R_0. Moreover, we can further calculate the NRET efficiency (Q_F) by R_0 and d by below formula: [25]

$$Q_F = \frac{R_0{}^6}{d^6 + R_0{}^6} \qquad \text{5-2}$$

Therefore, we can clearly find the distance dependence from the formula: if d << R_0, the Q_F will close to 1, it means that nearly no energy loss during the transfer by NRET process. If d >> R_0, the Q_F will close to 0, so that there are no NRET process occur. It can conclude that NRET is a highly distance-dependent phenomenon. Because we apply the Si QDs to increase the J_{SC} of the solar cell. Thus, Si QDs with higher NRET efficiency are needed to pursue. [26–28] We fabricated the Si QDs in the same size for standard comparison. Therefore, shortening the passivation ligand of Si QDs is an alternative way to shorten the total distance for NRET process.

5.4.2 Investigation of Si QDs with different ligands
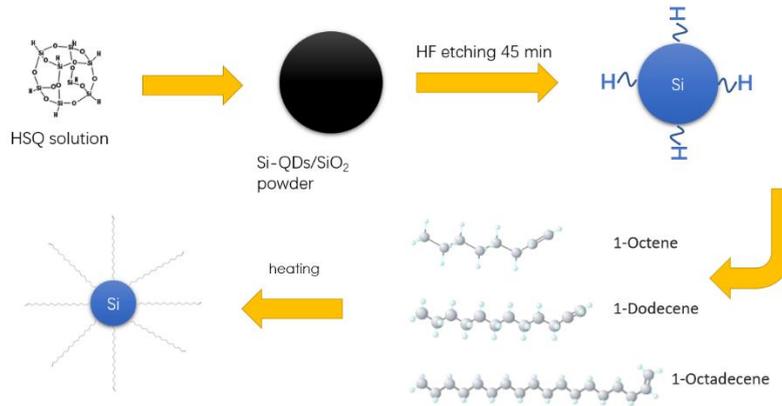
Figure 5.10 Schematics of the fabrication process of Si QDs with three different ligands.

As we discussed before, we hope to enlarge the NRET efficiency by shortening the distance with shorter passivation ligands. Here, we introduce two shorter ligands (1-octene, 1-dodecene) to replace the 1-octadecene to passivate the Si QD surface. The schematics of the fabrication process are shown in Figure 5.10. The length of 1-octene, 1-dodecene, 1-octadecene is around 0.75 nm, 1.25 nm, and 2 nm, respectively. [29] The fabrication process is nearly the same as normal. The only difference is the heating temperature is adjusted due to the reduced melting point of 1-octene, 1-dodecene. [30] The Si QDs samples with different passivation ligands were fabricated and called as octene sample, dodecene sample, and octadecene sample below for short.
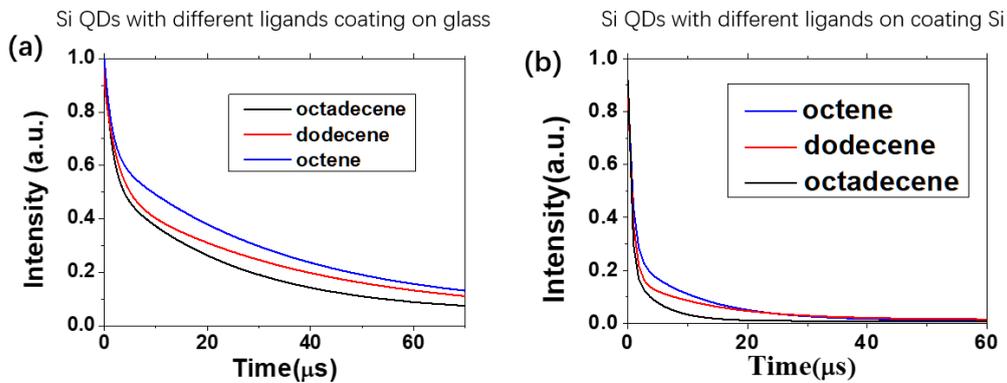
Figure 5.11 (a) PL decay of three samples coating on the glass. (b) PL decay of three samples coating on Si nanostructure.

Table 5.3 PL lifetime of three samples coating on glass and Si.

	τ_{glass} (μs)	$\tau_{silicon}$ (μs)
Octadecene	24.8	5.81
Dodecene	27.6	6.06
Octene	34.2	6.60

To check the transfer efficiency, PL decay of these three samples was measured, as shown in Figure 5.11 and fitting results of the lifetime are listed in Table 5.3. We find that the lifetime of Si QDs (both τ_{glass} and $\tau_{silicon}$) is increasing when the ligand length reduced from octadecene sample to octene sample. This is maybe due to the difficulty of passivation for the long ligands even using higher heating temperatures. So that the surface of Si QDs is not fully passivated which reduced its lifetime. The τ_{glass} is larger than $\tau_{silicon}$ in the dodecene sample and octene sample, which is the same as the octadecene sample. This is because of the Si QDs on glass is mainly affected by the RET, and less NRET occurs. But for the Si QDs on the silicon, RET is still alive, and NRET from Si QDs to Si surface contributes to the PL decay as another channel. Then, we can use the Formula 4-1, Formula 4-2 and Formula 4-3 to calculate the RET rate, NRET rate, and their ratio. The results are list in Table 5.4, and we can find that the NRET rate is faster than the RET rate in all the samples. The ratio between the RET rate and NRET rate are very close. It proves again that the NRET is the major process for energy transfer, and the passivated ligands change not change the ratio.

Table 5.4 Energy transfer rate of RET, NRET and their ratio of the three samples

	$\tau_{(RET)}^{-1}$	$\tau_{(NRET)}^{-1}$	$\tau_{(NRET)}^{-1}/\tau_{(RET)}^{-1}$
Octadecene	$(19.37\mu s)^{-1}$	$(12.48\mu s)^{-1}$	1.55
Dodecene	$(20.20\mu s)^{-1}$	$(12.61\mu s)^{-1}$	1.60
Octene	$(22.00\mu s)^{-1}$	$(13.00\mu s)^{-1}$	1.69

Based on the energy transfer rate of samples, we can, therefore, calculate the Forster radius R_0 and NRET efficiency Q_F by the Formula 5-1 and Formula 5-2, which we introduced in the last section. The results are listed in Table 5.5. The R_0 of three samples is highly related to eh distance that the octadecene sample is longer than the dodecene sample and then octene of 3.9 nm, 3.1 nm, and 2.6 nm, respectively. However, the NRET efficiency of the three samples is a different trend. It is concluding that the octene sample has the highest NRET efficiency of 68.76%, which is higher than the dodecene sample of 66.96% and octadecene sample of 64.88%. This means that the octene sample is most effective to transfer the energy by the NRET process. This is achieving our purpose that enlarging of the NRET efficiency by shortening the distance with shorter passivation ligands.

Table 5.5 Distance, Forster radius and NRET efficiency of the three samples

	d (nm)	R_0 (nm)	Q_F
Octadecene	3.5	3.9	64.88%
Dodecene	2.75	3.1	66.96%
Octene	2.25	2.6	68.76%
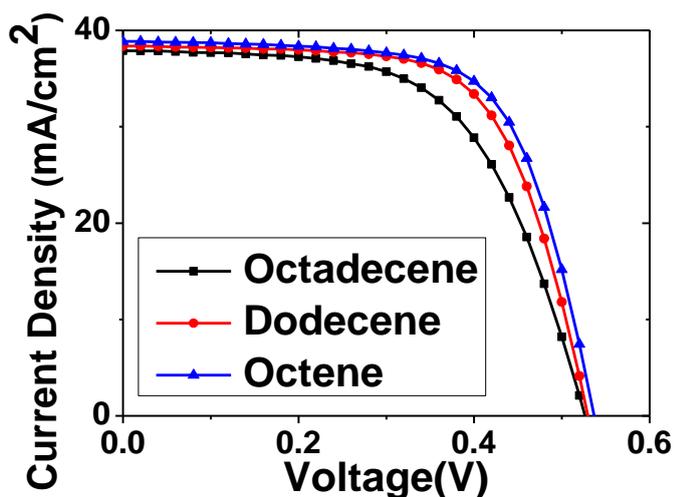
Figure 5.12 The solar cell devices performance after coating the three samples

Table 5.6 Parameters of solar cell performance after coating the three samples

	J_{SC} (mA/cm²)	V_{OC} (V)	FF	η(%)
Octadecene	37.98	0.54	0.62	12.7
Dodecene	38.52	0.54	0.65	13.5
Octene	38.90	0.55	0.66	14.1

Moreover, we fabricated the hybrid PEDOT：PSS/Si heterojunction solar cells by coating the three samples. The solar cell device performances are shown in Figure 5.12, and the parameters of the solar cell performance are list in Table 5.6. Compared with the device coating octadecene sample, the performance was improved in devices coating the octene and dodecene samples. The device with the octene sample shows the highest J_{SC} of 38.90 mA/cm². This highest J_{SC} proves that it is possible to enlarge the NRET efficiency by shortening the ligand length of Si QDs. Furthermore, the FF also increases from the octadecene sample to the octene sample. It is because the ligand-terminated Si QDs can be considered as a hydrophilic layer, which

effectively enhances the contact between the PEDOT: PSS and Si nanotips. This gives a low series resistance after coating Si QDs, resulting in higher FF. In addition, the octene sample can be passivated well due to its short length of the ligand. This gives higher hydrophilic property compared to other ligand cases and improves the contact between the PEDOT: PSS and Si nanotips, resulting in the highest FF of 0.66. Finally, the efficiency of the octene sample is increased to 14.1%, due to the improvements in J_{SC} and FF.
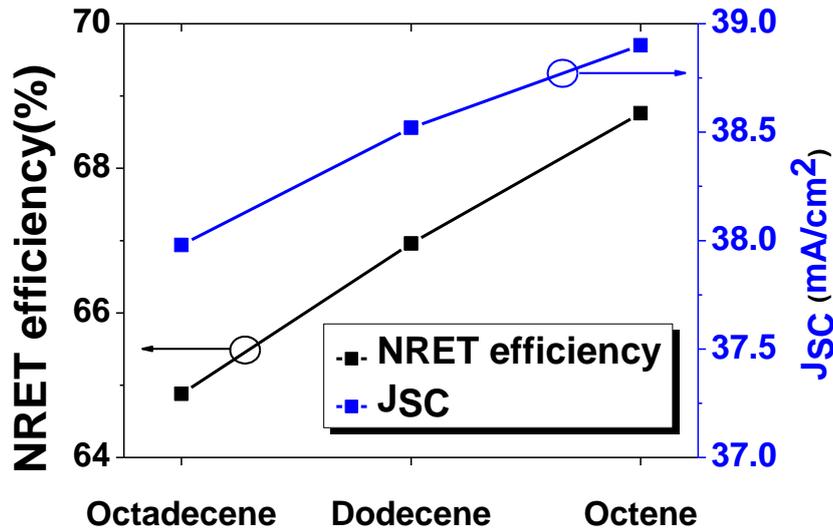
Figure 5.13 The relationship between J_{SC} improvement and NRET efficiency

Table 5.7 NRET efficiency, J_{SC}, and respective increment of the three samples.

	Q_F (%)	percentage increment	J_{SC} (mA/cm^2)	percentage increment
Octadecene	64.88	N/A	37.98	N/A
Dodecene	66.96	3.2%	38.52	1.4%
Octene	68.76	6.0%	38.90	2.4%

To more clearly understand the effect of different Si QDs on the solar cell, the relationship between J_{SC} improvement and NRET efficiency is shown in Figure 5.13. The value of NRET efficiency, J_{SC}, and respective increment of the three samples are listed in Table 5.7. It shows that higher NRET efficiency correlates to higher J_{SC}. This is because more energy can be transferred to generate and separate photo-carriers by Si QDs through the NRET process. These results suggest that shorter ligand passivated Si QDs are more effective to enhance the performance due to their higher NRET efficiency. So that for the application of the hybrid PEDOT: PSS solar cells, it is more beneficial to the device performance.

5.5 Summary

In this chapter, we fabricated the hybrid heterojunction solar cell of PEDOT：PSS and Si nanostructure. It combines the broadband optical absorption capability of the Si nanostructures and the simple production processes of the solution-based PEDOT：PSS polymer.

1. We coated the Si QDs on the hybrid heterojunction solar cell, which gives a large improvement of J_{SC}. The energy transfer process is more effective in the PEDOT：PSS/Si hybrid device than it in the homojunction device, due to the Si QDs are closer to the depletion region.

2. Because the NRET process is a highly distance-dependent phenomenon, we shorten the passivation ligand of Si QDs for achieving higher NRET efficiency. Si QDs with a short ligand of octene was fabricated, which achieve a longer lifetime and higher NRET efficiency. This gives the higher J_{SC} after applying the Si QDs to the solar cell.

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Chapter 6.　　Conclusion

This thesis focused on Si nanostructures and their applications for solar cell devices. We clearly showed effective ways of achieving high-performance Si nanostructure solar cells with the aim of solving society's energy problem by using feasible Si nanostructure solutions.

In Chapter 1, the basics of solar cells and Si nanostructures were introduced. The roadmap of past researches was reviewed to show our purpose to achieve high-performance Si nanostructure solar cell.

In Chapter 2, we developed Si nanostructures by wet and dry etching methods. Si homojunction solar cells were fabricated based on these nanostructures. For the Si nanowires formed by wet etching, we introduced a UV/Ozone treatment and successfully increased nanowire density which resulted in better anti-reflection properties and therefore a higher current density for the solar cell device. For the Si nanopencils formed by dry etching, we compared it with the nanopillars to show its better optical property caused by its tapered nanostructure and higher density. We developed a chemical polish etching method for the nanopencils to form a smooth surface and remove excess surface states.

In Chapter 3, we established a novel structure for front metal electrodes using a micro-grid pattern. These micro-grid electrodes not only minimize the shading loss of the surface but also help to increases the current density. We further investigated changes to the micro-grid pattern and achieved higher performance by using a hexagonal pattern.

In Chapter 4, to enhance light absorption in the low wavelength range, Si QDs were fabricated which were able to absorb extra broad-band wavelengths in the solar spectrum. This part of the energy is then transferred to the Si nanostructure by non-radiative energy transfer and radiative energy transfer. The NRET process shows a faster transfer rate than the RET process. Thus, the Si nanowire solar cell with Si QDs coating obtained a higher photocurrent.

In Chapter 5, a hybrid heterojunction solar cell device was developed by using PEDOT: PSS as a hole-transporting path and combined it with the n-type core of the Si nanostructure. We also applied the Si QDs to the hybrid device, which has been found to be more effective. Moreover, short passivated ligands for the Si QDs were investigated and obtain high NRET efficiency.

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List of publication

[1] **J. Chen**, T. Subramani, W. Jevasuwan, N. Fukata, Improvement of silicon nanowire solar cells made by metal catalyzed electroless etching and nano imprint lithography, Jpn. J. Appl. Phys. 56 (2017) 04CP03. DOI:10.7567/JJAP.56.04CP03.

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