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ABSTRACT

Low-temperature synthesis of polycrystalline (poly-) Ge on insulators is a key technology to integrate Ge-CMOS into existing devices. However, Fermi level control in poly-Ge has been difficult because poly-Ge has remained naturally highly p-type due to its defect-induced acceptors. We investigated the formation of n-type poly-Ge (thickness: 100–500 nm) using the advanced solid-phase crystallization technique with Sb-doped densified precursors. Sb doping on the order of 10^{20} cm^{-3} facilitated lateral growth rather than nucleation in Ge, resulting in large grains exceeding 15 μm at a low growth temperature (375 °C). The subsequent heat treatment (500 °C) provided the highest electron mobility (200 cm^2/V s) and the lowest electron density (5×10^{17} cm^{-3}) among n-type poly-Ge directly grown on insulators. These findings will provide a means for the monolithic integration of high-performance Ge-CMOS into Si-LSIs and flat-panel displays.

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Ge complementary metal–oxide–semiconductors (CMOSs) are expected to be promising for scaling beyond the Si-CMOS limit because Ge has a higher carrier mobility than Si for both electrons and holes and is compatible with conventional Si processing.[1–4] For both p and n channels, effective mobilities in Ge MOS field-effect transistors (MOSFETs) have exceeded those in Si-MOSFETs because of the development of device technologies including gate stacks.[4–8] The most promising usage of such high-performance Ge-CMOS is to integrate it into Si large-scale integrated circuits (LSIs) or flat-panel displays. To achieve this, low-temperature Ge-on-insulator (GOI) technology has been developed, including solid-phase crystallization (SPC),[9–13] laser annealing,[14–18] chemical vapor deposition,[19,20] flash-lamp annealing,[21] the seed layer technique,[22] and metal-induced crystallization.[23–27] Using the resulting polycrystalline (poly-) Ge layers, p/n-channel MOSFETs[12,13,17,21,27] and even CMOS operation have been successfully demonstrated.[28] However, for exceeding the performance of Si-CMOS, further investigation to improve both the hole and electron mobilities of poly-Ge layers is necessary.

Generally, a poly-Ge layer is naturally highly p-type because of its defect-induced acceptors.[29] We recently found that the atomic density of amorphous Ge (a-Ge) significantly influenced subsequent SPC.[30–32] By using a densified a-Ge on a GeO_2 underlayer, we fabricated a poly-Ge layer with a hole mobility of 620 cm^2/V s,[33] which greatly exceeds that of bulk-Si (430 cm^2/V s). These achievements initiated the prospect of the development of inversion-type poly-Ge n-MOSFETs that surpass Si-MOSFETs. However, n-type poly-Ge on insulators with high carrier mobility (>200 cm^2/V s) is yet to be achieved. Although n-type doping to poly-Ge in a low thermal budget is challenging because of the low solid solubility of n-type dopants in Ge,[34,35] heavy n-type doping (>10^{19} cm^{-3}) to Ge thin films has been achieved by short-time annealing techniques.[18,36] These techniques are promising for fabricating source/drain junctions for n-MOSFETs.

Conversely, to use n-type poly-Ge for the channel layer of inversion-type p-MOSFETs, low electron density n as well as high electron mobility μ_n is required. However, there has been difficulty in lowering n because counter doping to naturally highly p-type poly-Ge is unavoidable. In the present study, we aimed at the fabrication of n-type poly-Ge with high μ_n and low n by using our recent SPC technique. That is, we examined the low-temperature SPC of Sb-doped densified a-Ge layers. We discovered the phenomenon of crystal grain enlargement by Sb doping and therefore μ_n exceeded 200 cm^2/V s, while n was on the order of 10^{17} cm^{-3}. μ_n and n are the highest and the lowest record values among n-type poly-Ge layers directly grown on insulators, respectively.

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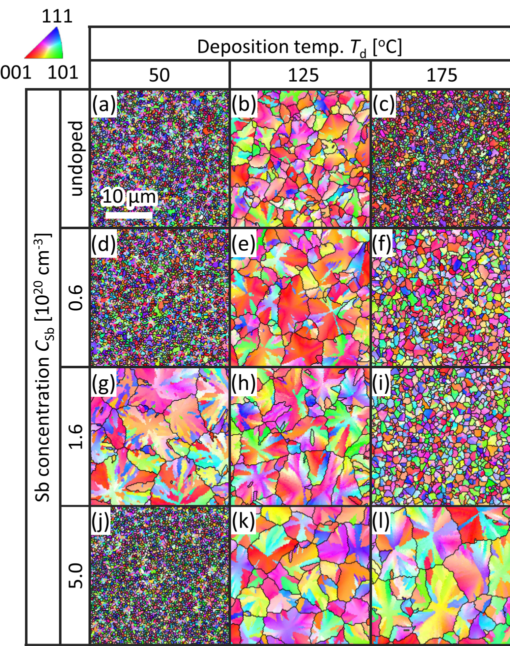

FIG. 1. IPFs of Sb-doped SPC-Ge summarized as the matrix composed of T_d (50, 125, and 175 °C) and C_{Sb} (0.6×10^{20}, 1.6×10^{20}, and 5.0×10^{20} cm^{-3}). Here, $t = 100$ nm and $T_g = 450$ °C. The data for undoped Ge are shown for comparison. The coloration indicates the crystal orientation (refer to the inset legend). The black solid lines in IPFs indicate random grain boundaries, where the grain boundary tolerance angle used to delineate one grain from another is 5°.

In experiments, Sb-doped Ge precursors were deposited on SiO_2 glass substrates using a Knudsen cell of a molecular beam deposition system (base pressure: 5×10^{-7} Pa). The Ge thickness, t, ranged from 100 to 500 nm, where the deposition rate of Ge was fixed at 1.0 nm/min. The temperature of the substrate during deposition, T_d, ranged from 50 to 200 °C. T_d spontaneously increased from room temperature to 50 °C even though the substrate was not heated; this was due to the heat radiation from the Knudsen cell. To modulate the Sb concentration, C_{Sb}, in the Ge layer, the temperature of the Sb Knudsen cell ranged from 260 to 300 °C. Using secondary ion mass spectrometry (SIMS), C_{Sb} was determined to be 0.6×10^{20}, 0.9×10^{20}, 1.6×10^{20}, 2.8×10^{20}, and 5.0×10^{20} cm^{-3} when the Sb Knudsen cell temperature was 260, 270, 280, 290, and 300 °C, respectively. C_{Sb} was constant regardless of T_d and before and after annealing. For comparison, undoped samples were also prepared. The samples were then loaded into a conventional tube furnace under a N_2 (99.9%) atmosphere and annealed at a growth temperature, T_g, of 450 °C for 5 h, 400 °C for 20 h, and 375 °C for 150 h to induce crystallization. For the samples with $T_d = 125$ °C, we performed postannealing (PA) at 500 °C for 5 h.

The inverse pole figures (IPFs) with grain boundaries in Ge were obtained using electron backscattering diffraction analyses (JEOL JSM-7001F with the TSL OIM analysis attachment). Figure 1 shows that the grain size strongly depends on both T_d and C_{Sb}. The grain size of undoped samples [Figs. 1(a)–1(c)] is dramatically improved by optimizing T_d. This phenomenon has been explained as the effect of densifying an amorphous precursor.[30] For $T_d = 125$ °C, the Sb-doped samples [Figs. 1(e), 1(h), and 1(k)] have an approximately two times larger grain size than the undoped sample [Fig. 1(b)]. For $C_{Sb} = 1.6 \times 10^{20}$ and 5.0×10^{20} cm^{-3}, large grains were also observed at $T_d = 50$ and 175 °C, respectively. To understand these phenomena, we investigated the influence of Sb doping on the crystallization rate.

We examined the C_{Sb} dependence of the crystallization rate from the annealing-time evolution observed by Raman spectroscopy (JASCO NRS-5100, spot diameter 20 μm, wavelength 532 nm). The crystallinity of the Ge layer is defined as the ratio of the Raman peak intensity of crystalline Ge (c-Ge) to that of a-Ge, as representatively shown in the inset in Fig. 2(a). Figure 2(a) shows that the annealing time for completing crystallization depends on C_{Sb}. Compared with undoped Ge, crystallization is fast for $C_{Sb} = 1.6 \times 10^{20}$ cm^{-3} while slow for $C_{Sb} = 5.0 \times 10^{20}$ cm^{-3}. We evaluated the crystallization rate more quantitatively using *in situ* optical microscopy during annealing (Linkam 10042 D with Keyence VH-5500). Figure 2(b) shows the typical growth evolution of SPC. The micrographs indicate that, during annealing, Ge nucleation occurs and then the domain grows laterally with increasing annealing time. The Ge domain size is saturated when the domains collide with each other. Figure 2(c) shows that the domain growth rate and the saturated domain size significantly vary with C_{Sb}. For $C_{Sb} = 1.6 \times 10^{20}$ cm^{-3}, both nucleation and lateral growth rates are higher than those of undoped Ge. This result is consistent with the phenomenon of impurity doping promoting the migration of semiconductor atoms and then enhancing the recrystallization rate of amorphous films.[37] Therefore, the grain size enlargement for

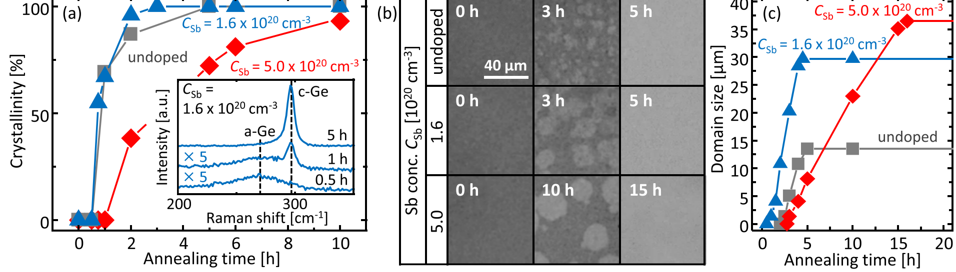

FIG. 2. Characteristics of the crystallization rate of undoped and Sb-doped ($C_{Sb} = 1.6 \times 10^{20}$ and 5.0×10^{20} cm^{-3}) SPC-Ge, where $t = 100$ nm, $T_d = 125$ °C, and $T_g = 400$ °C. (a) Crystallinity as a function of annealing time, determined by the annealing-time evolution of Raman spectra representatively shown in the inset. (b) *In situ* optical microscopy observation, where the dark-colored area indicates a-Ge and the bright-colored area indicates c-Ge. (c) Annealing time dependence of the domain size derived from the micrographs.

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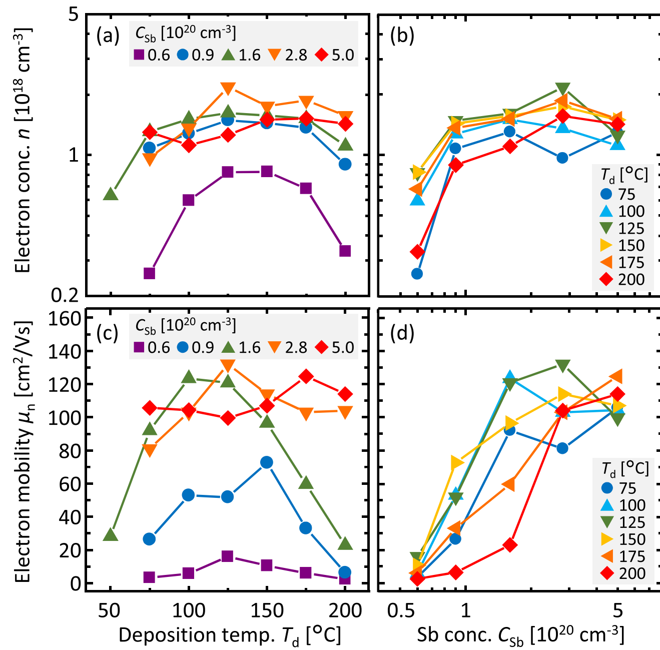


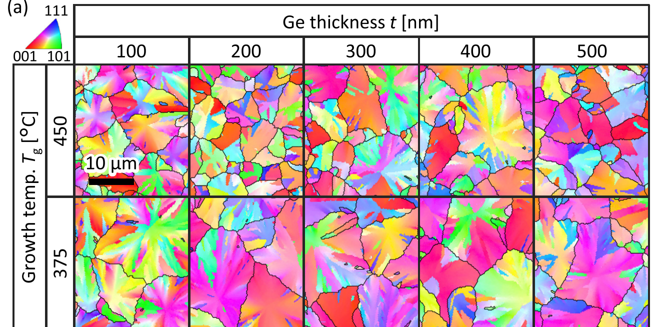
FIG. 3. Electrical properties of the Sb-doped SPC-Ge layers with $t = 100$ nm and $T_g = 450\,°C$, obtained from Hall effect measurements with the van der Pauw method. (a) and (b) n and (c) and (d) μ_n as functions of (a) and (c) T_d and (b) and (d) C_{Sb}.

$C_{Sb} \leq 1.6 \times 10^{20}\,cm^{-3}$ [Figs. 1(e) and 1(h)] is attributed to the promotion of lateral growth. The migration promotion of Ge atoms due to Sb doping likely densified a-Ge even at $T_d = 50\,°C$, resulting in large grain growth [Fig. 1(g)]. A similar behavior has also been reported in Sn-doped SPC-Ge.[38,39] Conversely, for $C_{Sb} = 5.0 \times 10^{20}\,cm^{-3}$, both nucleation and lateral growth rates are lower than those of undoped Ge. Therefore, for $C_{Sb} = 5.0 \times 10^{20}\,cm^{-3}$, the grain size enlargement [Fig. 1(k)] is owing to the suppression of nucleation. This is consistent with the fact that the grain size is enlarged even at $T_d = 175\,°C$ [Fig. 1(l)], where the as-deposited undoped Ge layer has dense nuclei.[30] Consequently, Sb doping in the Ge precursor has a large influence on the nucleation and lateral growth in subsequent SPC, allowing for large grain growth.

The electrical properties of the Sb-doped SPC-Ge layers were evaluated using Hall-effect measurements with the van der Pauw method (Bio-Rad HL5500PC). All samples showed n-type conduction owing to the self-organizing activation of Sb during SPC. Figure 3(a) shows that n depends on both T_d and C_{Sb}. In all C_{Sb}, n takes the maximum value around T_d that provides the maximum grain size (Fig. 1). This behavior is likely because the larger grain size provides the lower defect-induced acceptors[30,31] and/or the less Sb segregation at grain boundaries. Figure 3(b) shows that n is saturated at around $C_{Sb} = 2.8 \times 10^{20}\,cm^{-3}$ for each T_d. The activation ratio of Sb in Ge was estimated to be approximately 1% in the whole range of C_{Sb}, when not considering the acceptors in poly-Ge.[9,18] The solid solubility limit of Sb in Ge at $T_g = 450\,°C$ is approximately $10^{18}\,cm^{-3}$,[34] which is one reason for such a low activation ratio. Figure 3(c) shows that μ_n has the same tendency as n in each C_{Sb}: μ_n attains its maximum value around T_d that provides the maximum grain size (Fig. 1). This suggests that μ_n is determined by grain boundary scattering. Figure 3(d) shows that μ_n increases with increasing C_{Sb} and becomes the largest at approximately $C_{Sb} = 2.8 \times 10^{20}\,cm^{-3}$. This behavior is likely owing to the balance of the following effects: (i) a lower energy barrier height for the grain boundary, E_B, by higher n;[40] and (ii) larger carrier scattering by more segregated inactive Sb. A maximum μ_n of 130 cm²/Vs was achieved for $C_{Sb} = 2.8 \times 10^{20}\,cm^{-3}$ and $T_d = 125\,°C$.

To further improve μ_n, we investigated the effects of T_g and t. Figure 4(a) shows that the grain size increases by lowering T_g, reflecting the decrease in the nucleation frequency.[9,30] Conversely, the grain size is almost constant with respect to t. As shown in Fig. 4(b), generally, the grain size of undoped Ge decreases with increasing t. This behavior was explained as the bulk nucleation occurring in thick films while interfacial nucleation remained predominant in thin films.[31,38] These results suggest that crystallization was completed before bulk nucleation started owing to the growth rate enhancement by Sb doping. The grain size for $T_g = 375\,°C$ approaches twice that for $T_g = 450\,°C$ and exceeds 15 μm, the largest grain size among SPC-Ge, in the whole t range.

We investigated the effects of high-temperature PA (500 °C) on n and μ_n. We first discuss the data before PA. Figure 5(a) shows that n



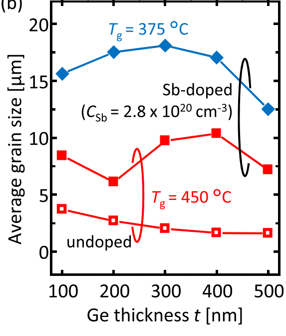


FIG. 4. Effect of T_g and t on the grain size of Sb-doped SPC-Ge with $C_{Sb} = 2.8 \times 10^{20}\,cm^{-3}$ and $T_d = 125\,°C$. (a) IPFs of the SPC-Ge summarized as the matrix composed of t (100, 200, 300, 400, and 500 nm) and T_g (450 and 375 °C). The coloration indicates the crystal orientation (refer to the inset legend). The black solid lines in IPFs indicate random grain boundaries, where the grain boundary tolerance angle used to delineate one grain from another is five degrees. (b) t dependence of the average grain size quantitatively calculated from electron backscattering diffraction analysis software. The data of undoped SPC-Ge are shown for comparison (Ref. 31).

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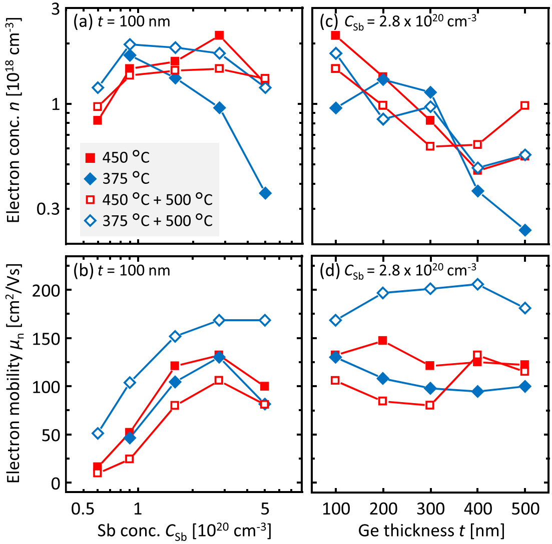

FIG. 5. Electrical properties of the Sb-doped SPC-Ge, where $T_d = 125\,^\circ$C and $T_g = 450$ and $375\,^\circ$C before and after PA ($500\,^\circ$C). (a) n and (b) μ_n for $t = 100$ nm samples as a function of C_{Sb}. (c) n and (d) μ_n for $C_{Sb} = 2.8 \times 10^{20}$ cm^{-3} samples as a function of t.

decreases with increasing C_{Sb} for $T_g = 375\,^\circ$C. Generally, in poly-Ge, n is determined by the balance between activated n-type dopants and defect-induced acceptors.[18] The lower T_g provides the lower solubility limit of Sb in Ge and then the more segregation of excess Sb, which produces defects in Ge. Therefore, the decrease in n with increasing C_{Sb} is likely because of the increase in defect-induced acceptors. Figure 5(b) shows that μ_n for $T_g = 375\,^\circ$C is slightly lower than that for $T_g = 450\,^\circ$C, which is attributed to larger carrier scattering caused by more Sb segregation and/or higher E_B by lower n.[40] Figure 5(c) shows that n decreases with increasing t for both $T_g = 375$ and $450\,^\circ$C. Although the reason is unclear, it is possible that an increase in the total amount of Sb increases the Sb segregation in Ge. Figure 5(d) shows that μ_n does not change significantly with respect to t. This reflects the balance between lower interface scattering due to larger t[31,38] and higher E_B due to lower n [Fig. 5(c)]. Thus, before PA, the $T_g = 375\,^\circ$C samples have no advantageous electrical properties over the $T_g = 450\,^\circ$C samples, whereas the $T_g = 375\,^\circ$C samples have larger grains than $T_g = 450\,^\circ$C samples.

PA improved the electrical properties of the $T_g = 375\,^\circ$C samples, while those of $T_g = 450\,^\circ$C samples were degraded or not changed. For $t = 100$ nm, both n and μ_n increased by PA in the whole C_{Sb} range [Figs. 5(a) and 5(b)]. Although such an increase in n was not pronounced for $t \geq 200$ nm [Fig. 5(c)], μ_n was improved approximately two times by PA [Fig. 5(d)]. To interpret the above behaviors in a unified way on n and μ_n, further investigations on the crystal quality, C_{Sb} and its state in Ge, and E_B are now underway. Consequently, n reaches 5×10^{17} cm^{-3} and μ_n over 200 cm^2/V s, which are the lowest n and highest μ_n values among n-type poly-Ge grown on insulators. Such a low n is because of the low density of defect-induced acceptors, that is, the high crystal quality of the current SPC-Ge. Although the current process is quite simple, long annealing time is required due to slow growth at low T_g. For commercial applications, growth promotion is necessary using a method such as adding Sn in Ge.[38,39]

In conclusion, Sb doping into an a-Ge precursor significantly influenced the subsequent SPC. The Sb doping on the order of 10^{20} cm^{-3} facilitated the SPC and increased the grain size of the resulting Ge layer. By superimposing the optimum T_d ($125\,^\circ$C) and low T_g ($375\,^\circ$C), the grain size exceeded 15 μm. PA at $500\,^\circ$C improved μ_n over 200 cm^2/V s. Moreover, the high crystallinity of the current SPC-Ge provided low defect-induced acceptors and achieved a low n of 5×10^{17} cm^{-3}. μ_n and n are the highest and the lowest values among n-type poly-Ge formed on insulators at low temperatures (<$900\,^\circ$C), respectively. Thus, impurity doping in the densified a-Ge precursor for SPC was quite effective for fabricating high-quality n-type poly-Ge on insulators at low temperatures. The findings in this study will provide a pathway for the monolithic integration of high-performance Ge-CMOS onto Si-LSIs and flat-panel displays.

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