# High hole mobility (≥ 500 $cm^2/Vs$) polycrystalline Ge films on $GeO_2$-coated glass and plastic substrates

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The highest recorded hole mobility in semiconductor films on insulators has been updated significantly. We investigate the solid-phase crystallization of a densified amorphous Ge layer formed on $GeO_2$-coated insulating substrates. The resulting polycrystalline Ge layer with a glass substrate consists of large grains (~10 μm) and exhibits a hole mobility as high as 620 $cm^2/Vs$, despite a low process temperature (500 °C). Even for the Ge layer formed on a flexible polyimide substrate at 375 °C, the hole mobility reaches 500 $cm^2/Vs$. These achievements will aid in realizing advanced electronics, simultaneously allowing for high performance, inexpensiveness, and flexibility.

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Monolithic integration of electronic and optoelectronic materials is a key technology for fabricating next-generation devices such as three-dimensional large-scale integrated circuits and multifunctional mobile terminals. Ge on insulator (GOI) is one of the most promising solutions for realizing advanced integrated devices because Ge has good compatibility with Si as well as high carrier mobility.[1–4] The process temperature for GOI is strictly limited by the thermal resistance of the substrates or underlying devices, which makes it challenging to achieve high-quality crystalline Ge thin films. So far, researchers have been investigating various techniques such as solid-phase crystallization (SPC),[5–9] laser annealing,[10–13] chemical vapor deposition,[14,15] flash lamp annealing,[16] and metal-induced crystallization.[17–22] However, the effective mobility of the Ge thin-film transistors (TFTs) has been no match for that of Si metal-oxide-semiconductor field-effect transistors (MOSFETs),[8,9,13,16,22] whereas the device technologies for Ge-MOSFETs have matured considerably.[23–27] Therefore, fabricating a high-quality Ge film with high carrier mobility is the most important issue to further improve Ge-TFTs.

SPC has many advantages over other methods, that is, no metal contamination, no melting-induced surface-ripples, and a simple process. However, for many years, the Hall hole mobility in conventional SPC-Ge on glass has been limited to 140 $cm^2/Vs$ by grain boundary scattering due to the small grains (< 1 μm).[5–9] Since 2015, research on incorporating Sn in Ge has become active,[28,29] which lowered the grain boundary scattering and improved the hole mobility up to 380 $cm^2/Vs$.[30,31] On the other hand, we recently found that the atomic density of amorphous Ge (a-Ge) significantly influenced subsequent SPC,[32] and updated the hole mobility to 450 $cm^2/Vs$ using a densified a-Ge.[33] This hole mobility was the highest ever recorded for a thin film directly grown on an insulator at temperatures below 900 °C.

In the present study, we focus on the underlayer material during SPC of the densified a-Ge. The crystallinity of Ge thin films is often influenced by interfacial materials, because

heterogeneous nucleation at interfaces is dominant.[21,29,34] By using $GeO_2$, which is also most suitable as a gate insulating material for Ge-MOSFETs,[24–27] we significantly break the existing record with a hole mobility of 620 $cm^2/Vs$. Furthermore, we develop a flexible plastic substrate and achieve a hole mobility of 500 $cm^2/Vs$ even at a low temperature process up to 375 °C.

In the experiment, to investigate the effects of the underlayer material, we prepared a 50-nm-thick insulating layer (SiN, $Al_2O_3$, and $GeO_2$) on a $SiO_2$ glass substrate using RF magnetron sputtering (base pressure: $3.0 \times 10^{-4}$ Pa). After that, an a-Ge layer was prepared using a Knudsen cell of a molecular beam deposition system (base pressure: $5 \times 10^{-7}$ Pa) while heating the samples at 150 °C. The thickness of the a-Ge layer, $t$, ranged from 100 to 600 nm. The samples were then loaded into a conventional tube furnace in a $N_2$ atmosphere and annealed to induce SPC. The growth temperature, $T_g$, was 450 °C for 5 h and 375 °C for 150 h. After evaluating these samples, we performed post annealing (PA) at 500 °C for 5 h. For comparison, a sample without forming an insulating layer, called a $SiO_2$ sample, was also prepared. In addition, a sample with a $GeO_2$-coated plastic substrate (125-μm-thick polyimide, Du Pont-Toray Co., Ltd.) was also prepared at 375 °C for 150 h.

The electron backscattering diffraction (EBSD) images in Figs. 1(a)–1(d) show that the grain size of the SPC-Ge layer strongly depends on the kind of the underlayer. This suggests that the frequency of Ge nucleation was changed because of the change of the interfacial energy between Ge and the underlayer.[21,29,34] From the EBSD analyses, the average grain size was determined to be 2.9 μm for $SiO_2$, 1.4 μm for SiN, 5.3 μm for $Al_2O_3$, and 4.5 μm for $GeO_2$. We used Hall-effect measurements with the Van der Pauw method to evaluate the electrical properties of the SPC-Ge layers. All samples showed p-type conduction, similar to conventional undoped SPC-Ge on glass.[5,6,32] This is because the point defects in Ge provide shallow acceptor levels that generate holes at room temperature.[35] Figure 1(e) shows that the

hole concentration $p$ and the hole mobility $\mu_p$ also depend on the underlayer material. The $GeO_2$ sample exhibits the lowest $p$ of $2.7\times10^{17}$ $cm^{-3}$ and the highest $\mu_p$ of 440 $cm^2/Vs$ among these underlayer materials. This improvement of $\mu_p$ likely reflects the reduction of grain boundary scattering and impurity scattering.[32] Therefore, we examined further improvement of carrier mobility focusing on the $GeO_2$ sample.

Figures 2(a)–2(f) show that the Ge grains of the $GeO_2$ sample are almost randomly oriented and that the grain size varies with both $t$ and $T_g$. Figure 2(g) shows that the Ge grain size, as determined by the EBSD analyses, is significantly improved by the insertion of $GeO_2$. The grain size decreases with increasing $t$ for all the sample conditions, likely reflecting the increase in bulk nucleation with increasing $t$.[30,33,35] The lower $T_g$ provides a larger grain size, which agrees with the conventional SPC.[5,30] This behavior, grain-size enlargement at lower temperature, is remarkable for the $GeO_2$ sample. The $GeO_2$ sample for $t$ = 100 nm and $T_g$ = 375 °C exhibits a grain size over 10 μm, which is the largest among SPC-Ge(Sn).[30-33]

We evaluated $p$ and $\mu_p$ of the samples before PA. Figures 3(a) and 3(b) show that $p$ decreases by inserting $GeO_2$ for all $t$ and $T_g$. This behavior suggests that the $GeO_2$ insertion lowered the defects in Ge generating holes, i.e., improved Ge crystallinity. Figures 3(c) and 3(d) show that the larger $t$ provides the higher $\mu_p$ despite the grain becoming smaller (Fig. 2(g)). This behavior was also seen in previous studies and explained to be due to interface scattering.[30,33] For $t \leq 200$ nm, the $GeO_2$ samples exhibit lower $\mu_p$ than the $SiO_2$ samples despite the much larger grain size (Fig. 2(g)). These results suggest that current Ge/$GeO_2$ interface provides larger interface scattering than Ge/$SiO_2$ interface. Conversely, for $t > 200$ nm, the $GeO_2$ samples exhibit higher $\mu_p$ than the $SiO_2$ samples. According to Matthiessen's rule and Irvin's curve,[1] $\mu_p$ for $t > 200$ nm is determined by the balance between grain boundary scattering and impurity scattering.[32,33] Therefore, $\mu_p$ enhancement by $GeO_2$ insertion is attributed to a decrease in grain boundary scattering by a large grain size and a reduction in

impurity scattering by $p$ reduction.

PA at 500 °C was performed for all the samples to reduce the point defects in Ge and then decrease the impurity scattering. Figures 3(a) and 3(b) show that, for both $GeO_2$ and $SiO_2$ samples, $p$ decreased after PA. This result suggests that the Ge atoms locally migrated via thermal diffusion and passivated point defects, generating holes, in the Ge layers. Figures 3(c) and 3(d) show that, for both $GeO_2$ and $SiO_2$ samples, $\mu_p$ improves for $t \geq 200$ nm, especially for $T_g = 375$ °C. This reflects in reduction of $p$, that is, impurity scattering. The highest $\mu_p$ of 620 $cm^2/Vs$ is recorded for the $GeO_2$ sample for $t = 500$ nm and $T_g = 375$ °C after PA.

Thus, we found that a $GeO_2$ underlayer dramatically improves the crystal and electrical properties of the SPC-Ge layer. For application to flexible devices, we prepared a 400-nm-thick Ge layer on a $GeO_2$-coated plastic substrate and induced SPC at $T_g = 375$ °C. Figure 4(a) shows that a Ge layer is formed on a plastic substrate and maintains its flexibility after the heat treatment. As shown in Fig. 4(b), the SPC-Ge layer on the plastic substrate has large grains equivalent to the SPC-Ge layer formed on $GeO_2$-coated glass (Fig. 2). The Ge layer exhibited $p$ of $3.1 \times 10^{17}$ $cm^{-3}$ and $\mu_p$ of 500 $cm^2/Vs$. This $\mu_p$ is much higher than that of any other semiconductor films synthesized on a plastic substrate.

Figure 4(c) shows that the current SPC-Ge layer on $GeO_2$-coated glass has the lowest $p$ among poly-Ge(Sn) on insulators, indicating that the Ge layer contains relatively few defects. The resulting $\mu_p$ of 620 $cm^2/Vs$ is higher than that for any other polycrystalline semiconductor layers, and even higher than that for single-crystal Ge layers epitaxially grown from Si-on-insulator substrates.[37,38] Moreover, $\mu_p$ reached 500 $cm^2/Vs$ even on a plastic substrate, exceeding that of single-crystal Si wafers.[1] These results mean that single-crystal wafers are no longer necessary for fabricating semiconductor films with a high carrier mobility.

In conclusion, we significantly updated the highest recorded $\mu_p$ of semiconductor films

directly grown on insulators at low temperatures (< 900 °C). The SPC of a densified a-Ge layer formed on a $GeO_2$-coated glass substrate provided $\mu_p$ of 620 $cm^2/Vs$, despite the temperature process being as low as 500 °C. This achievement was due to the reduction of both grain boundary scattering and impurity scattering owing to the grain size enlargement and the passivation of defect-induced acceptors. Even for Ge on a plastic substrate formed at 375 °C, $\mu_p$ reached 500 $cm^2/Vs$. Besides the advantages on carrier mobility and thermal budget, the process developed herein is simple enough for practical industrial applications. Therefore, these findings will aid in realizing advanced electronics, simultaneously allowing for high performance, inexpensiveness, and flexibility.

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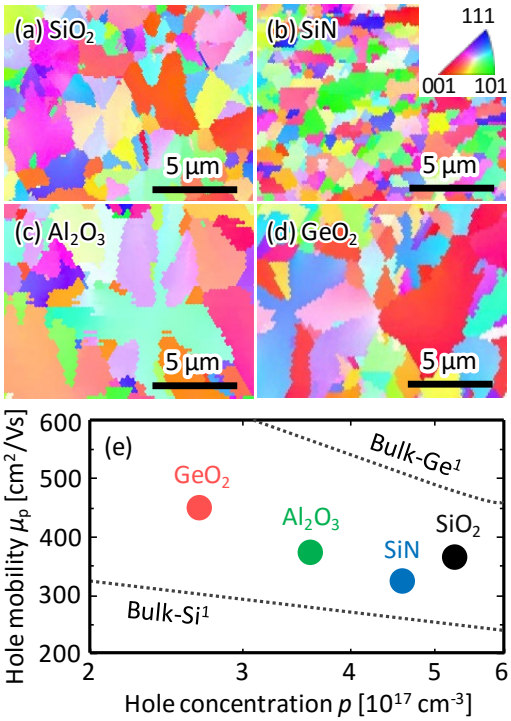


**FIG. 1.** Characteristics of the SPC-Ge layers for $t$ = 300 nm and $T_g$ = 450 °C, grown on various underlayers ($SiO_2$, SiN, $Al_2O_3$, and $GeO_2$) formed on a glass substrate. (a)–(d) EBSD images of the Ge layers, where the colors indicate the crystal orientation, according to the inserted color key. (e) Comparison of hole mobility $\mu_p$ and hole concentration $p$ of the samples. The data for single-crystal bulk Si and Ge are shown by dotted lines [Ref. 1].

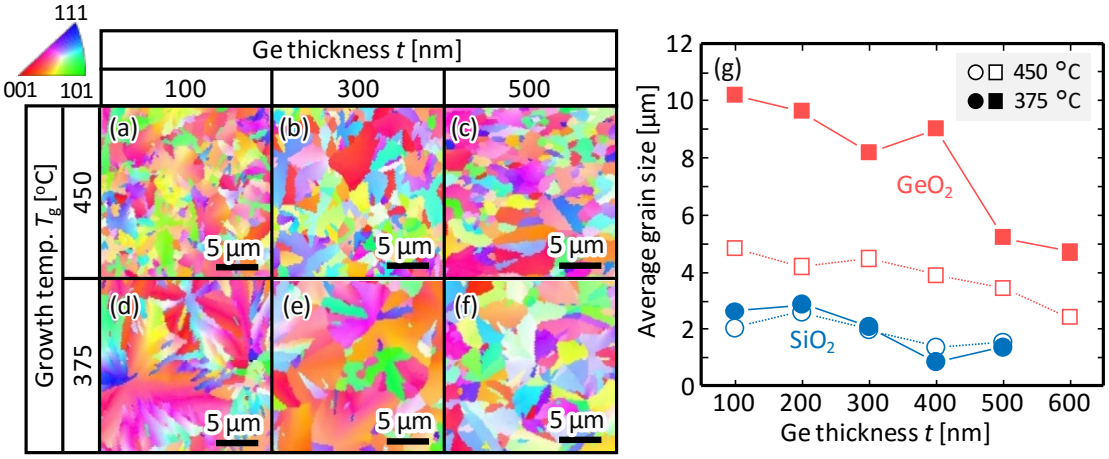


**FIG. 2.** Grain size of the SPC-Ge layers on a $GeO_2$-coated glass substrate. (a)–(f) EBSD images as a matrix of $t$ and $T_g$. The colors indicate the crystal orientation, according to the inserted color key. (g) Average grain size determined by the EBSD analyses with $T_g$ = 450 °C and 375 °C as a function of $t$. The data for the sample without $GeO_2$ (named $SiO_2$ sample) are shown for comparison.

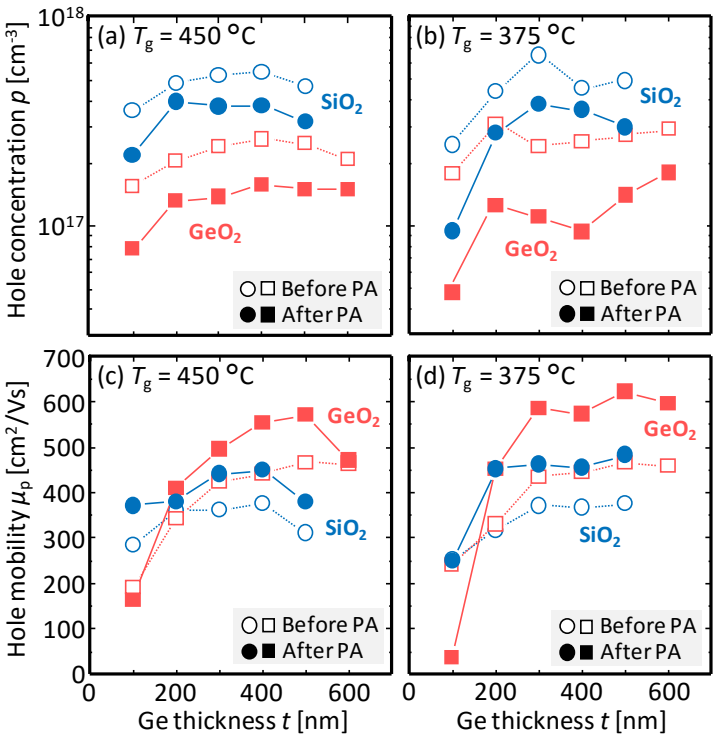


**FIG. 3.** Electrical properties of the SPC-Ge layers before and after PA (500 °C) as a function of $t$. (a),(b) Hole concentration $p$ and (c),(d) hole mobility $\mu_p$ for the $GeO_2$ and $SiO_2$ samples where $T_g$ = (a),(c) 450 °C and (b),(d) 375 °C. The data before PA are shown by open symbols and after PA by closed symbols.

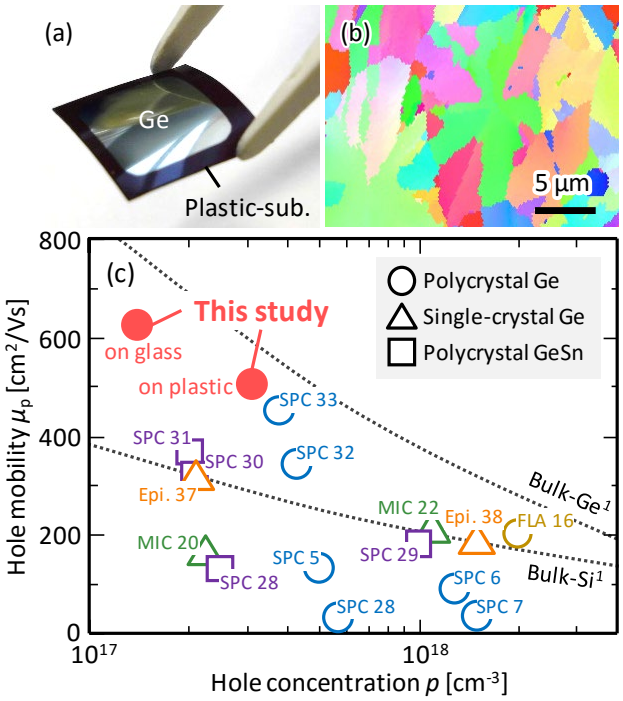


**FIG. 4.** (a) Photograph and (b) EBSD image of the SPC-Ge layer formed on a $GeO_2$-coated plastic substrate where $t$ = 400 nm and $T_g$ = 375 °C. (c) Comparison of the hole mobility $\mu_p$ and hole concentration $p$ of Ge(Sn) films on insulators. The growth method and the reference number are shown near each symbol. The data for single-crystal bulk Si and Ge are shown by dotted lines [Ref. 1].