Modeling and Characterization of Near-Interface Traps in SiC Metal-Oxide-Semiconductor Devices

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Modeling and Characterization of Near-Interface Traps in SiC Metal-Oxide-Semiconductor Devices

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To my family

Abstract

With the strong demand for energy saving and CO_2 reduction, power semiconductor devices have become indispensable in power-electronics applications, including hybrid vehicles and electrical vehicles, smart grid and so on. Since the past several decades, silicon (Si)-based devices have played an important role in power-electronics fields. However, the limits of Si material properties are far from enough to satisfy the increasing requirements. Therefore, wide-band gap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), which possess higher breakdown electric field and higher thermal conductivity than conventional Si semiconductors, have drawn much attention in recent years.

With regards to the wide-band gap materials, SiC is the only one which can be thermally oxidized to form the gate oxide layer (SiO_2), making it beneficial to fabricating metal-oxide-semiconductor field-effect transistors (MOSFETs). SiC MOSFETs have been extensively studied and commercialized in the power devices market. However, their performance is far from satisfactory and they are still encountering some big challenges, including the low channel mobility and threshold voltage instability. This is mainly ascribed to the high density of interface states (D_{it}). The possible origins of D_{it} have been explored for decades, and, among them, near-interface traps (NITs) have been considered as a major cause. NITs are the oxide traps which locate close to the interface of SiO_2/4H-SiC and can make response to the AC signal during *C–V* (capacitance-voltage) measurements. They act like interface traps electrically. However, physical origin of NITs is still unclear. Therefore, the NIT spatial distribution, which has not been fully considered, is very important to be investigated to further understand the nature of NITs. Besides, most of the early studies only focus on the NIT investigation in the conduction band side of 4H-SiC. Investigation of NITs in the valance band side is far from satisfactory, despite poor electrical properties of p-channel SiC MOSFETs. In this study, the density distribution of NITs near the conduction band edge is evaluated for 4H-SiC MOS capacitors with a modified distributed model, by taking the electron tunneling process into account. Besides, NITs in the valence band side are investigated by using a modified conductance method. This thesis consists of five chapters.

In Chapter 1, material properties of SiC and interface characteristics of the SiC MOS structures are introduced.

In Chapter 2, the modeling and characterization of NITs for n-type 4H-SiC MOS structures are investigated. A distributed model is applied for n-type 4H-SiC MOS capacitors by considering the tunneling process. The assumption of exponentially decaying distribution of NITs successfully explained the frequency dependence of capacitance and conductance in the strong accumulation conditions for the 4H-SiC MOS capacitors with different oxidation processes. The NIT density changes significantly by NO annealing.

In Chapter 3, the impact of oxide thickness on NITs for n-type 4H-SiC MOS structures is investigated. By investigating thickness dependence of NITs, the exponentially decaying distribution assumption of NITs is verified. In addition, the NIT density distribution as a function of oxide thickness is evaluated.

With increasing oxide thickness, total NIT density increases.

In Chapter 4, the modeling and characterization of NITs in the valance band side are investigated for p-type 4H-SiC MOS structure. The existence of NITs has been examined with a modified conductance method. The fast response of interface states contributes to the high frequency responses and can be evaluated by the standard conductance method. The low frequency responses are attributed to the NITs, which has been estimated with Cooper's model. The NIT density at different energy levels from the valence band edge of 4H-SiC is estimated.

In Chapter 5, the conclusions of this study are summarized. Furthermore, suggestions for future work are proposed.

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Contents

Chapter 1

Introduction

1.1 Background

With the development of human society, the global warming is becoming one of the most serious problems. Since the industrial revolution, the emission of carbon dioxide (CO_2) due to coal combustion and exhaust emission by human beings has been increasing year by year [1]. The global warming has been causing the deterioration of ecological environment, such as rising sea levels, melting of polar ice caps, raised temperatures, and so on [2]. Therefore, in order to slow down global warming and to achieve sustainable development, it is particularly urgent to realize energy conservation and CO_2 emission reduction.

In order to save energy, one of the urgent issues is to improve the energy conversion efficiency because energy loss occurs during many conversion steps from the power plants to the practical use in our daily life. The key to improving the energy conversion is using power electronics technology. Power electronics is the application of power semiconductor devices for the control and conversion of electric power, including AC/DC, DC/AC, DC/DC, and AC/AC conversions [3]. Therefore, the power semiconductor technology is the core to reduce energy loss. Since 1950s, the development of power semiconductor fields has been dominated by silicon (Si)-based devices, such as metal-oxide-semiconductor field-effect transistors (MOSFETs), gate turn-off thyristors (GTOs), insulated gate bipolar transistors (IGBTs), and so on. However, with higher requirements for power electronic equipment in modern industry, such as higher power, lower heat flux, smaller volume of an inverter, the conventional Si-based power devices are facing more challenges. The limits of material properties and unsatisfactory device performance make Si devices difficult to meet the growing industry demands. Therefore, the wide bandgap semiconductors have been attracting more attention for recent decades of years.

As a typical representative of wide bandgap material, silicon carbide (SiC) has been the preference in the area of high power applications. The SiC market growth is gradually accelerating in recent years due to the improved device performances.

1.2 Material properties of SiC

SiC is the group-IV compound semiconductor material and has the same number of Si and C atoms. SiC is a tetrahedral structure, formed by the connection of Si_4C or C_4Si. An outstanding feature of SiC is that more than 250 polytypes can be formed under different physical and chemical environments. According to the different stacking sequences of the Si-C bilayer, cubic (3C-SiC), hexagonal (*n*H-SiC), or rhombohedral (*n*R-SiC) crystal structures can be formed, where bilayer number of Si-C in one cycle is represented by *n*. In a close-packed system, the occupied sites are schematically shown in Fig. 1.1, where the denotations of A, B, and C are three possible sites, respectively. Among many

polytypes, three popular types—3C-SiC, 4H-SiC, and 6H-SiC are demonstrated in Fig. 1.2 [4, 5]. The material property comparisons are shown in Table 1.1 [4, 5]:

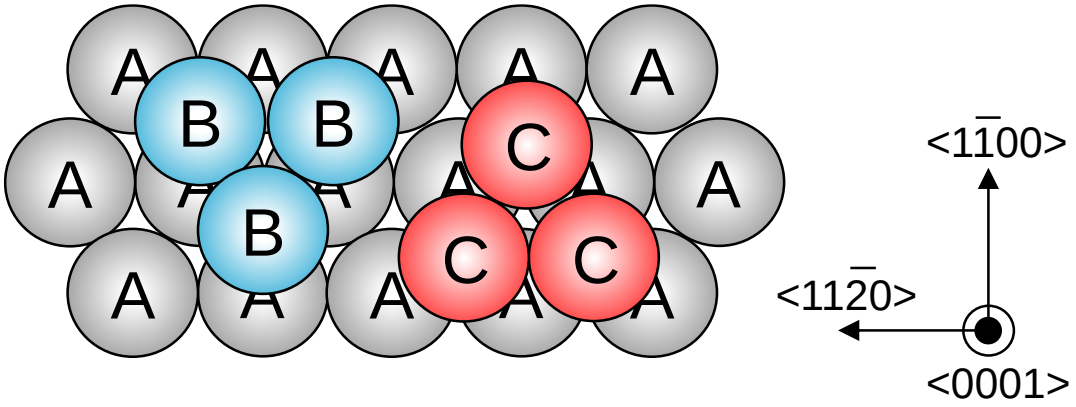
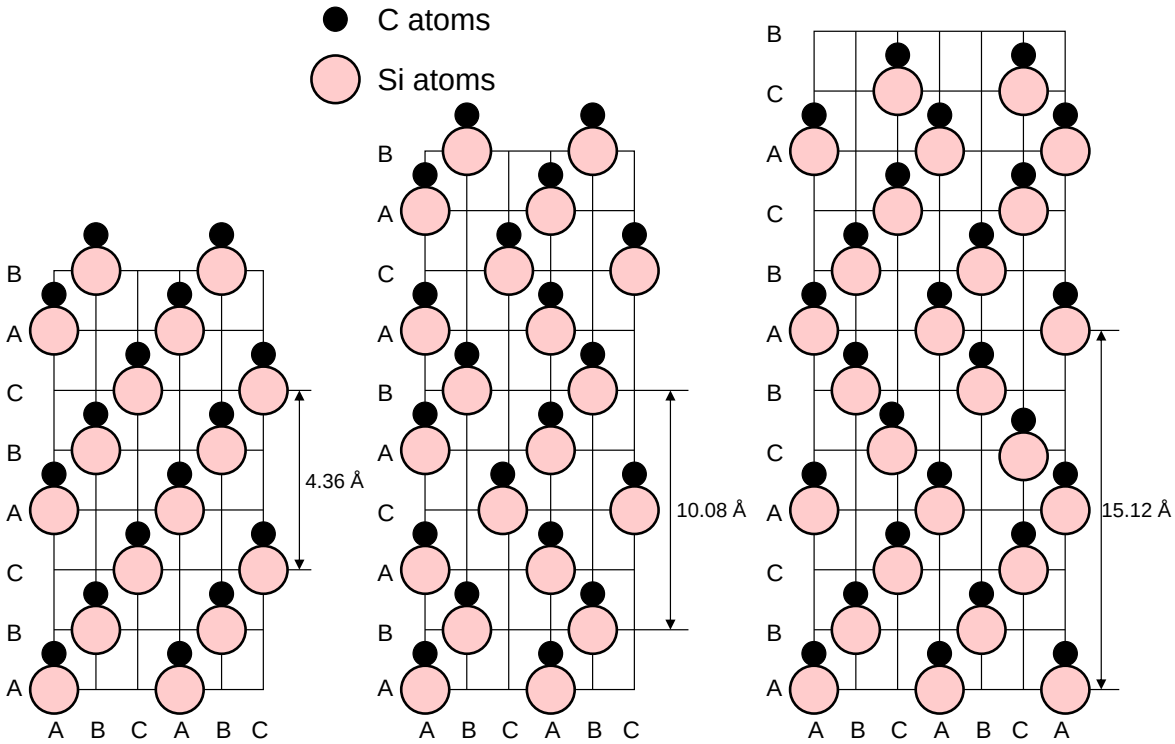


Fig. 1.1. Three possible occupation sites (denoted as A, B, and C) in the hexagonal close-packed system.



(a) 3C-SiC (b) 4H-SiC (c) 6H-SiC

Fig. 1.2. Stacking sequences of (a) 3C-SiC, (b) 4H-SiC, and (c) 6H-SiC, where Si and C atoms are distinguished by different sizes.

(a) Wide energy bandgap

The energy bandgap of 4H-SiC is almost three times wider than Si, which could lead to the low intrinsic carrier density in SiC devices and thus result in low off-state leakage current. Therefore, SiC devices can reduce the power loss and they are suitable for high temperature and high power applications, such as solar inverter, rail transport, smart grids and so on. Also, because of the superior

stability of SiC, SiC devices can be applied in the aerospace field to resist radiation and strong electromagnetic interference.

Table 1.1 Physical properties of Si, 3C-, 4H-, and 6H-SiC [4, 5].

Properties	Si	3C-SiC	4H-SiC	6H-SiC
Bandgap (eV)	1.12	2.23	3.26	3.02
Critical breakdown field (MV/cm)	0.3	1.5	2.8	3
Thermal conductivity ($W \cdot cm^{-1} \cdot K^{-1}$)	1.5	4.9	4.9	4.9
Saturation drift velocity ($cm \cdot s^{-1}$)	1.0×10^7	2.7×10^7	2.2×10^7	1.9×10^7
Relative permittivity	11.9	9.72	9.7 ($\perp c$) 10.2 ($//c$)	9.7 ($\perp c$) 10.2 ($//c$)
Electron mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	1350	1000	1000 ($\perp c$) 1200 ($//c$)	450 ($\perp c$) 100 ($//c$)
Hole mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	420	50	120	100

(b) High critical breakdown field

Critical breakdown field is an important parameter of power devices, namely, the highest electric field in avalanche breakdown. The critical breakdown field of 4H-SiC is about 10 times of Si. In other words, in the case of the same drift layer thickness, 4H-SiC can endure higher voltages, which makes SiC devices significantly superior in high voltage applications more than 1 kV. In general, the on-resistance has a trade-off relationship with breakdown field; therefore, in the same voltage rating, the on-resistance of 4H-SiC unipolar devices can be reduced significantly. Besides, for the same blocking voltage, the drift layer of 4H-SiC devices can be thinner and the doping concentration can be higher, thus significantly reducing the on-resistance and conduction loss.

(c) High thermal conductivity

Temperature change is the main factor for the instability of devices. Especially, carrier mobility can be affected strongly and it would decrease dramatically with increasing temperature. Therefore, it is necessary to dissipate the heat in devices generated due to the impedance loss during long-term and high-temperature operations. Thus, thermal conductivity is an important parameter to judge the heat dissipation efficiency. The thermal conductivity of 4H-SiC is around three times higher compared with that of Si, which is beneficial to heat dissipation.

(d) High electron saturation drift velocity

For microwave devices, it is important to improve the transconductance by reducing the channel length and using the material with higher electron saturation drift velocity. When the channel length is short enough, the velocity of electrons in the channel reaches the saturation value because of high electric field. Under high electric field condition of the microwave devices, the transconductance is proportional to the saturation drift velocity. The high electron saturation drift velocity of 4H-SiC also makes 4H-SiC devices suitable for microwave applications.

(e) Low relative permittivity

Compared with Si, the lower relative permittivity of SiC can reduce the parasitic capacitance and

thus improve the operating speed of SiC devices, which would be suitable for high-frequency and microwave devices.

(f) The ability to form oxide by thermal oxidation

SiC is the only compound semiconductor which is able to form SiO_2 by thermal oxidation. This unique property makes the fabrication of SiC MOSFETs compatible with mature fabrication process of Si MOSFETs, which would be beneficial to realize good performance of devices and to promote the industrialization of SiC MOSFETs.

In light of the analysis above, SiC power devices possess many merits compared with conventional Si power devices, including low on-resistance, low switching loss, fast frequency response, and good stability at high temperature, which makes them suitable for the power fields of high power, high voltage, high temperature, high frequency, anti-radiation, and low power loss. Among commercially available SiC polytypes, due to the wide bandgap and high electron mobility, 4H-SiC is the most popular polytype for SiC device fabrication. Therefore, the study of this thesis keeps the focus on 4H-SiC.

1.3 SiC power devices

As described in the section above, the superior physical and electrical properties of 4H-SiC make 4H-SiC power devices possess much higher figure of merit (FOM) than conventional power devices. The SiC power electronic devices mainly include (i) unipolar-type diodes such as Schottky barrier diodes (SBDs) [6–8], (ii) bipolar-type diodes such as PiN diodes [9–11], (iii) unipolar-type transistors such as MOSFETs [8, 12, 13], junction-gate field-effect transistors (JFETs) [14], and (iv) bipolar transistors such as bipolar junction transistors (BJTs) [15] and insulated gate bipolar transistors (IGBTs) [16, 17]. Unipolar and bipolar transistors are mainly used for power switching devices to control the electric power to a load.

Because the conduction of the current is controlled by the depletion layer of a p-n junction, the threshold voltage (V_{th}) of SiC JFETs tends to be negative. SiC BJTs are suitable for high power devices because of the small forward drop voltage and small on-resistance. However, as the current-controlled devices, the drive circuit of SiC BJTs is complex and the current gain is low. SiC IGBTs are expected to be the devices with significantly high blocking voltages more than 10 kV, which requires very thick, low concentration and high quality epitaxial layers. Due to the high requirements of the substrate and the immature fabrication process of SiC IGBTs, the commercialization of SiC IGBTs is still on the way. Because SiC IGBTs are based on the MOS gate control, the interface properties of SiC IGBTs are also important and the electron injection efficiency is strongly affected by the channel resistance for the n-channel case [17]. So far, the development of 4H-SiC MOSFETs is the fastest, not only due to their compatible process with Si MOSFETs, but also owing to the reason that the drain current is controlled by gate bias, and extra gate voltage is not required on off-state. Besides, the current conduction in the drift layer only relies on the majority carriers and the switching speed of SiC MOSFETs is very fast.

As a kind of unipolar devices, 4H-SiC MOSFETs feature low on-resistance, high input impedance,

fast switching speed and relatively high blocking voltage (typically 600 V to 3.3 kV). They are considered as ideal high power switching devices. By using 4H-SiC MOSFETs, the power loss can be saved significantly in the fields of photovoltaic inverters, high railway, hybrid electric vehicle, appliance, *etc*. [18]. Therefore, this study aims at the investigation of 4H-SiC MOSFETs.

1.4 SiC MOSFETs and MOS structures

1.4.1 Challenges of SiC MOSFETs

The schematic structure of 4H-SiC double-implanted MOSFET (DMOSFET) is shown in Fig. 1.3. The on-resistance (R_{on}) in a typical 4H-SiC DMOSFET consists of many components except R_{drift}, as illustrated in Fig. 1.3, containing source contact resistance (R_{cs}), source resistance (R_n), channel resistance (R_{ch}), JFET resistance (R_j), substrate resistance (R_{sub}), and drain contact resistance (R_{dc}). In ideal case, the minimum value of R_{on} depends on the specific drift resistance, which is expressed as follows:

$$R_{\text{drift,sp}} \propto \frac{V_B^2}{\mu_N \varepsilon_S F_{\text{crit}}^3}, \tag{1.1}$$

where V_B is the blocking voltage, μ_N the electron mobility vertical to the interface of SiO_2/SiC, ε_S the permittivity of SiC, F_{crit} the critical breakdown field. The specific on-resistance represents the ideal resistance in the drift layer (R_{drift}) and neglects other resistances. Because of much higher breakdown field of SiC, the specific resistance of SiC devices can be reduced significantly compared with Si devices in theory, as shown in Fig. 1.4.

However, the effect of channel resistance (R_{ch}) on the specific on-resistance has to be considered in 4H-SiC MOSFETs because of low channel mobility. The specific R_{ch} can be expressed as follows:

$$R_{\text{ch,sp}} = \frac{LP}{2C_{ox}\mu_n^{ch}(V_G - V_{th})}. \tag{1.2}$$

Here, L, P, $C_{ox,}$ and μ_n^{ch}, are the channel length, cell pitch, capacitance of SiO_2 per unit area and the electron mobility in the inversion layer, respectively. Gate voltage is represented by V_G, and threshold voltage is represented by V_{th} [19]. $C_{ox}(V_G - V_{th})$ is equal to $\varepsilon_{ox}F_{ox}$, where ε_{ox} represents permittivity of the oxide and F_{ox} stands for the oxide electric field. The interface property of SiO_2/SiC determines the V_{th} and μ_n^{ch}, and thus affects R_{ch} and R_{on}. The effect of μ_n^{ch} on R_{on} is illustrated in Fig. 1.4, where L, P and F_{ox} are assumed with the values of 0.5 μm, 8 μm, and 3 MV/cm, respectively.

In the SiC case, due to the existence of high-density interface states at and near the interface of SiO_2/SiC, channel mobility is extremely low and thus R_{ch} would be very high [20–24]. The high R_{ch} would contribute to the high on-resistance and thus degrade the performance of 4H-SiC MOSFETs. So far, for the commercial 4H-SiC MOSFETs, the channel mobility can only reach up to 50 $cm^2V^{-1}s^{-1}$ with the optimized nitric oxide annealing, the standard passivation technique to reduce interface states [25]. Besides, interface states at the interface and in the oxide also lead to large V_{th} instability [26–28], which degrades the stability of 4H-SiC MOSFETs.

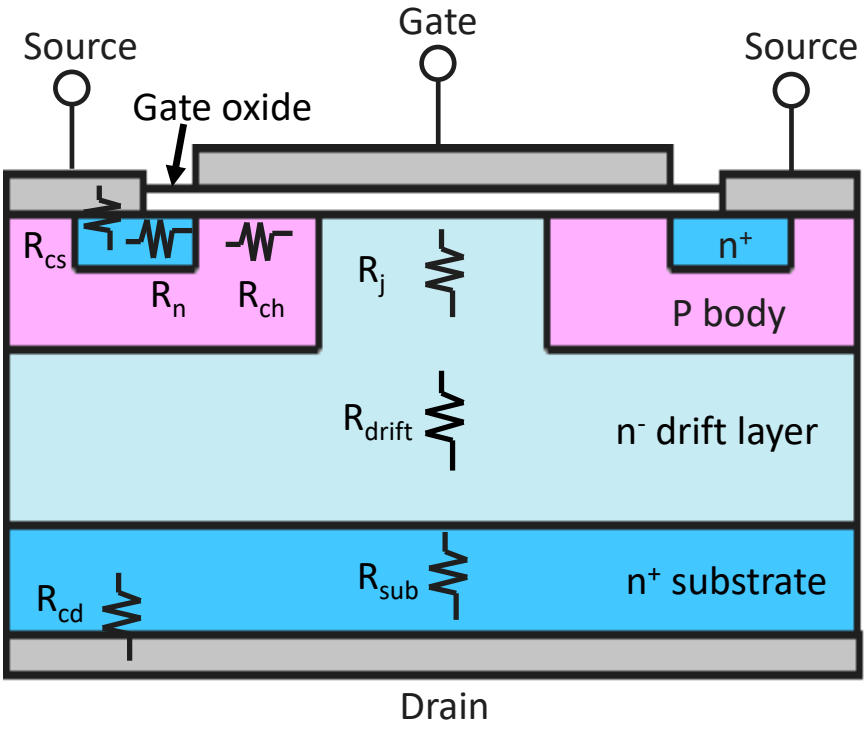


Fig. 1.3. Schematic of SiC DMOSFET.

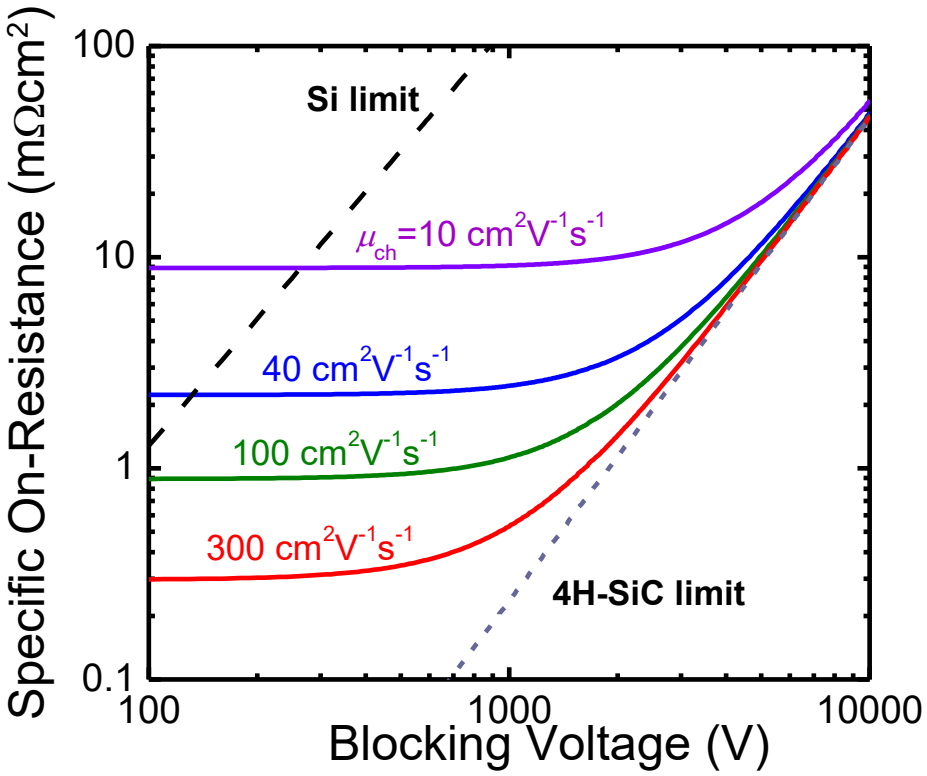


Fig. 1.4. Specific on-resistance versus blocking voltage for Si and 4H-SiC power DMOSFETs and channel mobility. Here, the values of 0.5 μm, 8 μm, and 3.0 MV/cm are assumed for channel length, cell pitch and electric field in the gate oxide, respectively.

To solve these problems mentioned above in 4H-SiC MOSFETs, it is significant to investigate the interface properties by using 4H-SiC MOS capacitors.

1.4.2 SiC oxidation

Similar with the oxidation process of Si, the oxide layer can be formed by thermally oxidizing SiC. However, the oxidation rate of SiC is much slower by comparison with Si case at the same temperature, and it has strong surface orientation dependence [29]. The oxidation process can be governed by the reaction expressed below:

$$2SiC + 3O_2 \rightarrow 2SiO_2 + 2CO\,. \tag{1.3}$$

Because in SiC, there exist both Si and C atoms, the oxidation process becomes much more complex and thus the conventional "Deal-Grove model" [30] failed to directly explain the oxidation kinetics of SiC. In recent years, Hijikata *et al*. proposed a "Si and C emission" model and explained the oxidation rate of SiC [31–35]. In this model, the Si and C atoms are considered to emit into SiO_2 and with increasing the oxidation time, the Si and C interstitials would accumulate in SiO_2 and thus lead to the low oxidation rate [31–35]. The complex oxidation process of SiC may lead to the high density of interface states. By far, the interface state origin is still under debate and many investigations have been made to explore the possible reasons.

1.4.3 Possible origins of high trap density at SiC/SiO_2 interface

The interface state density (D_{it}) at SiO_2/SiC interface is typically two orders higher than SiO_2/Si and it has reached to 10^{13}–10^{14} $cm^{-2}eV^{-1}$ near the conduction band edge (E_c) of SiC [4, 22, 23]. Pensl *et al*. summarized three possibilities of D_{it} origin, as shown in Fig. 1.5 [36].

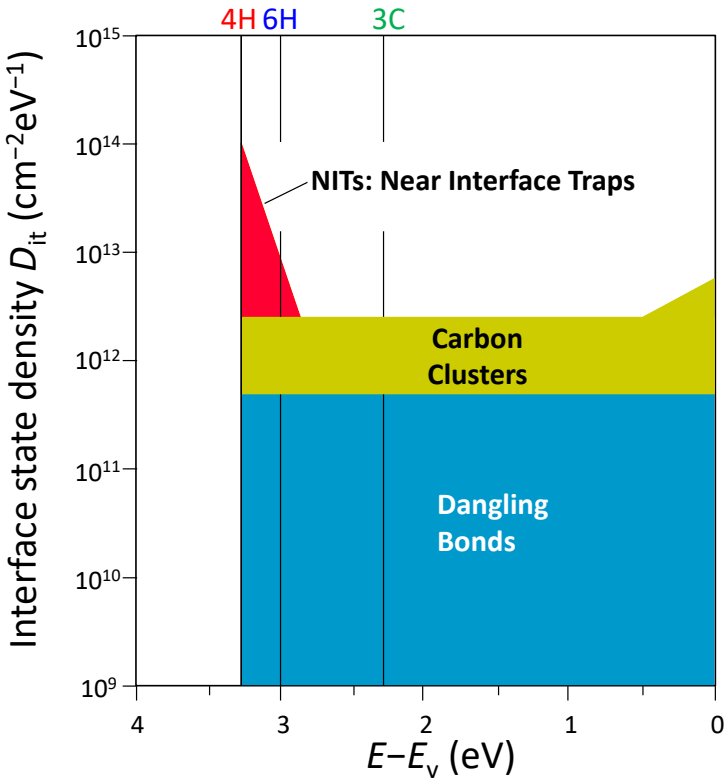


Fig. 1.5. Schematic illustration of D_{it} at SiC/SiO_2 interface [36].

(1) Si and C dangling bonds

In conventional SiO_2/Si interface system, Si dangling bonds, which are caused by the lattice mismatch between SiO_2 and Si, are the main reason for the high D_{it}. The Si dangling bonds are called "Pb center", and one of the bonds of Si is dangling bond and the other three are bonded with Si atoms in the substrate [37, 38]. These Si dangling bonds were effectively passivated by post oxidation annealing with hydrogen at 400 ^{o}C. Due to the interface similarity of SiO_2/SiC and SiO_2/Si interfaces, Si dangling bonds have also been considered as the possible reason. However, previous studies reported that the H_2 annealing at around 400 ^{o}C is not effective to reduce the D_{it} in SiO_2/SiC case [39, 40]. This indicates that Si dangling bonds cannot be the main origin of high trap density in SiC MOS structures. Later, electron paramagnetic resonance (EPR) measurements detected the C dangling bonds [41, 42], and they were passivated by annealing in H_2 atmosphere at a high temperature around 800 ^{o}C [43]. However, the density of C dangling bonds is not so high.

(2) Carbon clusters

The main reason for the big difference between SiO_2/SiC and SiO_2/Si is the existence of C atoms. During the oxidation of SiC, in ideal case, all of C atoms should have reacted with O_2, and the C atoms should be emitted out the oxide with the forms of CO and/or CO_2. However, in the practical oxidation process of SiC, C atoms cannot be emitted completely and excess carbon remains at the SiO_2/SiC interface. Many experimental studies, including the X-ray photoelectron spectroscopy (XPS) [44], atomic force microscope (AFM) [45], and electron energy loss spectroscopy (EELS) analysis [46], revealed the existence of excess carbon, which is considered as an important origin of high D_{it}. Afanas'ev *et al*. reported that the carbon clusters are the main existent forms of the excess carbon by employing the measurements of the internal photoemission of electrons (IPE) [39, 40].

However, the existence of carbon cluster is questioned afterwards. Based on the measurements of tunable high energy X-ray photoemission spectrometer (THE-XPS) by Virojanadara *et al*. [47], positron annihilation spectroscopy (PAS) by Dekker *et al*. [48], high-resolution transmission electron microscopy (HRTEM), EELS by Pippel *et al*. [49], and the synchrotron XPS by Watanabe *et al*. [50], the carbon clusters or the graphitic regions at and near the SiO_2/SiC interface were not detected. According to medium energy ion scattering (MEIS) measurements by Zhu *et al*., the detected excess carbon is less than 1.8×10^{14} cm^{-2} [51]. Therefore, it is very controversial about the existence of the carbon clusters.

(3) Near-interface traps (NITs)

Another important origin of high D_{it} is considered to be NITs. The general consensus is that NITs are the main reason for high D_{it} near the E_c of 4H-SiC [52]. Afanas'ev *et al*. conducted photon stimulated tunneling (PST) measurements and revealed that NITs are the intrinsic defects in SiO_2 and their energy levels are around 2.8 eV below the E_c of SiO_2. This finding is also supported by Schörner *et al*. [53]. The schematic band diagrams of Si, SiO_2, and various SiC polytypes (3C-, 6H-, and 4H-SiC) are demonstrated in Fig. 1.6. It can be seen that the NIT energy level is very close to the E_c of 4H-SiC. Therefore, they can capture and scatter the free channel carriers in 4H-SiC MOSFETs and thus dramatically degrade the channel mobility.

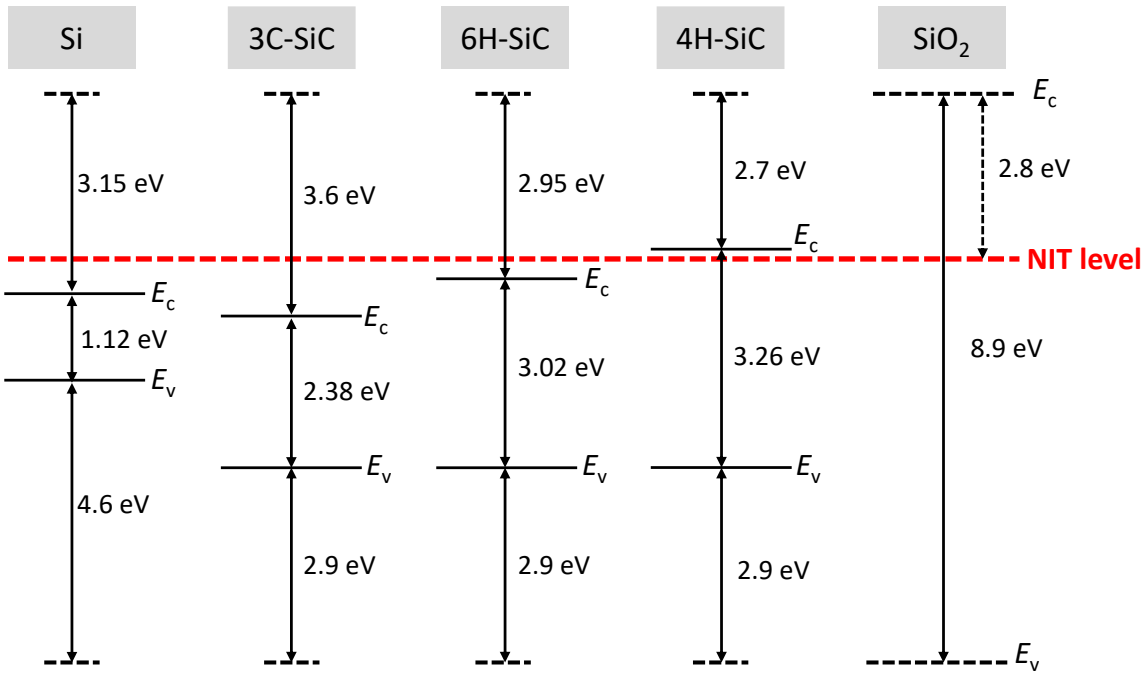


Fig. 1.6. Schematic band diagrams for Si, SiO_2, 3C-, 6H-, and 4H-SiC [39].

From the review of D_{it} investigations, despite the unclear origin of D_{it}, it could be deduced that the NITs near the E_c of 4H-SiC are considered to be harmful defects, resulting in the low channel mobility and large threshold voltage instability for n-channel MOSFETs. It should be pointed out that most of early studies have focused on the NITs near the E_c of 4H-SiC. However, the investigation of NITs in the valence band side is also important. In n-channel 4H-SiC MOSFETs, because the channel region is p-type 4H-SiC, hole trapping would also cause the threshold voltage instability [54, 55]. Also, p-channel 4H-SiC MOSFETs, indispensable for the application of complementary MOS (CMOS) logic devices [56, 57] and complementary inverters [58, 59], suffer from high channel resistance and large V_{th} instability [60, 61]. The NITs near the valence band side of 4H-SiC can be considered as a main reason. Therefore, the investigation of NITs for both n- and p-type 4H-SiC MOS structures would be very important.

1.4.4 Review of studies for NITs

Figure 1.7 illustrates the schematic diagram of NITs in a typical SiO_2/4H-SiC MOS structure [62]. It can be seen that the NITs locate close to the interface of SiO_2/4H-SiC. Therefore, they can exchange charges with 4H-SiC during the measurements.

As discussed in the section above, in order to enhance the interface properties of 4H-SiC MOS structures, it is significant to investigate the NITs. The existence of NITs was first detected by PST measurements as described above [39, 40]. Since then, some measurement techniques have been used to investigate the nature of NITs.

The thermal dielectric relaxation current (TDRC) method was applied to SiO_2/SiC interface by Rudenko *et al*. Based on the TDRC spectra with varying charging and discharging temperatures, the

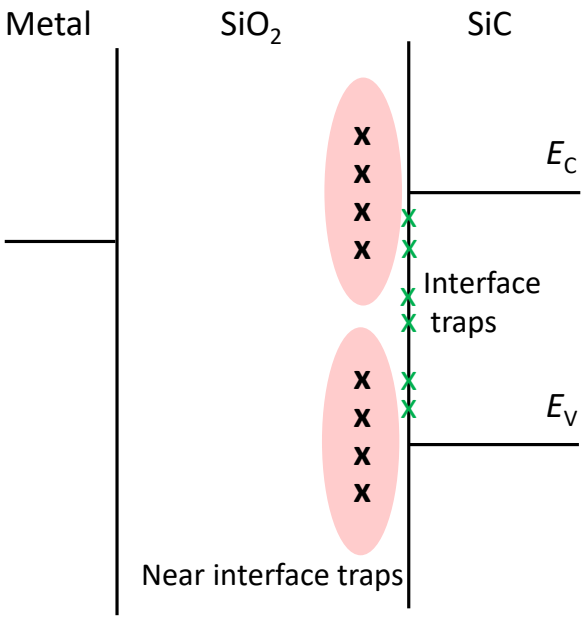


Fig. 1.7. Schematic diagram of NITs in a typical SiO_2/4H-SiC MOS structure.

existence of NITs was identified [63, 64]. Around the same time, Ólafsson *et al*. observed both the fast and slow interface states in the shallow region near the E_c of 4H-SiC by constant-capacitance deep level transient spectroscopy (CCDLTS) [65]. From the two different orders of capture cross sections obtained by CCDLTS, the smaller capture cross sections reflect the existence of NITs [65]. Later, Chen *et al*. supported this finding with CCDLTS and double-CCDLTS measurements [66]. The different capture cross sections, which varied several orders of magnitude, revealed that a significant proportion of traps locate at some distances from the interface. By comparing obtained trap profiles with Hi-Lo *C*–*V* method and CCDLTS measurements, Chen *et al*. pointed out that the large trap density close to the E_c of 4H-SiC cannot be detected accurately by CCDLTS measurement because of the measurement time scale [66]. This is also consistent with the fast recovery of threshold voltage after the release of gate bias reported by Sometani *et al*. [26–28].

Recently, Moghadam *et al*. proposed transient current method to investigate the NITs [67]. By changing the gate voltage sharply, the transient current was monitored as a function of time. By considering electron tunneling process to the near interface traps, the density of NITs was extracted. In his work, a uniform distribution of NITs was assumed [67]. However, the distribution of NITs was not fully considered. More recently, transient capacitance (*C*–*t*) measurements at various temperatures were conducted by Fujino *et al*. to estimate the effective density of NITs versus energy levels from E_c of 4H-SiC [68]. Despite the fact that the spatial distribution of NITs was not considered, the capacitance discrepancy between the high and low temperature *C*–*t* results revealed that there exist more NITs in the oxide adjacent to the interface [68].

From different kinds of experimental methods, the existence of NITs is identified. However, the possible origin of NITs is still unclear. Afanas'ev *et al*. believed that NITs may originate from the excess Si atoms or oxygen vacancies [39]. This is also consistent with the Si and C emission into SiO_2 during SiC oxidation [31]. To further make the possible reasons of NITs clear, several groups have focused on the first principle calculations while no consensus is reached. Knaup *et al*. reported that

the Si interstitials or carbon dimers may be responsible for the NITs [69]. However, these defects cannot explain the NIT existence at SiO_2/Si interface which has been indicated by PST measurements [35, 36]. Shen *et al*. reported C di-interstitials in the SiC side would be the possible origin of interface states [70]. Based on the hybrid density functions by Devynck *et al*., the generated energy levels of various possible defects in both SiC and SiO_2 sides, including hydrogen-related, carbon-related, and oxygen-related defects were calculated [71]. The Si_2-C-O structure in SiO_2 side is considered to be the origin of NITs because this structure produces narrow peaks both near E_c and E_v of 4H-SiC, compatible with NITs [71].

Despite various early studies of NITs, the nature of NITs is still under debate and the quantitative analysis is far from enough. Therefore, it is necessary to investigate NITs for the n- and p-type 4H-SiC MOS structures.

1.5 Objectives and outline of this thesis

The existence of NITs in the E_c and E_v sides of SiO_2/4H-SiC interface is considered to be the major reason for low channel mobility and large threshold voltage shift of 4H-SiC MOSFETs, which hinders their development. Therefore, investigation of NITs is very important to solve the problems. However, according to early studies, the possible origin of NITs is still unclear, and the quantitative analysis of NITs is far from enough. In order to further understand the nature of NITs, the investigation of the spatial distribution of NITs is very important.

In this thesis, the modeling and quantitative characterization of NITs are studied for both the E_c and E_v sides of 4H-SiC.

In Chapter 2, the modeling and characterization of NITs for n-type 4H-SiC MOS structure are estimated. A distributed model was applied with consideration of the tunneling process for n-type 4H-SiC MOS capacitors. By assuming an exponentially decaying distribution of NITs, the frequency-dependent properties of capacitance and conductance were successfully explained in the strong accumulation conditions for the capacitors with dry oxidation and nitrided passivation with different times. NO annealing dramatically changed the density of NITs.

In Chapter 3, the impact of oxide thickness on NITs in the E_c side of 4H-SiC is investigated. With investigation of thickness dependence of NITs, the exponentially decaying distribution assumption of NITs was verified. In addition, NIT density distribution as a function of SiO_2 thickness was evaluated and it was revealed that there exist more NITs in thicker SiO_2.

In Chapter 4, the modeling and characterization of NITs in the E_v side were investigated for p-type 4H-SiC MOS structure. The existence of NITs was examined with a modified conductance method. High frequency responses were ascribed to fast response of interface states, which were characterized by Gaussian fitting with the conductance method. Low frequency responses were attributed to the NITs, which was estimated with Cooper's model. The NIT density versus the energy level from E_v of 4H-SiC was estimated.

In Chapter 5, the conclusions of this work were summarized. Finally, suggestions for future work were proposed.

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Chapter 2

Modeling and characterization of NITs for n-type 4H-SiC MOS structure

2.1 Introduction

As written in Chapter 1, it is known that the existence of NITs near the conduction band edge (E_c) of 4H-SiC is considered to be one of the most important reasons for the low channel mobility and high instability of threshold voltage in n-type 4H-SiC MOSFETs. Therefore, the investigation of NITs would be important to solve the problems and to improve the performance of n-type 4H-SiC MOSFETs. Some early studies have been performed to evaluate NITs, as introduced in Chapter 1. However, the early studies mainly focused on the qualitative analysis of NITs, and NIT spatial distribution has not been fully estimated. Because of the unclear NIT origin, the spatial distribution investigation of NITs would be important, which can facilitate the understanding of NIT nature. Therefore, in this chapter, the spatial distribution of NITs in the E_c side of SiO_2/4H-SiC interface was studied.

Because NITs locate in the SiO_2 layer and their energy levels are evaluated to be close to the E_c of 4H-SiC [1, 2], as schematically illustrated in Fig. 2.1, it makes NIT investigation more difficult. To estimate the density distribution of NITs near the E_c of 4H-SiC, frequency dispersion of capacitance and conductance was investigated with a modified distributed circuit model by considering the electron tunneling process with NITs in the strong accumulation condition. This model will be described in next section.

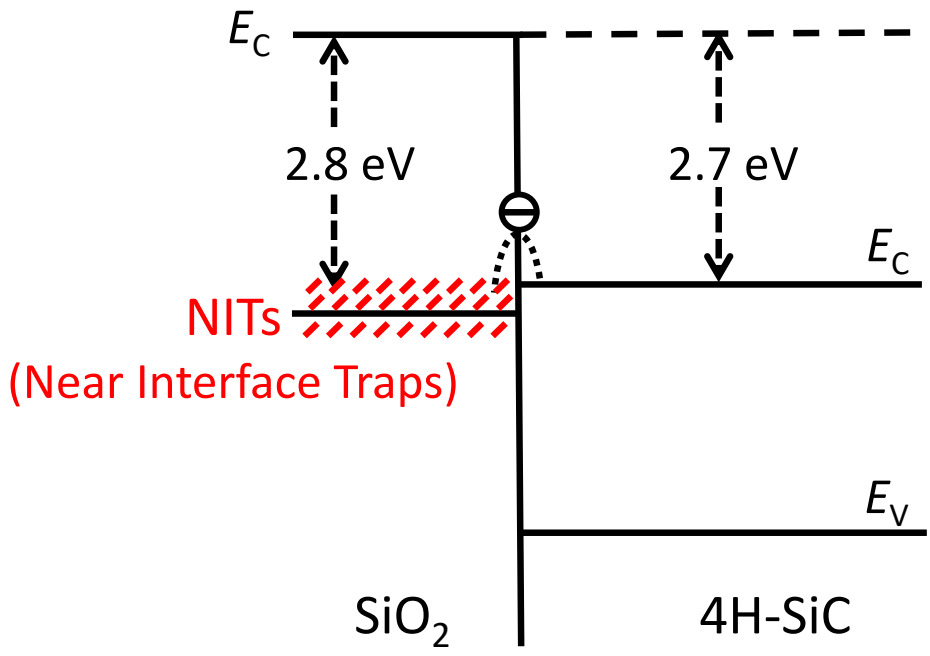

Fig. 2.1. Schematic band diagram of a typical n-type 4H-SiC MOS structure.

2.2 Description of modified distributed circuit model

For the n-type 4H-SiC MOS capacitors, NITs in SiO_2 can exchange charge with electrons in the E_c of 4H-SiC through tunneling in the strong accumulation condition. The tunneling process between NITs and the E_c of n-type 4H-SiC is illustrated schematically in Fig. 2.2.

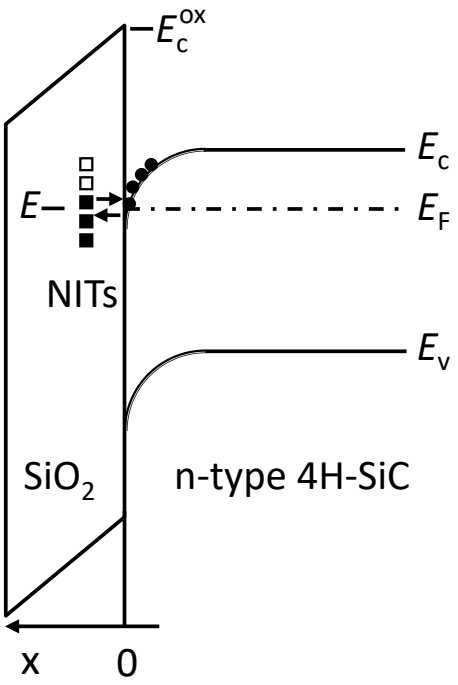

Fig. 2.2. Schematic band diagram of electron tunneling between NITs and the conduction band edge (E_c) of 4H-SiC in the strong accumulation condition.

Based on the tunneling mechanism, the time constant of NITs increases exponentially along the depth x from the interface of SiO_2/4H-SiC [3], expressed by Eq. (2.1):

$$\tau(x) = f_0 \tau_0 e^{2\kappa x}. \tag{2.1}$$

In this equation, f_0 is the Fermi-Dirac function, which means the probability that an electron can occupy a trap with the energy E, and τ_0 is the time constant *at the interface*. κ is the tunneling attenuation coefficient of the electron wave function of energy E, expressed as follows:

$$\kappa = \sqrt{2m^*(E_C^{ox} - E)} \big/ \hbar, \tag{2.2}$$

where m^* is the electron effective mass for direct tunneling [4], $E_C^{ox} - E$ energy barrier height for the tunneling, and $\hbar$ reduced Plank constant.

According to $\tau(x)$ expression of NITs based on the tunneling mechanism, for a certain gate voltage, the NITs located at different depths would have different responses to a given frequency. Therefore, the NITs would contribute to the admittance and thus lead to the frequency dispersion. In order to evaluate the admittance effect of NITs located at different depths, a modified distributed circuit model, which was first proposed by Yuan *et al*. [5, 6] for Al_2O_3/InGaAs interface, was applied to

SiO_2/4H-SiC case, which was demonstrated in Fig. 2.3. Prior to the explanation of the modifications, the original distributed circuit would be introduced.

In the distributed circuit model, the oxide capacitance (C_{ox}) is separated into an infinite number of

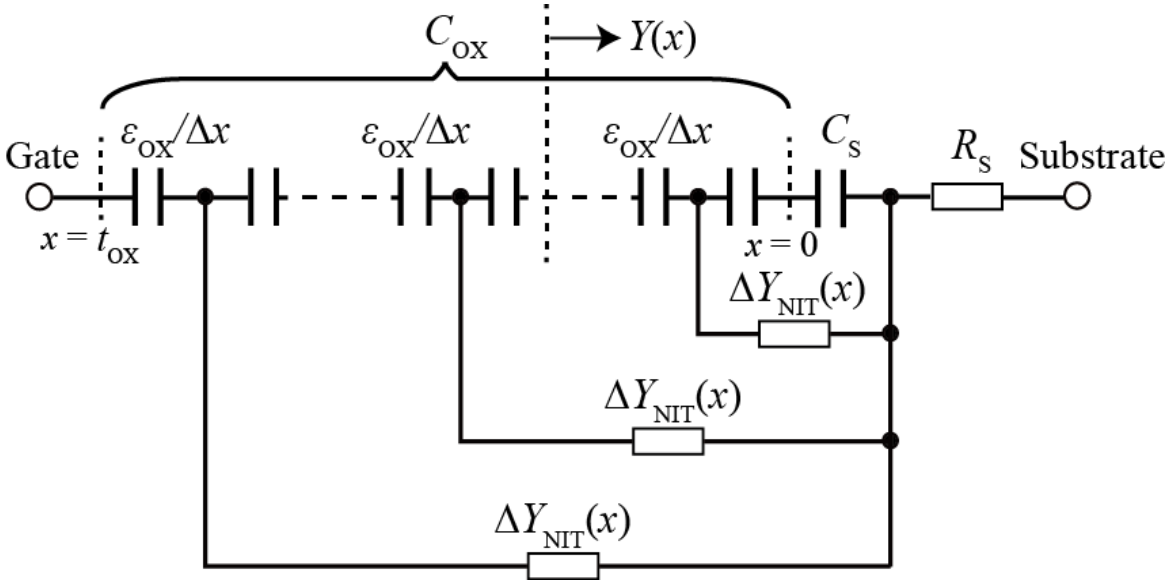

Fig. 2.3. Equivalent circuit of MOS capacitors with consideration of NITs in the strong accumulation condition.

segments with the incremental admittance, $\Delta Y_{NIT}(x)$, at different depths. ε_{ox} and C_s stand for the permittivity of oxide and capacitance of semiconductor, respectively. According to the recursive nature of the model, the differential equation of the NIT admittance $Y(x)$ can be expressed by Eq. (2.3) [5, 6]:

$$\frac{dY}{dx} = -\frac{Y^2}{j\omega\varepsilon_{ox}} + \frac{q^2 N_{NIT}(x)\ln(1+j\omega\tau_0 e^{2\kappa x})}{\tau_0 e^{2\kappa x}}. \tag{2.3}$$

Here, $N_{NIT}(x)$ is the density per volume per energy at a certain depth x, in units of $cm^{-3}eV^{-1}$. In the boundary condition, the admittance $Y(x = 0)$ is equal to $j\omega C_s$. The total Y can be calculated numerically by integrating (2.3) from $x = 0$ to t_{ox}, where t_{ox} is the SiO_2 thickness. Because the real and imaginary parts of the admittance represent the conductance (G) and capacitance (C), from the total admittance $Y(x = t_{ox})$, the corresponding modeled G (G_{mod}) and C (C_{mod}) were expressed by:

$$Y(x = t_{ox}) = G_{mod} + j\omega C_{mod}. \tag{2.4}$$

Based on the description of the distributed circuit model, the C and G of NITs versus frequency can be modeled [5, 6]. In order to apply the III-V model to 4H-SiC case, two modifications were conducted.

(1) The series resistance of R_s

In the modified distributed circuit model, the series combination of series resistance (R_s) was considered, illustrated in Fig. 2.3. In the strong accumulation condition and range with high frequency, the effect of R_s on the measured impedance has to be considered because the impedance of capacitor becomes lower. By considering the different sources of R_s, contact resistance and the semiconductor

resistance, including the substrate and epi-layer resistances dominate the R_s value [7]. Therefore, R_s should be independent of frequency. In order to extract R_s and to correct the measured capacitance and conductance, the three-element model was considered [8]. The measurement equivalent and the three-element circuit model by considering R_s are shown in Figs. 2.4 (a) and 2.4 (b). By considering the equivalence of these two circuits, the measured capacitance (C_m) and conductance (G_m) can be expressed as follows:

$$C_m = \frac{C_C}{(1+R_S G_C)^2 + \omega^2 C_C^2 R_S^2}, \tag{2.5a}$$

$$G_m = \frac{G_C + R_S G_C^2 + \omega^2 C_C^2 R_S}{(1+R_S G_C)^2 + \omega^2 C_C^2 R_S}, \tag{2.5b}$$

where ω, C_c, and G_c are the angular frequency, corrected capacitance and correct conductance, respectively. For the *C–V* measurements, in the general frequency range, the approximations of $R_s G_c \ll 1$ and $\omega C_c R_s \ll 1$ are valid [8], and thus the expressions of C_m and G_m can be expressed by:

$$C_m = C_C \tag{2.6a}$$

$$G_m = G_C + \omega^2 C_m^2 R_S . \tag{2.6b}$$

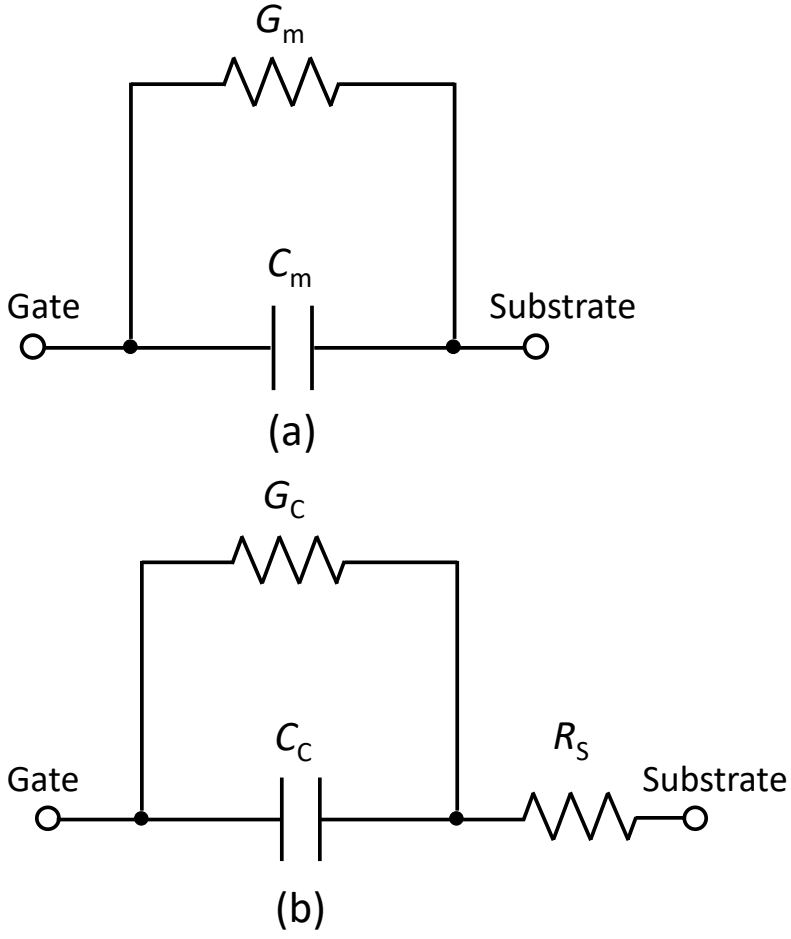

Fig. 2.4. (a) Measured equivalent circuit and (b) three-element circuit model of a MOS capacitor.

By transforming the equation of (2.6b), $G_m/(\omega C_m^2)$ versus ω can be plotted at high frequency range and R_s can be extracted as the slope. After R_s extraction, the corrected capacitance and conductance can be calculated. Because the extraction of C_c and G_c is difficult by using Eqs. (2.5a) and (2.5b), the impedance data are used for the calculation, as expressed in the following:

$$C_c = -\frac{X_m}{\omega[(R_m - R_s)^2 + X_m^2]}, \tag{2.7a}$$

$$G_c = \frac{R_m - R_s}{(R_m - R_s)^2 + X_m^2}, \tag{2.7b}$$

where the measured impedance's real part is represented by R_m, and the imaginary part is related with X_m. It should be noted that C_c and G_c are employed to compare with the modeled results of C_{mod} and G_{mod}.

(2) Assumption of exponentially decaying distribution for NITs

The second modification for the distributed circuit model is that assumed NIT distributions are different. In the Al_2O_3/ InGaAs interface, a uniform distribution was assumed. It should be pointed out that in the III-V case, Al_2O_3 was formed by utilizing the atomic layer deposition (ALD) technique. Also, the thickness of Al_2O_3 was only around 5 nm. However, in the 4H-SiC MOS case, SiO_2 was formed by thermal oxidation and the SiO_2 thickness was about 50 nm. Therefore, the different oxidation processes would lead to different formation mechanisms of NITs or border traps. Therefore, in 4H-SiC case, an exponentially decaying spatial distribution is assumed for NITs, which is given by

$$N_{NIT}(x) = N_{NIT0}\exp(-\alpha x). \tag{2.8}$$

Here, N_{NIT0} is the density of NITs at the SiO_2/4H-SiC interface ($x = 0$), x the distance from the interface, and α a decay constant in units of nm^{-1}, which can be regarded as fitting parameters [9]. The schematic diagram of the exponentially decaying distribution of NITs is shown in Fig. 2.5.

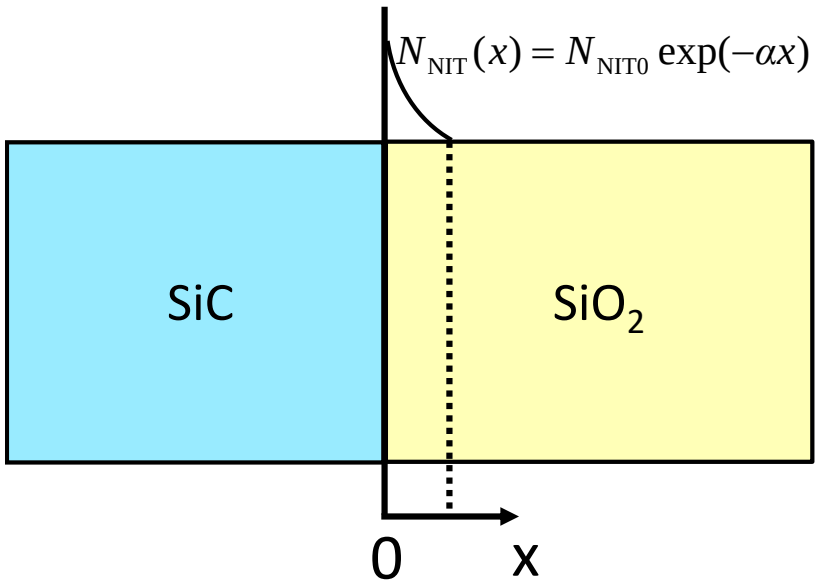

Fig. 2.5. Schematic diagram of the exponentially decaying distribution of NITs.

The parameter specification should be explained before the fitting process. Here, the important parameters are categorized as three types, explained in the following:

(1) Free parameters

In the modified distributed model, the N_{NIT0} ($cm^{-3}eV^{-1}$) and α (nm^{-1}) can be considered as the free parameters.

(2) Variable parameters

First, the time constant at the interface, τ_0, is regarded as a variable parameter, expressed by the equation as follows [10]:

$$\tau_0 = \frac{1}{\sigma_{n0} v_{th} N_D \exp(\frac{q}{kT}\psi_s)}, \tag{2.9}$$

where v_{th} is the electron thermal velocity at temperature T, σ_{n0} the capture cross section at the interface, N_D the doping concentration of nitrogen, $q\psi_s$ surface potential, or the conduction band bending of 4H-SiC, k Boltzman constant, and T the measurement temperature. $q\psi_s/(kT)$ is the normalized surface potential. For a given MOS capacitor, v_{th} and N_D can be determined. Therefore, τ_0 is determined by $q\psi_s$ and σ_{n0}. However, under the strong accumulation condition, the Fermi level (E_F) is very close to the E_c of 4H-SiC and it is difficult to determine $q\psi_s$ because of lacking reliable methods [11, 12]. By far, the Hall-effect measurements may be the best approach to determine $q\psi_s$ because the surface carrier concentration extracted by the Hall-effect measurements has one-to-one correspondence with $q\psi_s$ [13]. However, the Hall-effect measurement itself is not perfect due to the uncertainty of the Hall factor [11, 13]. Therefore, $q\psi_s$ can be considered as a fitting parameter. Because σ_{n0} is related with the trap energy and generally, it would decrease toward the band edge [14]. The uncertainty of surface potential and thus the energy level would lead to the difficulty to determine σ_{n0}. Besides, the experimentally-obtained σ_n includes the effect of NITs and is always smaller than the σ_{n0}. The obtained capture cross sections by different methods vary significantly [15–18]. Thus, it is difficult to accurately determine σ_{n0}. Therefore, $q\psi_s$ and σ_{n0} can be considered as fitting parameters.

Second, C_s, the semiconductor capacitance, is considered the other variable parameter. Based on the Poisson's equation [19], C_s can be expressed as

$$C_s(\psi_s) = \frac{qN_D \left|\exp(\frac{e\psi_s}{kT})\right|}{\sqrt{\frac{2kTN_D}{\varepsilon_{SiC}}\left\{\exp(\frac{e\psi_s}{kT}) - \frac{e\psi_s}{kT} - 1\right\}}}. \tag{2.10}$$

ε_{sic} is the permittivity of 4H-SiC. It can be found that C_s is a function of ψ_s.

(3) Constant parameters

First, κ is regarded as a constant parameter. From the expression (2.2), κ is mainly determined by the energy difference of $E_C^{ox} - E$. The trap energy very close to the E_F should be most responsible for the small AC signal for a given gate bias. In the strong accumulation, the E_F is very close to the E_c of 4H-SiC at the surface. Despite uncertainty of $q\psi_s$, the large conduction band offset between E_C^{ox} and E_c of 4H-SiC, with the value of around 2.7 eV [20], makes the uncertainty hardly affect the value of κ

and the band offset mainly determines κ. Therefore, κ can be considered as a constant. By using m^*=0.3 m_0 [4], the corresponding κ value is considered to be 4.6 nm^{-1}.

Second, the oxide thickness is a constant parameter, estimated by the accumulation capacitance at high frequency because the NITs have smallest capacitance contribution at high frequency and thus smallest effect on the accumulation capacitance [5, 6].

Thirdly, ε_{ox}, the permittivity of SiO_2, is regarded as a constant, with the value of $3.9\varepsilon_0$, where ε_0 is the vacuum permittivity and its defined value is 8.85×10^{-12} F/m. The permittivity of SiO_2 has dependence on the temperature and frequency, especially in the very high frequency range above 1 GHz [21, 22]; thus, in this work, the analysis frequency was up to 1 MHz and only room temperature was considered.

Based on the description of the model and related parameters, the specific fitting process between the experimental data and modeled data is shown in Fig. 2.6. The fitting processes were run with MATLAB code. Mean squared error (*MSE*) functions were applied to estimate the errors between the experimental (C_{exp}, G_{exp}) and modeled (C_{mod}, G_{mod}) results [23]. The *MSE* functions of *C* (*MSE C*) and *G* (*MSE G*) were expressed by Eqs. (2.11a) and (2.11b), and *n* was the number of data points. It should be noted that the normalized errors of *C* and *G* need to be extracted, in order to exclude the effect of absolute value difference between *C* and *G* on error estimation. The extraction of normalized errors in *C* and *G* are shown in Eqs. (2.12a) and (2.12b). The mean square error's square root was calculated and then divided by the value difference of the largest and smallest C_{exp} (G_{exp}). Then, the Pareto optimality concept [23] was employed to obtain the best trade-off of errors between *C* and *G* and thus the optimized fitting solution. Because the fitting parameters are uncertain, fitting solutions approximate to the optimized case were considered.

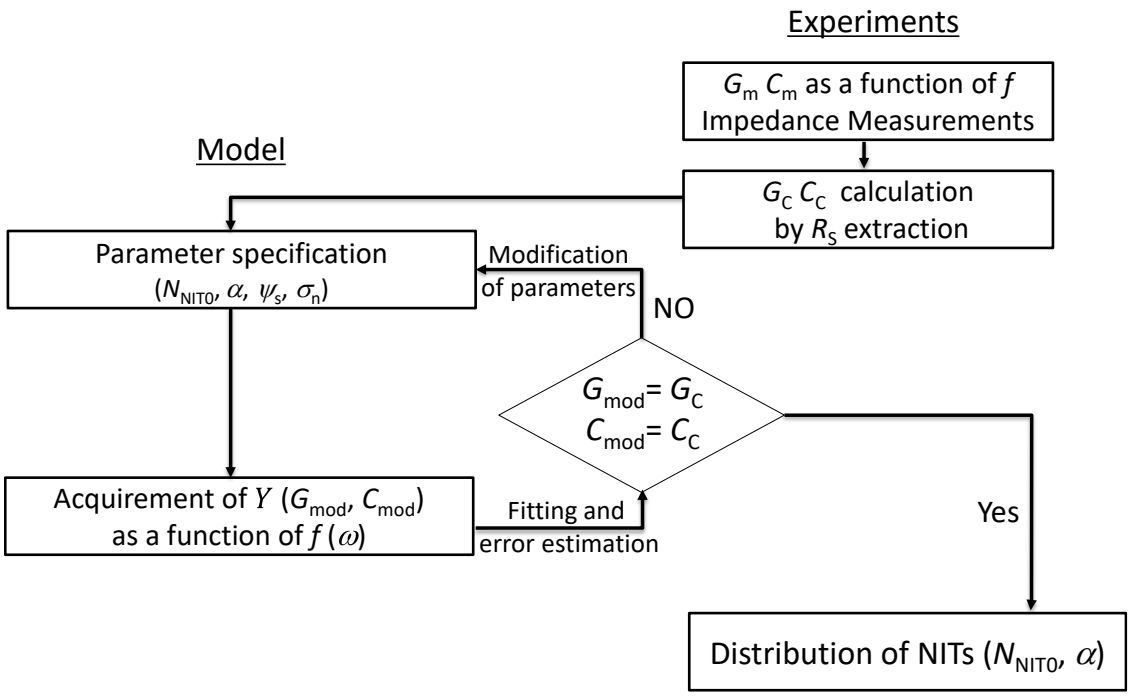

Fig. 2.6. The flow chart of the fitting process between the experimental and modeled data.

$$MSEC = \frac{1}{n}\sum_{i=1}^{n}(C_{\text{exp}} - C_{\text{mod}})^2 \tag{2.11a}$$

$$MSEG = \frac{1}{n}\sum_{i=1}^{n}(G_{\text{exp}} - G_{\text{mod}})^2 \tag{2.11b}$$

$$NorErr\_C = \frac{\sqrt{MSEC}}{C_{\text{exp,max}} - C_{\text{exp,min}}} \tag{2.12a}$$

$$NorErr\_G = \frac{\sqrt{MSEG}}{G_{\text{exp,max}} - G_{\text{exp,min}}} \tag{2.12b}$$

From the optimized fitting results, the density distribution of NITs can be obtained with reliable values of N_{NIT0} and α. Specific measurements were introduced in the next section.

2.3 Experiments

An n-type 4H-SiC epilayer was employed to fabricate three MOS capacitors. Its nitrogen concentration was about 1×10^{16} cm^{-3} and thickness was 10 μm. The n-type epilayer was grown on an n-type 4° off-axis (0001) Si-face substrate, which possessed low bulk resistivity, with the value of around 0.02 Ωcm and thickness of around 350 μm. First, standard RCA (Radio Corporation of America) cleaning was performed. Then, dry oxidation process was conducted at 1200 °C with the oxidation time of 170 min, and the oxide thickness was around 50 nm. This sample was denoted as Dry. After that, post oxidation annealing processes were performed for the other two dry oxidized samples with nitric oxide (NO) at 1250 °C for 10 and 60 min. These two nitrided samples were denoted as NO-10 and NO-60. After NO annealing, the oxide thickness increased slightly. At last, Al evaporation was conducted to realize gate and backside ohmic contacts. The circular gate electrodes were 500 μm in diameter.

The multi-frequency impedance measurements were conducted for the three n-type 4H-SiC MOS capacitors in the strong accumulation condition (V_{G} = 20 V) at room temperature by using a Keysight E4990A impedance analyzer and a 42941A impedance probe kit with proper calibration. The special measurement setup, schematically shown in Fig. 2.7, was used to minimize the series components during the MOS capacitor measurements. Because large noises exist in the frequency range below 10 kHz, and the data above 10 MHz would be affected by the residual impedance, the frequency range used for the fitting analysis was 10 kHz to 1 MHz. For the estimation of series resistance (R_{s}), a frequency range of 1 to 10 MHz was employed, because precise extraction of R_{s} needs a relatively higher frequency [8].

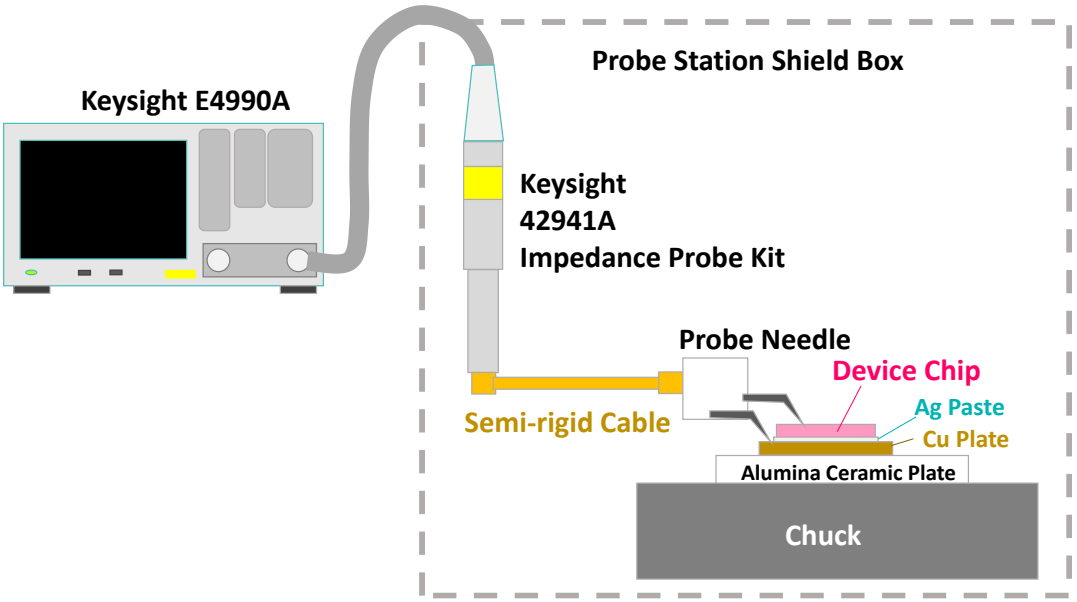

Fig. 2.7. Special measurement setup to measure the MOS capacitor in order to minimize series components.

2.4 Density distribution estimation of NITs

2.4.1 R_s extraction

Prior to the fitting, the values of R_s were extracted as the slopes for the three 4H-SiC MOS capacitors. Figure 2.8 shows the plotted $G_m/(\omega C_m^2)$ versus ω curves for the three samples. The R_s values of Dry, NO-10, and NO-60 were 3.5, 2.4, and 2.2 Ω, respectively. According to the extracted R_s

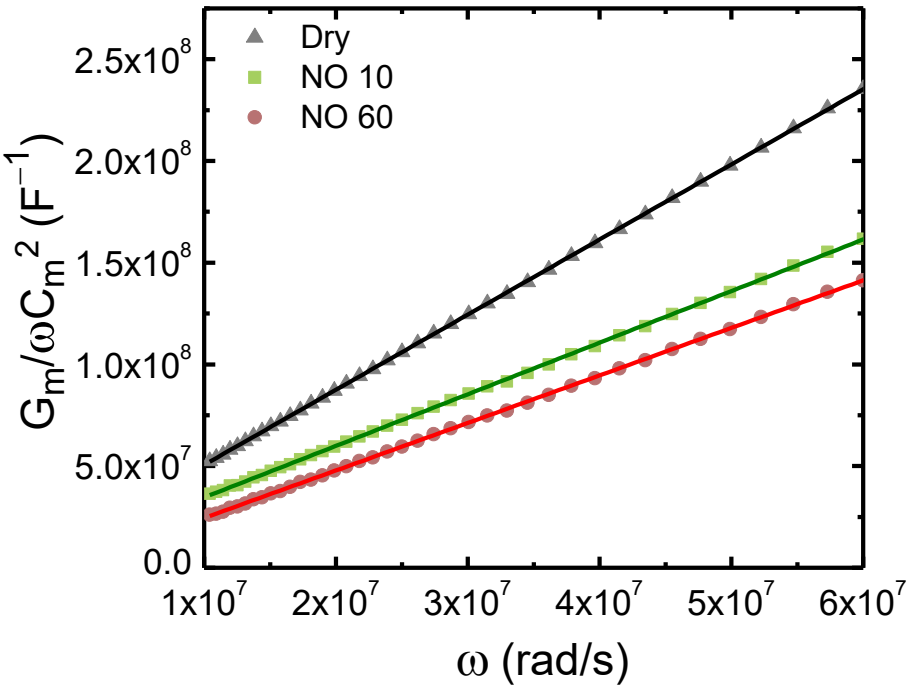

Fig. 2.8. $G_m/(\omega C_m^2)$ as a function of angular frequency ω for Dry (denoted as triangle), NO-10 (denoted as square), and NO-60 (denoted as circle). R_s can be extracted as the slopes.

values, the C_c and G_c can be obtained. The measured and corrected C–f and G–f characteristics at V_G = 20 V before and after R_s correction were shown in Figs. 2.9 (a) and 2.9 (b).

It can be seen that R_s almost has no effect on the accumulation capacitance, which is also consistent with the approximation of Eq. (2.6a), while it has obvious effect on the accumulation conductance. Therefore, it is significant to extract R_s and to rule out its effect on the measured data, especially the conductance.

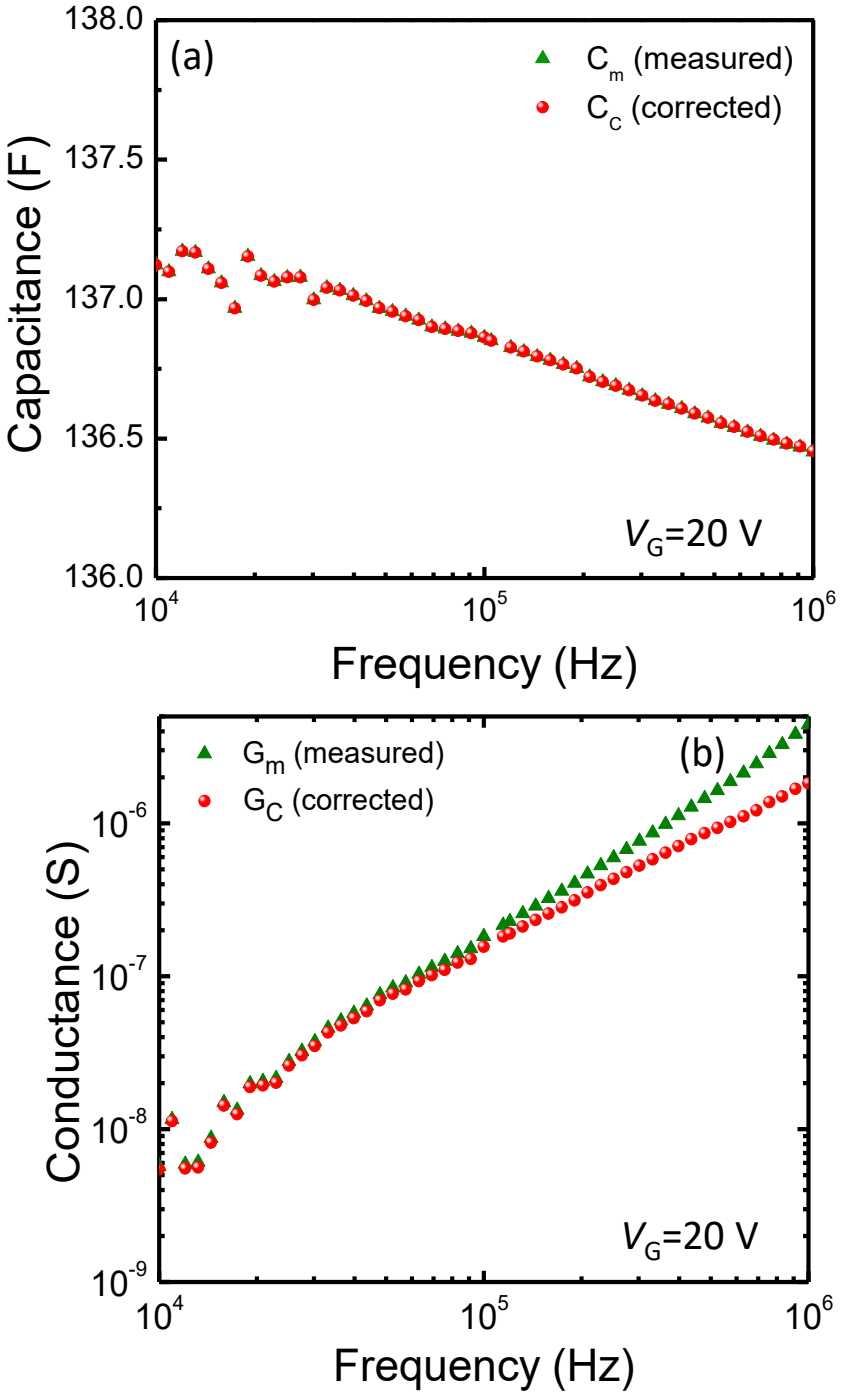

Fig. 2.9. Frequency dependence of (a) capacitance and (b) conductance before and after R_s extraction. Here, the Dry sample was taken as an example.

It can be seen that there was a decrease in capacitance and an increase in conductance versus frequency in the accumulation condition. The small changing tendency versus frequency is usually overlooked in the SiC field, but in fact the changes in C_c and G_c existed. Provided that the simplest equivalent circuit is applied in the strong accumulation condition, where C_{ox} and R_s are connected in series [7], the frequency dependence of capacitance and conductance would not exist. Note that all the experimental values of C and G were corrected by R_s precisely, indicating the changing tendency of C and G are not attributed to R_s. Moreover, this phenomenon could not be explained by interface states because they possess very short time constants in the strong accumulation condition, and thus could not lead to frequency dispersion in the general frequency range below 1 MHz [10]. For the explanation of the frequency dispersion, the electron tunneling between the NITs and 4H-SiC surface should be taken into account, which is similar with the case of Al_2O_3/InGaAs interface [5, 6]. It should be noted that the smaller change in C_c and G_c, in comparison with the Al_2O_3/InGaAs structure [5, 6], is owing to the much thicker thickness of SiO_2 in the 4H-SiC MOS structure.

2.4.2 Analysis of the fitting results

In this section, the modified distributed circuit model was employed with an exponentially decaying distribution assumption. By choosing proper values for the different parameters, as listed in Table 2.1, the optimal fitting solutions of *C–f* and *G–f* properties at V_G = 20 V for Dry, NO-10, and NO-60 samples were obtained, shown in Figs. 2.10 (a) and 2.10 (b). It can be seen that the modeled and experimental data fitted well with the assumption of exponentially decaying distribution of NITs.

Table 2.1 Parameter specification used in the model for Dry, NO-10, and NO-60 samples.

Parameters	Dry	NO-10	NO-60
N_{NIT0} ($cm^{-3}eV^{-1}$)	1.1×10^{21}	5.6×10^{20}	2.7×10^{20}
α (nm^{-1})	1.8	1.8	2.6
τ_0 (s)	5.6×10^{-10}	6.7×10^{-11}	8.6×10^{-12}
C_s ($\mu F/cm^2$)	3.6	5.3	13.4
t_{ox} (nm)	49.7	51.0	51.4

Here, other possibilities of NIT distributions were also considered, including a uniform, boxed-shaped and linearly-decaying distributions, which were schematically shown in Figs. 2.11 (a) – 2.11 (c). With the three distributions, the modified distributed circuit model, shown in Fig. 2.3, was applied to examine the fitting results of *C–f* and *G–f* properties. Here, the tunneling depth of NITs was assumed to be β nm in the box-shaped distribution. Similarly, the slope in the linearly-decaying distribution shown in Fig. 2.11 (c) was assumed to be c $cm^{-3}eV^{-1}nm^{-1}$, which means that the NITs would decay γ $cm^{-3}eV^{-1}$ per nanometer. The parameters of β and γ are the fitting parameters, similar with the decay constant α in the exponentially decaying distribution. By choosing proper values for different parameters in each kind of distribution, shown in Table 2.2, the optimized fitting results of

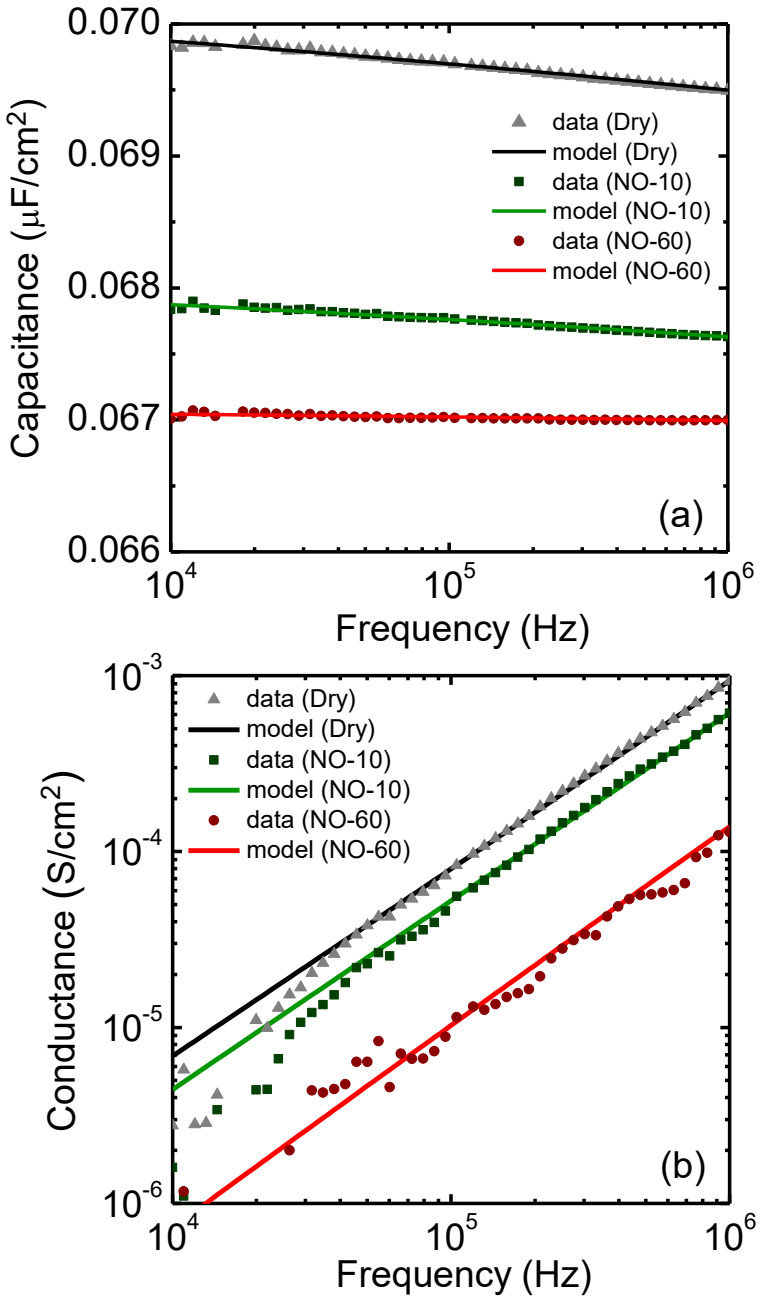

Fig. 2.10. Experimental and fitting results for (a) *C*–*f* and (b) *G*–*f* characteristics at V_G = 20 V.

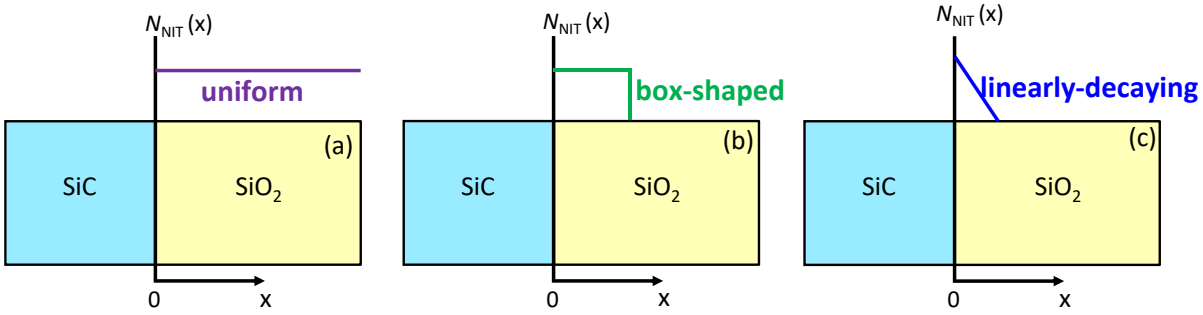

Fig. 2.11. Different kinds of NIT density distributions: (a) uniform distribution, (b) box-shaped distribution, and (c) linearly-decaying distribution.

Table 2.2 Parameter specification used in the model with different kinds of distributions.

Parameters	uniform	box-shaped	Linearly-decaying
N_{NIT0} ($cm^{-3}eV^{-1}$)	1.0×10^{20}	2.5×10^{21}	1.9×10^{21}
β (nm)	–	0.6	–
γ ($cm^{-3}eV^{-1}nm^{-1}$)	–	–	1.9×10^{21}
τ_0 (s)	1.1×10^{-11}	5.6×10^{-8}	1.4×10^{-8}
C_s ($\mu F/cm^2$)	9.7	6.5	6.5
t_{ox} (nm)	49.7	49.7	49.7

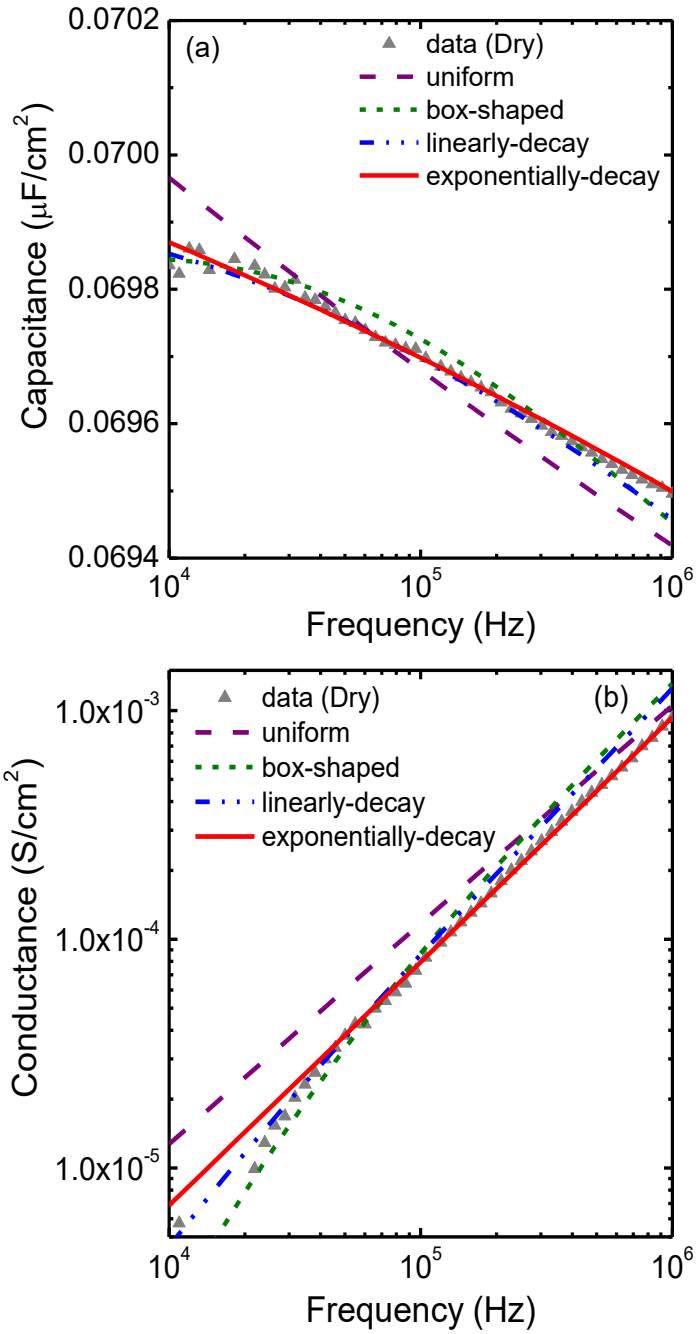

Fig. 2.12. The optimized fitting results of (a) capacitance and (b) conductance with different distribution assumptions.

C–f and *G–f* were obtained. The optimized fitting results of *C–f* and *G–f* by using exponentially decaying distribution were compared with the results of the three kinds of distributions, which were illustrated in Figs. 2.12 (a) and 2.12 (b). Here, the Dry sample was taken as an example. It can be seen that the exponential distribution achieved the optimized fitting solution with the least error in capacitance and conductance. The normalized error in capacitance for the uniform distribution was 13.6%, box-shaped distribution 5.4%, linearly-decaying distribution 4.3%, and exponentially decaying distribution 3.2%; and the corresponding conductance errors were 6.8%, 12.3%, 5.7%, and 0.7%, respectively. The assumption of exponential distribution for NITs can successfully explain the *C–f* and *G–f* properties in the strong accumulation condition.

Based on the optimized fitting results, the distributions of NIT density along the tunneling depth can be extracted for the three capacitors, which was shown in Fig. 2.13. It should be noted that the fitting errors for N_{NIT0} and α were ±2%.

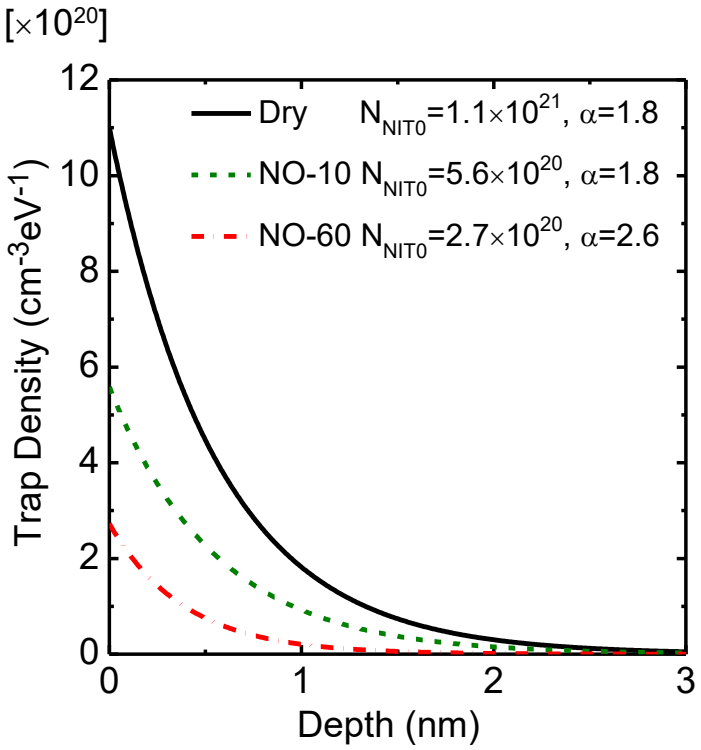

Fig. 2.13. Density distribution of NITs against the tunneling depth from the best fitting results for Dry, NO-10 and NO-60 samples.

It can be observed that the NIT density was significantly reduced with increased nitridation time. Note that for the three samples of Dry, NO-10, and NO-60, the obtained trap energy levels ($E_c - E$) were around 0.03, 0.01, and −0.04 eV, respectively. By estimating the fitting errors in $q\psi_s$, the corresponding trap energy levels for each sample were within 0.02 eV. Note that the respective flatband voltages extracted by the 1 MHz *C–V* data for Dry, NO-10, and NO-60 were 1.2, 0.9, and 0.2 V, respectively. Therefore, the $q\psi_s$ or oxide fields at V_G = 20 V are slightly different for all the samples, but trap density comparison is still valid. When nitridation time increased, the density of NITs reduced and more free electrons accumulated at the surface of semicondutor, which led to larger

conduction band bending at V_G = 20 V. This also explains why C_s increased, and time constant at the interface decreased with increased nitrigon passivation time, as demonstrated in Table 2.1.

2.5 Discussion

With regards to the electrical properties in the strong accumulation condition, the assumption of exponential NIT distribution can successfully explain the frequency dispersion of capacitance and conductance. However, the NIT origin is still unclear. Nevertheless, the origin of exponential distribution could be dicussed based on past studies. Watanabe *et al*. conducted the synchrotron x-ray photoelectron spectroscopy measurements, by which weak intensity of the suboxide components was detected and C-related defect peaks in the oxide were not observed. This indicates that the transition layer between SiO_2/4H-SiC interface is thin enough, within only a few monolayers [24]. Besides, based on the medium-energy ion scattering measurements, the observed C atoms were less than 1.8×10^{14} cm^{-2} from the oxide surface to a few monolayers beneath the SiO_2/4H-SiC interface, and a laterally near-perfect SiO_2 stoichiometry was revealed according to the Si and C surface peaks [25]. Therefore, it can be deduced that the NITs are present within a few monolayers (< 1 nm) of the interface. The assumption of exponentially-decaying distribution is a good candidate for the true NIT distribution, which confirms that the NITs are mainly located within a few monolayers of the interface. By nitridation passivation, NIT density was reduced. This result is consistent with the transient-capacitance (*C–t*) results by Fujino *et al*. The *C–t* analysis revealed that most of the NITs located within a few monolayers of the interface [26]. Recent results of frequency dependence in charge-pumping measurements in our group also revealed that the NIT distribution can be fitted using exponential functions [27]. In addition, the significant decrease in NIT density with an increase in nitridation annealing time is in accrodance with the results reported by Sometani *et al*., in which the fast V_{th} shift was suppressed by nitridation, compared with dry samples [28].

2.6 Summary

In summary, the NITs in the conduction band side of 4H-SiC were analyzed. A distributed circuit model was applied, which considered the electron tunneling of NITs in the accumulation condition. With an assumption of exponentially decaying distribution of NITs, the capacitance and conductance as functions of freuquency were explianed for the n-type 4H-SiC MOS capacitors in the strong accumulation condition. Three kinds of n-type MOS capacitors with different oxidation processes (dry-oxidized and nitrided samples) were analyzed. It was found that nitridation passivation dramatically reduced the NIT density. The NIT analysis in light of the modified circuit model would be beneficial to studying the NIT effects on the characteristics of 4H-SiC MOSFETs, such as thereshold voltage shift and low field-effect mobility.

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Chapter 3

Impact of oxide thickness on NITs for n-type 4H-SiC MOS structure

3.1 Introduction

In Chapter 2, a distributed circuit model was applied to characterize NITs near the conduction band edge (E_c) of 4H-SiC. The *C–f* and *G–f* properties in the strong accumulation condition were successfully explained with an assumption of exponentially decaying distribution for NITs. However, due to the thick oxides, with the thickness of around 50 nm, the frequency dispersion of accumulation capacitance is not that obvious. Thus, the exponentially decaying distribution assumed in Chapter 2 has not been fully validated.

With the purpose of assessing the validity of the assumption, an effective way is to investigate the MOS capacitors with various oxide thicknesses. Figures 3.1 (a) and 3.1 (b) schematically show the 4H-SiC MOS structures with thin and thick oxides. From these two figures, it can be seen clearly that the capacitance ratio of NITs to the total capacitance is different. In the thin oxides, the "NIT ratio" to the total oxide thickness is large and the capacitance contribution would be more obvious. However, in the thick oxides, the "NIT ratio" to the total oxide thickness is small and the total capacitance would be dominated by the oxide capacitance in the strong accumulation condition. Therefore, the

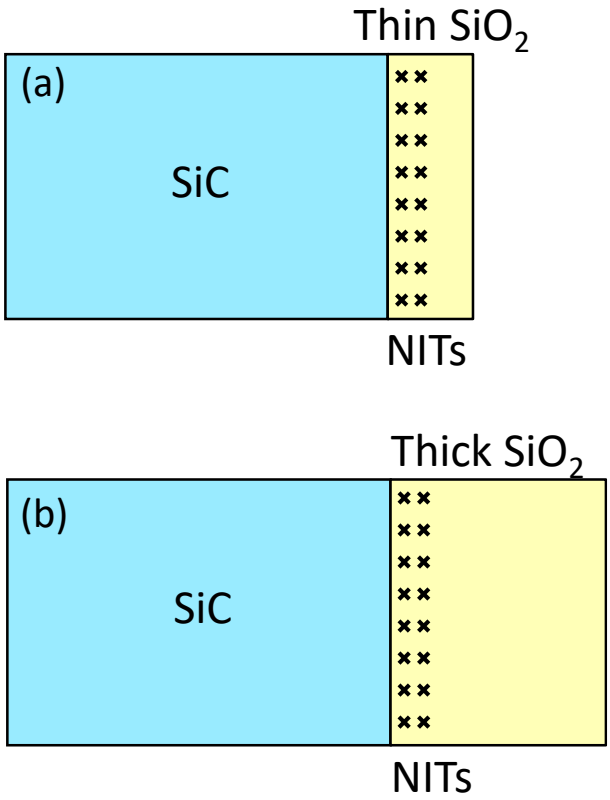

Fig. 3.1. Schematic diagrams of NIT ratios in (a) thin SiO_2 and (b) thick SiO_2.

admittance effects of NITs on the *C–f* and *G–f* properties for MOS capacitors with various oxides would be different. Therefore, in this Chapter, n-type 4H-SiC MOS capacitors which possessed various oxide thicknesses from a few nanometers to several tens of nanometers were fabricated and employed to characterize the possible distribution of NITs.

In this investigation, the thickness dependence of trap density should be also considered. Watanabe *et al*. reported the dependence of the interface trap density (D_{it}) on the SiO_2 thickness, and there was an increase in D_{it} when the oxide thickness increases in the depletion region [1]. Therefore, the effect of SiO_2 thickness on the density distribution of NITs was evaluated in the strong accumulation conditions. Furthermore, the possible physical reasons for the thickness-dependent characteristics were discussed.

3.2 Experiments

An n-type 4H-SiC epilayer was used to fabricate five MOS capacitors with varying SiO_2 thicknesses. The net donor concentration of the epilayer was about 1×10^{16} cm^{-3} and thickness was about 10 μm. The epilayer was grown on an n-type 4° off-axis (0001) Si-face substrate, which possessed low bulk resistivity, with the value of around 0.02 Ωcm, and thickness of 350 μm. First, standard RCA (Radio Corporation of America) cleaning was performed. Then thermal dry oxidation was conducted at 1200 °C for different oxidation times. The thicknesses of SiO_2 varied from 8.7 nm to 66.4 nm. Al deposition was conducted to form gate and backside ohmic contacts. The circular gate electrodes were 500 μm in diameter. For the five 4H-SiC MOS capacitors, multi-frequency capacitance–voltage (*C–V*) and conductance–voltage (*G–V*) curves from 1 kHz to 200 kHz were measured with a LCR meter of Keysight E4980A. Specifically, for per decade of frequency, ten frequency points were measured, which ensured the same datum space in the logarithmic coordinates on the adjacent frequency and thus realized balance of error estimation in each frequency range. Even though the frequency range was relatively limited, the experimental values of *C* and *G* were reliable. This is because the effect of noise on the experimental data in lower frequency range was ruled out, and series component effect on the experimental data in higher frequency range was also excluded, which was essential for the process of fitting estimation. The ultra-low frequency (1 Hz) *C–V* characteristics were measured for each MOS capacitor by using a Keysight B2912A Precision Source/Measure Unit. The interface state density (D_{it}) was evaluated for the five MOS capacitors by the conventional Hi-Lo method in the depletion region [2]. After that, the modified distributed circuit model, which has been described in Chapter 2, was employed to evaluate the thickness dependence of NIT density distributions in the strong accumulation conditions.

3.3 Thickness dependence of D_{it} in the depletion region

The D_{it} in the energy range of 0.2 to 0.6 eV below the E_c of 4H-SiC for the five MOS structures was illustrated in Fig. 3.2. When the energy level of traps is located closer to the E_c of 4H-SiC, the value of D_{it} increases. It can be seen that the order of D_{it} value, at the energy of $E_c - E = 0.2$ eV, exceeds

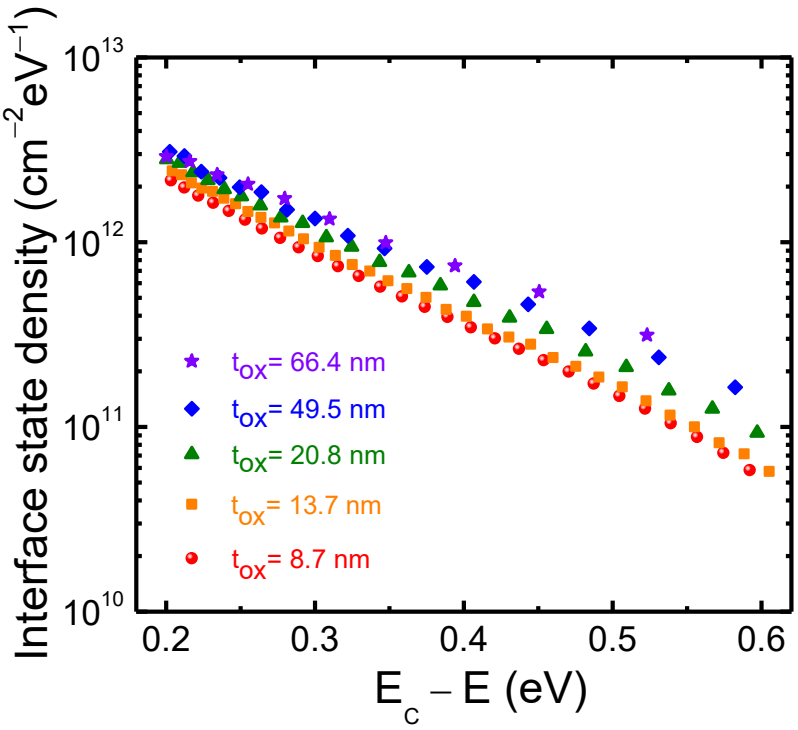

Fig. 3.2. Interface state density versus energy position below the conduction band edge of 4H-SiC in the depletion region for the five MOS capacitors. The trap density is estimated by the conventional Hi-Lo method [2].

10^{12} cm^{-2}eV^{-1}, which implies poor interface properties in the conduction band side of 4H-SiC. Note that at the identical energy position, there is a slight increase in D_{it} with the increase in the oxide thickness. This is in accordance with the results of Watanabe *et al*. [1].

3.4 Thickness dependence of NITs in the strong accumulation conditions

To investigate the thickness dependence of NITs in the strong accumulation conditions near the E_c of 4H-SiC, the distributed circuit model, which has been introduced in Chapter 2, was applied to estimate the admittance effect of NITs (Y_{NIT}) on the *C–f* and *G–f* properties for the fabricated MOS capacitors with various oxides. The fitting process and error estimation method have been introduced in Chapter 2 and this Chapter would omit the specific description. The optimized fitting results according to the model calculation would be shown directly in the next section.

3.4.1 *C–f* and *G–f* fitting with exponentially decaying distribution

For each 4H-SiC MOS capacitor, the optimal fitting solutions of *C–f* and *G–f* curves in the strong accumulation conditions were demonstrated in Figs. 3.3 (a) and 3.3 (b), respectively. Different oxide thicknesses require different gate voltages to reach almost the same electric field. Here, gate voltages with values of 4, 6, 9, 22, and 29 V were applied for the five MOS capacitors from thin to thick, to ensure almost the same surface potential. The surface potential was estimated by the fitting process and the corresponding energy levels are around 0.02 to 0.07 eV below the E_c of 4H-SiC for each

sample. It should be noted that the capacitance was normalized by the capacitance at 1 kHz, with the purpose of comparing the *C–f* characteristics easily for the MOS capacitors with different t_{ox}. From the *C–f* characteristics in Fig. 3.3 (a), it can be observed that the slope of the *C–f* curve becomes steeper when decreasing the oxide thickness. This reflects different NIT effects on the electrical properties. Due to the large "NIT ratio" in thin oxides, the admittance contribution of NITs is more

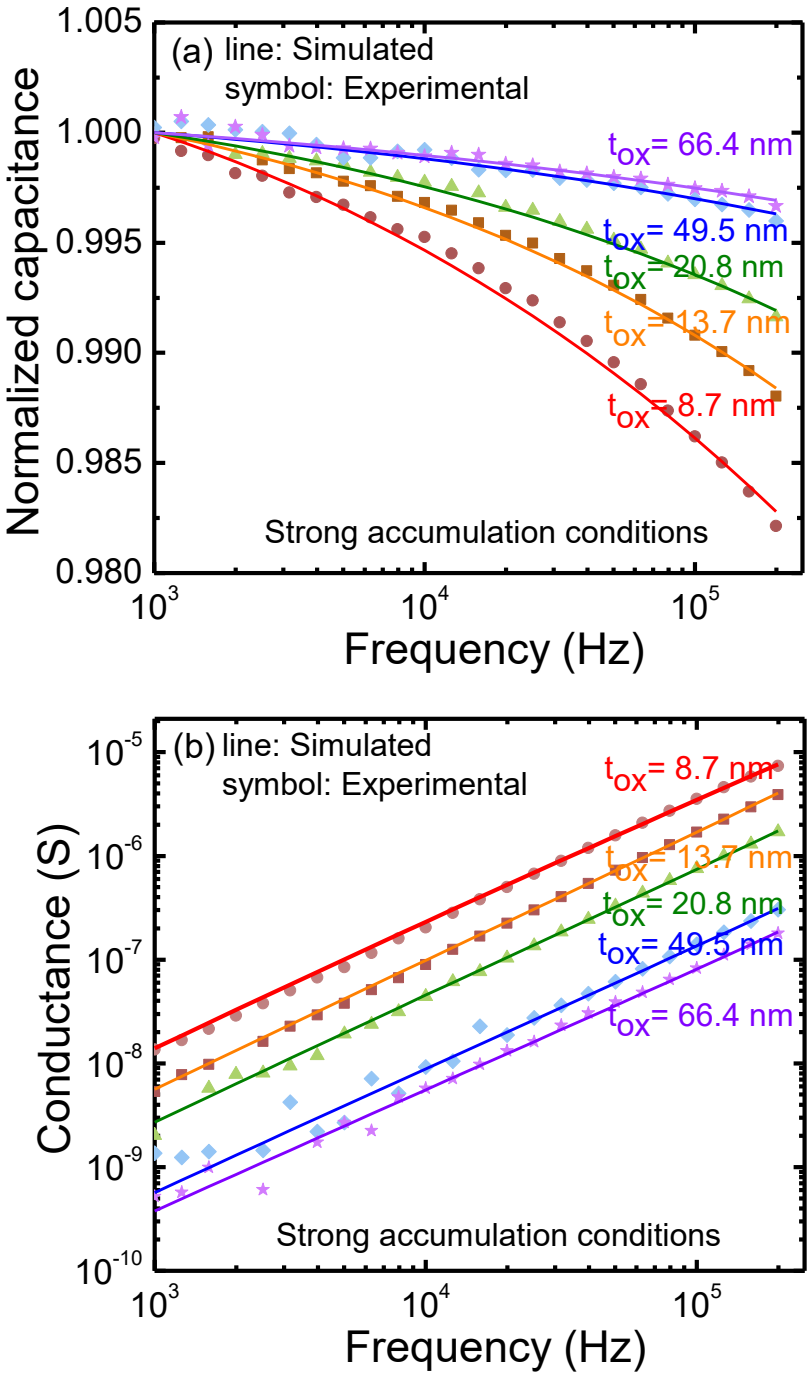

Fig. 3.3. Optimized fitting solutions of (a) *C–f* and (b) *G–f* properties between the experimental and modeled data for the five MOS capacitors with varying SiO_2 thicknesses. The distributed model was applied and an exponentially decaying distribution of NITs was assumed under strong accumulation conditions.

obvious. From these two figures, it is clear that the measured and modeled *C–f* and *G–f* characteristics fitted well, which can be well explained by the exponentially decaying distribution of NITs. Therefore, the exponentially decaying distribution can be considered as a good candidate for approximation of true NIT distribution.

3.4.2 *C–f* and *G–f* fitting with other possible distributions

In addition to the exponentially decaying distribution, other possibilities were also examined. Four possibilities were estimated, as shown in Figs. 3.4 (a)–3.4 (d). Besides the uniform, box-shaped and linearly decaying distributions, the complementary error function distribution of NITs was also examined. Based on the Si and C emission model during the thermal oxidation of SiC, the Si and C interstitials are usually distributed what resembles a complementary error function or exponential function [3]. Therefore, it is important to examine the feasibility of complementary error function distribution. Here, the sample with the thinnest oxide was taken as an example. The optimal fitting solutions by different kinds of distribution assumptions were illustrated in Figs. 3.5 (a) and 3.5 (b). It can be observed that the optimized fitting results by the four distribution assumptions were not good, while the exponentially decaying distribution assumption possessed the best fitting. Therefore, it can be deduced that the most plausible and simplified approximation of the true distribution for NITs would be the exponentially decaying distribution.

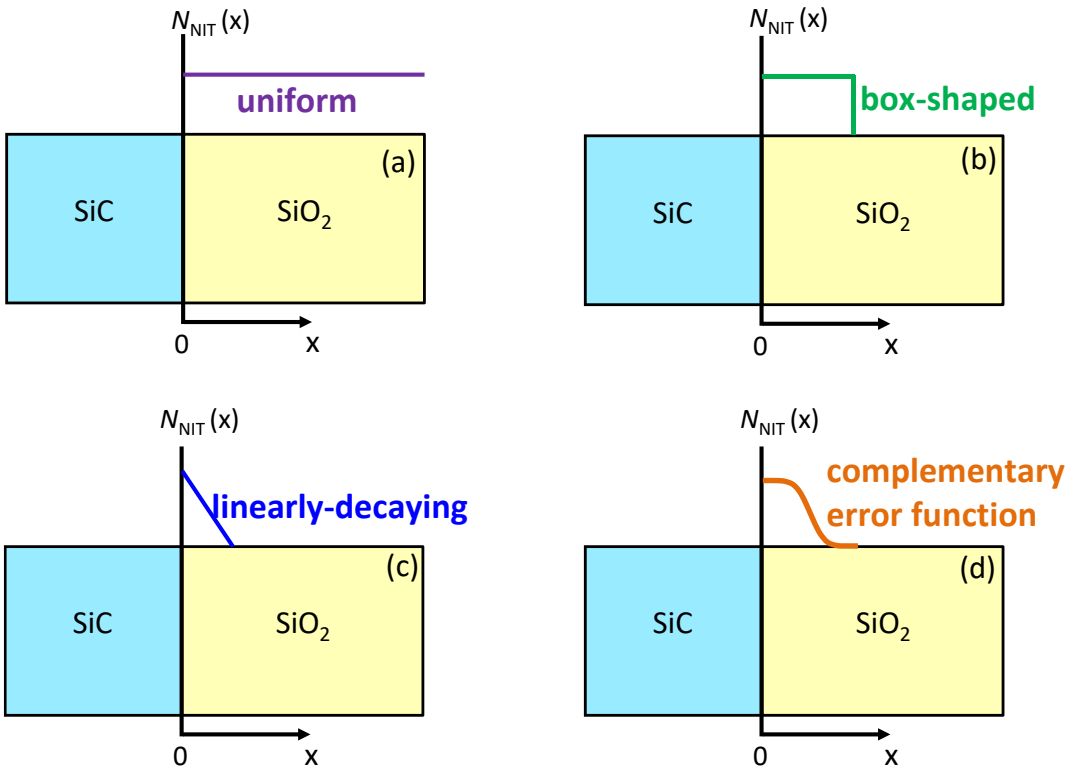

Fig. 3.4. Different kinds of NIT density distributions: (a) uniform distribution, (b) box-shaped distribution, (c) linearly-decaying distribution, and (d) complementary error function distribution.

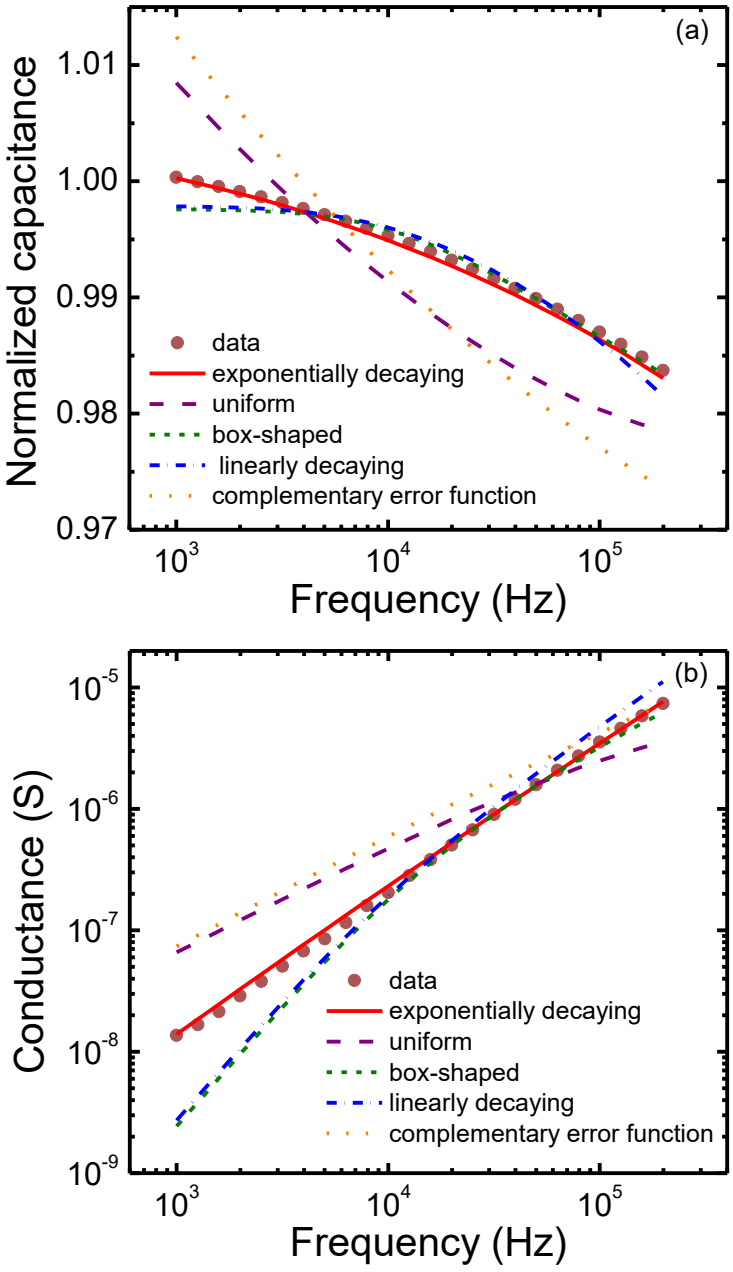

Fig. 3.5. Comparison of optimal fitting solutions by considering different distribution possibilities—uniform, linearly decaying, box-shaped, complementary error function, and exponentially decaying distributions. The 4H-SiC MOS capacitor with t_{ox} = 8.7 nm was taken as an example.

3.5 Thickness dependence of NIT density distribution

In light of the optimized fitting results of frequency-dependent properties of capacitance and conductance, the distributions of NIT density along the tunneling depth from the interface were extracted for the different samples, as illustrated in Fig. 3.6.

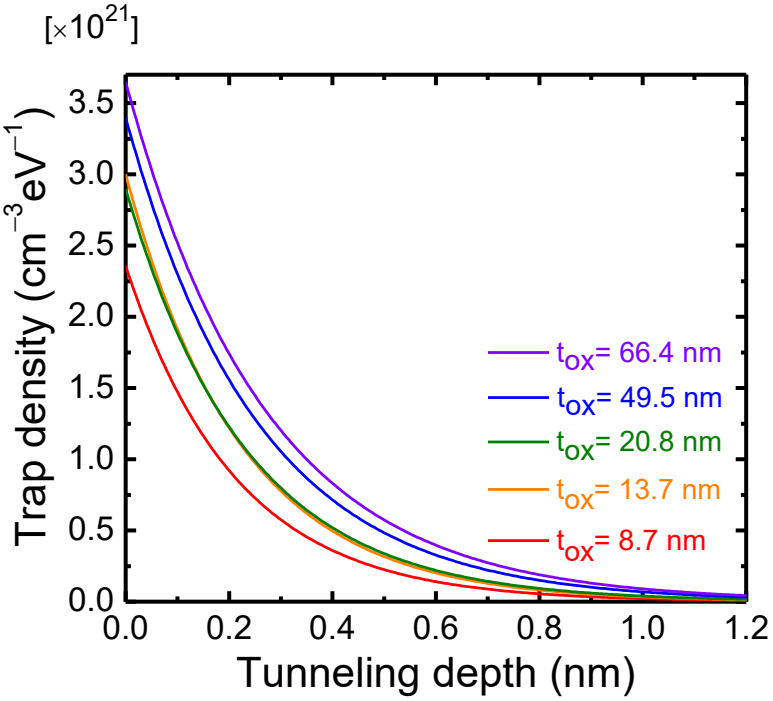

Fig. 3.6. Density distribution of NITs along the tunneling depth from the interface of SiO_2/4H-SiC MOS structures with various oxide thicknesses.

It is clear that the NIT density distributions decay significantly along the tunneling depth, which indicates that the NITs are only present within a few monolayers of the interface, agreement with the results by synchrotron XPS [1]. When oxide thickness increases, the NIT density increases. The thickness dependences of the density distribution of NITs, including NIT density at the interface (N_{NIT0}), and the decay constant α were demonstrated in Figs. 3.7 (a) and 3.7 (b). With increasing t_{ox}, N_{NIT0} increases while α decreases. By considering that tunneling attenuation coefficient of κ would affect α, the uncertainty of the electron tunneling mass m^*, which affects κ, was taken into account. m^* was determined to be $0.3m_0$ in this work [4], and ±10% error in m^* was considered [5, 6]. The fitting analysis revealed 10% error in m^* would introduce errors in N_{NIT0} and α, with the values smaller than 3% and 2%, respectively. The changing tendencies of N_{NIT0} and α with oxide thickness were hardly affected by the error deviation. Figure 3.8 demonstrates the total areal NIT density as a function of SiO_2 thickness. By integrating $N_{NIT}(x)$ over the oxide thickness, the total areal NIT density was calculated. It is obvious that the increase in SiO_2 thickness would lead to the increase in total NIT density.

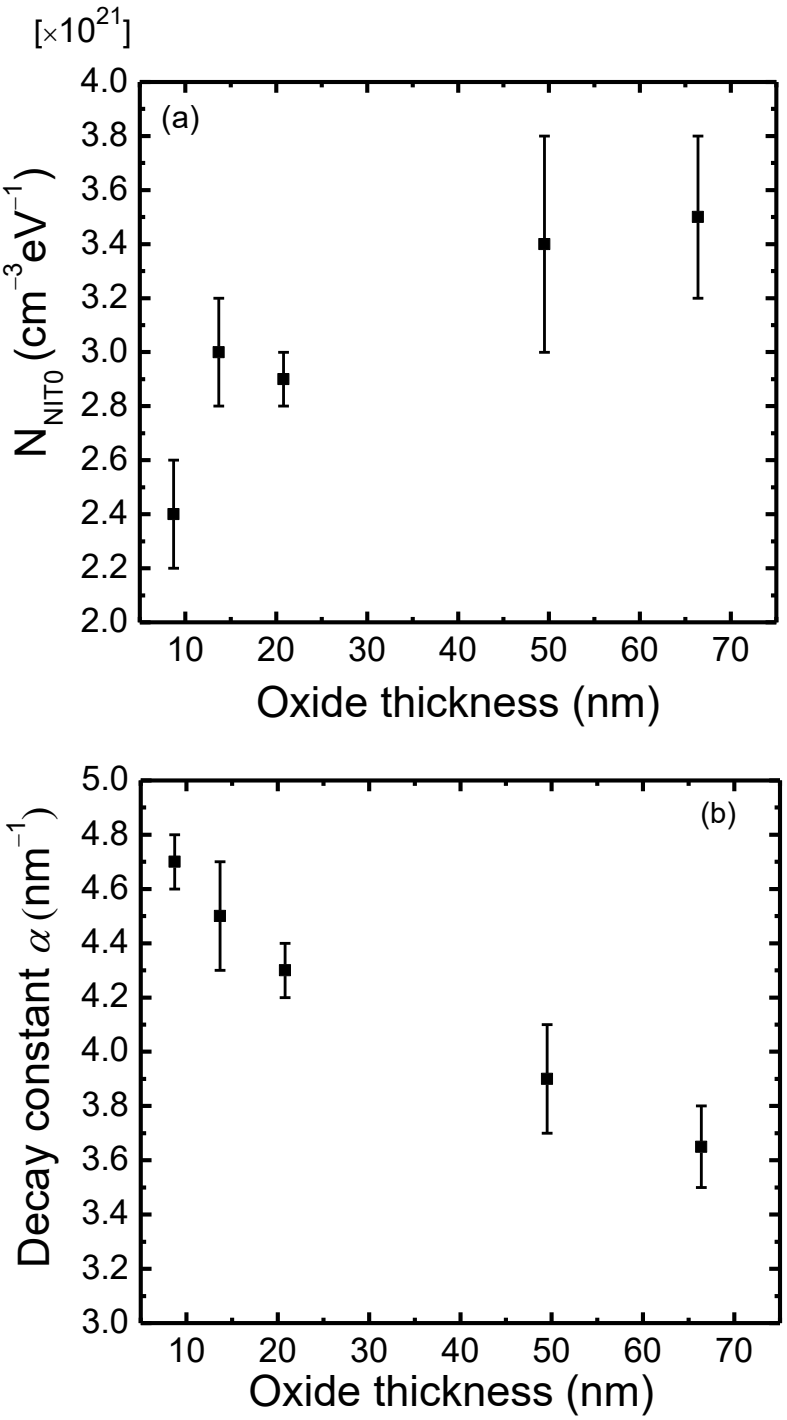

Fig. 3.7. Thickness dependence of (a) N_{NIT0} and (b) α.

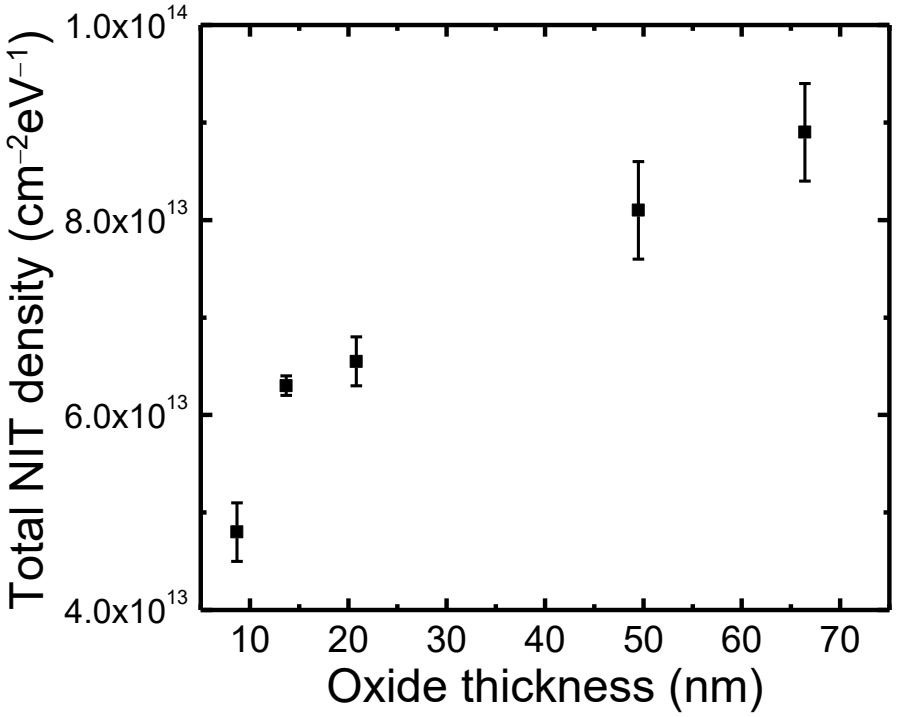

Fig. 3.8. Total areal NIT density as a function of SiO_2 thickness.

3.6 Discussion

Here, the thickness dependence of NITs would be briefly discussed. In prior that, the physical origin of NITs should be considered. According to the analysis by Afanas'ev *et al*., the oxygen vacancies or excess Si atoms in SiO_2 would generate NITs, and the NITs exist both in Si and SiC MOS structures with different polytypes [7, 8]. For the origin investigation of NITs, theoretical studies with first principle calculation can analyze the possible defect structures. Knaup *et al*. found that the origin of NITs may be due to the Si interstitials and doubly bonded C-C dimers [9]. In light of the hybrid density function calculations, which is more accurate and can calibrate the bandgap values of SiC and SiO_2, and also the band offset, Devynck *et al*. estimated different kinds of defects in the SiC and SiO_2 sides. They revealed that the Si_2-C-O structure would generate narrow peaks not only near the E_c of 4H-SiC, but also near the valence band edge (E_v) of 4H-SiC. The Si_2-C-O structure was considered to be the possible reason for NITs [10]. Despite unclear NIT origin, the generation of NITs would strongly depend on the oxidation process. During the oxidation process, large interface stress would occur because of the expansion of Si lattices [11]. Based on the oxidation analysis with the "Si and C emission" model proposed by Hijikata *et al*., the Si and C interstitials would emit into SiO_2, with the purpose of releasing the interface stress [3]. When the oxidation time is short, it is easy for Si and C interstitials to emit to the SiO_2 surface and to be immediately oxidized or evaporated. When the SiO_2 thickness increases, the Si and C interstitials are difficult to emit outside immediately [12]. This would result in the Si and C interstitials accumulating in SiO_2, which may promote the generation of defect structures that result in higher density of NITs.

3.7 Summary

The NIT density distribution as a function of oxide thickness was evaluated for n-type SiO_2/4H-SiC structures. By analyzing the NITs with the distributed tunneling model for different MOS capacitors by varying SiO_2 thicknesses, the exponentially decaying distribution of NITs was assessed. The frequency dispersions of capacitance and conductance for all of the MOS structures were explained successfully. The uniform, box-shaped, linearly decaying and complementary error function distributions were also considered, but they could not yield good fitting results with the experimental data. However, the exponentially decaying distribution obtained optimized fitting. Therefore, an exponentially decaying distribution would be the most plausible approximation for the true density distribution of NITs. Then, the effect of oxide thickness on NIT density distribution was estimated by using the optimized fitting solutions under strong accumulation conditions. It is found that there is an increasing tendency as the SiO_2 thickness increases. Despite the unclear origin of NITs, thickness dependent properties of NIT density were discussed by considering the Si and C emissions, which occurs during SiC oxidation. As SiO_2 thickness increases, more Si and C interstitials accumulate near the interface and more possible defect structures would be generated, which could result in higher density of NITs.

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Chapter 4

Modeling and characterization of NITs for p-type 4H-SiC MOS structure

4.1 Introduction

In Chapters 2 and 3, the spatial distribution of NITs near the conduction band edge (E_c) of 4H-SiC was characterized with a modified distributed circuit model, which would make a significant contribution to understanding the nature of NITs and to further enhancing the development of n-channel 4H-SiC power MOSFETs. Likewise, the development of p-channel 4H-SiC power MOSFETs is also important because they are indispensable in the application of complementary inverter [1, 2] or complementary MOS (CMOS) logic devices [3, 4]. However, p-channel 4H-SiC power MOSFETs also face similar challenges, such as low channel mobility and large threshold voltage (V_{th}) instability. Therefore, the study of NITs in the valence band side of 4H-SiC is also necessary. However, the distributed circuit model applied for n-type 4H-SiC MOS capacitors in the strong accumulation conditions is not valid for the p-type 4H-SiC MOS capacitors. With regards to the p-type 4H-SiC MOS capacitors fabricated by dry oxidation process, there exists a large amount of effective positive fixed charge, which would lead to a large negative flatband voltage shift (ΔV_{FB}). Therefore, it is difficult to achieve the strong accumulation conditions within the general gate voltage range by measurements for the p-type MOS capacitors. For example, maximum DC output voltage of a standard impedance analyzer (Keysight E4990A) is limited to ±40 V, which is not enough to obtain strong accumulation condition in this case. Thus, in this Chapter, the conductance method was employed to evaluate the interface properties of SiO_2/p-type 4H-SiC interface and the conductance-frequency (G_p/ω–f) properties in the low frequency range is considered to be related to NITs, which was analyzed with a model originally used for the slow trap characterization of insulator/semiconductor interface on III-V compound semiconductors.

4.2 Conductance method

4.2.1 Principle of conductance method

The AC signal conductance method is an approach to calculating interface state density (D_{it}) and capture cross section by measuring the conductance versus gate voltage and frequency for a typical MOS capacitor. The conductance method is the most accurate and sensitive small signal steady-state method, established by Nicollian *et al*. [5, 6]. It is known that the interface traps and NITs can exchange electrons with the conduction band of 4H-SiC and holes with the valence band of 4H-SiC. Figures 4.1 (a)–4.1 (c) schematically show the band-bending diagrams of a p-type 4H-SiC MOS capacitor under various gate biases. When the gate bias changes, the status of hole occupancy by the traps changes. The band bending without gate bias in Fig. 4.1 (a) is caused by the work function difference of metal-semiconductor and the effective fixed charge existing at and near the interface.

The traps located below the Fermi level (E_F) are full and the ones above the E_F are empty. When a negative gate bias is imposed, the valence band edge (E_v) at 4H-SiC surface moves towards the E_F,

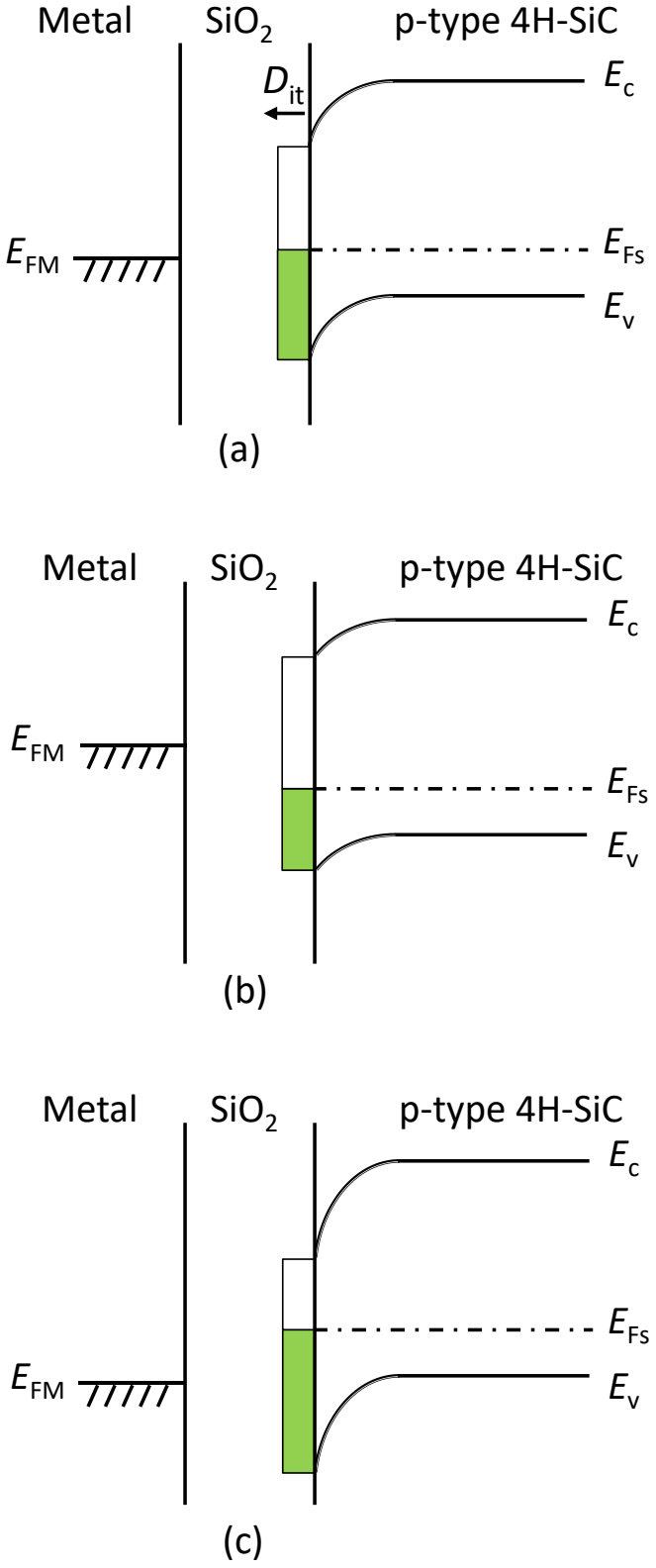

Fig. 4.1. Schematic band-bending diagrams which show the change of hole occupancy of traps at various gate bias conditions of (a) no gate bias, (b) negative gate bias and (c) positive gate bias for a typical p-type 4H-SiC MOS structure.

and thus the traps can capture the holes, as demonstrated in Fig. 4.1 (b). When a positive gate bias is imposed, the E_c at 4H-SiC surface moves towards the E_F and the traps would emit holes, illustrated in Fig. 4.1 (c). By means of the small change of the imposed gate voltage, the hole occupancy by the traps would change and this would cause the energy loss. The conductance method can be used to analyze the energy loss and thus to detect the information of traps.

In order to explain the energy loss, an n-type 4H-SiC MOS structure is taken as an example. The energy loss can be considered as the average energy change of the total electrons. The small AC signal is typically 25 mV (rms). For a given AC gate signal, in the positive half cycle, the E_c at the surface of 4H-SiC moves towards the E_F, and thus the average electron energy would increase immediately. When the change of the average energy is able to be measured at a certain frequency, the interface traps cannot respond to the frequency immediately, while they would lag behind the AC gate signal. Therefore, some of the trap energy levels below the E_F of 4H-SiC would be empty. The energy loss would occur when the electrons with higher energy level are captured by the traps with lower energy, which makes the obtained electron energy the same with the free electrons. During this process, the energy loss would be taken up by phonons, leading to the crystal lattice heating. Similarly, in the negative half cycle, the E_c at the surface of 4H-SiC moves away from the E_F, which makes the average electron energy filled by traps higher than the electron energy in 4H-SiC. The emitted electron energy from the traps would be the same with the free electrons, and this process would also produce energy loss [5, 6].

Therefore, during the measured cycle when the AC gate signal is provided, the energy loss would be generated. The average energy loss can be represented by the equivalent parallel conductance (G_p). Besides the energy loss, traps keeping the captured electrons for a period would generate the capacitance (C_{it}). The energy loss at a certain frequency depends on the response speed and density of the traps. According to the energy loss at various frequencies and DC gate biases, the trap density can be calculated.

In the conductance method, by measuring the impedance or admittance at various frequencies and DC gate biases, the trap density and time constant can be obtained versus DC gate voltage. Then, the low frequency *C–V* characteristics should be measured to estimate the relationship between the band bending and gate bias, that is, the surface potential at each DC gate bias. Thus, the energy distribution of the traps can be obtained.

4.2.2 Parameter extraction by conductance method

In order to define the parallel conductance (G_p) and capacitance (C_p), the measured circuit and the equivalent circuit are shown in Figs. 4.2 (a) and 4.2 (b). The C_p should be the parallel combination of interface trap capacitance and the semiconductor capacitance. By considering the equivalence of these two circuits, the G_p/ω was expressed as:

$$\frac{G_p}{\omega} = \frac{\omega C_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}, \tag{4.1}$$

where ω is the angular frequency, C_m and G_m the measured capacitance and conductance, and C_{ox} the oxide capacitance. According to Eq. (4.1), the values of G_p/ω can be obtained from measurements.

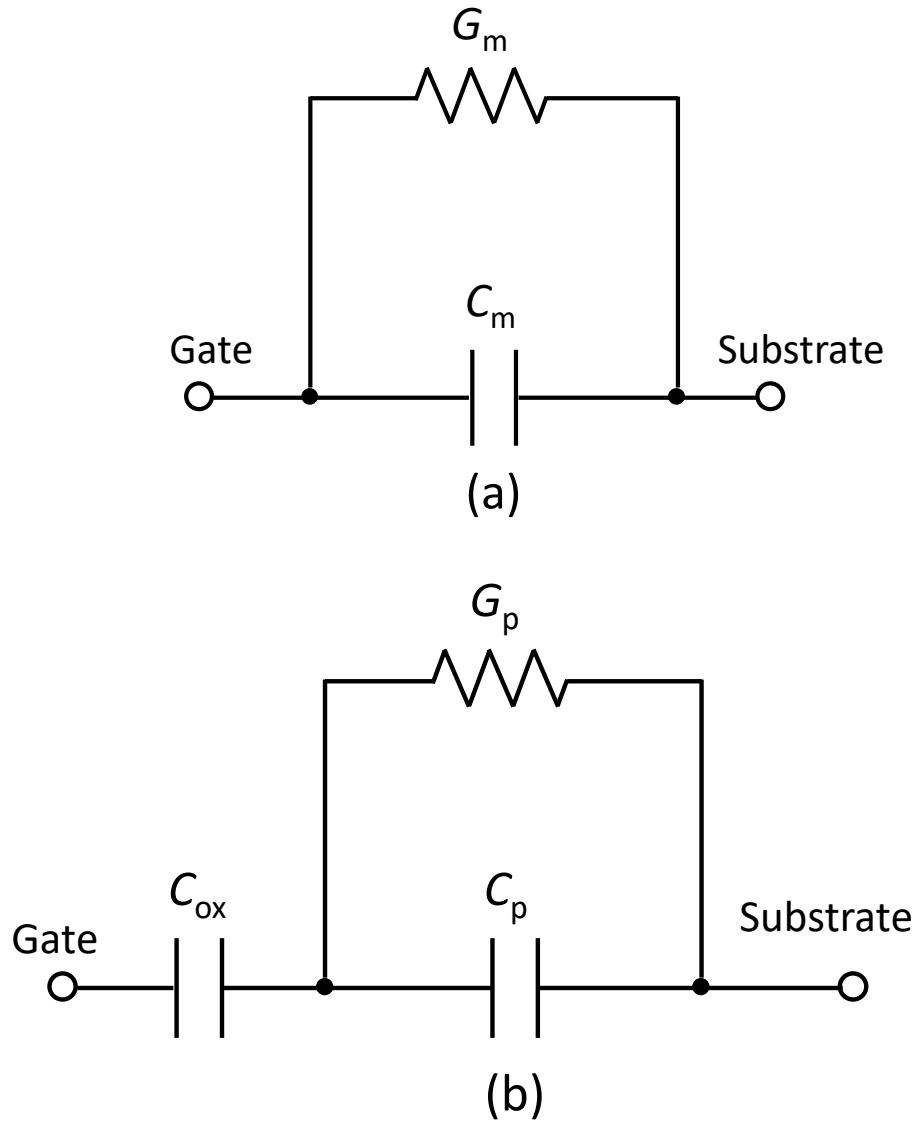

Fig. 4.2. (a) Measured circuit and (b) equivalent circuit defining equivalent parallel conductance (G_p) and capacitance (C_p).

Next, the Gaussian fitting method for G_p/ω versus frequency (G_p/ω–f) characteristics proposed by Brews *et al*. is introduced [7]. The parameters of surface potential fluctuation (σ_s), interface trap density (D_{it}), time constant of interface traps (τ_p), and capture cross section (σ_p) can be extracted.

(1) The extraction way of σ_s proposed by Brews will be introduced [7]. Figure 4.3 shows a theoretical G_p/ω–f curve. The σ_s determines the width of G_p/ω–f curve. A simple way to evaluate the width of G_p/ω–f curve is using an arbitrary fraction, as expressed by Eq. (4.2):

$$G_p/\omega = f_w(G_p/\omega)_p . \tag{4.2}$$

Here, $(G_p/\omega)_p$ is the peak value of G_p/ω, and f_w is a fraction which is selected to determine the width.

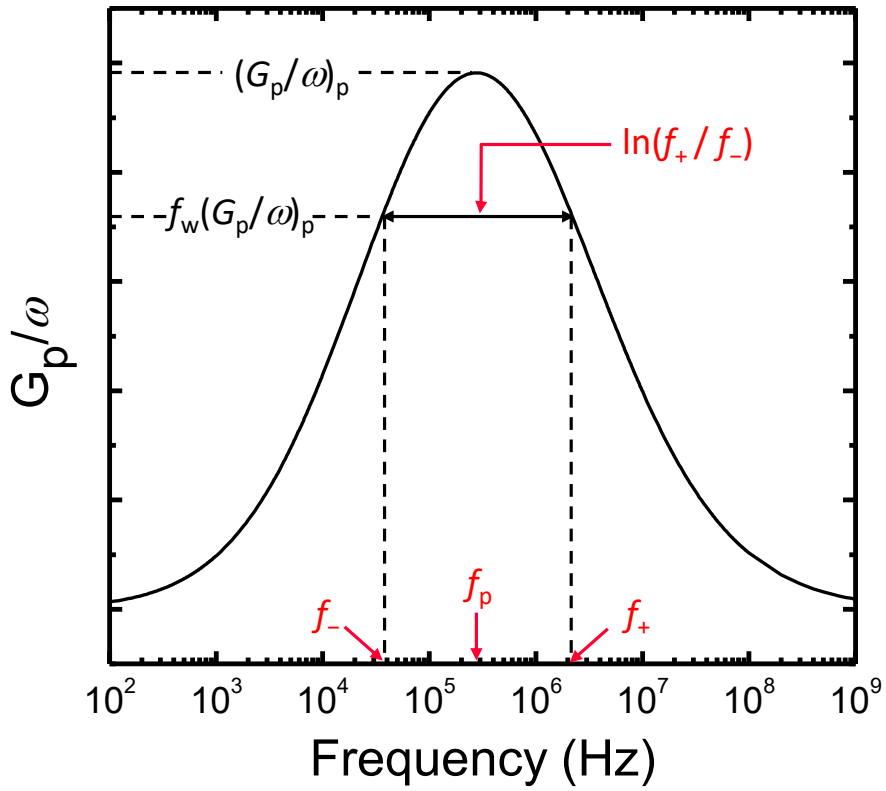

Fig. 4.3. A typical G_p/ω–f curve at a certain gate voltage for a MOS structure.

According to the theory of Nicollian and Goetzberger [5, 6], for the given σ_s, G_p/ω is a function of ξ, which can be expressed as:

$$\xi = \omega\tau_p . \tag{4.3}$$

Here, τ_p is the time constant that the interface traps capture the holes. Note that the subscript "p" represents the p-type substrate and holes are the major carriers. τ_p can be expressed by Eq. (4.4):

$$\tau_p = \frac{\exp(U_s)}{C_p N_A} . \tag{4.4}$$

U_s is the normalized surface potential, and N_A the hole doping concentration in units of cm^{-3}. C_p is the capture probability of holes, in units of cm^3/s, which can be expressed by Eq. (4.5):

$$C_p = \sigma_p \times v_{th} , \tag{4.5}$$

where σ_p is the capture cross section in units of cm^2, and v_{th} the thermal velocity.

According to the symmetry of G_p/ω–f curve, a given fraction of f_w in Eq. (4.2) corresponds to two values on a G_p/ω–f curve at two frequencies, f_+ and f_-. Therefore, the two values of ξ_+ and ξ_- can be determined. The G_p/ω–f width is estimated by $\ln(\xi_+/\xi_-)$. Given that C_p and N_A do not affect the value of ξ, the width can be expressed as follows:

$$\ln(\xi_+ / \xi_-) = U_s(+) - U_s(-) . \tag{4.6}$$

According to Eq. (4.6), it is obvious that the difference of the bend banding is the G_p/ω width. From the expression of ξ in Eq. (4.3), G_p/ω width can be calculated by the frequency difference, as shown in Eq. (4.7):

$$\ln(\xi_+ / \xi_-) = \ln(f_+ / f_-) = \ln f_+ - \ln f_- . \tag{4.7}$$

The peak width estimation based on Eq. (4.7) is illustrated in Fig. 4.3. From Eq. (4.6), the relationship between σ_s and $\ln(\xi_+/\xi_-)$ with various values of f_w is shown in Fig. 4.4. The σ_s can be determined from the chosen f_w.

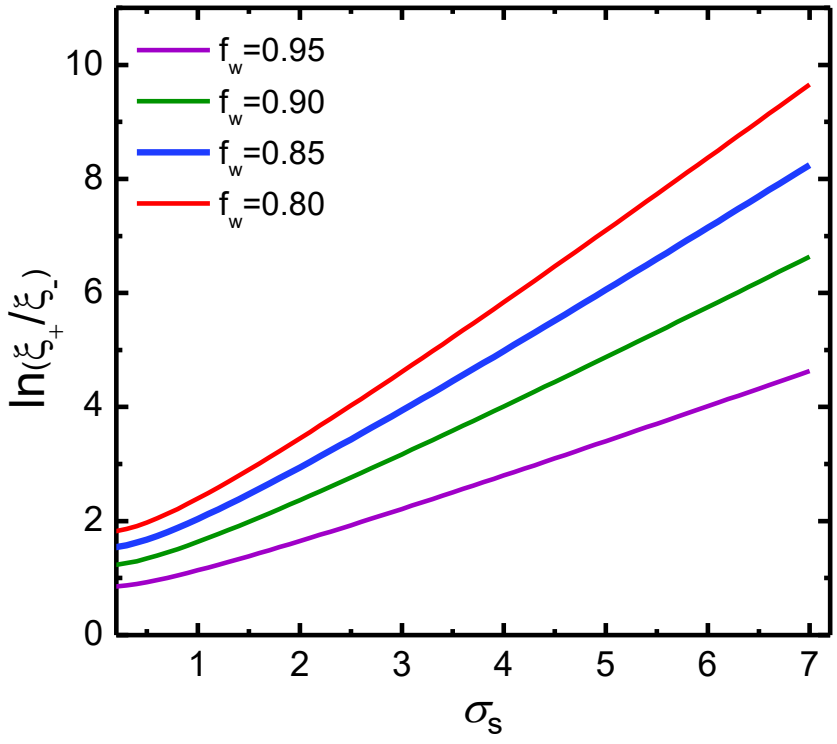

Fig. 4.4. The relationship between f_D and surface potential fluctuation σ_s.

(2) Next, in order to extract D_{it}, $(G_p/\omega)_p$ is needed. Based on the theory of Gaussian fitting proposed by Nicollian [5, 6], the relationship between $(G_p/\omega)_p$ and D_{it} can be expressed as:

$$\frac{(G_p/\omega)_p}{qD_{it}} = \frac{1}{2\xi_p}\int_{-\infty}^{\infty} \ln\left[1+\xi_p^{\,2}\right] P(U_s)\, dU_s , \tag{4.8}$$

where $P(U_s)$ is a probability that U_s is the band bending, expressed by:

$$P(U_s) = \frac{1}{\sqrt{2\pi\sigma_s^{\,2}}} \exp\left[-\frac{(U_s - \bar{U}_s)^2}{2\sigma_s^2}\right]. \tag{4.9}$$

$\bar{U}_s$ is the normalized mean surface potential. ξ_p is equal to $\omega_p(C_pN_A)^{-1}\exp(U_s)$, where ω_p is the angular peak frequency. In order to calculate D_{it}, the right side of Eq. (4.8) can be represented by a parameter f_D, and D_{it} can be expressed as:

$$D_{it} = (G_p / \omega)_p [f_D(\sigma_s) q]^{-1}. \tag{4.10}$$

The relationship of $f_D(\sigma_s)$ versus σ_s can be obtained numerically, as shown in Fig. 4.5. According to the extracted σ_s, f_D can be determined and thus D_{it} can be extracted.

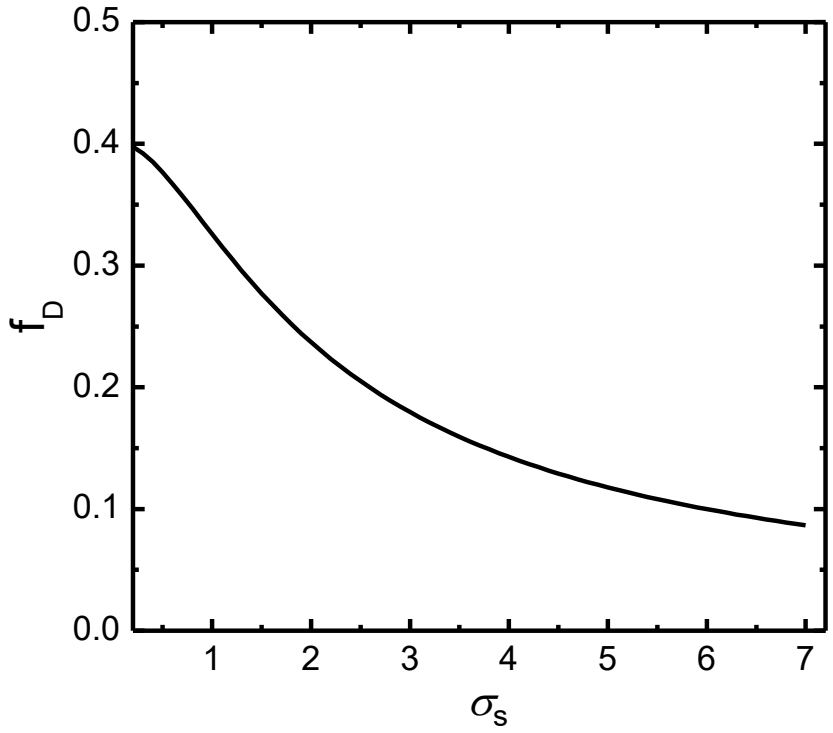

Fig. 4.5. The relationship between f_D and σ_s by numerical calculation.

(3) Finally, the trap time constant (τ_p) and capture cross section (σ_p) can be extracted. τ_p can be determined by the following condition:

$$\frac{d}{d\xi}\left(\frac{G_p}{\omega}\right) = 0. \tag{4.11}$$

By solving Eq. (4.11), the ξ_p versus σ_s can be yielded with numerical calculation and ξ_p can be found by the corresponding σ_s [7]. In light of Eqs. (4.3)–(4.5), the capture cross section (σ_p) can be calculated.

Based on the introduction of the conductance method, the conductance measurements would be introduced in the following section.

4.3 Experiments

A 5 μm-thick p-type 4H-SiC epilayer, with a net acceptor concentration of 1×10^{16} cm^{-3} was used to fabricate MOS capacitors. The epilayer was formed on a p-type 8° off-axis (0001) Si-face substrate. The bulk resistivity of the substrate was around 1.7 Ωcm and the thickness was around 366 μm. First, standard RCA (Radio Corporation of America) cleaning was conducted. Then, the sample was subjected to dry thermal oxidation at 1200 °C for 170 min. Subsequently, post-oxidation annealing

was performed in Argon (Ar) ambient for 30 min, and the thickness of SiO_2 was around 60 nm. Finally, the gate and backside ohmic contacts were formed by Al evaporation. The circular gate electrodes were 500 μm in diameter.

Multi-frequency impedance measurements were conducted at various gate voltages by using a Keysight E4990A impedance analyzer and a 42941A impedance probe kit with proper calibration. *C–V* measurements were also conducted with the E4990A. Besides, a Keysight B2912A Precision Source/Measure Unit was used to measure the *C–V* characteristics at 10 Hz to obtain low-frequency *C–V* curves.

4.4 G_p/ω–f characteristics

The *C–V* characteristics at different frequencies of the p-type 4H-SiC MOS structure were shown in Fig. 4.6. It should be noted that series resistance (R_s) correction was conducted, aiming at ruling out its effect on capacitance and conductance especially in the high frequency range [5]. By comparing with the ideal *C–V* curve illustrated in Fig. 4.6, it can be seen that large ΔV_{FB} exists, with the value of −33.4 V, which is attributed to the high density of effective positive fixed charges. The G_p/ω versus frequency characteristics at various gate voltages were shown in Fig. 4.7. Due to the limitation of the maximum gate voltage of −40 V, the oxide capacitance (C_{ox}) was determined by the maximum capacitance at −40 V. Note that by using B2912A, the maximum gate voltage can reach −45 V and the capacitance just slightly increased. This would almost have no effect on the G_p/ω characteristics. From Fig. 4.7, the G_p/ω–f characteristics were not symmetric and G_p/ω signals also exist in the low frequency range.

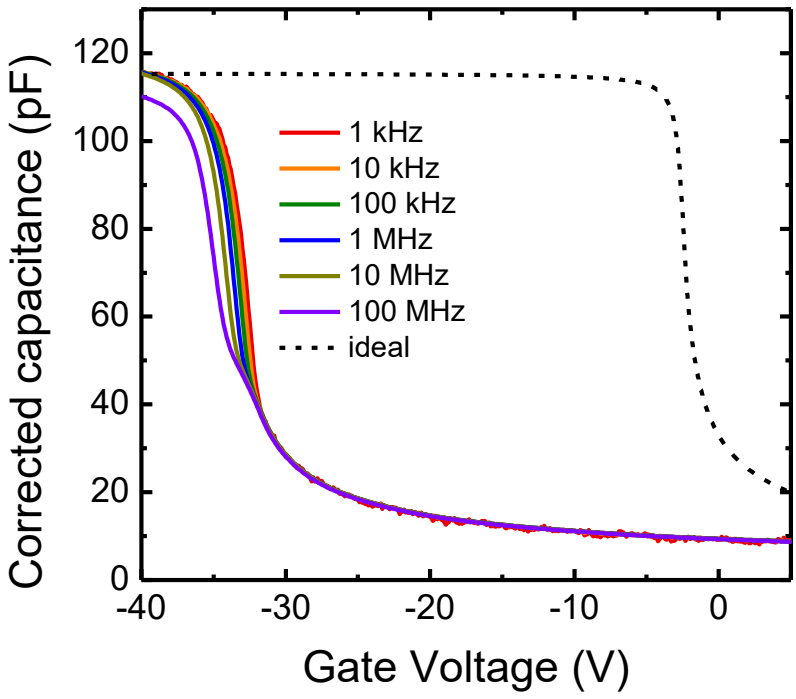

Fig. 4.6. *C–V* characteristics at different frequencies of the p-type 4H-SiC MOS structure.

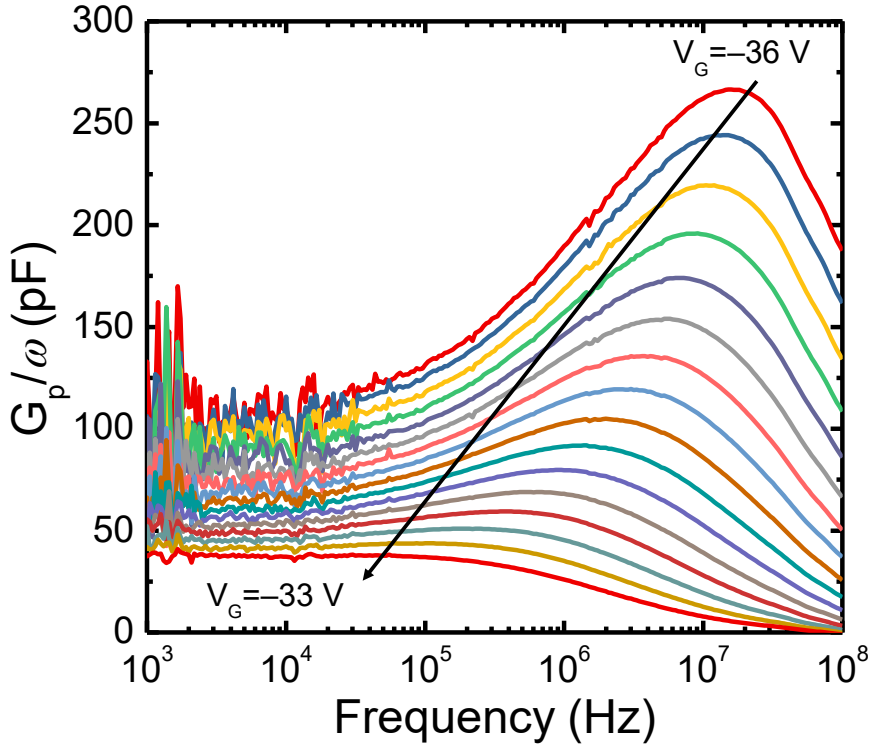

Fig. 4.7. G_p/ω versus frequency characteristics at various gate voltages for the p-type 4H-SiC MOS structure.

The G_p/ω signals in the high frequency range can be attributed to energy loss induced by the fast interface states, whose capture and emission of holes lag behind the change of the AC signal measurements. On the other side, the non-zero G_p/ω signal in the low frequency range indicates that the occurrence of energy loss would be due to the NITs in the SiO_2, which possess longer time constants than fast interface states [8–10]. Therefore, in the p-type case, both interface states and NITs are considered to contribute to the G_p/ω–f characteristics, as schematically shown in Fig. 4.8.

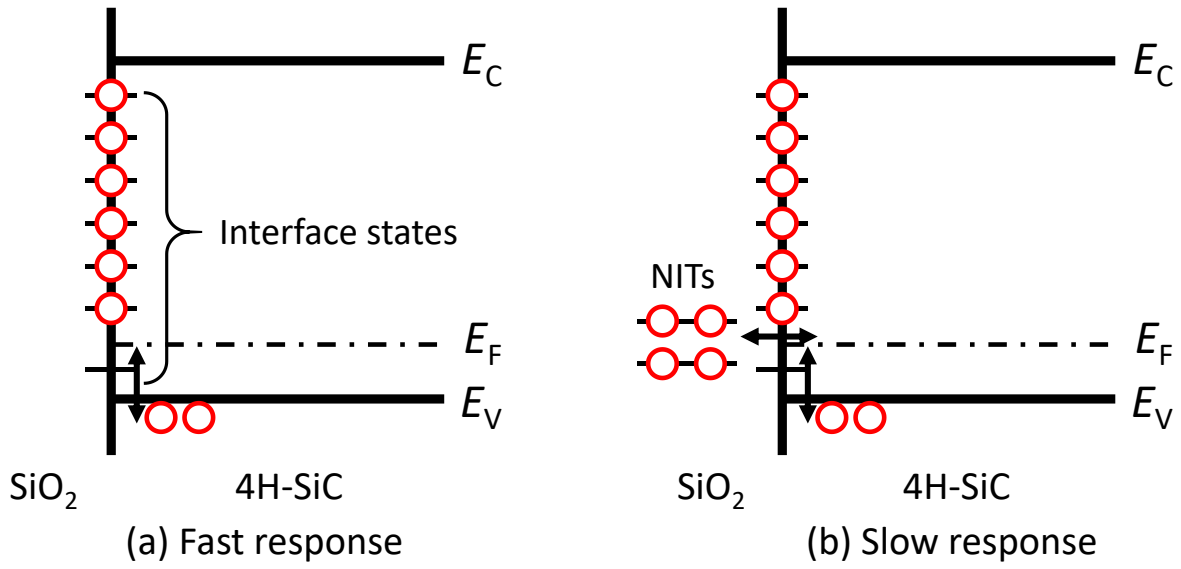

Fig. 4.8. Schematic illustrations of (a) fast response by interface states and (b) slow response by NITs.

Here, a typical G_p/ω–f curve at V_G = −35.6 V was taken as an example, which was demonstrated in Fig. 4.9. It is obvious that the G_p/ω–f curve can be divided into the high-frequency response curve and low-frequency response curve, as illustrated in Fig. 4.9. In terms of the G_p/ω signals in the high frequency range, the Gaussian fitting model proposed by Nicollian *et al*. [5] and the parameter extraction methodology by Brews were employed [7]. After that, the high frequency response can be subtracted by the total G_p/ω signals and thus, the G_p/ω signals in the low frequency range can be obtained.

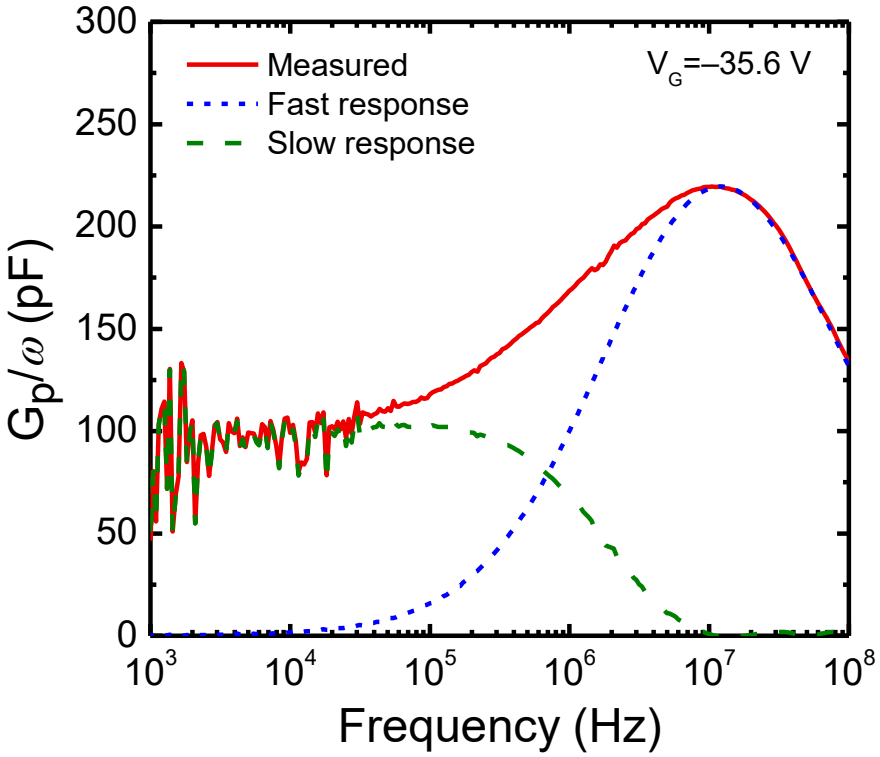

Fig. 4.9. The measured G_p/ω–f characteristic at V_G = −35.6 V. The fast and slow responses were schematically illustrated by blue and green dashed lines, respectively.

4.4.1 G_p/ω–f characteristics in the high frequency range

First, the fitting process for high frequency responses was conducted, as shown by the dashed blue line in Fig. 4.9. By applying the Nicollian's model for various gate voltages, important parameters of D_{it}, σ_s, σ_p and τ_p were extracted versus energy positions from the E_v of 4H-SiC: the results were shown in Figs. 4.10–4.13. Berglund integral was employed to obtain the surface potential and thus the trap energy level [11]. The surface potential at V_G equal to flatband voltage (V_{FB}), determined by the C–V curve at 100 MHz, was considered as the integral constant (ψ_{s0}). It can be seen that the order of D_{it} was 10^{12} $cm^{-2}eV^{-1}$ (Fig. 4.10), and the σ_s was almost constant (Fig. 4.11). The extracted capture cross section was in the order of around 10^{-16} to 10^{-13} cm^2. The energy dependence of trap time constant in Fig. 4.13 indicates that hole capture and emission follow the Shockley−Read−Hall (SRH) statistics [5].

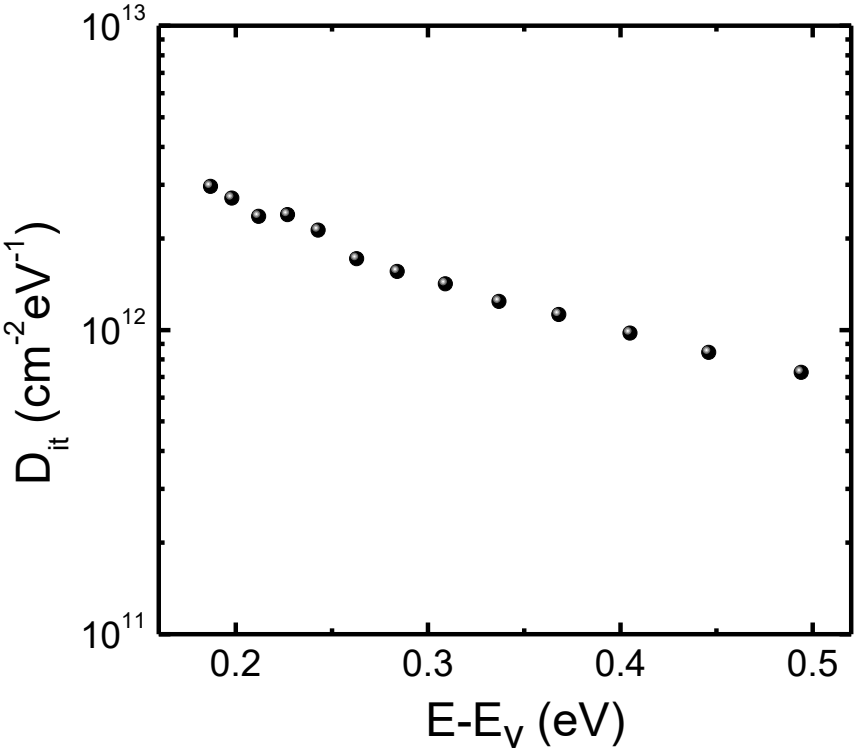

Fig. 4.10. Interface state density versus trap energy level from the E_v of 4H-SiC extracted by Gaussian fitting for high frequency range.

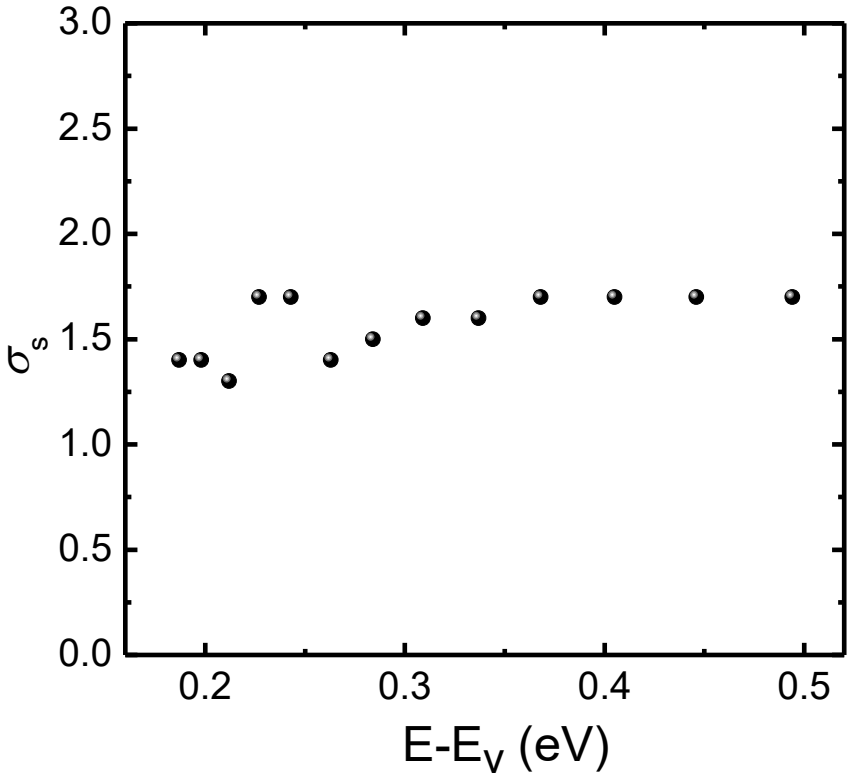

Fig. 4.11. Surface potential fluctuation versus trap energy level from the E_v of 4H-SiC extracted by Gaussian fitting for high frequency range.

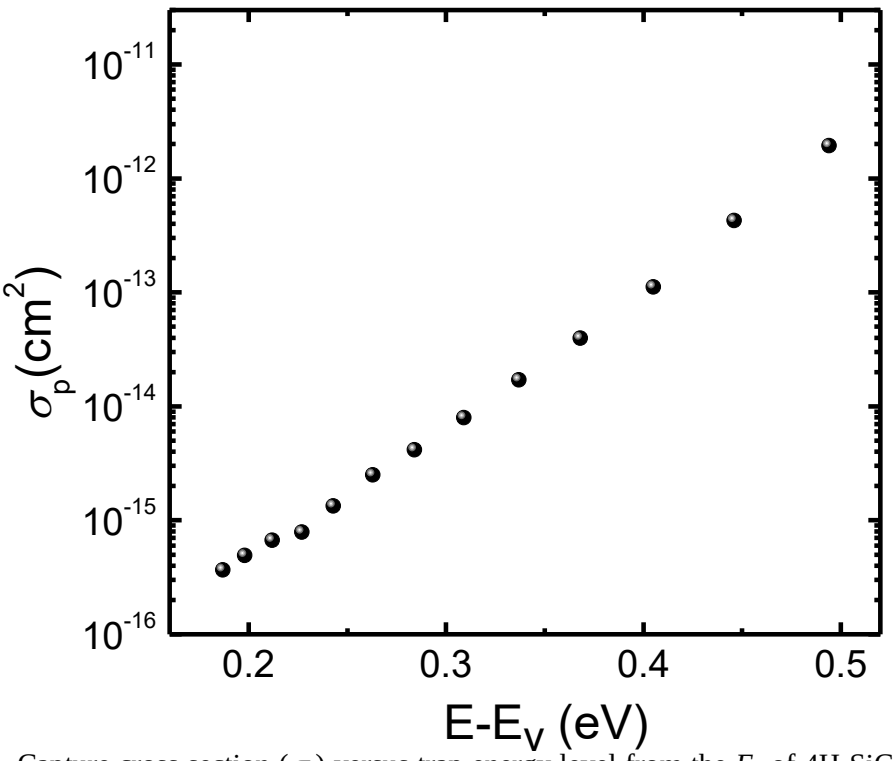

Fig. 4.12. Capture cross section (σ_p) versus trap energy level from the E_v of 4H-SiC extracted by Gaussian fitting for high frequency range.

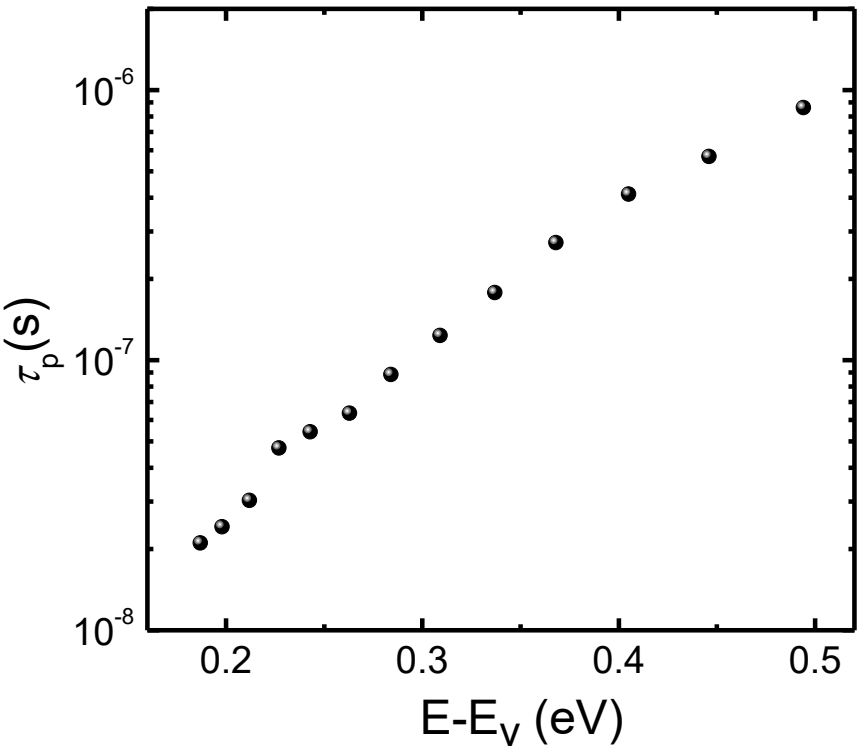

Fig. 4.13. Trap time constant (τ_p) versus trap energy level from the E_v of 4H-SiC extracted by Gaussian fitting for high frequency range.

4.4.2 G_p/ω–f characteristics in the low frequency range

After subtracting the high-frequency G_p/ω–f signals, the G_p/ω–f signals in the low frequency range

were extracted at various gate biases, as shown in Fig. 4.14. It is obvious that the low-frequency G_p/ω–f signals were not symmetric, which implies that Gaussian fitting model by Nicollian *et al*. could not be directly used and the NITs located in SiO_2 should be considered. The similar phenomenon was observed at the Si_3N_4/GaAs interface, and Cooper *et al*. proposed a model and analyzed the G_p/ω–f signals in the low frequency range by considering NITs [12]. Here, Cooper's model, explained in the following section, would be also applied for SiO_2/p-type 4H-SiC case.

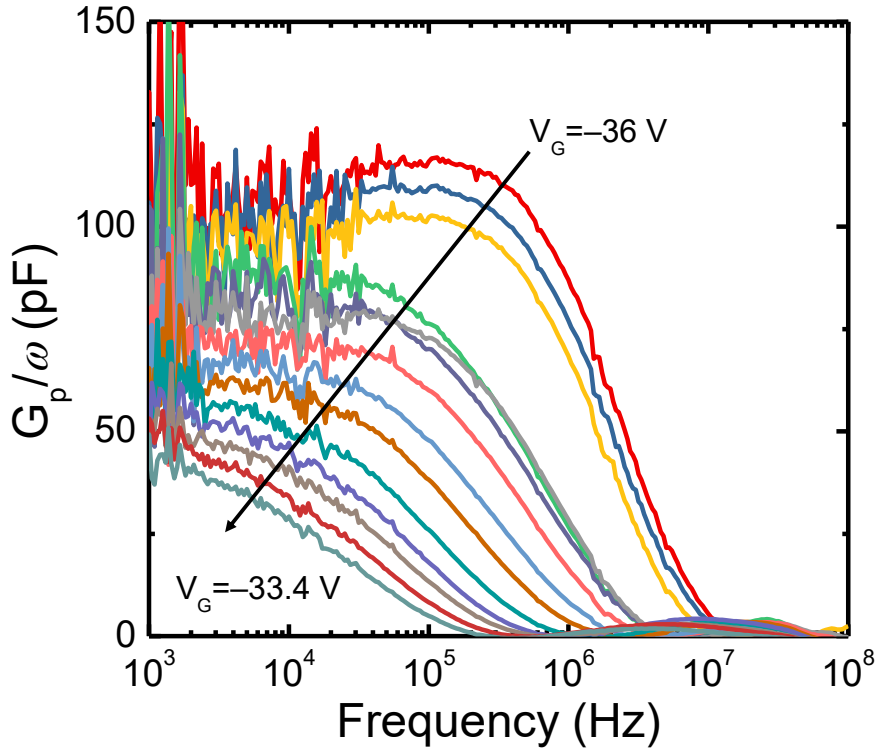

Fig. 4.14. G_p/ω–f signals in the low frequency range at various gate biases.

4.4.3 Cooper's model with consideration of NITs

In Cooper's model, by taking the tunneling of holes to the NITs into account, the conductance contribution induced by NITs can be expressed as [12]:

$$\frac{G_p}{\omega}=\frac{qN_{ot}}{2\kappa_0}\left\{\frac{\pi}{2}+\frac{1}{\sqrt{2\pi}\sigma_s}\int_{-\infty}^{\infty}-Z\left[\frac{1}{2}\exp(-Y)\ln\left[1+\exp(2Y)\right]-\tan^{-1}\left[\exp(Y)\right]\right]dU_s\right\}, \tag{4.12}$$

where Y is equal to $\ln(\omega\tau_{ot})$, and Z can be expressed by Eq. (4.13) as follows:

$$Z=\exp\left[\frac{\left(U_s-\overline{U_s}\right)^2}{\sigma_s^2}\right]. \tag{4.13}$$

In Eq. (4.12), N_{ot} is the density of NITs in units of $cm^{-3}eV^{-1}$, τ_{ot} the time constant of NITs, and κ_0 the tunneling attenuation coefficient of the electron wave function of energy E, which can be expressed as follows:

$$\kappa_0 = \frac{\sqrt{2m^*\left(E - E_v^{ox}\right)}}{\hbar}. \tag{4.14}$$

The tunneling process between NITs and the E_v of p-type 4H-SiC is illustrated schematically in Fig. 4.15. The m^* is the effective mass of holes for direct tunneling, and $m^* = 0.58\ m_0$ is used [13]. $E-E_v^{ox}$ is the tunneling barrier height for holes and it mainly depends on the energy offset between E_F and E_v^{ox}. By considering the valence band offset of SiO_2/4H-SiC with the value of about 2.9 eV [13], and the bulk E_F in 4H-SiC, the value of $E-E_v^{ox}$ was estimated to be about 3.1 eV. From Eq. (4.13), the σ_s, U_s, and $\bar{U}_s$ were also used. Note that the same values with the ones obtained in the high frequency calculation were used. By assuming proper values for N_{ot} and τ_{ot}, the $G_p/\omega-f$ curves can be analyzed with this model.

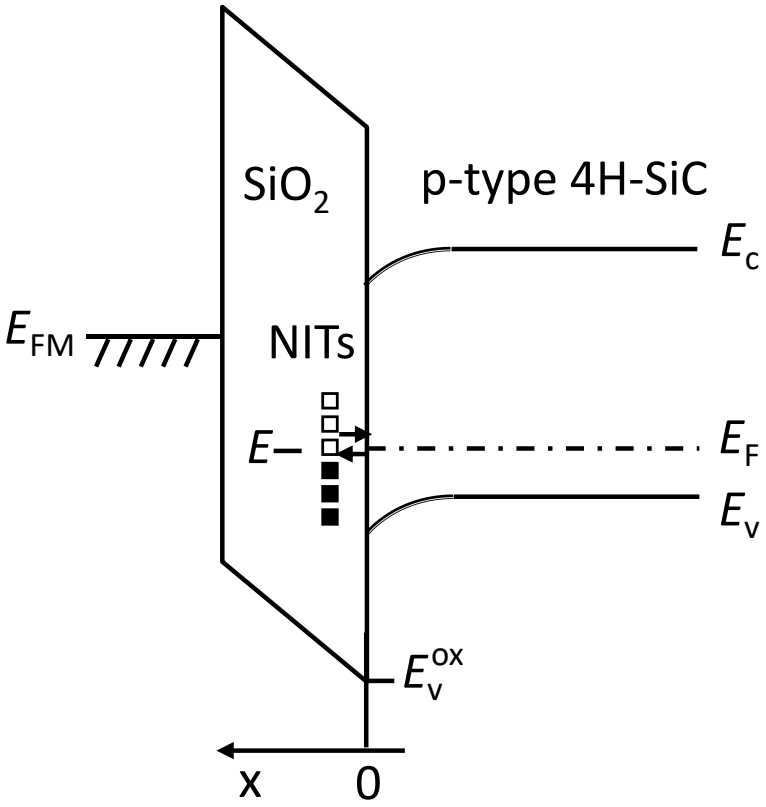

Fig. 4.15. Schematic band diagram of hole tunneling between NITs and the valence band edge of 4H-SiC in the depletion region. Note that the existence of many effective positive charges results in the opposite band bending between SiO_2 and p-type 4H-SiC.

4.4.4 NIT estimation with Cooper's model

Based on Cooper's model, the low-frequency $G_p/\omega-f$ signals were analyzed. The fitting result at $V_G = -35.6$ V was demonstrated in Fig. 4.16. The trap distribution was assumed to be constant [12]. The N_{ot} and τ_{ot} mainly determine the shape of the low-frequency $G_p/\omega-f$ signals. The height of the shape is affected by N_{ot} and the right side of the curve changes with τ_{ot}. σ_s almost has no effect on the low-frequency $G_p/\omega-f$ shape. By applying the fitting process to various gate voltages, the NIT density

as a function of trap energy level from the E_v of 4H-SiC was extracted, which is shown in Fig. 4.17. It can be seen that the extracted NIT density is in the order of 10^{19}–10^{20} $cm^{-3}eV^{-1}$.

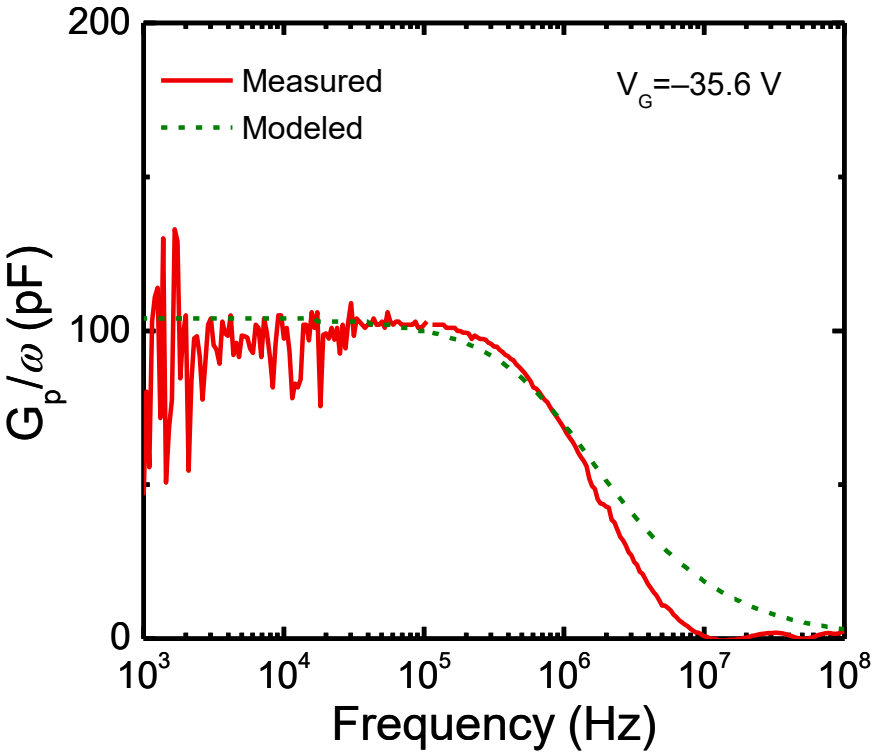

Fig. 4.16. Measured G_p/ω–f curve (denoted by solid line) and fitted G_p/ω–f curve in the low frequency range by Cooper's model with considering NITs.

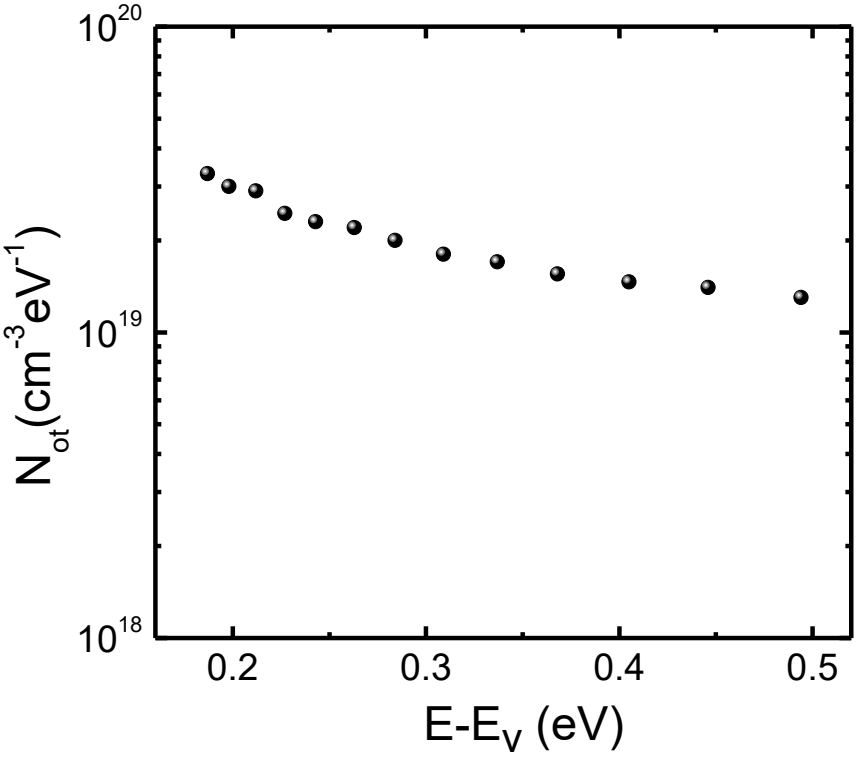

Fig. 4.17. NIT density as a function of trap energy position from the E_v of 4H-SiC.

4.5 Discussion

Here, the relationship between the small surface potential fluctuation (σ_s) and large flatband voltage shift (ΔV_{FB}) should be discussed. In general, the main reason for the surface potential fluctuation is the existence of the distributed charges at the interface between the oxide and semiconductor or the ones in the oxide, including the charged interface states, NITs, and fixed oxide charges [14–16]. However, according to the ΔV_{FB} value, the density of effective fixed charges was relatively large, with the value of around 1.2×10^{13} cm^{-2}, while the estimated values of σ_s, shown in Fig. 4.11, were not that large. This difference could be explained by different contributions of the oxide charges on the two parameters. Werner *et al*. investigated the effect of the oxide charge position on the σ_s and they found that the surface potential fluctuation is dominated by the charges very close to the oxide/semiconductor interface [17]. However, there is a linear relationship between ΔV_{FB} and the charge position from the interface and the charges separated from the interface can affect ΔV_{FB} significantly [17]. Despite the difficulty to compare the σ_s and ΔV_{FB} quantitatively in this work, the difference between the extracted σ_s and ΔV_{FB} implies that the NITs or fixed oxide charges distribute widely in SiO_2.

It should be noted that the limitation exists in the quantitative analysis of the NIT density in this work, because of the uncertainty in physical parameters. Specifically, the determination of the tunneling constant κ_0 would lead to errors because of the uncertainty in the hole tunneling mass (m^*) and the valence band offset. According to Copper's model in Eq. (4.12), this would introduce the error in the NIT density. 10% error in m^* or valence band offset would introduce around 5% error in N_{ot}. Even though reasonable values were used for the physical parameters at present, more precise determinations are needed. Also, in the valence band side of 4H-SiC, the error estimation method for the fitting process also needs to be improved. Besides, the extraction of the high-frequency peaks in the $G_p/\omega - f$ characteristics should be careful, because the high and low frequency responses may overlap and thus introduce artificial errors. However, the N_{ot} estimation would not be affected, because it is dominated by the height of the $G_p/\omega - f$ shape in low-frequency range. Despite the limitations mentioned above in this analysis, it is still valid to discuss the presence of slow interface traps near the SiO_2/p-type 4H-SiC interface to some extent.

With regards to the physical origin of the slow traps in the valence band side of 4H-SiC, it is still unclear. For the conduction band side of 4H-SiC, NITs are considered to be responsible for the high D_{it} values near the E_c of 4H-SiC [18]. The first principle calculation by Devynck *et al*. found that the energy position of Si_2-C-O structure in the SiO_2 side is consistent with the reported energy levels of NITs in the conduction band side [19]. Devynck *et al*. reported that the Si_2-C-O structure could generate trap levels not only close to the E_c of 4H-SiC, but also close to the E_v of 4H-SiC [19]. Therefore, the Si_2-C-O structure may be the origin of NITs in the SiO_2/4H-SiC MOS structures. However, further analysis is needed to investigate the NITs near the E_v of 4H-SiC, as revealed in this study.

4.6 Summary

The interface properties of SiO_2/p-type 4H-SiC MOS structure with dry oxidation were analyzed

with a modified conductance method. It is found that the $G_p/\omega-f$ signals exist both in the high frequency and low frequency range, which are dominated by the interface states and NITs, respectively. The interface states were characterized with the standard conductance method which used the Gaussian fitting model for the $G_p/\omega-f$ characteristics in the high frequency range. The NITs which contribute to the $G_p/\omega-f$ signals in the low frequency range were characterized by using Cooper's model, which considered the tunneling process of holes to the NITs, and the NIT density was estimated. The trap density of the dry oxide is extremely high and the development of passivation methods taking into consideration of the near-interface traps is required.

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Chapter 5

Conclusions

5.1 Conclusions

4H-SiC power MOSFETs are promising devices for power applications, but their low channel mobility and large threshold voltage instability are two main obstacles, which would be mainly ascribed to the near interface traps (NITs). However, the NIT investigation had been far from satisfactory and the physical origin has been unclear. In this study, modeling and quantitative characterization were conducted to investigate NITs in both conduction and valence band sides of 4H-SiC.

In Chapter 2, the modeling and characterization of NITs in the conduction band side of 4H-SiC was investigated. A distributed model which considered the electron tunneling to NITs was applied for n-type 4H-SiC MOS capacitors. An exponentially decaying distribution of NITs was assumed, by which the frequency dependence of capacitance and conductance in the strong accumulation conditions were successfully explained for the 4H-SiC MOS capacitors with different oxidation processes. Besides, with increasing the NO annealing time, the NIT density decreased significantly.

In Chapter 3, the impact of oxide thickness on NITs in the conduction band side of 4H-SiC was investigated. The exponentially decaying distribution assumption of NITs was verified by investigating the thickness dependence of NITs. Also, NIT density distribution was evaluated for the n-type 4H-SiC MOS capacitors with various oxide thicknesses and the total NIT density increased with increasing oxide thickness.

In Chapter 4, NITs in the valance band side of 4H-SiC were characterized. The conductance method was applied to investigate the interface properties of SiO_2/p-type 4H-SiC interface. The fast response of interface states contributes to the high frequency responses and can be characterized by the standard conductance method. The existence of NITs has been confirmed with the non-zero low-frequency G_p/ω signals, which has been estimated with Cooper's model. The NIT density as a function of the energy level from the valence band edge of 4H-SiC was estimated.

Based on this study, the total configuration of NITs in both the conduction and valence band sides of 4H-SiC was obtained, which would be beneficial to further understanding the nature of NITs and to promoting the performance of 4H-SiC MOSFETs.

5.2 Suggestions for future work

This study focused on the modeling and characterization of NITs in SiO_2/4H-SiC interface. However, only the Si-face (0001) 4H-SiC was investigated. The channel mobility of 4H-SiC MOSFETs depends on the surface orientation. Therefore, the crystal orientation dependence of NITs, such as $(000\bar{1})$, $(11\bar{2}0)$, and $(1\bar{1}00)$ faces should be investigated. This would facilitate the understanding of the different oxidation rates for different crystal orientations.

Besides, it should be noted that the NIT estimation in the valence band side of 4H-SiC has some limitations in this study. Therefore, further investigation of NITs in the valence band side is required and the possible distributions should be discussed carefully, which would be useful for the origin exploration of NITs.

Finally, in this work, the relationship between the threshold voltage shift and NIT density distributions was only discussed briefly in Section 2.5; the NIT distribution could be related to the fast threshold voltage shift in 4H-SiC MOSFETs. However, it is very important to quantitatively evaluate the relationship between the threshold voltage shift and NIT density distributions. This would boost the understanding of NIT effect on the device performance, promote the discovery of the new technique to reduce the NITs, and fabricate 4H-SiC power MOSFETs with better performance.

List of publications

A. Academic journals

1. **X. Zhang**, D. Okamoto, T. Hatakeyama, M. Sometani, S. Harada, R. Kosugi, N. Iwamuro, and H. Yano, "Characterization of near-interface traps at 4H-SiC metal-oxide-semiconductor interfaces using modified distributed circuit model", Appl. Phys. Express **10**, 064101 (2017).
2. **X. Zhang**, D. Okamoto, T. Hatakeyama, M. Sometani, S. Harada, N. Iwamuro, and H. Yano, "Impact of oxide thickness on the density distribution of near-interface traps in 4H-SiC MOS capacitors", Jpn. J. Appl. Phys. **57**, 06KA04 (2018).
3. Y. Karamoto, **X. Zhang**, D. Okamoto, M. Sometani, T. Hatakeyama, S. Harada, N. Iwamuro, and H. Yano, "Analysis of fast and slow responses in AC conductance curves for p-type SiC MOS capacitors", Jpn. J. Appl. Phys. **57**, 06KA06 (2018).

B. Presentations at international conferences

1. **X. Zhang**, D. Okamoto, T. Hatakeyama, M. Sometani, S. Harada, R. Kosugi, N. Iwamuro, and H. Yano, "A Distributed Model for Near-Interface Traps in 4H-SiC MOS Capacitors", in 47th IEEE Semiconductor Interface Specialists Conference (*SISC*), 11.15, 2016.
2. **X. Zhang**, D. Okamoto, T. Hatakeyama, M. Sometani, S. Harada, N. Iwamuro, and H. Yano, "Impact of oxide thickness on the density distribution of near-interface traps in 4H-SiC MOS capacitors", in Proceedings of International Workshop on Dielectric Thin Films for Future Electron Devices (*IWDTF*), 150–151, 2017.
3. Y. Karamoto, **X. Zhang**, D. Okamoto, M. Sometani, T. Hatakeyama, S. Harada, N. Iwamuro, and H. Yano, "Analysis of fast and slow responses of interface traps in p-type SiC MOS capacitors by conductance method", in Proceedings of International Workshop on Dielectric Thin Films for Future Electron Devices (*IWDTF*), 146–147, 2017.

C. Presentations at domestic conferences

1. **X. Zhang**, D. Okamoto, T. Hatakeyama, M. Sometani, S. Harada, R. Kosugi, N. Iwamuro, and H. Yano, "A Distributed Model for Near-Interface Traps in 4H-SiC MOS Capacitors", Ext. Abstr. 77th Autumn Meet. Japan Society of Applied Physics, 2016, 16a-C302-10.
2. D. Okamoto**, X. Zhang**, T. Hatakeyama, M. Sometani, S. Harada, R. Kosugi, N. Iwamuro, and H. Yano, "Analysis of SiC MOS interface by impedance measurements considering series resistance", Ext. Abstr. 77th Autumn Meet. Japan Society of Applied Physics, 2016, 16a-C302-9.
3. **X. Zhang**, D. Okamoto, T. Hatakeyama, M. Sometani, S. Harada, R. Kosugi, N. Iwamuro, and H. Yano, "Quantitative Estimation of Near-Interface Traps with Distributed Circuit Model for 4H-SiC MOS Capacitors", the 3rd Meeting on Advanced Power Semiconductors, 2016, P-97.
4. **X. Zhang**, D. Okamoto, T. Hatakeyama, M. Sometani, S. Harada, R. Kosugi, N. Iwamuro, and H. Yano, "Verification of Modified Distributed Circuit Model for Near-Interface Traps in 4H-SiC

MOS Interface", Ext. Abstr. 22nd Symposium on Electron Device Interface Technology (*EDIT*), 199–202, 2017.

5. **X. Zhang**, D. Okamoto, T. Hatakeyama, M. Sometani, S. Harada, R. Kosugi, N. Iwamuro, and H. Yano, "Verification of density distribution of near-interface traps in 4H-SiC MOS capacitors with different oxide thicknesses", Ext. Abstr. 78th Autumn Meet. Japan Society of Applied Physics, 2017, 5a-A203-5.
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