Investigation of short-circuit failure mechanisms of SiC MOSFETs by varying DC bus voltage

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Abstract

In this study, the experimental evaluation and numerical analysis of short-circuit mechanisms of 1200 V SiC planar and trench MOSFETs were conducted at various DC bus voltages from 400 to 800 V. Investigation of the impact of DC bus voltage on short-circuit capability yielded results that are extremely useful for many existing power electronics applications. Three failure mechanisms were identified in this study: thermal runaway, MOS channel current following device turn-off, and rupture of the gate oxide layer (gate oxide layer damage). The SiC MOSFETs experienced lattice temperatures exceeding 1000 K during the short-circuit transient; as Si insulated gate bipolar transistors (IGBTs) are not typically subject to such temperatures, the MOSFETs experienced distinct failure modes, and the mode experienced was significantly influenced by the DC bus voltage. In conclusion, suggestions regarding the SiC MOSFET design and operation methods that would enhance device robustness are proposed.

1. Introduction

Owing to their wide band gap and higher thermal capability,[1, 2] silicon carbide (SiC) power metal oxide semiconductor field effect transistors (MOSFETs), which typically have lower on-resistances and switching losses for a given blocking voltage, are expected to replace silicon (Si) - insulated gate bipolar transistors (IGBTs) in many application areas, such as electric vehicles (EVs), plug-in hybrid vehicles (PHEVs), and traction. As such applications have strict requirements for systemwide stability, it is essential to explore optimized structures and operations for SiC MOSFETs to facilitate the future development of SiC MOSFETs with greatly enhanced robustness.

There is a particularly strict requirement for SiC MOSFETs to be capable of withstanding the high-current flow that occurs during a short-circuit state, such as a ground fault or a load short circuit, while supporting high voltage being applied to the drain electrode. This “withstand capability”, under simultaneous application of high current and high voltage during short-circuit states, is referred to as the short-circuit safe operating area (SCSOA). The SCSOAs of SiC MOSFETs have already been evaluated, using experimental and simulation methods, in many studies[3-23], and some explanations of the internal physical mechanisms responsible for the devices’ short-circuit failures have been proposed. Thermal runaway is a well-known short-circuit failure mechanism of SiC MOSFETs as well as Si IGBTs.[3, 4] It has been reported that, in addition to thermal runaway, there are other failure modes during the short-circuit state, such as increased gate leakage current and gate oxide rupture.[5-8] For example, SiC planar and trench MOSFETs with thin gate oxide layers experience high electric fields (2-3 MV/cm) and temperatures (> 1700 K), leading to a breakdown of the gate oxide layer.[9, 10] Unlike in Si IGBTs, lattice temperatures in SiC MOSFETs have been reported to exceed 1000 K during the short-circuit transient without device failure.[4] SiC MOSFETs can withstand such temperatures because, under short-circuit condition, the applied electric field and the current density in their n-drift region can exceed 2.0 MV/cm and 1000 A/cm^2, respectively, which are much higher than those of Si IGBTs.

Therefore, excessive gate leakage current and oxide layer rupture, which have not been reported as Si IGBT failure mechanisms, appear to be the causes of short-circuit failure in SiC MOSFETs.[5-10] Another SiC MOSFET failure mode that has been reported is the

melting of surface metallization during the short-circuit transient.[11, 12] In addition, under unclamped inductive switching (UIS) conditions, a SiC MOSFET was reported to be destroyed by the MOS channel current, even after device turn-off.[24]

DC input voltage is frequently altered in order to control the output AC voltage (and thereby the motor speed) in many existing inverter system[25], particularly in EV / PHEV applications; thus, it is important to note that the investigations in this study are extremely relevant to existing SiC MOSFET applications. According to Ref. 26, SiC planar MOSFETs have two failure mechanisms at different DC bus voltages. In this study, we conducted a precise experimental and numerical investigation of SiC planar and trench MOSFET failure mechanisms during the short-circuit state by varying the DC bus voltage and negative gate voltage, and examined which failure mode occurred at each DC bus voltage.

2. Experimental and simulated methods

SiC MOSFETs of two commercially available designs, one with a planar structure and the other a trench gate structure, were measured and analyzed, with their schematic cross sections shown in Fig. 1. The trench device is SCT3030AL (rated 650 V / 70 A)[27] and the planar one is C2M0160120D (rated 1200 V / 19 A).[28] The trench MOSFET was designed with deep p+ regions in order to reduce the electric field at the trench bottom when a high drain-to-source voltage is applied.[29] In the planar MOSFET, the thickness of the n-drift layer was 10 μm, and the doping concentration was of 6.0×10^{15} cm^{-3}. In the trench MOSFET, the thickness of the n-drift layer was 8 μm, and the doping concentration was 7.5×10^{15} cm^{-3}. The gate oxide thickness was 50 nm in both devices. The off- and on-state characteristics of the devices are shown in Fig. 2. At room temperature, the breakdown voltage and specific on-resistance (R_{ON}・A) of the planar MOSFET were 1670 V [with a drain current (I_d) of 1 mA] and 4.4 mΩ cm^2 [gate-to-source voltage (V_{gs}) of 20 V], respectively. The corresponding values for the trench MOSFET were 1270 V (I_d of 1 mA) and 3.3 mΩ cm^2 (V_{gs} of 20 V), respectively. Although the rated voltage of the SiC trench MOSFET is 650 V, the breakdown voltage of the device is over 1200 V. Therefore, both devices can be considered 1200 V SiC MOSFETs. The active area of the planar MOSFET was 3.09 mm^2, and that of the trench MOSFET was 9.18 mm^2. The gate threshold voltages

were 2.5 V for the planar MOSFET and 4.7 V for the trench MOSFET at room temperature. The gate threshold voltage was defined as the gate voltage when the drain current was at one-thousandth of the rated current at an applied drain-to-source voltage of 10 V.

Figure 3 shows the experimental setup for the short-circuit test and a diagram of the equivalent circuit. A DC power supply (V_{dd}) with a maximum DC voltage of 800 V was used. According to Ref. 10, a high drain surge voltage in a MOSFET after device turn-off can trigger an avalanche failure. Therefore, in this study, a gate resistor providing a relatively high gate resistance (R_g) of 47 Ω was connected to the gate electrode when measurements were taken. In this paper, SCSOA measurements were performed at room temperature, while varying the voltage from 400 to 800 V, in order to investigate the failure mechanisms described above.

The calculated device structures of planar and trench MOSFETs were modeled to meet the current-voltage characteristics of I_d-V_{gs} and I_d-V_{ds} curves of the measured devices mentioned above. Figure 4 shows the comparison of I_d-V_{gs} and I_d-V_{ds} curves of the simulated results, measured results, and published results in a datasheet [27]. Since there is no equipment that can measure a static drain current of more than 20 A in our laboratory, the calculated device structures were also modeled in the higher drain current region using data published in the datasheet as shown in Fig. 4 (c).

3. Results and discussion

3.1 Short-circuit capability at high DC bus voltage (800 V)

A DC bus voltage of 800 V is very high, corresponding to roughly 48 and 63% of the breakdown voltages of the planar and trench MOSFETs in this study, respectively; thus, extremely high drain currents were generated in the devices, resulting in a severe power dissipation during the short-circuit state, continuing until the short-circuit condition ended. On the basis of the feedback to the MOSFET control circuit, many of the MOSFETs used in existing power electronics applications will successfully turn off, when experiencing short-circuit conditions, before the device undergoes destructive failure. At a DC bus voltage of 800 V, this shut down must occur within roughly 10 μs, which is the standard requirement for 1200 V Si IGBT devices.[30]

Figure 5 shows the measured short-circuit current and voltage waveforms of the SiC

planar and trench MOSFETs. For these measurements, the gate voltages were set at +18 to -5 V for the planar MOSFET, and +15 to -4 V for the trench MOSFET. The negative gate biases are set to the recommended values written in the datasheets. Our dynamic measurement hardware cannot measure currents of more than 300 A. The drain current of SiC trench MOSFETs exceeded 300 A with a positive gate bias of 18 V. Owing to the need to reduce the drain current, the positive gate bias was set to 15 V in the SiC trench MOSFETs. Both devices were configured to enter a short-circuit state in response to the gate turn-on signal. Energy dissipation during the short-circuit state is described by

$$E_{\mathrm{SC}} = \int_0^{t_{\mathrm{SC}}} V_{\mathrm{ds}} I_{\mathrm{d}} dt \ , \qquad (1)$$

where E_{SC} is the short-circuit energy dissipated during the short-circuit state, t_{SC} is the short-circuit time, V_{ds} is the drain-to-source voltage, and I_{d} is the drain current. In devices with the same rated current, the dies of SiC MOSFETs are typically designed to be smaller than those of Si IGBTs, owing to the lower on-resistances of SiC MOSFETs. In the present study, immense short-circuit power dissipation occurred in the SiC MOSFETs owing to the simultaneous presence of high voltage and current density; as t_{SC} increases, the inner temperature of these devices increases rapidly, eventually resulting in device failure. In this study, the critical period of time from the beginning of short-circuit conditions until device turn-off (due to the gate turning off) is defined as the short-circuit capability, $t_{\mathrm{SC_CR}}$.

The measured $t_{\mathrm{SC_CR}}$ values were 5.8 and 5.7 μs and the measured E_{SC} values were 10.4 and 9.9 J/cm^2 for the SiC planar and trench MOSFETs, respectively. At device turn-off, the device failures had not occurred; however, at 2.6 and 4.0 μs after device turn-off, for the planar and trench MOSFETs, respectively, delayed failures were observed. In addition, an increased leakage current appeared as a tail current after device turn-off, despite the fact that such a tail current should not be present in unipolar devices. The tail current occurred primarily because the combination of high voltage and increased hole current generated a severe power dissipation in the device, despite the short-circuit conditions no longer being present. If the dissipated power exceeds the power being transferred away from the device, the hole current will further increase and temperatures will increase, leading to a positive feedback process known as thermal runaway.[3)]

In order to better investigate the interior of the SiC planar and trench MOSFETs, a two-dimensional electrothermal mixed-mode device simulation was conducted. The simulated SiC planar and trench MOSFETs were designed on the basis of the current-voltage characteristics of the devices and data from Refs. 26 and 29, with simulations performed under the same conditions as those of the aforementioned measurements of the actual devices. Figures 6 and 7 show the simulated drain current and maximum temperature waveforms, hole densities, and temperature distributions for the SiC planar and trench MOSFETs during the short-circuit transient. It was revealed that the highest-temperature region was initially and principally located in the n-drift layer, spreading to the device surface over time. As shown in Fig. 7(d), the simulated lattice temperature and hole density in the n-drift layer increased with the short-circuit time, reaching roughly 1700 K and 4.5×10^{11} cm^{-3}, respectively, immediately after the gate voltage was turned off. As a result, the generated hole current passing through the p-well layer underneath the n+ source region increased, enabling the activation of the parasitic npn bipolar junction transistor (as shown in Fig. 8), and finally, the device failed. From these simulated results, the time delay between MOSFET turn-off and actual device failure (shown in Fig. 6) corresponds to the time required for heat to generate in the n-drift region and diffuse to the p-well/n+ source junction in the parasitic npn transistor, and finally, for activating this transistor. This positive feedback loop is the SiC MOSFET failure mechanism known as thermal runaway, which occurs almost identically in Si IGBTs.[30, 31]

Figure 9 shows a top view of one of the SiC trench MOSFETs after a short-circuit test at a DC bus voltage of 800 V. It is clear that the source electrode near the bonding wires melted as a result of a sudden marked increase in drain current immediately after the aforementioned activation of the parasitic npn transistor. Table I shows the measured resistances between three terminals (R_{gs}, R_{gd}, and R_{ds}) of the failed SiC planar and trench MOSFETs after the short-circuit test. It is apparent that the extremely low resistances between the electrodes resulted in all of them becoming completely shorted.

In Fig. 7(d), it can be seen that the simulated lattice temperature in the MOS channel region became extremely high (roughly 1500 K); as a result, the SiC MOSFET could not turn off completely, even after gate turn-off owing to the reduction in the gate threshold voltage. This is similar to the aforementioned scenario reported by Fayyaz *et al*., in which

a SiC MOSFET was destroyed by the MOS channel current during the UIS transient.[24)] Figure 10 shows the measured short-circuit waveforms of the SiC trench MOSFET when the negative gate voltage (V_{gs_off}) was set to higher than -10 V. It is clear that there was minimal improvement in t_{SC_CR}, and the current and voltage waveforms were almost identical to those shown in Fig. 5(b); thus, the electron current flowing through the MOS channel after device turn-off was not the primary cause of device failure under the specified conditions.

As seen in the measured waveforms shown in Fig. 5, the gate voltages in both types of MOSFET decreased gradually as the short-circuit transient increased. This change in the gate voltage ΔV_{gs} was caused by gate oxide degradation caused by an increase in gate leakage current due to high gate electric field and lattice temperature. This gate leakage current, which is caused by Fowler-Nordheim tunneling and Poole-Frenkel emission,[32, 33)] increased as a result of the higher temperature, resulting in damage to the gate oxide layer. Note that this damage to the gate oxide layer was encountered during the gate turn-on (V_{gs_on}) period. Figure 11 shows the measured short-circuit waveforms of the trench MOSFET at a reduced V_{gs_on} of 12 V. It can be seen that ΔV_{gs} becomes lower than 0.8 V, indicating that the gate leakage current was successfully reduced. However, the values of E_{SC} remain almost identical (9.9 J/cm^2 at a V_{gs_on} of 15 V, and 10.0 J/cm^2 at a V_{gs_on} of 12 V). These results indicate that neither increased gate leakage current nor gate oxide rupture was the principal cause of device failure under the specified conditions.

Therefore, at the high DC bus voltage of 800 V, the SiC MOSFETs failed owing to the activation of their npn transistors induced by a thermally generated hole current in the n-drift layer. Moreover, there was no significant difference in the failure modes of the planar and trench MOSFETs.

3.2 Short-circuit capability at medium DC bus voltage (600 V)

In order to evaluate the effect of reducing the concentration of thermally generated holes produced by a high electric field in the n-drift layer, V_{dd} was set to the lower DC bus voltage of 600 V, corresponding to roughly 36 and 47% of the breakdown voltages of the planar and trench MOSFETs, respectively. Figure 12 shows the measured short-circuit current and voltage waveforms for the two types of MOSFET. For these measurements, the

gate voltages were set from +18 to -5 V in the planar devices and from +15 to -4 V in the trench devices. The t_{SC_CR} values were 9.0 and 8.6 μs and the E_{SC} values were 12.4 and 10.3 J/cm^2 for the planar and trench MOSFETs, respectively. As can be seen in Fig. 12, the currents increased suddenly in the planar MOSFET when device failure occurred, and these failures resemble the thermal runaway process described in Sect. 3.1. However, the sudden increase in drain current ended abruptly in the trench MOSFETs. Device failure was characterized by a collapse in the gate voltage waveform from -4 to -3.4 V in the trench MOSFET. The obtained results differed between the planar and trench MOSFETs at a DC bus voltage of 600 V. As with the results at a DC bus voltage of 800 V, the E_{SC} of the planar MOSFET was greater than that of the trench MOSFET. It is assumed that the higher breakdown voltage of the planar MOSFET (roughly 31%) was due to a lower electric field in the n-drift layer, which reduced power dissipation in the n-drift layer during the short-circuit transient, resulting in the greater E_{SC} of the planar MOSFET.

From Fig. 12(a), the drain current kept flowing after device turn-off. It was suggested that the planar MOSFET cannot be turned off completely even after gate turn-off because of the high temperature (as described in the previous section). The planar MOSFET has a lower threshold voltage (2.5 V) than the trench MOSFET (4.7 V). A device with a lower threshold voltage is easy to operate during normally-on operation, but the trench MOSFET is not easy to operate during normally-on operation owing to its higher threshold voltage.

Figure 13 shows the measured short-circuit current and voltage waveforms at an increased V_{gs_off} of -10 V in the planar MOSFET and at the decreased V_{gs_off} of 0 V in the trench devices. Unlike the results in Fig. 12, it can be clearly seen that the current and voltage waveforms were markedly different whereas t_{SC_CR} was almost independent of V_{gs_off}. As V_{gs_off} was set at an increased value of -10 V, the sudden increase in drain current ended abruptly in the planar MOSFET. Device failure was characterized by a collapse in the gate voltage waveform from -10 to -5 V in the planar MOSFET. On the other hand, in the trench MOSFET, the drain current increased immediately after device turn-off.

Figure 14 shows the simulated short-circuit current and temperature waveforms at the higher and lower V_{gs_off} values in the planar and trench devices, respectively. There is no significant difference in the current and temperature waveforms until the device turn-off at each V_{gs_off}. After the device turn-off, the drain current kept flowing at the lower V_{gs_off} in

both devices. Therefore, it is found that the devices failed because of the thermal runaway triggered by a normally-on mechanism at the lower V_{gs_off} owing to the reduced threshold voltage.

Tables II and III show the measured resistances between three terminals of the failed devices (R_{gs}, R_{gd}, and R_{ds}), with and without increased negative gate bias. It can be seen from these results that the resistance between the gate and source electrodes became extremely low, while the blocking characteristics between the drain and source terminals were not altered with increasing V_{gs_off}, indicating that device failure occurred in the gate oxide layer. Figure 15 shows a top view of the surface of a failed trench MOSFET shown in Fig. 12(b), revealing that the metal layers on the gate and source electrodes were completely undamaged. It is believed that, at the lower negative gate voltage, even when the device was turned off, the MOS channel current kept flowing, and that this channel current triggered device failure. Therefore, by increasing the negative gate voltage, the MOS channel current was successfully stopped, or at least reduced considerably; thus the drain current and gate voltage waveforms were completely changed after device turn-off.

Note that the measured gate threshold voltage of the planar MOSFET was 2.5 V, which was 2.2 V lower than that of the trench MOSFET; thus, in the planar MOSFETs, device failure due to the MOS channel current could be avoided with a higher V_{gs_off} setting. An increased V_{gs_off} and/or a higher gate threshold voltage could be used to effectively prevent certain short-circuit failures by reducing the probability of generating a MOS channel current induced by an increased lattice temperature.

3.3 Short-circuit capability at low DC bus voltage (400 V)

Further investigation of the effect of DC bus voltage on short-circuit capability was conducted by carrying out short-circuit tests at a DC bus voltage of 400 V, corresponding to small percentages of the MOSFET breakdown voltages, roughly 24 and 31% for the planar and trench MOSFETs, respectively. Figure 16 shows the measured short-circuit current and voltage waveforms of the SiC planar and trench MOSFETs. The gate voltages were set from +18 to -5 V in the planar devices and from +15 to -4 V in the trench devices. The t_{SC_CR} values were 19.5 and 20.4 μs and the E_{SC} values were 13.5 and 12.1 J/cm^2 in the planar and trench MOSFETs, respectively. Device failure can be recognized by the

collapse in the gate voltage waveform from -5 to -4.4 V at 6.0 μs after device turn-off (planar MOSFET) and from -4 to -2.8 V at 4.3 μs after device turn-off (trench MOSFET). No significant differences between the failure mechanisms of the respective devices could be seen. Furthermore, unlike the results at 800 V, the drain current did not increase at all, and a tail current could hardly be detected. As no tail current was seen after the devices were turned off, it is clear that there were few thermally generated holes in either of the SiC MOSFETs. Table IV shows the measured resistances between three terminals of the failed SiC planar and trench MOSFET (R_{gs}, R_{gd}, and R_{ds}). The resistance between the gate and source electrodes became very low, whereas the blocking characteristics between the drain and source terminals were not altered, indicating that device failure was due to damage of the gate oxide layer, similarly to the events described in Sect. 3.2 (which occurred under higher negative gate bias conditions at V_{dd} of 600 V). As device failure occurred in the gate oxide layer, the metal layers on the gate and source electrodes were completely undamaged, as shown in Fig. 17.

Figure 18 shows the simulated electric field and temperature distribution during the short-circuit state, at a V_{dd} of 400V. During the short-circuit transient, a high electric field of 2.5 MV/cm and a lattice temperature of 1550 K occurred in the gate oxide layer near the n+ source and p well; as a result, the gate leakage current induced by Fowler-Nordheim tunneling and Poole-Frenkel emission began to increase owing to increasing temperature (as discussed in Sect. 3.1), resulting in damage to the gate oxide layer. Gate leakage currents estimated using $\Delta V_{gs}/R_g$ from Fig. 17 are 36 and 21 mA in the planar and trench MOSFETs, respectively. As can be clearly seen in Fig. 19, t_{SC_CR} and E_{SC} degraded rapidly with increasing V_{gs_on}.

These results suggest that a moderately thick gate oxide layer is suitable for improving short-circuit capability in the low DC voltage range, even though SiC MOSFETs typically have lower surface channel mobility characteristics than their Si counterparts. In addition, as the gate oxide layer simultaneously experienced high electric field and lattice temperature at the same time during the period of V_{gs_on}, some of the electric-field-shielding structures of the SiC trench MOSFET were ineffective in preventing failure owing to the rupture of the gate oxide layer.

4. Conclusions

The short-circuit failure mechanisms of 1200 V planar and trench SiC MOSFETs were precisely investigated using experimental and numerical methods. Three SiC MOSFET failure mechanisms were identified: thermal runaway, MOS channel current, and damage of the gate oxide layer. Furthermore, it was revealed that the DC bus voltage significantly determined which failure mechanism occurred.

At the high DC bus voltage of 800 V, the MOSFETs failed owing to thermal runaway (i.e., a thermally generated hole current activated the parasitic npn transistor, ultimately causing device failure). This failure mechanism also occurs in Si IGBTs in an almost identical manner.

Short-circuit failure mechanisms were also investigated at the medium DC bus voltage of 600 V. On the basis of simulation results showing a higher lattice temperature near the channel region, and the measured short-circuit waveforms at an increased V_{gs_off}, it was concluded that a MOS channel current caused the SiC MOSFETs to fail after the gate was turned off.

At the low DC bus voltage of 400 V, the SiC MOSFETs failed owing to damage of the gate oxide layer caused by damage to the layer resulting from the simultaneous occurrence of high electric field and high lattice temperature during the period of V_{gs_on}. As no tail current was seen after device turn-off, it was clear that there were few thermally generated holes in the MOSFETs, suggesting that some of the electric-field-shielding structures in the SiC trench MOSFETs were not effective in preventing this failure mechanism.

Finally, note that there was no significant difference in the failure mechanisms experienced by the planar and trench MOSFETs under equivalent DC bus voltage conditions.

It was further revealed that, unlike Si IGBTs, SiC MOSFETs could be destroyed by the MOS channel current flow and damage the gate oxide layer (as detailed in Sects. 3.2 and 3.3). This is primarily because the SiC material is characterized by a wide band gap; thus thermal runaway does not occur easily, especially under low- and medium-DC voltage conditions. Therefore, the SiC MOSFET design and operation methods incorporating an optimal combination of a moderately thick gate oxide layer increased gate threshold voltage, and/or the use of a significant negative gate voltage would be effective in

enhancing short-circuit capability in the low- and medium-DC voltage ranges.

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Figure Captions

Fig. 1. (Color online) Schematic cross section of the planar and trench MOSFETs investigated in this study. In the trench MOSFET, deep p+ regions are implemented to reduce the electric field at the trench bottom.

Fig. 2. (Color online) Measured (a) output current-voltage waveforms and (b) breakdown characteristics of the SiC planar and trench MOSFETs.

Fig. 3. (Color online) (a) Short-circuit measurement hardware and (b) diagram of the equivalent circuit, at drain voltages from 400 to 800 V. The gate resistance was set at 47 Ω.

Fig. 4. (Color online) Typical measured and simulated (a) I_d-V_{gs} waveforms of the SiC planar MOSFET and (b) I_d-V_{ds} waveform of the trench ones. Simulated and published I_d-V_{ds} results in datasheet [27] are also shown in (c).

Fig. 5. (Color online) Measured short-circuit waveforms of the (a) planar and (b) trench MOSFETs at a DC bus voltage of 800 V. Turn on- and turn off-gate voltages were set from (a) +18 to -5 V and (b) +15 to -4 V.

Fig. 6. (Color online) Simulated drain current and maximum temperature in the SiC (a) planar and (b) trench MOSFETs at a DC bus voltage of 800 V and gate voltages from +15 to -4 V.

Fig. 7. (Color online) Simulated results for (i) hole density and (ii) temperature distribution in the SiC planar and trench MOSFETs at a DC bus voltage of 800 V and V_{gs} from +18 to -5 V and V_{gs} from +15 to -4 V, respectively, during the short-circuit transient. Graphics (a) - (d) correspond to the points shown in Fig. 5.

Fig. 8. (Color online) Simulated total current density distribution of the SiC planar and trench MOSFETs at point (e) in Fig. 5. The parasitic npn transistor was activated.

Fig. 9. (Color online) A top view of one of the SiC trench MOSFETs following a short-circuit failure. The DC bus voltage was 800 V and V_{gs} values were from +15 to -4 V.

Fig. 10. (Color online) Measured short-circuit waveforms of the SiC trench MOSFET at a DC bus voltage of 800 V and gate voltages from +15 to -10 V.

Fig. 11. (Color online) Measured short-circuit waveforms of the SiC trench MOSFET at a DC bus voltage of 800 V and gate voltages from +12 to -4 V.

Fig. 12. (Color online) Measured short-circuit waveforms for the (a) planar and (b) trench MOSFETs at a DC bus voltage of 600 V. The on- and off-gate voltages were set at (a) +18 to -5 V and (b) +15 to -4 V.

Fig. 13. (Color online) Measured short-circuit waveforms for the (a) planar and (b) trench MOSFETs at a DC bus voltage of 600 V. The on- and off-gate voltages were set at (a) +18 to -10 V and (b) +15 to 0 V. The sudden increase in drain current ends abruptly in both the planar and trench MOSFETs.

Fig. 14. (Color online) Simulated drain current and temperature waveforms, with a DC bus voltage of 600 and V_{gs_off} set at -5, -10 and 0 V, -4 in the (a) SiC planar and (b) trench MOSFETs, respectively.

Fig. 15. Top view of one of the SiC trench MOSFETs following a short-circuit failure. The DC bus voltage was set at 600 V and V_{gs} was +15 to -4 V.

Fig. 16. (Color online) Measured short-circuit waveforms for the (a) planar and (b) trench MOSFETs at a DC bus voltage of 400 V. The on- and off-gate voltages were set from (a) +18 to -5 V and (b) +15 to -4 V.

Fig. 17. Top view of one of the SiC trench MOSFETs following a short-circuit failure. The DC bus voltage was set at 400 V and V_{gs} was from +15 to -4 V.

Fig. 18. (Color online) Simulated (a) electric field and (b) lattice temperature distribution in SiC planar and trench MOSFETs immediately before device turn-off. The DC bus voltage was at 400 V and $V_{\mathrm{gs_on}}$ was set at +18 and +15 V.

Fig. 19. (Color online) Measured results of the correlations between $V_{\mathrm{gs_on}}$ and (a) $t_{\mathrm{SC_CR}}$, (b) E_{SC} in SiC planar and trench MOSFETs at the DC bus voltage at 400 V.

Table I. Resistances between gate and source (R_{gs}), gate and drain (R_{gd}), and drain and source (R_{ds}) of the SiC planar and trench MOSFETs after a short-circuit test at 800 V and V_{gs_on} / V_{gs_off} = +18 V / -5 V and +15 V / -4 V.

	Planar resistance (Ω)	Trench resistance (Ω)
R_{gs}	0.5	12.5
R_{gd}	0.5	13.1
R_{ds}	0.5	0.8

Table II. Resistances between gate and source (R_{gs}), gate and drain (R_{gd}), and drain and source (R_{ds}) of the SiC planar MOSFET after a short-circuit test at 600 V.

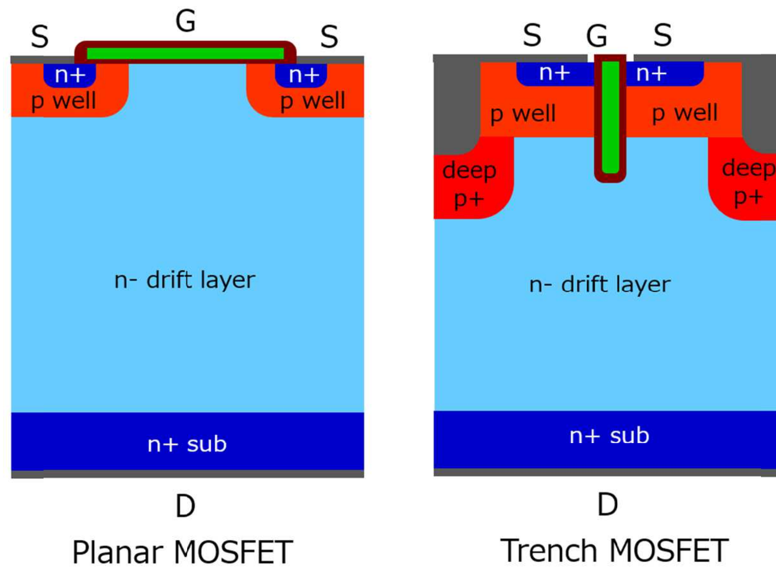
	Resistance (Ω) V_{gs_on} / V_{gs_off} = +18 V / -5 V	Resistance (Ω) V_{gs_on} / V_{gs_off} = +18 V / -10 V
R_{gs}	4.1	44.3
R_{gd}	4.0	30 M
R_{ds}	0.2	∞

Table III. Resistances between gate and source (R_{gs}), gate and drain (R_{gd}), and drain and source (R_{ds}) of the SiC trench MOSFET after a short-circuit test at 600 V.

	Resistance (Ω) V_{gs_on} / V_{gs_off} = +15 V / 0 V	Resistance (Ω) V_{gs_on} / V_{gs_off} = +15 V / -4 V
R_{gs}	2.7	4.1 k
R_{gd}	4.2	14 M
R_{ds}	1.4	∞

Table IV. Resistances between gate and source (R_{gs}), gate and drain (R_{gd}), and drain and source (R_{ds}) of the SiC planar and trench MOSFET after a short-circuit test at 400 V and V_{gs_on} / V_{gs_off} = +18 V / -5 V and +15 V / -4 V.

	Planar resistance (Ω)	Trench resistance (Ω)
R_{gs}	209	619
R_{gd}	3.2 M	0.8 M
R_{ds}	∞	3.7 M



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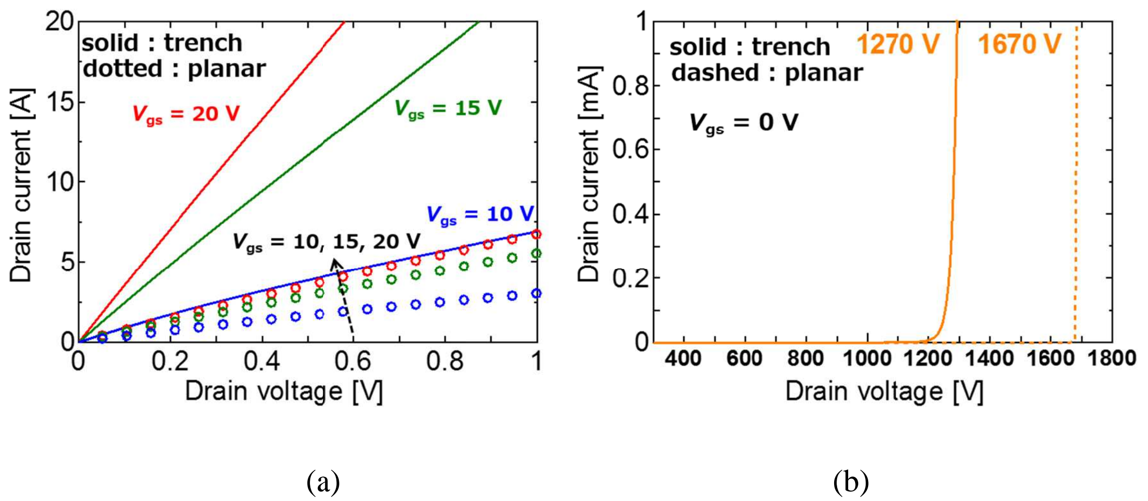

(a) (b)

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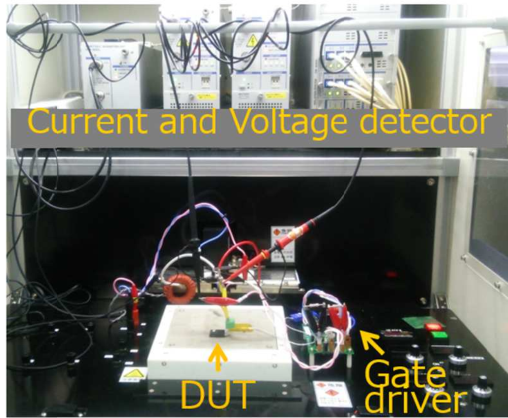

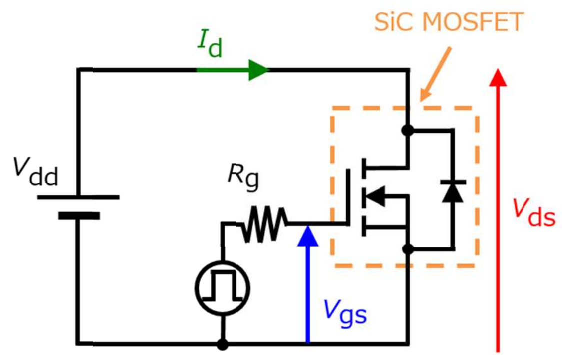

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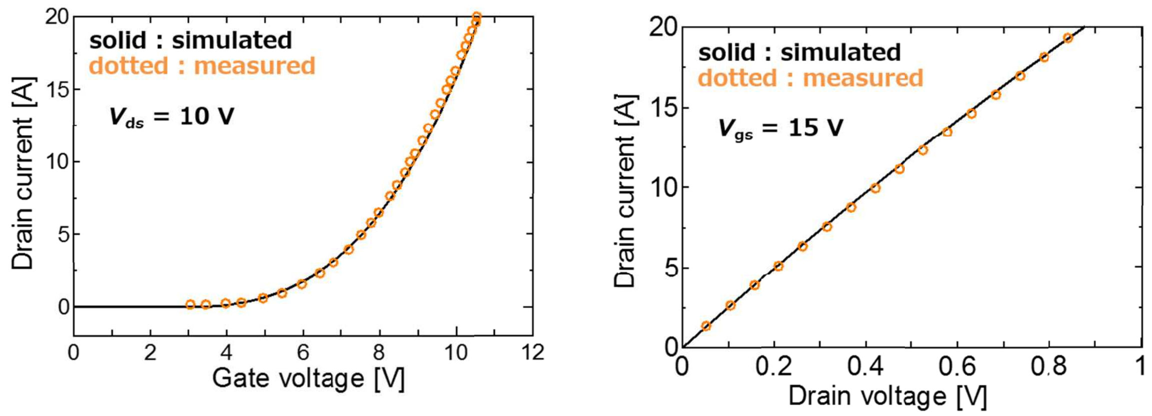

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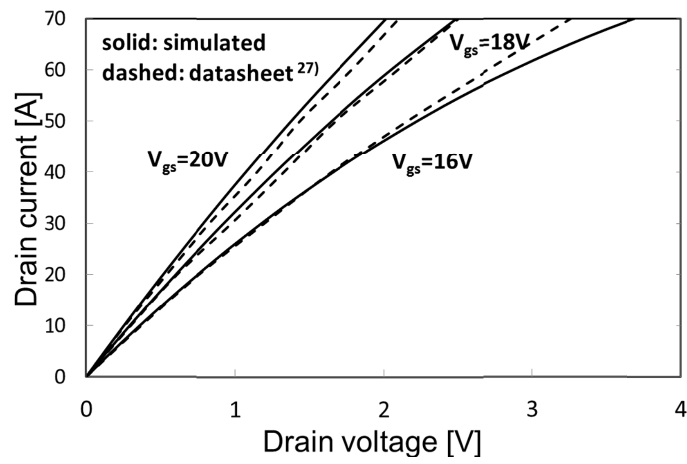

(c)

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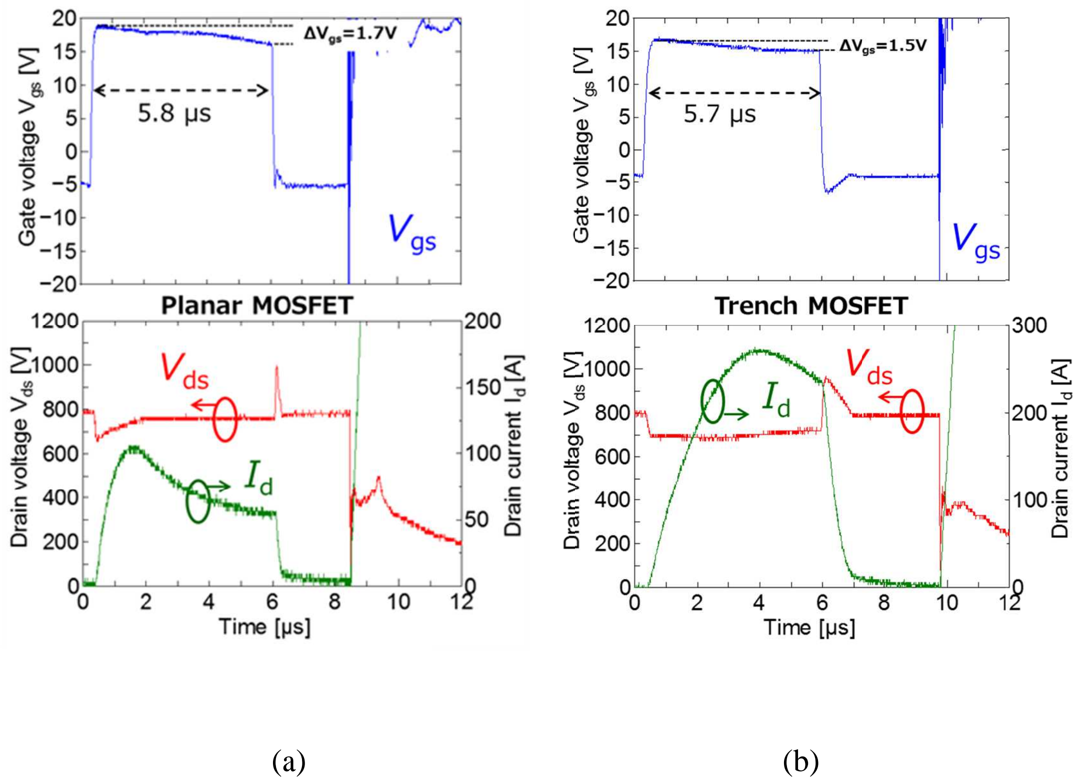

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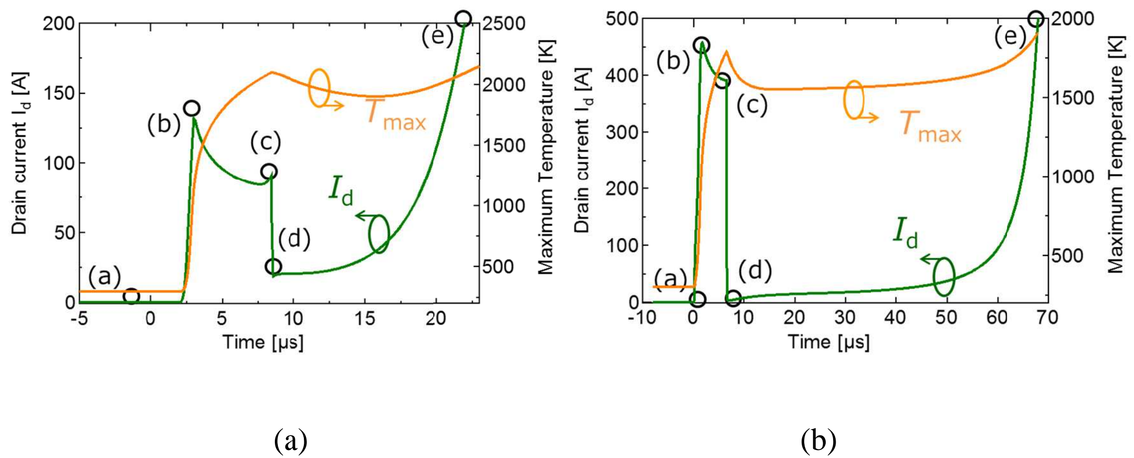

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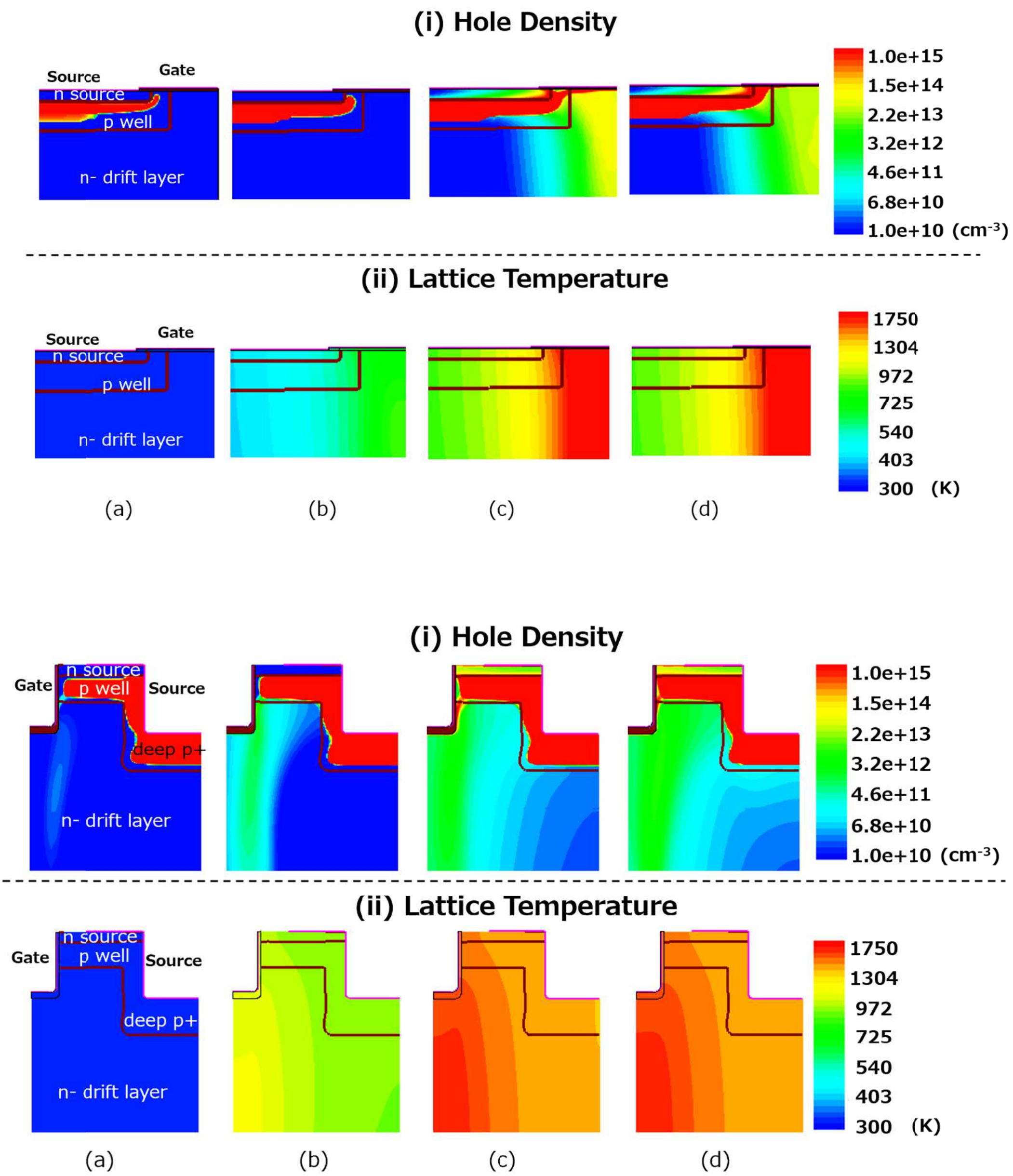

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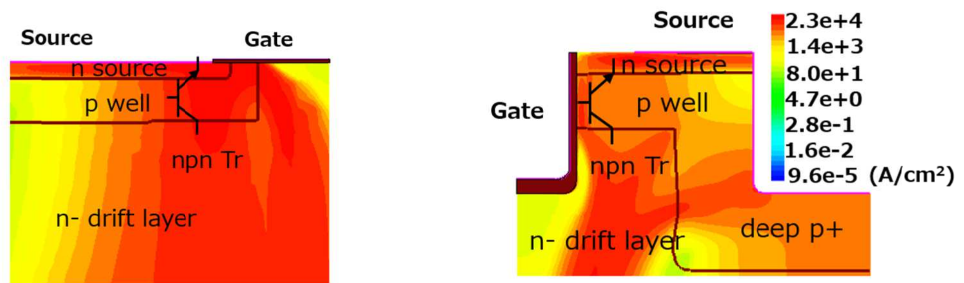

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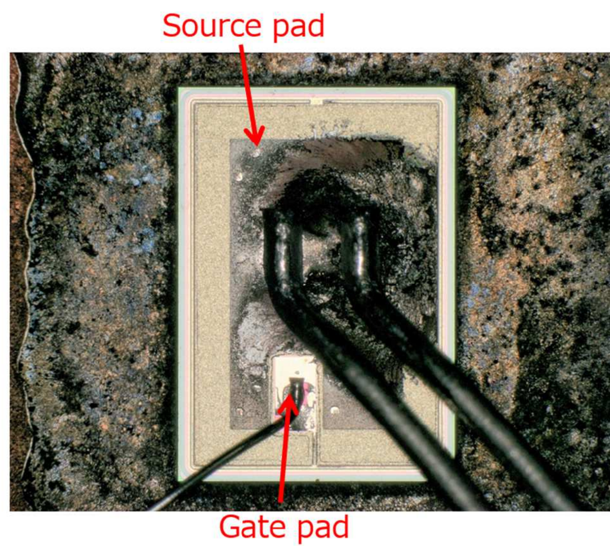

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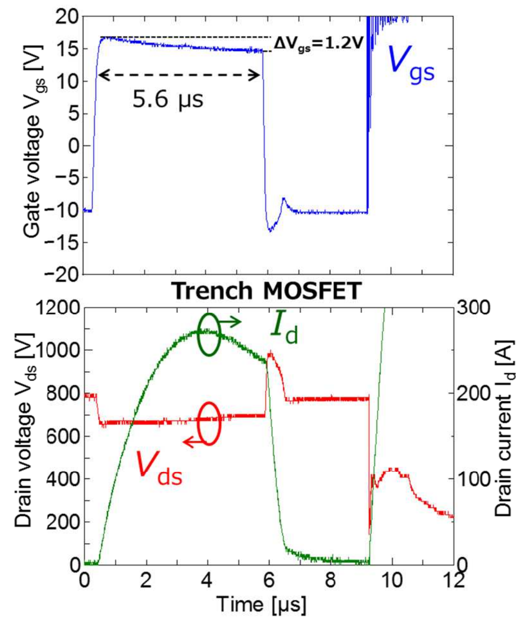

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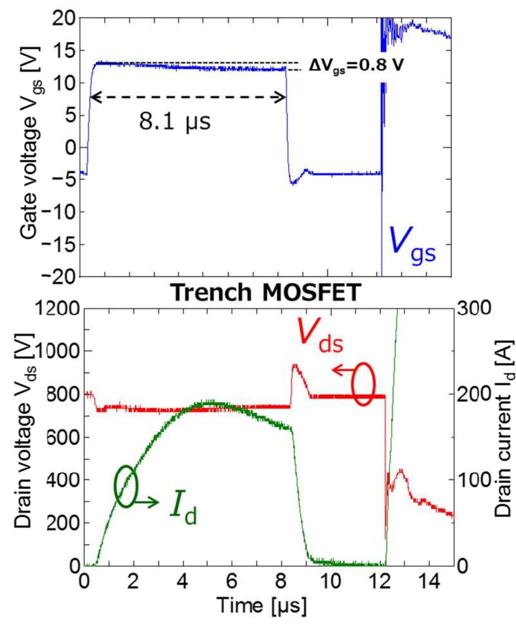

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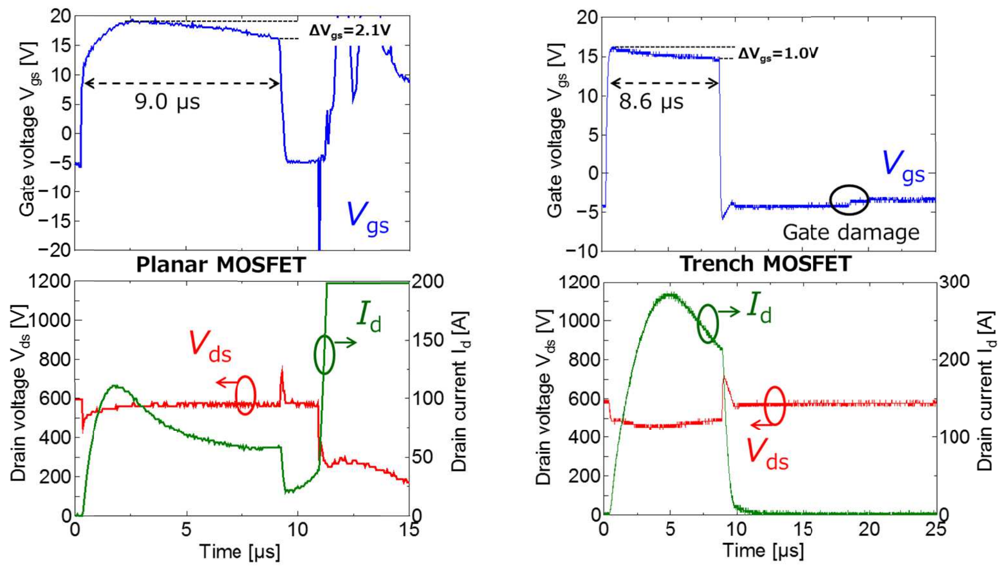

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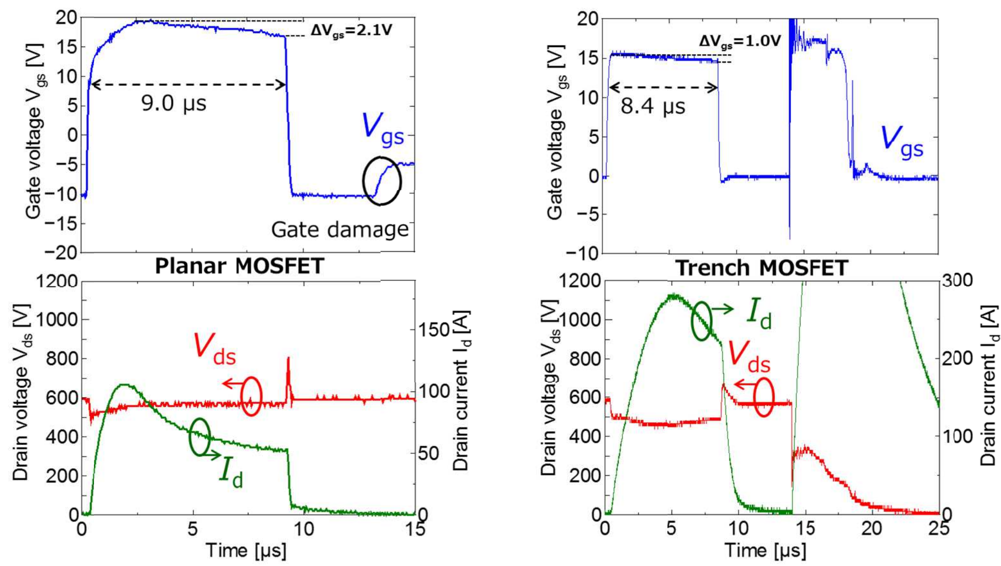

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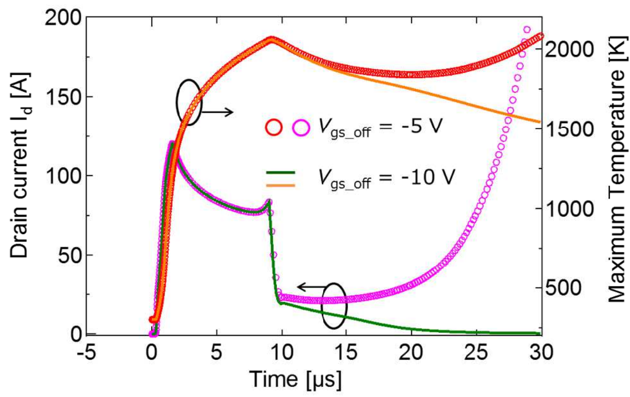

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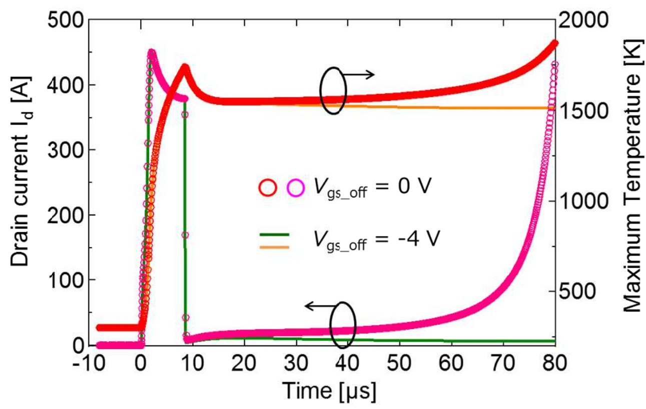

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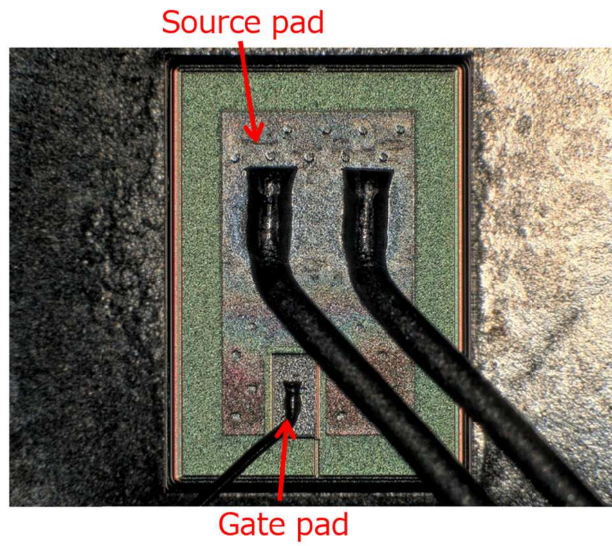

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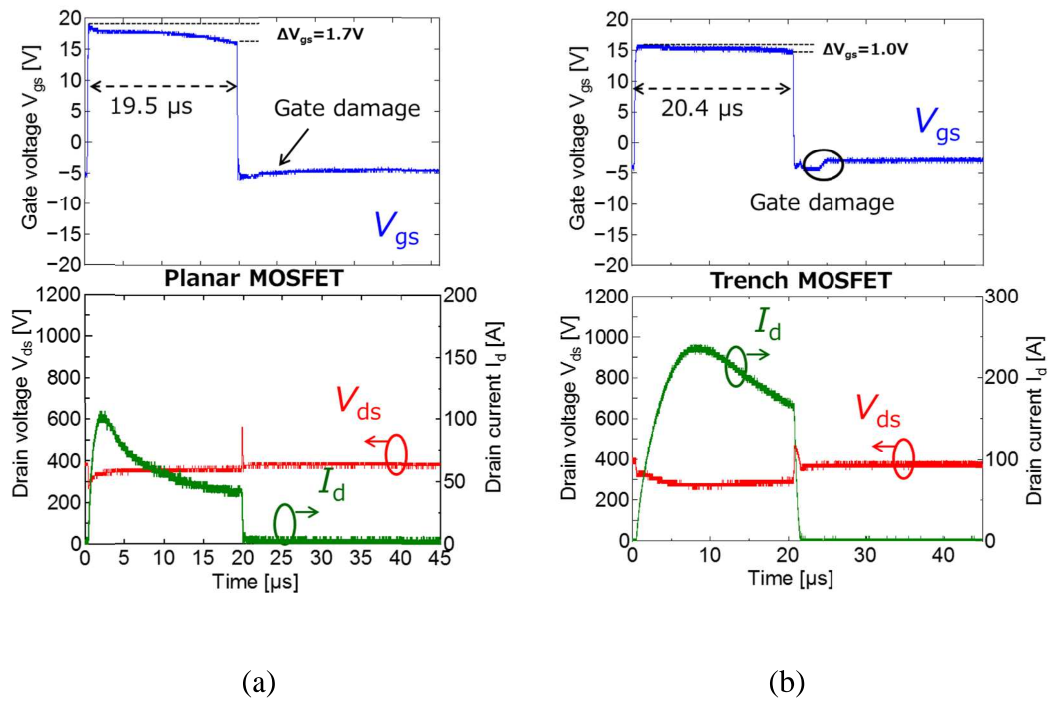

(a) (b)

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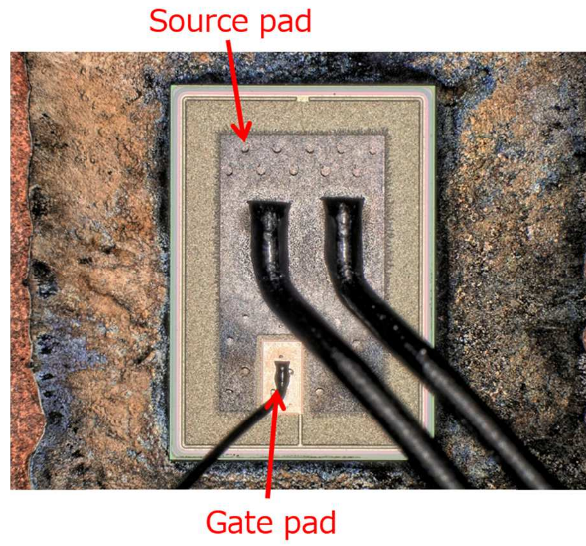

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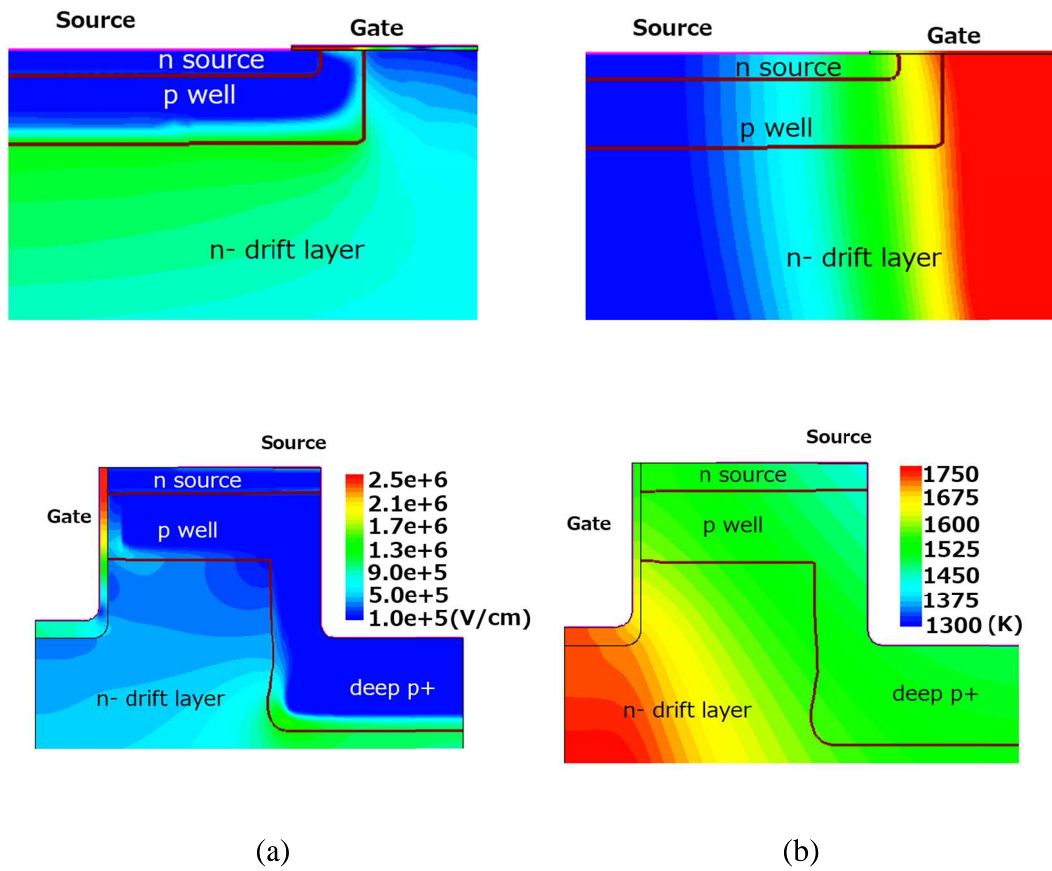

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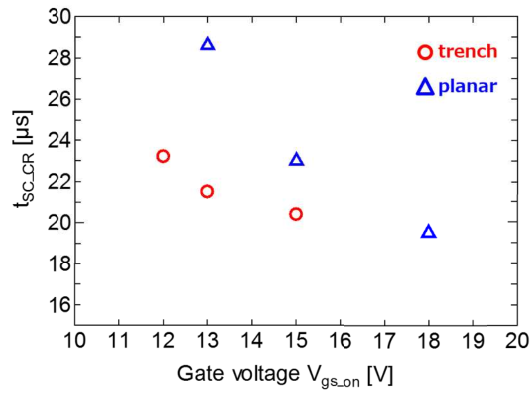

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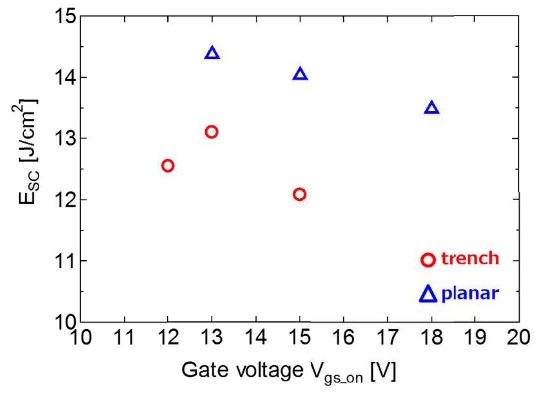

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Figure 19 (Color online)