Study on Robustness Issues and Related Mechanisms for Silicon Carbide Power MOSFETs

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Contents

Introduction

Progress in Electronics

Research and development of semiconductor materials and devices are the profoundly influence and strong driving force for the revolutionary progress to our modern society. Since the first invention of silicon (Si)-based metal-oxide-semiconductor field effect transistor (MOSFET) in 1950s, semiconductor devices have entered a new era and been recognized as the fundamental components of the power electronic systems [1]. Nowadays, Si-based power semiconductor and large scale integrated circuit (LSI) are the key components in electronic systems. Despite the physical limitations of Si material, remarkable progress has been made in Si-based semiconductor. Even now, various power device and solar cells are also mainly produced by using silicon.

Since 1990s, compound semiconductors have been held an important position to replace the status of Si-base devices in some applications due to the inherent limitations of Si material properties. As the representatives, gallium arsenide (GaAs) and indium phosphide (InP) have been widely used for high frequency, high power and light emitting devices [2].

As development of advanced technology in society, various requirements have been arisen for semiconductor devices, such as low power consumption and high temperature operation. Improvement of energy efficiency is one of the most important solutions because it is estimated that over 50% electricity used in the world is controlled by power semiconductor devices and this ratio continues to increase as time goes on. With the widespread use of electronics in many application fields as shown in Fig. 1.1, such as the industrial, consumer, and transportation, realization of high performance power semiconductor devices have a major impact on the society not only due to energy saving but also because of reducing of environmental pollution [3].

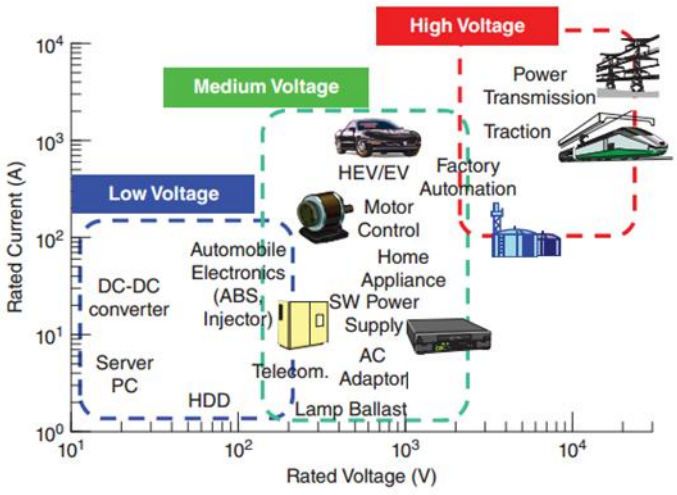

Fig. 1 Application areas of power devices [3].

Nowadays, Si has been widely used in semiconductor for power devices. The characteristics of Si-based power devices including power MOSFET and insulated gate bipolar transistor (IGBT) have been greatly promoted. However, the increasing requirements of lower power dissipation, higher frequency and temperature operation, and larger power density for power electronic system make Si-based power devices approach their performance limits gradually. Due to its superior physical properties, silicon carbide (SiC) is promising for the advanced power devices.

SiC is a IV‑IV compound material and exhibits a wide bandgap, high critical electric field, and high saturation drift velocity compared with Si. The N and P type with a wide doping range is relatively easy to form by ion-implantation at high temperature in SiC [3]. In addition, the native oxide of SiC is silicon dioxide (SiO_2), making it to be easily fabricated. Due to these advanced properties, SiC is a promising candidate for low power loss, high temperature applications.

History of SiC Power Devices

SiC power devices was proposed and theoretically analyzed by Baliga for the first time in 1980s [4]. As development of epitaxial growth and fabrication technologies, the high voltage SiC schottky barrier diode (SBD) with low on-state resistance was reported in 2001[5]. Nowadays, the maximum breakdown voltage of SiC diode has been exceeded 20 kV [6]. As a fast diode, SiC SBD is widely used in the power system, such as such as power supply, traction control system, and etc. Due to small reverse recovery current of SiC SBD, the power loss can be dramatically reduced and the switching frequency can be increased, resulting in the miniaturization of passive components for the whole power system.

Together with the progress in SiC diode, fabrication of vertical SiC MOSFET began in 1990s. Purdue University reported a first planar SiC MOSFET with the breakdown voltage of 760 V in 1997 and a 1.4 kV/15 $m\Omega \cdot cm^2$ 4H-SiC trench MOSFET in 1998.[7] 4H-SiC power MOSFET has been commercially available and puts into practical use in transportation applications since 2010 [8].

Nowadays, the high voltage SiC MOSFET and SiC Schottky Barrier Diode (SBD) that over 1700 V are commercial available and start to be widely put into practical use in transportation applications, such as power supply, traction control system, etc. However, the further improvement of SiC power device should be continued, such as reliability improvement and cost reduction.

Research Background of Robustness Issues for SiC MOSFETs

The safe operating area (SOA) is defined as the voltage and current conditions over that the device can be expected to safety operate without any damage [9]. The SOA of power MOSFET is shown in Fig. 2. The area can be divided into three limits: the drain current limit, the maximum power dissipation limit and the drain voltage limit. Although the superior performance in static and dynamic characteristics for the SiC MOSFET over the traditional Si-based device has been confirmed for most applications, similar with the other switching devices, it is of great benefit to evaluate the reliability in withstanding of harsh and stressful conditions (i.e., large energy density and high case temperature) for

the SiC MOSFET. Normally, the dominated features of the reliability for SiC devices can be considered as the withstanding operation current, voltage and temperature that out of their nominal ratings. Therefore, it is mandatory for SiC MOSFET to be designed with a reasonable out-of-SOA robustness. The key reliability issues are the unclamped inductive switching (UIS) capability and short-circuit capability of SiC MOSFET, respectively.

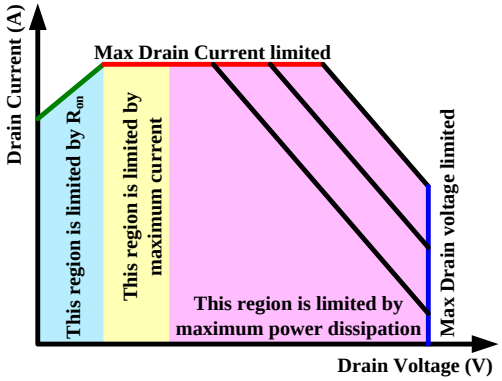

Fig. 2 SOA area of power MOSFET

Similar with the other switching devices, high *dI*/*dt* coupled with an inductive load (i.e., built-in or parasitic) is able to force the SiC MOFET to work in the avalanche mode especially in the high switching transient, resulting in a rapid increase in junction temperature and self-damage. It is easy to fail if the UIS capability of the SiC MOSFET is poor.

As we all know that SiC MOSFET is widely used in the power system for high frequency application. However, the ultra-high switching frequency brings the problem of electro-magnetic interference (EMI) to gate driver and parasitic oscillation in a half bridge circuit that also can trigger the on-state and short circuit for the device even it is switched off. Owing to the high requirement of stability for the whole application system, thus, it is essential for SiC MOSFET with the much higher short-circuit capability.

For Si-based power devices, various papers related to UIS and short-circuit capability and their failure mechanism are reported [10]-[20]. Same topics have been discussed for SiC MOSFET. For example, P. Alexakis gives an experimental comparison between SiC MOSFET and Si IGBT during UIS transient in [21]. It has been shown that the SiC MOSFET is more rugged and can withstand higher temperature surges than that of Si IGBT. A. Castellazzi provides a summarization for SiC power MOSFETs performance, robustness and technology maturity in [22]. In [23], 1200 V SiC MOSFET have shown the high junction operation temperature capabilities (i.e., beyond 473 K) for the long-term reliability, nevertheless, the avalanche characterization has not yet exhibited a great advantage to its silicon counterparts. Furthermore, C. DiMarino predicts and characterizes the avalanche performance of 1200 V SiC MOSFET in [24]. A. Fayyaz and J. Hu have been performed on the development of an electro-thermal simulation to predict the avalanche capability, including withstanding avalanche time and simulated current distribution at different conditions [25], [26]. Since most of them show a temperature-related failure mechanism for the SiC MOSFET under avalanche

mode, it is not clear what the key factor is responsible for avalanche failure. Moreover, the critical temperature for avalanche event has not yet been classified. Prior research on the short-circuit characterization for the commercially available SiC MOSFETs has simply proved in some papers. For example, Z. Wang give an experimental analysis of temperature dependent short-circuit capability for SiC MOSFET by comprising two available devices from Cree and Rohm, respectively [27]. Similarly, X. Huang analyzes the short-circuit capability of 1200 V SiC MOSFET and JFET for fault protection in [28].

Until now, the UIS and short-circuit capabilities and their failure mechanisms for SiC MOSFET, especially for SiC p-channel MOSFET, have not been fully studied combined with experiment, mathematical model and simulation.

Outline of This Dissertation

In this dissertation, the robustness issues including the short-circuit and the avalanche characteristics and related failure mechanisms for SiC power MOSFET are analyzed based on the experimental demonstration and numerical analysis. After introduction of the theoretical background, a commercial available device simulator based on the various physical models relevant to SiC is built in order to put a physical insight to the failure mechanism about robustness issues for SiC MOSFET. Combined with the simulation results and on the basis of the thermal diffusion equation, the analytical formulae for the robustness issues of SiC MOSFET and their dependence on the ambient temperature are carried out in order to verify the critical temperature range and investigate the failure mechanism. After that, experimental results are performed to investigate the short-circuit and avalanche capability for SiC MOSFET. The methodology and new structure for enhanced short-circuit capability of SiC MOSFET are discussed in the following chapter. Finally, the bench mark for the typical characterization of robustness issues is provided to define the critical operation condition for SiC MOSFET. The construction of this work is illustrated as follows:

Chapter 1 recalls the main physical properties of SiC, such as band gap, breakdown electric field, and thermal conductivity. In addition, intrinsic carrier concentration, built-in voltage, and critical electric field of SiC related to reliability issues are quantitatively analyzed compared with Si.

Chapter 2 briefly introduces the physical models and simulation procedure used in TCAD simulator. The complete sets of models including their parameters are comprehensively presented for entire simulations.

Chapter 3 shows the experimental evaluation and numerical analysis of the UIS capability and short-circuit capability for the 1200 V n-channel vertical 4H-SiC MOSFET (SiC n-MOSFET). Firstly, unclamped inductive switching test is presented to evaluate energy handing ability and maximum junction temperature of 1200 V SiC n-MOSFET during avalanche mode. It is verified that commercial 1200 V n-SiC MOSFET can easily withstand almost ten microseconds avalanche time with 1 mH inductance and 400 V DC bus at the temperature of 300 K in avalanche mode. In addition, three reasonable evaluation methods of the maximum junction temperature for SiC n-MOSFET are summarized at different case temperatures. Secondly, the short-circuit test of the 1200 V n-SiC

MOSFET with a thin gate oxide layer is reported. Two different failures, including the gate oxide breakdown and the thermal runaway of the device caused by the high gate electric field and elevated lattice temperature, are initially investigated and their critical temperature points for two failure modes are accurately extrapolated by solving the thermal diffusion equation. It is confirmed that short-circuit robustness depends not only on thermal properties of the material but also on dimensional parameters of the device and that the heat is the dominant factor that causes device failure during short-circuit transient. At last, methodology and new structure for enhanced short-circuit capability of SiC MOSFET are introduced.

Chapter 4 introduces a p-channel vertical 4H-SiC MOSFET (SiC p-MOSFET), which has been successfully fabricated as a potential candidate for the complementary inverter application. The static characteristics and the robustness, including short-circuit and avalanche capabilities of the p-MOSFET, are experimentally tested. Moreover, the comparison between the p-MOSFET and similar rating n-MOSFET is carried out. The short-circuit capability is 15% higher than that of the n-channel MOSFET. Furthermore, the section also provides the physical insights into the failure mechanism during the short-circuit transient of the p- and n-MOSFET. Meanwhile, an electro-thermal analytical model is proposed to explain the thermal distribution during this transient. Lastly, the avalanche withstand time of the fabricated SiC p-MOSFET is experimentally demonstrated to be 27% higher than that of the n-channel one.

Chapter 5 concludes the dissertation.

Based on this research topic, several papers are published in the top journal and conference, such as IEEE Trans. on Electron Device, IEEE International Electron Device Meeting (IEDM), IEEE International Symposium on Power Semiconductor Devices & ICs (ISPSD) and etc. The main contribution and innovation of this work are summarized as following.

1. The short-circuit and UIS capabilities and related failure mechanisms for SiC n-MOSFET are firstly analyzed based on the experimental evaluation, mathematical model and numerical analysis. Methodology and new structure for enhanced short-circuit capability of SiC MOSFET are experimental demonstrated and simulative proposed.
2. A p-channel SiC p-MOSFET has been successfully fabricated for the first time in the world. The higher short-circuit and UIS capabilities of SiC p-MOSFET are experimentally demonstrated and systematically analyzed. It is concluded that the fabricated SiC p-MOSFET could be a competitive power switch applicable for high frequency complementary inverters.

Some results discussed in this dissertation are related to the papers published in [29]-[34].

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1. Properties of Silicon Carbide

1.1 Material Properties

Silicon power devices including unipolar and bipolar have been improved significantly over the past several decades to serve a very broad range of applications in power system [1]. However, these devices have almost reached material theoretical limits due to an increasing demand for high frequency and high power capabilities. Therefore, new alternatives are needed to satisfy these new requirements of power devices. Silicon carbide (SiC) is a wide bandgap semiconductor with superior physical and electrical properties to replace the statue of silicon for the high voltage and low loss power electronics application in the future.

The fundamental properties of silicon carbide and silicon are summarized and compared in table 1.1. The properties for the 4H poly-types silicon carbide are superior to those of the other poly-types silicon carbide. The basic properties related to power SiC MOSFETs are the energy band gap, the relative dielectric constant, the critical breakdown electric field, the thermal conductivity, the electron affinity, and the carrier mobility.

TABLE 1.1

Comparison of material properties between SiC and Si

Symbol	SiC	Si	Unit
Energy Band Gap	3.26	1.11	eV
Relative Dielectric Constant	9.7	11.7	
Breakdown field	2.0-3.0	0.3	MV/cm
Thermal Conductivity	3.7	1.5	W/cmK
Electron Affinity	3.7	4.05	eV
Saturation velocity	2.0	1.0	10^7 cm/s
Density of States Conduction Band	1.23×10^{19}	2.80×10^{19}	cm^{-3}
Density of States Valence Band	4.58×10^{18}	1.04×10^{19}	cm^{-3}

It should be noted that the energy band gap for 4H-SiC is three times larger than that of silicon. It leads to a much lower intrinsic carrier concentration for silicon carbide when compared with silicon at any temperature. The critical breakdown field for 4H-SiC is almost ten times larger than that of silicon, resulting in a much high breakdown voltage capability. For example, much higher doping level or thinner drift layer thickness can be achieved by using SiC-based power devices with same breakdown voltage level compared with Si-based counterparts. The advantage of thermal conductivity for 4H silicon carbide enables superior heat extraction from devices. The cooling system or heat sink can be effectively reduced or removed by using SiC-based power device. The difference in the electron affinity between two materials appears small. However, it is quite important for the characteristics of schottky barrier contacts. The high switching frequency of SiC power device can be realized due to high drift velocity. In addition, SiC is the only compound semiconductor whose native oxide is SiO_2,

which makes it possible to fabricate the MOS-based (metal-oxide-semiconductor) power devices in SiC material. Thus, SiC is the most favorable material for high power, high frequency, and high temperature device applications.

1.2 The Intrinsic Carrier Concentration

The intrinsic carrier concentration is determined by the thermal generation of electron-hole pairs across the energy band gap of a semiconductor. As discussed as before, silicon carbide has a wide bandgap, which means the energy gap between conduct band and valence band is wider than other materials, leading to a smaller generation of electron-hole pairs. Its value can be expressed by the energy band gap (E_G) and the density of states in the conduction (N_C) and valence (N_V) bands:

$$n_i = \sqrt{np} = \sqrt{N_C N_V} e^{-E_G/2kT} \tag{1}$$

where k is Boltzmann's constant and T is the temperature. For silicon carbide, the intrinsic carrier concentration can be given by:

$$n_i(SiC) = 1.70 \times 10^{16} T^{3/2} e^{-(2.08 \times 10^4)/T} \tag{2}$$

while that for silicon can be given by:

$$n_i(Si) = 3.87 \times 10^{16} T^{3/2} e^{-(7.02 \times 10^3)/T} \tag{3}$$

From these equations, the intrinsic carrier concentration can be simply defined as the temperature dependent. The comparison of intrinsic carrier concentration for two materials is plotted in Fig. 1.1. It is worth to note that the intrinsic carrier concentration of SiC is far smaller than that of Si due to wide band gap.

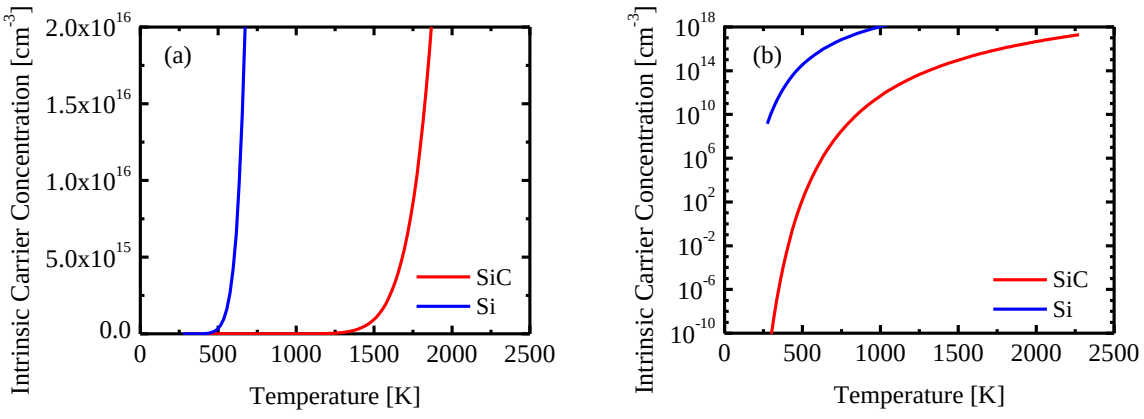

Fig. 1.1 Intrinsic carrier concentration

The intrinsic carrier concentration for SiC is equal to 6.7 $\times 10^{-11}$ cm^{-3} while that for Si is 1.4 $\times 10^{10}$ cm^{-3} at room temperature. In addition, the intrinsic carrier concentration that equals to a typical drift layer doping concentration is 1 $\times 10^{15}$ cm^{-3} at a temperature of 540 K while that for SiC is 1515 K. Therefore, thermally generated leakage current at high temperature can be negligible for SiC power

device but not for silicon power device.

1.3 Built-in Voltage

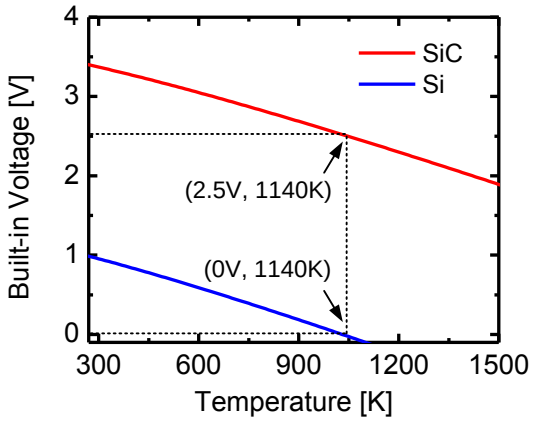

Fig. 1.2 The built-in voltage as a function of temperature for a PN junction in SiC and Si at $N_A^- N_D^+ = 2\times10^{36}\,\mathrm{cm}^{-3}$.

The built-in voltage of PN junctions plays an important role because it determines the performance and design of power semiconductor devices. One of most significant influence should be the on-state voltage of PN junction. It also determines the zero bias depletion width, which can affect the on-state resistance of power MOSFETs. The built-in voltage can be expressed by:

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A^- N_D^+}{n_i^2}\right) \tag{4}$$

where N_A^- and N_D^+ are the ionized impurity concentrations of the PN junction. The calculated built-in voltage as a function of temperature for the typical operating range of power devices in SiC and Si is shown in Fig. 1.2. The product of ionized impurity concentrations for the PN junction in SiC and Si are both $N_A^- N_D^+ = 2\times10^{36}\,\mathrm{cm}^{-3}$. This would be applicable for a heavily doping with the typical doping concentration of 1×10^{19} cm^{-3} and a lightly doping with the typical doping concentration of 2×10^{16} cm^{-3}. The doping concentration chosen in here refers to the typical doping in n+ source and p well region in the MOSFET. The built-in voltage for SiC is much larger than that for Si due to the far smaller values of the intrinsic carrier concentration. It can be considered a disadvantage because of the larger zero bias depletion width for silicon carbide, leading to the larger zero bias depletion width and increasing the on-resistance in JFET region in MOSFET. However, the larger built-in voltage can be taken advantage of high temperature operation. For example, we can see that the built-in voltage in Si decreases to zero at 1140 K, corresponding to 2.5 V in SiC. It is obvious that activation of PN junction for SiC in a typical operation range is much more difficult than that for Si. This can be recognized the advantage of high temperature operation and can avoid the miss conduction of PN junction at high lattice temperature.

1.4 Critical Breakdown Field and Width of the Depletion Region

The main advantage of SiC for power device applications comes from the very low resistance of the drift region even it has a larger breakdown voltage. The critical breakdown field is one of the most significant factors for power semiconductor to determine the blocking characteristic, corresponding to the electric field when impact ionization takes place. The analysis of an abrupt PN junction can be used to well understand the design of the drift region in power devices. When a reverse biased apply on this junction, a depletion region is formed in the lower doping region (here is N region) along with the generation of a strong electric field within it that supports this reverse biased voltage. The Poisson's equation for the N region is given to define the relationship between electric field and doping concentration:

$$\frac{d^2V}{dx^2} = -\frac{dE}{dx} = -\frac{Q(x)}{\varepsilon_s} = -\frac{qN_D}{\varepsilon_s} \tag{5}$$

where *Q(x)* is the charge in the depletion region, ε_S is the dielectric constant, *q* is the electron charge, and N_D is the doping concentration in the N region. The maximum electric field at the junction can be obtained by solving Poisson's equation using the boundary condition:

$$E_{\max} = \sqrt{\frac{2qN_DV_a}{\varepsilon_s}} \tag{6}$$

where V_a is the applied reverse voltage. The width of the depletion region is also related to the applied reverse voltage that can be expressed by:

$$W_D = \sqrt{\frac{2\varepsilon_S V_a}{qN_D}} \tag{7}$$

The breakdown voltage and the corresponding maximum depletion layer width can be also simplified by substituting the Fulop's power law with the electric field distribution given by Poisson's equation [1]:

$$BV(SiC) = 3.0\times10^{15} N_D^{-3/4} \tag{8}$$

and

$$W_D(SiC) = 1.82\times10^{11} N_D^{-7/8} \tag{9}$$

while that for Si can be given by:

$$BV(Si) = 5.34\times10^{13} N_D^{-3/4} \tag{10}$$

and

$$W_D(Si) = 2.67\times10^{10} N_D^{-7/8} \tag{11}$$

The breakdown voltage as a function of the doping concentration is shown in Fig 1.3. The breakdown voltage is decrease with increasing of the doping concentration. It can be seen that the breakdown voltage for SiC is much higher than that for Si at same doping concentration. It worth to point out that the breakdown voltage for SiC is 56.17 times higher than that of Si at same the same doping concentration. As an example, the breakdown voltage for SiC is 3000 V while only 53.4 V for Si at 1×10^{16} cm^{-3}. Therefore, it is possible to support a much larger voltage for SiC by adopting the high doping concentration. This results in an extremely low on-state resistance of power device when compared with its counterpart silicon.

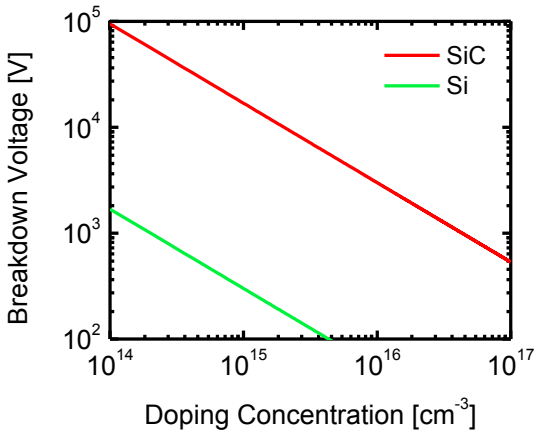

Fig. 1.3 Breakdown voltage for PN junction in SiC and Si

The maximum depletion width as a function of the doping concentration is shown in Fig 1.4 for SiC and Si. The maximum depletion width shows a decrease tendency with increase of the doping concentration. As discussed before, the critical electric field for SiC is one order magnitude higher than that for Si. The maximum depletion width for SiC is 6.81 times larger than that for silicon at same doping concentration. However, the depletion width for SiC is far smaller than that of Si at same breakdown voltage because the much larger doping concentration can be used in the drift region for SiC. For example, the depletion width is 6.52 μm for SiC while 105 μm for Si at a breakdown voltage of around 1200 V. Therefore, high doping concentration in drift layer associated with the smaller depletion width leads to a small on-state resistance, making SiC to be the superior semiconductor material for the high voltage power device application.

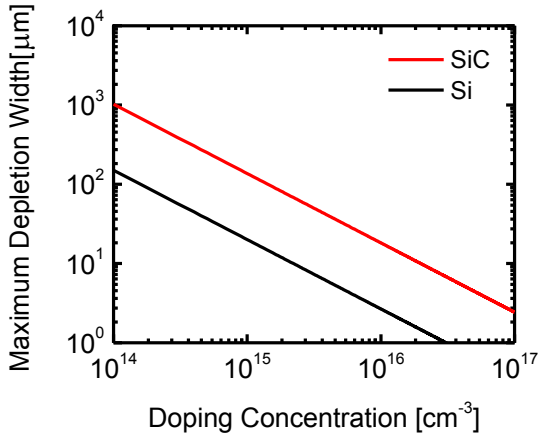

Fig. 1.4 Maximum depletion width in SiC and Si

1.5 Critical Electric Field

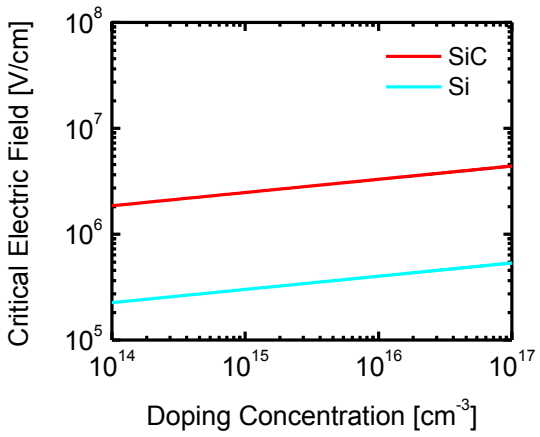

Fig. 1.5 Critical electric field in SiC and Si

The critical electric field is key factor to decide the breakdown for SiC, which can be given by combining equation 6 and 8:

$$E_C(SiC) = 3.3\times10^4 N_D^{1/8} \tag{12}$$

while for Si can be given by:

$$E_C(Si) = 4010 N_D^{1/8} \tag{13}$$

The comparison result of critical electric field as a function of doping concentration for breakdown in SiC and Si is shown in Fig1.5. Different from the former cases, the critical field for breakdown increase with increase of doping concentration. The critical electric field for SiC is 8.22 times larger than that for Si at same doping concentration. It should be pointed out that the critical electric field has a weak dependence of doping concentration.

Conclusion

This chapter briefly introduces the fundamentally physical properties of SiC related to reliability issues, such as band gap, breakdown electric field, and thermal conductivity. In addition, intrinsic carrier concentration, built-in voltage, and critical electric field are quantitatively compared with Si. It is obvious that excellent properties make SiC to be the superior candidate for the high voltage power device application.

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2. Physical Models

The results based on the simulation can give the physical insight to the device and highly depend on the physical models and related parameters. A number of physical models in the TCAD simulator are used for precise simulation. In this chapter, a brief introduction is carried out to give an overview to the TCAD simulator. The simulation using several of physics equations and models describes the basic transport phenomenon in SiC MOSFETs [1].

2.1 Physics Equations

Poisson's, carrier continuity and transport equations are three basic equations to complete the simulation of the electrical characteristics of the required simulation device. The following is a brief introduction of these three equations.

The Poisson's equation is decided by electrostatic potential (φ) and net charge density. It can be given by the following expression:

$$\nabla \cdot (\varepsilon \nabla \varphi) = -\rho \tag{14}$$

where ε is the electrical permittivity and ρ is the net charge density that can be given by

$$\rho = q(p - n + N_D^+ - N_A^-) \tag{15}$$

where q is the electronic charge, n and p are the electron and hole densities, respectively N_D is the concentration of ionized donors, N_A the concentration of ionized acceptors. Among them, the electron and hole densities can be obtained by

$$n = N_C \exp(-\frac{E_C - E_F}{kT}) \tag{16}$$

$$p = N_V \exp(-\frac{E_F - E_V}{kT}) \tag{17}$$

where N_C and N_V are the effective density-of-state, E_F is the quasi-Fermi energy levels, E_C and E_V the conduction and valence band edges.

The continuity equation is used to describe the concentration of mobile charges for semiconductor device and can be expressed by

$$\nabla \cdot J_n = qR_{net,n} + q\frac{\partial n}{\partial t} \tag{18}$$

$$-\nabla \cdot J_p = qR_{net,p} + q\frac{\partial p}{\partial t} \tag{19}$$

where J_n and J_p are the electron and hole current densities, $R_{net,n}$ and $R_{net,p}$ are the electron and hole net recombination rate, respectively. When consider the relations of drift and diffusion, the current can be simplified as

$$J_n = -nq\mu_n \nabla \Phi_n \tag{20}$$

$$J_p = -pq\mu_p \nabla \Phi_p \tag{21}$$

where Φ_n and Φ_p are the electron and hole quasi-Fermi potentials, respectively.

2.2 Physics Models

The models used in the simulation are presented and calibrated with the experimental results for the SiC MOSFETs, including generation/recombination model, mobility model, bandgap narrowing model and incomplete ionization model.

Due to relatively shallow impurity level, the doping impurities for narrowband semiconductor materials such as Si are completely ionized. However, we must consider the incomplete ionization of impurities if the impurity levels are relatively deep compared to the thermal energy *kT*. This is the case for indium acceptors in silicon and nitrogen donors and aluminum acceptors in silicon carbide and incomplete ionization must be considered for all dopants at decreased temperatures [2]. The Sentaurus TCAD software uses an incomplete ionization model and an activation energy based ionization model to calculate the ionization energy for the different doping conditions and net ionized acceptor and net ionized donor. The ionization is computed separately for each species present and can be expressed as follows

$$N_D^- = \frac{N_D}{1 + g_D \exp(\frac{E_{Fn} - E_D}{kT})} \tag{22}$$

$$N_A^- = \frac{N_A}{1 + g_A \exp(\frac{E_A - E_{Fp}}{kT})} \tag{23}$$

$$N_D^- = \frac{N_D}{1 + g_D \frac{n}{n_1}}, \text{ with } n_1 = N_C \cdot \exp(-\frac{\Delta E_D}{kT}) \tag{24}$$

$$N_A^- = \frac{N_A}{1 + g_A \frac{p}{p_1}}, \text{ with } p_1 = N_V \cdot \exp(-\frac{\Delta E_A}{kT}) \tag{25}$$

where, the g_D and g_A are the degeneracy factors that depend on the doping and temperature but do not depend on the free carrier densities.

Generation–recombination processes are very important in device physics, especially for bipolar devices processes, which can exchange carriers between the conduction band and the valence band. Several generation–recombination models are available in Sentaurus Device. For SiC material, they are Shockley-Read-Hall (SRH) recombination, Auger recombination and Avalanche generation.

Recombination through deep defect levels in the gap can be defined as SRH recombination. The following formula is used in Sentaurus Device [1].

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p (n + n_1) + \tau_n (n + p_1)} \tag{26}$$

with:

$$n_1 = n_{i,eff} \exp(\frac{E_{trap}}{kT}) \tag{27}$$

and:

$$p_1 = n_{i,eff} \exp(\frac{-E_{trap}}{kT}) \tag{28}$$

where E_{trap} is the difference between the defect level and intrinsic level. The value is accessible in the parameter file. The τ_n and τ_p are lifetimes of electron and hole, respectively. They are modeled as a product of a doping-dependent and temperature-dependent factor. In simulation, the Scharfetter relation is used to explain the doping dependence of SRH lifetimes:

$$\tau_{dop}(N_A + N_D) = \tau_{\min} + \frac{\tau_{\max} - \tau_{\min}}{1 + (\frac{N_A + N_D}{N_{ref}})^{\gamma}} \tag{29}$$

A formula using the low-temperature approximation of multiphonon theory [3] gives:

$$\tau_{SRH}(T) = \tau_{SRH}(300K) \cdot (\frac{T}{300K})^{-3/2} \tag{30}$$

From equation 30, the minority carrier lifetime is expected decrease with the rising temperature. The parameters of the doping and temperature dependent SRH recombination are shown in table 2.1.

TABLE 2.1

Scharfetter model: Default coefficients for silicon carbide

Symbol	Electron	Hole	Unit
τ_{min}	0	0	s
τ_{max}	2.5e-6	0.5e-6	s
N_{ref}	3.0e17	3.0e17	cm^{-3}
γ	0.3	0.3	1
T_a	1.72	1.72	1
C	2.55	2.55	1
E_{trap}	0	0	eV

It is crucial to consider the avalanche generated electron-hole pair when high field strength implies on the device. Once the width of a space charge region is greater than the mean free path between two ionizing impacts, charge multiplication occurs, resulting in the electrical breakdown [4]. The carriers generation rate can be expressed as fellow:

$$G_{ii} = \alpha_n n v_n + \alpha_p p v_p \tag{31}$$

where α_n and α_p are the ionization coefficient for electrons and holes, respectively. In Sentaurus device, several models for impact ionization are implemented, including Okuto–Crowell and Hatakeyama for SiC MOSFET.

Okuto and Crowell give the empirical model to define the ionization coefficient [5]:

$$\alpha(F_{ava}) = \alpha \cdot (1 + c(T - T_o)) F_{ava}^{\gamma} \exp[-(\frac{b[1 + d(T - T_o)]}{F_{ava}})^{\delta}] \tag{32}$$

Coefficients of Okuto–Crowell model for silicon carbide are list in table 2.2.

TABLE 2.2

Okuto–Crowell model: Default coefficients for silicon carbide

Symbol	Electron	Hole	Unit
a	2.10e7	2.96e7	V^{-1}
b	1.70e7	1.60e7	V/cm
c	0	7.511e-3	K^{-1}
d	0	1.381e-3	K^{-1}
γ	0	0	1
δ	1.0	1.0	1

The Hatakeyama avalanche model has been used to describe the anisotropic behavior in SiC power devices [6]. The impact ionization coefficient is obtained according to the Chynoweth law [4]:

$$\alpha = \gamma a e^{-\frac{\gamma b}{F}} \quad \text{with } \gamma = \frac{\tanh(\frac{\hbar\omega_{op}}{2kT_o})}{\tanh(\frac{\hbar\omega_{op}}{2kT})} \tag{33}$$

The coefficients a and b are computed dependent on the direction of the driving force F. The critical coefficients for Hatakeyama model are list in table 2.3.

TABLE 2.3

Hatakeyama model: Default coefficients for silicon carbide

Symbol	Electron	Hole	Unit
a_{0001}	1.76e8	3.41e8	cm^{-1}
a_{1120}	2.10e7	2.96e7	cm^{-1}
b_{0001}	3.30e7	2.50e7	V/cm
b_{1120}	1.70e7	1.60e7	V/cm
$\hbar\omega$	0.19	0.19	eV

Mobility shows the average carrier drift velocity per a unit field strength. According to the influence of different conditions, the mobility model can be divided into the low-field mobility, high-field mobility model and the surface mobility influenced by many factors such as surface roughness, interface trap and phonon scattering.

In doped semiconductors, degradation of the carrier mobility occurs due to the scattering of the carriers by charged impurity ions at the condition of low electric field. The Arora model is useful to explain the doping-dependent mobility at the low electric field:

$$\mu_{dop} = \mu_{\min} + \frac{\mu_d}{1 + ((N_{A,0} + N_{D,0}) / N_0)^{A^*}} \tag{34}$$

with:

$$\mu_{\min} = A_{\min} \cdot (\frac{T}{300K})^{\alpha_m},\ \mu_d = A_d \cdot (\frac{T}{300K})^{\alpha_m} \tag{35}$$

and:

$$N_0 = A_N \cdot (\frac{T}{300K})^{\alpha_N},\ A^* = A_a \cdot (\frac{T}{300K})^{\alpha_a} \tag{36}$$

The parameters used in Arora model are list in table 2.4.

TABLE 2.4

Arora model: Default coefficients for silicon carbide

Symbol	Electron	Hole	Unit
A_{min}	40	0	cm^2/Vs
α_m	-1.536	-0.57	1
A_d	910	113.5	cm^2/Vs
α_d	-2.397	-2.6	1
A_N	2.0e17	2.4e18	cm^{-3}
α_N	0.75	2.9	1
A_a	0.76	0.69	1
α_a	0.722	-0.2	1

TABLE 2.5

Caughty-Thomas model: Default coefficients for silicon carbide

Symbol	Electron	Hole	Unit
B_0	1.2	1.2	1
$B_{\exp}$	1	1	1
α	0	0	1

At high field intensities inside the device, the photon scattering significantly increases and the carriers can be easily accelerate to saturate with the magnitude of electric field increasing. At this time, the low-field mobility model is not suitable to analyze the carrier electrical characteristics. Caughty-Thomas model is used to describe the mobility relationship:

$$\mu_{high} = \frac{(\alpha+1)\mu_{low}}{\alpha + [1 + \frac{(\alpha+1)\mu_{low}E}{\upsilon_{sat}})^{\beta}]^{1/\beta}} \tag{37}$$

where μ_{low} is the carrier mobility at low electric field. The exponent β is temperature dependent according to:

$$\beta = \beta_0 (\frac{T}{300K})^{\beta_{\exp}} \tag{38}$$

The default values of silicon carbide are listed in table 2.5

The quality of SiC/SiO_2 interface is particularly critical for the performance of 4H-SiC MOSFETs

since it determines the concentration of trap density. The thermally grown process of SiO_2 produces different kinds of charges at the interface and in oxide. The presence of carbon during oxidation process of SiC leads to a higher concentration of traps at the interface. Moreover, the charges associated with the thermally grown SiO_2 on SiC are classified as mobile ion charges, oxide trapped charges and fixed charges. In the channel region of SiC MOSFETs, Coulomb scattering at the interface charges is the dominant scattering mechanism due to the high density of interface traps and fixed charge. Therefore, the general form of the mobility degradation components can be given by:

$$\mu_{Coulomb} = \frac{\mu_1 (\frac{T}{300K})^k \{1 + [c / (c_{trans} (\frac{N_{A,D}}{10^{18} cm^{-3}})^{\gamma_1} (\frac{N_{Coulomb}}{N_0})^{\eta_1})]^{\nu}\}}{(\frac{N_{A,D}}{10^{18} cm^{-3}})^{\gamma_2} (\frac{N_{Coulomb}}{N_0})^{\eta_2} \cdot D \cdot f(F_\perp)} \tag{39}$$

with:

$$f(F_\perp) = 1 - \exp[-(F_\perp / E_0)^{\gamma}] \tag{40}$$

$$D = \exp(-x / l_{crit}) \tag{41}$$

where $N_{coulomb}$ is interface charge density, x is the distance from the interface. Parameters for mobility degradation components due to Coulomb scattering are shown in table 2.6.

TABLE 2.6

Coulomb model: Default coefficients for silicon carbide

Symbol	Electron	Hole	Unit
μ_1	40	40	$cm^2V^{-1}s^{-1}$
k	1	1	1
c_{trans}	1.09e18	1.0e18	cm^{-3}
ν	1.5	1.5	1
η_1	1.0	1.0	1
η_2	0.5	0.5	1
γ_1	0	0	1
γ_2	0	0	1
l_{crit}	1.0e-6	1.0e-6	cm
E_0	2.0e5	2.0e5	V/cm
γ	2	2	1

In addition, the high transverse electric field forces carriers to interact strongly with the semiconductor–insulator interface in the channel region of SiC MOSFET. Carriers are also subjected to scattering by acoustic surface phonons and surface roughness. The models describing mobility degradation caused by these effects can be expressed by Lombardi model. The mobility degradation due to acoustic phonon scattering has the formula [7]:

$$\mu_{ac} = \frac{B}{F_\perp} + \frac{C(N_{A,0} + N_{D,0} + N_2) / N_0)^{\lambda}}{F_\perp^{1/3} (T / 300K)^K} \tag{42}$$

where $F_{\perp}$ is the transverse electric field normal to the semiconductor–insulator interface. The contribution of acoustic surface phonons scattering to the channel mobility of 4H-SiC MOSFET is not important at room temperature. However, it is critical to affect the mobility at high temperature due to the increase of phonons and decrease of Coulomb scattering at the interface. Moreover, the degradation attributed to surface roughness scattering is given by:

$$\mu_{sr} = \left(\frac{(F_{\perp} / F_{ref})^{A^*}}{\delta} + \frac{F_{\perp}^3}{\eta}\right)^{-1} \tag{43}$$

where δ and η are fit parameters which depend on the roughness of the SiC/SiO_2 interface. It can be seen from equation 43 that the higher the mobility μ_{sr} can be achieved by increasing the values of δ and η. In addition, the contribution of the surface roughness scattering for channel mobility is strongly dependent on the gate voltages. The surface roughness scattering become dominant as gate voltage rising. All parameters are accessible in the table 2.7.

TABLE 2.7

Coulomb model: Default coefficients for silicon carbide

Symbol	Electron	Hole	Unit
B	1.0e6	9.92e6	cm/s
C	580	2.95e3	$cm^{5/3}/V^{-2/3}\ s^{-1}$
N_0	1	1	cm^{-3}
λ	0.125	0.0317	1
k	1	1	1
δ	5.82e14	2.0546e14	cm^2/Vs
A	2	2	1
$\alpha\perp$	0	0	cm^3
N_1	1	1	cm^{-3}
v	1	1	1
η	5.82e30	2.055e30	$V^{-2}cm^{-1}s^{-1}$
l_{crit}	1.0e-6	1.0e-6	1

If more than one mobility model is activated for mobility calculation, the different mobility contributions for bulk and channel mobility are combined by Matthiessen's rule:

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \frac{1}{\mu_3} + \cdots \tag{44}$$

where μ1, μ1, μ1….are mobility as mentioned before.

2.3 Simulation Result

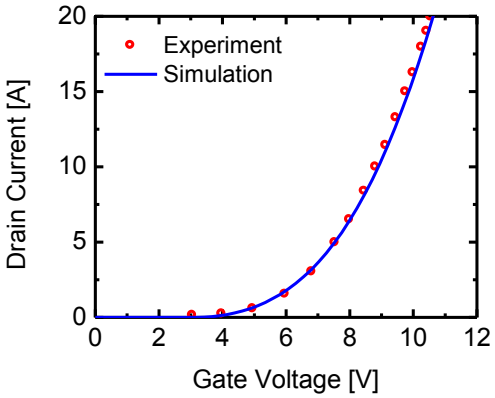

Fig. 2.1 Comparison results between experiment and simulation

Because the on-state characteristic of SiC MOSFET is sensitive to the UIS and short-circuits capabilities, it is significant to choose the right physical models. Fig. 2.1 shows that the simulation result has a good agreement with the experiment one. Therefore, the models used in the simulation are suitable for the simulation. It can give a good physical insight inner the device by using simulation.

2.4 Conclusion

The physical equations and models used in the simulator are briefly introduced in this chapter. The simulation result shows a good agreement with the experiment one in on-state characteristic by using the precise models.

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3. Robustness Issues for SiC n-channel MOSFET

In virtue of the excellent properties with the wider band gap, the higher critical electric field, the better thermal characterization, SiC MOSFET has been commercially available to replace the status of its silicon counterpart [1]. As a representative, the SiC MOSFET can be the best candidate for the power system application not only for its fast switching speed but for the low power dissipation during the on-state. Although the superior performance in static and dynamic for the SiC MOSFET over the traditional silicon-based device has been confirmed for most applications [2]-[6], robustness problem still blocks the process of wide application for SiC MOSFET. Since prior research on UIS and short-circuit are provide in [7]-[15], their failure mechanisms are still not clear. To that end, this chapter mainly focuses on the experimental and theoretical analyses of avalanche and short-circuits failure for SiC MOSFET. Finally, the methodology and new structure for enhanced short-circuit capability of SiC MOSFET are proposed and systematically discussed.

3.1 UIS Capability for SiC n-MOSFET

In this section, the avalanche energy handing capability and avalanche failure possibility for the 1200 V SiC MOSFET by UIS test with the different connected inductances and ambient temperatures are precisely presented and discussed On the basis of the thermal diffusion equation, the analytical formulae for the avalanche energy density of SiC MOSFET and their dependence on the ambient temperature, are carried out in order to verify the critical temperature range and investigate the failure mechanism. At last, the critical avalanche energy by the numerical simulation method is confirmed.

3.1.1 Experiment Results

Fig. 3.1 shows the test circuit schematic and experimental hardware. The devices under test (DUT) are planar SiC MOSFET rated at 1200 V/19 A. DUT are controlled by a gate driver with single-pulse, gate-source voltage +20/-5 V.

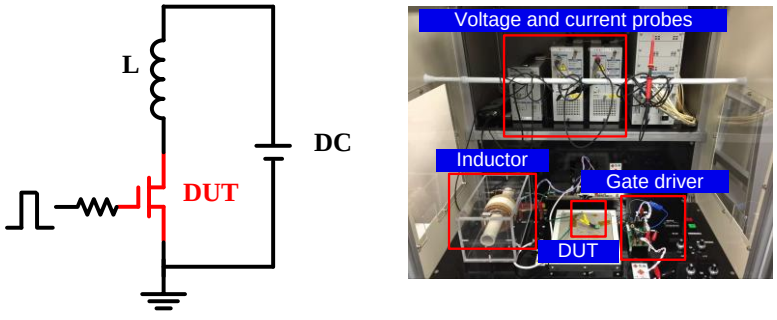


Fig. 3.1. (a) Test circuit and (b) experimental hardware.

3.1.1.1 Single-Pulse Tests at Room Temperature

A. Single-Pulse test with a fixed load inductance

Fig. 3.2(a) shows a single-pulse avalanche event where the 1200 V/19 A SiC MOSFET fails in a relatively long pulse transient of 67 μs for a power supplier of 400 V and a load inductance of 1mH at room temperature. The device survived single-pulse transient up to 66μs and peak avalanche current of 21.5 A in these test conditions. Actually, the next on-state single-pulse transient up to 66 μs and peak avalanche current of 22.1 A causes the device eventually avalanche failure. As it can be shown in Fig. 3.2(b), a significant increase of drain voltage suggests a rapid temperature increase inside the device. After that, zero drain voltage (without blocking capability) shows a complete damage for the device. Compared with Si-based devices, the thinner gate oxide layer and higher electric field of the SiC MOSFET cause a large gate leakage current if the device is not well-designed. This event becomes more obvious at the higher drain voltage associated with the higher lattice temperature due to the penetration of the electric field into the p-well region [16]. This has been also demonstrated by the result in Fig. 3.2(c), where the large burr and the degradation in gate voltage after failure could be interpreted as the deterioration in the gate electrode.

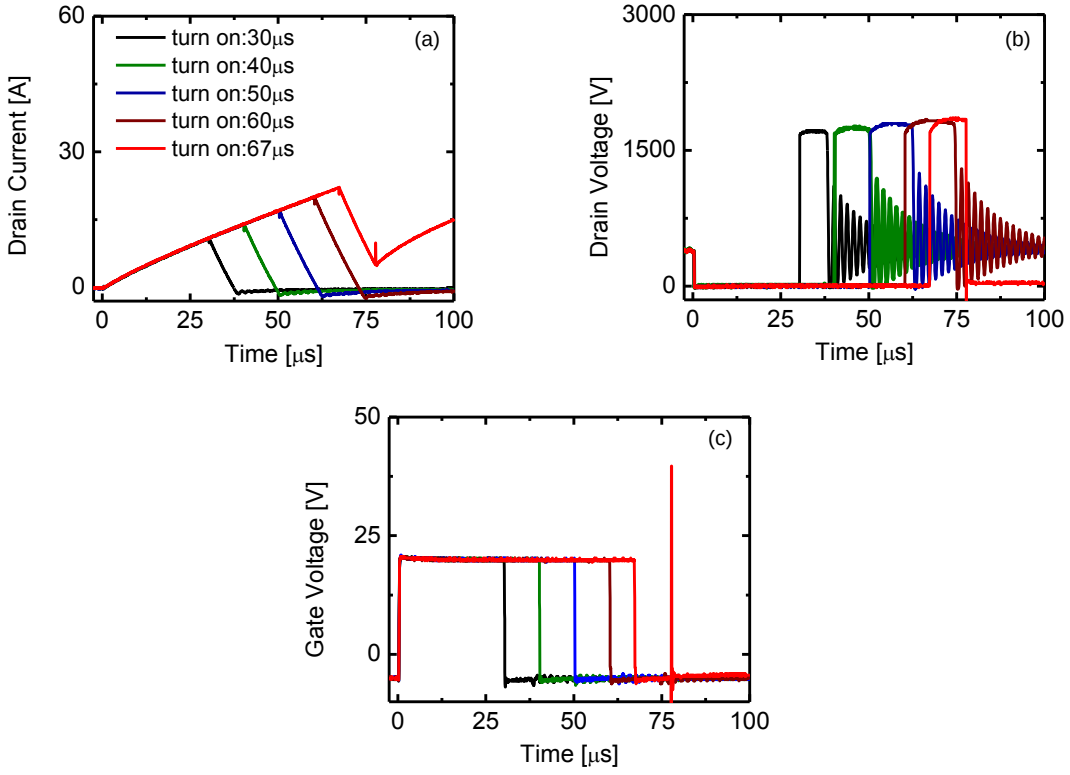


Fig. 3.2. Experimental results of (a) the drain current, (b) the drain voltage and (c) gate voltage as functions of the on-state time for the SiC MOSFET.

Post-failure device with the decapsulation process demonstrates a relatively small fusion localized in the vicinity of the source metallization, as it can be seen in Fig 3.3. The device seems to fail in a small temperature range due to the partial damage on the surface.

According to the prior literatures [17]-[21], a confirmed avalanche failure for the silicon-based devices is the activation of parasitic *npn* bipolar transistor (BJT). If the parasitic BJT is trigged on, the

drain current swiftly increases, resulting in a typical second breakdown failure and the catastrophic thermal runaway. There is no problem to assume the avalanche failure using this opinion. However, it is not feasible for the SiC MOSFET due to its wide band gap and low intrinsic carrier concentration. Fig. 3.4(a) exhibits the temperature dependence of the built-in voltage for the SiC and Si MOSFETs at condition of $N_A N_D = 2 \times 10^{36}\ cm^{-3}$ that the doping concentrations in n-source and p-well for both silicon and silicon carbide-based devices are 1×10^{19} and $2 \times 10^{17} cm^{-3}$, respectively. The built-in voltage of the Si MOSFET decreases to zero at 1140 K, corresponding to 2.5 V for the SiC MOSFET. It is obvious that the activation of parasitic BJT for the SiC MOSFET is much more difficult than that of the Si MOSFET.

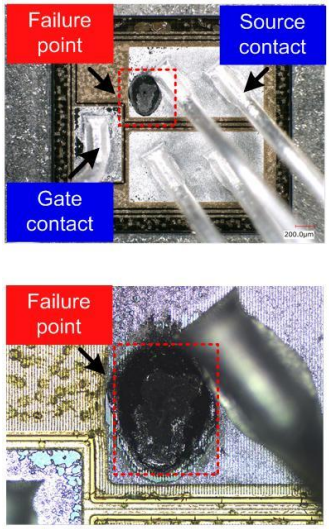


Fig. 3.3. Pictures of the failure SiC MOSFET with burned point and the enlarged image.

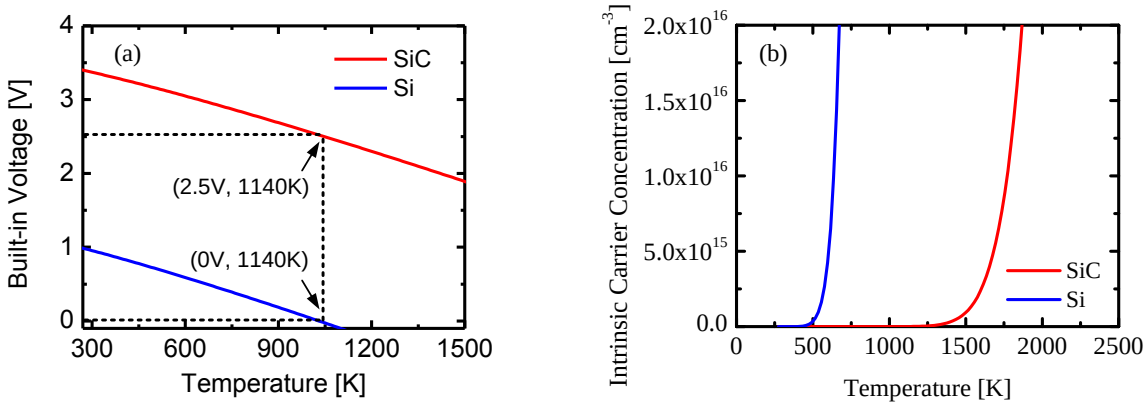


Fig. 3.4. Calculated results of (a) the temperature dependency of built-in voltage and resistivity for drain-base/emitter-base junction and body resistance of the SiC MOSFET and Si IGBT at $N_A N_D = 2 \times 10^{36} cm^{-3}$, and (b) the intrinsic carrier concentration as a function of temperature for the SiC and Si devices

Another failure mechanism is the intrinsic temperature limit, which can be defined as the thermally induced carriers concentration over the background carriers concentration. Fig. 3.4(b) shows that when

the carriers concentration for a rated voltage of 1200V device assumes to 5.0×10^{15} and 7.5×10^{13} cm^{-3}, the thermal temperatures are theoretically calculated to be 1515 and 455 K for the SiC MOSFET and Si IGBT, respectively. The SiC MOSFET, thus, has more than three times thermal capabilities than that of the Si IGBT by using this assumption.

In reality, the SiC MOSFET cannot be in safety before it reaches the previously discussed temperature limits. On the one hand, the process imperfections of device lead to the unbalance current and unharmonious thermal flux. That means that part of cells have much higher temperatures than other cells and result in a partial damage. On the other hand, the melting point of metal and the premature degradation point of gate oxide layer are much smaller than the intrinsic temperature limit (e.g., 1515 K). Those reasons are able to reduce the theoretical avalanche robustness of the SiC MOSFET, which has been confirmed by a regional burn-out point in Fig. 3.3.

B. Single-Pulse test with alterable load inductances

In order to validate the influence of peak avalanche current to the avalanche capability, the unclamped inductive switching (UIS) test is carried out with the load inductances of 1mH, 5mH and 10mH at room temperature. As it can be shown in Fig. 3.5(a), although the failed avalanche current of the device (point 'A' in the figure) with the load inductance of 1mH is close to the peak avalanche current (point 'B' in the figure) of the device with the load inductance of 10mH, the device with the largest inductance has almost four times avalanche transient when compared with that of the device with the smallest inductance. However, one important event that the deviations of drain voltage (ΔV) with the different load inductances are monotonic during the avalanche transient, as it can be seen in Fig. 3.5(b).

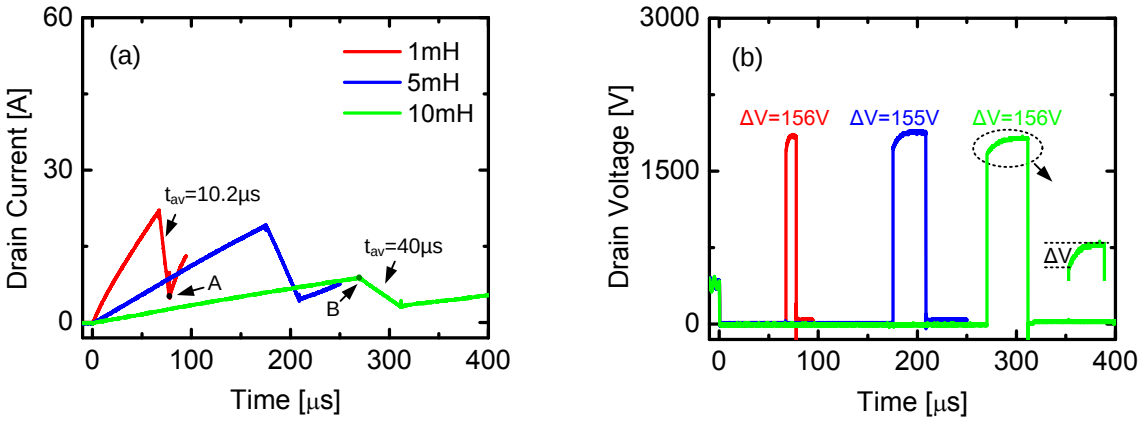


Fig. 3.5. Experimental results of (a) the drain current as a function of the on-state time, and (b) the drain voltage as a function of the on-state time for three SiC MOSFETs with the inductances of 1, 5 and 10mH, respectively.

Since the lattice temperature of the device is difficult to measure, previous study [22] have identified through the experimental result that the SiC device features a positive temperature coefficient of the breakdown voltage. The breakdown voltage of the SiC MOSFET depends, to a great extent, on the

ambient temperature if electric field at the drain terminal does not dramatically increase, which can be quantitatively illustrated by impact ionization coefficient (α) indicated by Chynoweth's law [23].

$$\alpha = (6.46\times10^{6} - 1.07\times10^{4}T)\cdot e^{-1.75\times10^{7}/E} \tag{45}$$

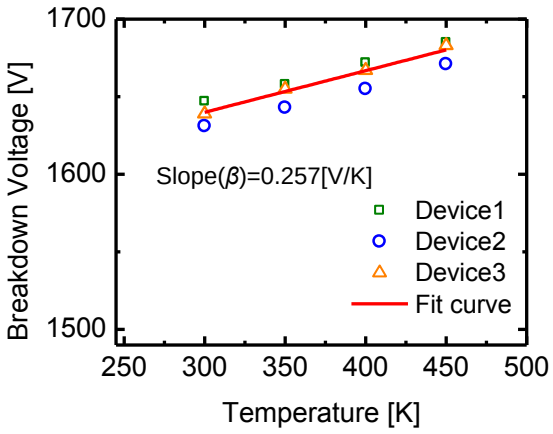


Fig. 3.6. Experimental results of breakdown voltages as functions of temperature for three SiC MOSFETs.

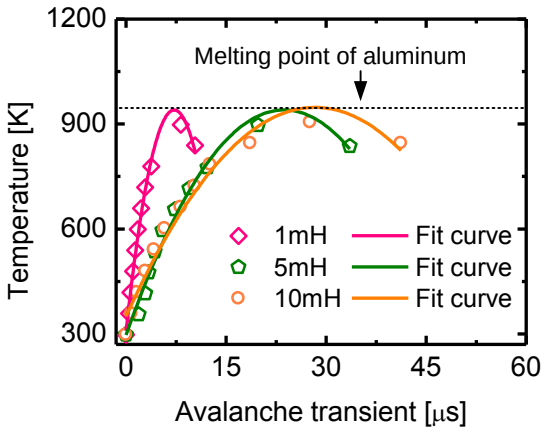


Fig. 3.7. Extrapolated results of rising lattice temperatures as functions of avalanche transient for three SiC MOSFETs with the inductances of 1mH, 5mH and 10mH, respectively.

From (45), the impact ionization coefficient could be reduced by the rising temperature, leading to a decrease to the multiplication coefficient and an increase to the breakdown voltage. Thus, the breakdown voltage is a good indicator for estimating the lattice temperature. To do that, the ambient temperature dependence of breakdown voltage for three SiC MOSFETs was subsequently conducted and analyzed at the end of the test. As it can be seen in Fig. 3.6, the slope of the fit curve gives a parameter (β) about the ambient temperature dependence of breakdown voltage, which equals to 0.257 in V/K. In addition to those results, every rising temperature point (ΔT) of the devices can be predicted using the following equation [24].

$$T_j = \Delta V / \beta + T_0 \tag{46}$$

Combined the above experimental results with fit curves [25], Fig. 3.7 exhibits a small difference between the tested devices due to the process discrepancy, the predicted maximum lattice temperatures of the three SiC MOSFETs are 940, 940 and 946 K for the load inductances of 1, 5, and 10 mH respectively. It is worth to note that these extrapolated values seem to be closed to the melting point of aluminum (934 K), which gives a possible point of view that the device reaches the failure limit leading into burning up of the metallic electrode pad.

3.1.1.2 Single-Pulse Tests at High Temperature

To the same extent, two new proposed methods give an investigation in order to characterize the avalanche event at the different ambient temperature based on the supervising of two parameters: a) avalanche energy and b) peak avalanche current. For that purpose, a load inductance of 1mH and the ambient temperature ranging from 300 to 450 K are selected for the tested SiC MOSFETs.

Temperature Dependence of Avalanche Energy Limit

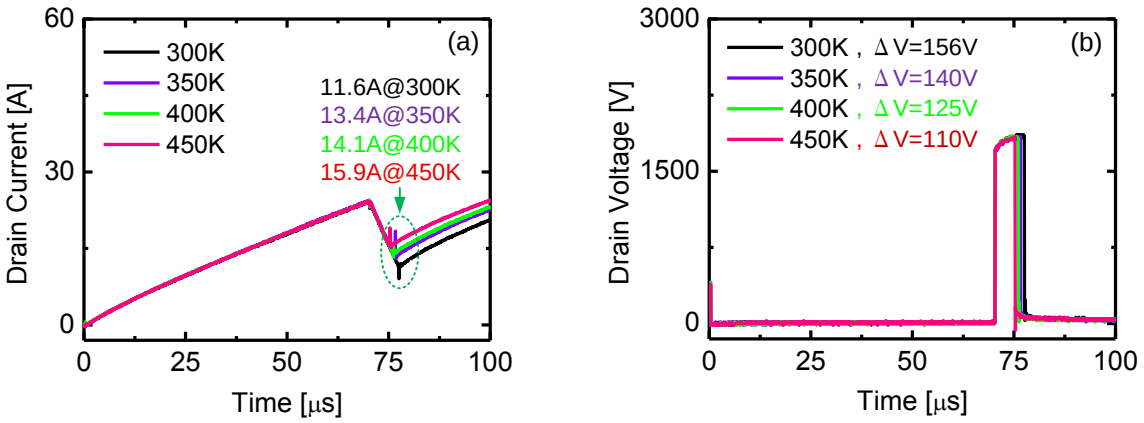


Fig. 3.8. Experimental results of (a) the drain current as a function of the operation time, b) the drain voltage as a function of the operation time for the SiC MOSFETs with the inductance of 1mH and the different ambient temperature ranging from 300 to 450 K by using the approach of avalanche energy limit.

Based on avalanche failures related to avalanche energy, a proposed approach is developed, which is dependent upon the negative dependence between avalanche energy and ambient temperature. The method is to define a peak avalanche current level (e.g., 24 A in Fig. 3.8(a)) during the avalanche event, which corresponds to the maximum avalanche energy limit sustained by the device. Meanwhile, the avalanche energy density can be described by (3).

$$E_{av} = \frac{1}{S_{\text{active}}} \int_0^{t_{av}} V_{av} \cdot I_{av} dt \tag{47}$$

Fig. 3.8(a) demonstrates that the defined peak avalanche current leads all of the tested devices to damage at different ambient temperature. It worth pointing out that despite the tested SiC MOSFETs have the same peak avalanche current, the sample with the higher ambient temperature is more inclined to breakdown. For instance, the avalanche transient decreased by 30.2% at the ambient temperature of 450 K when compared with that of the SiC MOSFET at the ambient temperature of 300 K. These results suggest that the temperature greatly impacts the avalanche capability for the SiC MOSFET. Similarly as the previous case, the variation of drain voltages (ΔV) for four SiC MOSFETs keeps a constant margin of 15 V at different ambient temperature, as it can be seen in Fig. 3.8(b). According to the aforementioned discussion, the failure points seem to occur at one critical temperature range.

Temperature Dependence of Peak Avalanche Current Limit

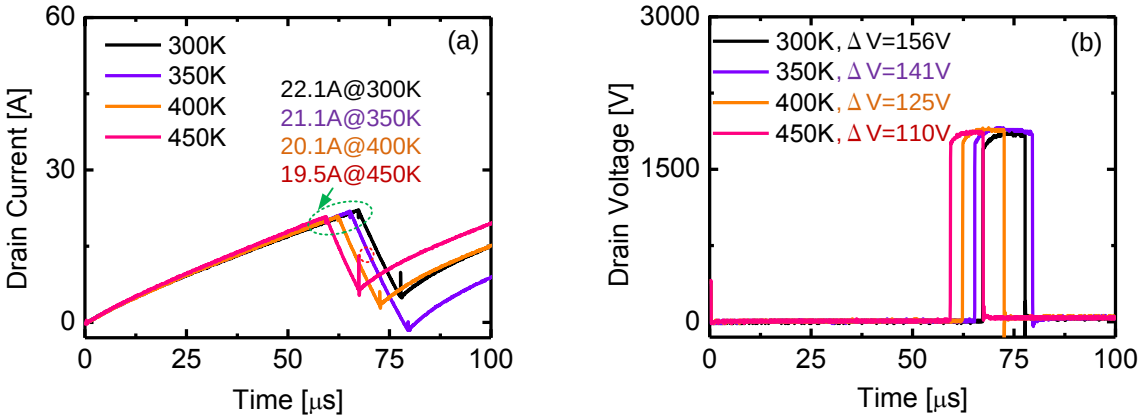


Fig. 3.9. Experimental results of (a) the drain current as a function of the operation time, b) the drain voltage as a function of the operation time for the SiC MOSFETs with the inductance of 1mH and the different ambient temperature ranging from 300 to 450 K by using the approach of peak avalanche current limit.

Based on the avalanche failures related to peak avalanche current, further verification is developed, which depends on the negative dependence between peak avalanche current and ambient temperature during avalanche event. This method constructs on applying a growth rate level (e.g., 0.1 A) for the peak avalanche during avalanche event, which corresponds to the peak avalanche current limit that sustained by the device. Fig. 3.9(a) shows that the peak avalanche current gradually decreases with increasing of the ambient temperature. Furthermore, there is a very important result that the avalanche failure occurs even the avalanche current has already fallen to zero at the ambient temperature of 350 K. This generated phenomenon exhibits a consequence that the device failure is largely dependent upon the lattice temperature induced by Joule heat, which may be the most possible thread for the SiC MOSFET since the critical criterion for avalanche robustness remains unknown. As it can be seen in Fig. 3.9(b), similarly as before, the variation of drain voltages (ΔV) for four SiC MOSFETs also keeps

a constant margin of 15 V at the different ambient temperature even the different evaluation method is adopted.

Lattice Temperature Prediction

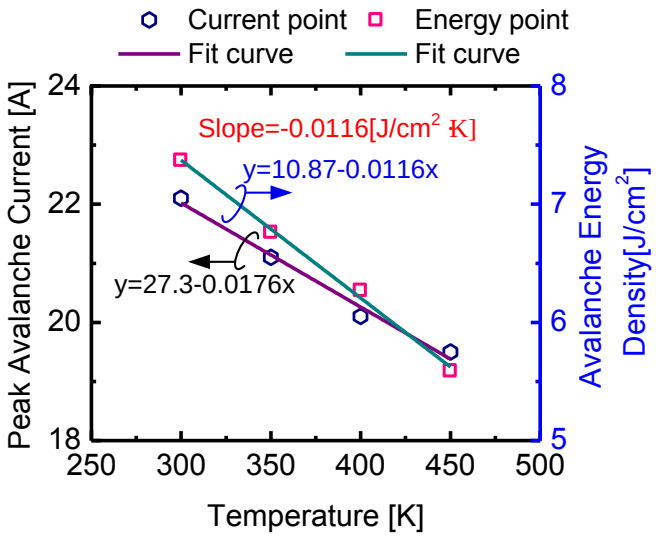


Fig. 3.10. Experimental results of the peak avalanche current and avalanche energy density as functions of the ambient temperature ranging from 300-450K.

In order to identify the critical operation conditions, Fig. 3.10 shows the results of the peak avalanche current and avalanche energy density as functions of the ambient temperature based on the experimental results in Fig. 3.8 and Fig. 3.9. The results with their fitting curve can be used to extrapolate the maximum lattice temperature during the avalanche event for the SiC MOSFET. To that end, the predicted principle is to find zero point-based avalanche energy density and peak avalanche current, which corresponds to the critical lattice temperature. From the fitting equations shown in Fig.3.10, the calculated critical lattice temperatures leading into the device failure for those two criteria are 937 and 1551 K respectively. These criteria exhibit an apparent difference probably due to the missing consideration of the critical failure factor for the peak avalanche current-based method. Additionally, the proposed approach relies on avalanche energy-dependent indicators seems to be more restrictive than the peak avalanche current criterion, although at the same test requirements. Therefore, the avalanche energy-dependent indicators could be easily applied for prediction of avalanche characterization at different temperatures.

3.1.2 Mathematic Models

In order to further validate the critical temperature leading into the avalanche failure for the SiC MOSFET, the mathematical models have been developed. Two processes have been adopted and identified based on the previous measurements on the SiC MOSFETs: a) on-state transient and b) avalanche transient.

3.1.2.1 On-state transient

When the positive bias voltage implied on the gate-source terminals exceeds the threshold voltage, the current flows from the power source to the drain side through the inductor. Concurrently, the energy can be stored during this period until the device turns off, which can be described by

$$E = \frac{1}{2} L I_{\text{peak}}^2 \tag{48}$$

Despite the high voltage power source is directly connected to the device and inductor, the lattice temperature can be ignored due to the relatively small power dissipation in a short on-state transient for the SiC MOSFET.

3.1.2.2 Avalanche transient

A. Safe operation

When the device switches off, the current is initially squeezed from the drain to source by means of linear reduction through the discharging of inductor. It may note that the higher voltage applied in the drain takes the SiC MOSFET into avalanche mode, resulting in a huge Joule heat that rises the lattice temperature. If the device can endure such high avalanche energy, as well as the high lattice temperature, the current performs a linear decrease and can be calculated as in

$$I_{av}(t) = I_{\text{peak}} - V_{av} \cdot t_{av} / L \tag{49}$$

The totally dissipated energy density from the beginning to any avalanche time can be given by

$$E_{av} = \frac{1}{2} L (I_{\text{peak}}^2 - I_{av}^2) \tag{50}$$

B. Avalanche failure

In fact, the device is not able to get through the avalanche period if the lattice temperature is high enough. Normally, the increasing temperature can be briefly estimated by using Ohm's thermal equivalent law as in

$$\Delta T = Z_{\text{th}} P \tag{51}$$

However, this equation is no longer adaptive for transient phenomenon and other quantities should be taken into account. The thermal diffusion equation could express the temperature as a function of coordination and time. It is a rigorously thermodynamic model to obtain the increasing temperature solution during the avalanche transient.

$$\rho \cdot c \cdot \frac{\partial T_{(x,y,z,\,t)}}{\partial t} = \nabla^2 (\kappa \cdot T) + Q_{(x,y,z,\,t)} \tag{52}$$

where

$$Q = \frac{P(x,y,z,t)}{V_{\text{volume}}} \tag{53}$$

TABLE 3.1

BASIC PARAMETERS OF THE SIC MATERIAL

Symbol	Parameters	SiC
c	Thermal capacity	0.6736 J/g·K
κ	Thermal conductivity	4.5 W/cm·K
ρ	Material density	3.21 g/cm^3
D_{sic}	Thermal diffusivity	2.21 cm^2/s

The basic parameters of silicon carbide material are listed in Table. 3.1. The solution of (52) can be solved by using Green function

$$\begin{aligned} T(r,t) &= T_0 + \int_0^{t_{av}} \frac{Q(t-\tau)}{\rho c} d\tau \int_{\Omega} G(r,r',t,\tau) dr' \\ &= T_0 + \int_0^{t_{av}} \frac{Q(t-\tau)}{\rho c} d\tau \\ &\quad \times \int_{\Omega} \left(\frac{1}{\sqrt{4\pi D_{\text{sic}} \tau}} \right)^3 \exp\left(\frac{-(r-r')^2}{4 D_{\text{sic}} \tau} \right) dr' \\ &= T_0 + \int_0^{t_{av}} \frac{Q(t-\tau)}{\rho c} d\tau \\ &\quad \times \int_{-x/2}^{x/2} \frac{1}{\sqrt{4\pi D_{\text{sic}} \tau}} \cdot \exp\left(\frac{-(x-x')^2}{4 D_{\text{sic}} \tau} \right) dx' \\ &\quad \times \int_{-y/2}^{y/2} \frac{1}{\sqrt{4\pi D_{\text{sic}} \tau}} \cdot \exp\left(\frac{-(y-y')^2}{4 D_{\text{sic}} \tau} \right) dy' \\ &\quad \times \int_{-z/2}^{z/2} \frac{1}{\sqrt{4\pi D_{\text{sic}} \tau}} \cdot \exp\left(\frac{-(z-z')^2}{4 D_{\text{sic}} \tau} \right) dz' \end{aligned} \tag{54}$$

where

$$D_{\text{sic}} = \frac{\kappa}{\rho c} \tag{55}$$

Supposing the location of maximum lattice temperature is in the center of device surface, (54) then can be simplified as

$$T(0,t) = T_0 + \frac{Q}{\rho c} \int_0^{t_{av}} d\tau \cdot \operatorname{erf}\left(\frac{x}{4\sqrt{D_{\text{sic}} \tau}} \right) \cdot \operatorname{erf}\left(\frac{y}{4\sqrt{D_{\text{sic}} \tau}} \right) \cdot \operatorname{erf}\left(\frac{z}{4\sqrt{D_{\text{sic}} \tau}} \right) \tag{56}$$

Here, *erf* is error function can be expressed using same approximation method in [26].

$$
\begin{aligned}
erf(x) &= \frac{2}{\sqrt{\pi}}\int_0^x e^{-t^2}dt \\
&= \frac{2}{\sqrt{\pi}}\sum_{n=0}^{\infty}\frac{(-1)^n \cdot x^{2n+1}}{n!(2n+1)} \\
&\approx \begin{cases} \frac{2}{\sqrt{\pi}}x & (x \le \frac{\sqrt{\pi}}{2}) \\ 1 & (x > \frac{\sqrt{\pi}}{2}) \end{cases}
\end{aligned}
\tag{57}
$$

For the SiC MOSFET, the three dimension parameters of device are particularly larger than the thermal diffusion distance due to relatively thicker substrate layer and larger active area. Hence, it is obvious that *erf* (*x/4sqrt*($D_{sic}\tau$) can be considered to be one. (56), then, can be calculated as in

$$
\begin{aligned}
T(t) &= T_0 + \frac{Q}{\rho c} \\
&= T_0 + \frac{Pt}{V_{volumn}\rho c} \\
&= T_0 + \frac{Pt}{S_{active}(W_{drift} + \sqrt{D_{sic}t_{av}})\rho c} \\
&= T_0 + \frac{E_{av}}{(W_{drift} + \sqrt{D_{sic}t_{av}})\rho c}
\end{aligned}
\tag{58}
$$

Additionally, the temperature distribution profile of the SiC MOSFET at the end of avalanche transient can be illustrated by described by (59) [16, 27].

$$
T(z,t_{av}) = \frac{E_{av}}{(W_{drift} + \sqrt{D_{sic}t_{av}})\rho c} e^{-(z/\sqrt{D_{SiC}t_{SC}})} + T_0 \tag{59}
$$

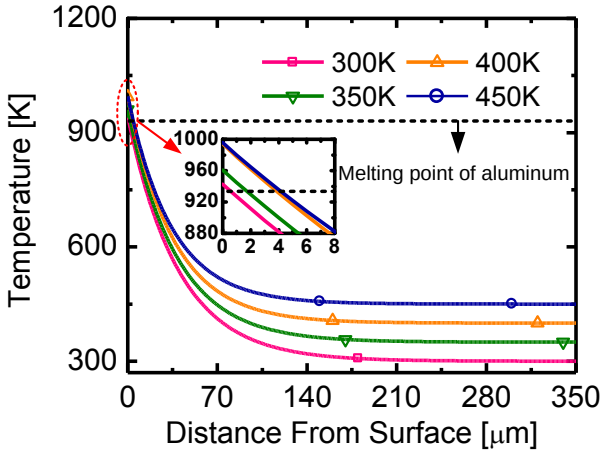


Fig. 3.11. Lattice temperature profile as function of device thickness.

Fig. 3.11 shows the calculated lattice temperature profiles as a function of the device thickness based on (59) at different ambient temperature. According to the calculated results, the maximum temperatures are ranging from 942 to 995 K during the avalanche transient. It should be noted that the thermally generated leakage current is able to accelerate the increase of lattice temperature due to the positive temperature coefficient. Therefore, the calculated lattice temperature is tiny higher at the ambient temperature of 450 K compared with that of the device at the ambient temperature of 300 K, as shown in the enlarged figure in Fig. 3.11. Moreover, the increasing lattice temperature is highly determined not only by the thermal characteristic of SiC material but by the dimension parameters of the device. It is effective to promote the avalanche capability by adopting the larger active area and thicker drift layer. For this reason, the SiC MOSFET with high rated voltage/current has congenital advantages in the avalanche robustness. Furthermore, the ambient temperature dependence of avalanche energy density, thus, can be expressed by

$$\begin{aligned}\frac{dE_{\text{av}}}{dT_0} &= -(W_{\text{drift}} + \sqrt{D_{\text{sic}} t_{av}})\rho c \\ &= -(13+40)\ [\mu\text{m}] \times 3.21\ [\text{g/cm}^3] \times 0.6736\ [\text{J/g}\cdot\text{K}] \\ &= -0.0115\ [\text{J/cm}^2\cdot\text{K}]\end{aligned} \tag{60}$$

The parameter of ambient temperature dependence of avalanche energy density, from (60), is calculated to be -0.0115 J/cm^{2}K, which shows a good match with the experiment result of -0.0116 J/cm^{2}K in Fig. 10. This model, hence, can be used to properly estimate the lattice temperature for the SiC MOSFET.

3.1.3 Simulation Results

Further validation of the mathematical models and the experimental findings, the numerical simulation is carried out using the TCAD device simulator. The avalanche characterization in simulation is mainly determined by two failure criteria: a) the thermal runaway inside the device and b) melting of metal on the surface of the device.

Table 3.2 and Fig. 3.12 show the ambient temperature dependence of the avalanche energy density settled by the experimental and simulation results. It is obvious that the simulation results using the metal melting-based failure criterion are in good agreement the experimental results. The slope in the fit curve is calculated to be -0.012 J/cm^{2}K, which is highly similar with the experiment result in Fig. 3.10. Therefore, from the results it can be concluded that the device fails in a temperature range which is independent upon the test condition (e.g., the load inductance and power source). The failure temperature window demonstrated in the aforementioned discussion exceeds the melting point of source metallization. Additionally, the average critical temperature for avalanche failure is considered to be 966 $\pm$ 5% K (average calculation), which is much smaller than the critical intrinsic temperature (e.g., 1515 K in this study). The high lattice temperature leading to the premature degradation of surface metallization and the gate electrode is the main factor taking responsibility for the avalanche failure.

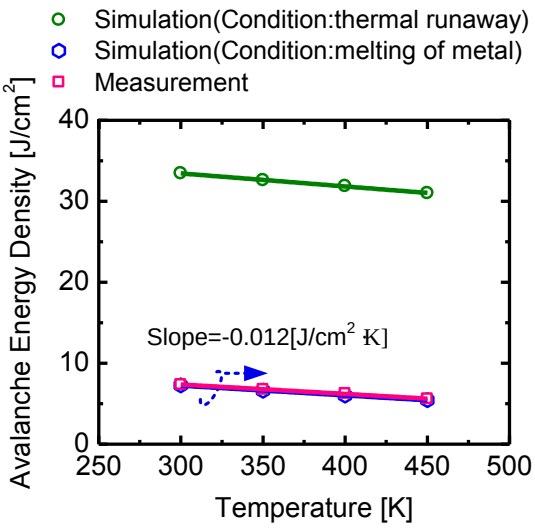


Fig. 3.12. Simulation and experimental results of avalanche energy density as a function of ambient temperature

TABLE 3.2

Temperature dependence of avalanche energy density

Temperature (K)	Measurement (J/cm^2)	Simulation(J/cm^2)	
		Melting of metal	Thermal runaway
300	7.39	7.25	33.4
350	6.76	6.61	32.6
400	6.27	6.01	31.9
450	5.59	5.44	31.0

3.2 Short-Circuit Capability for SiC n-MOSFET

Owing to the wide band gap and large dielectric constant of silicon carbide material, the SiC device exhibits electrical properties and reliability superior to those of the Si device, such as the thin drift layer, the lower on-state resistance, the extremely high operation temperature, and so on. Therefore, a low conduction loss, as well as a small lattice temperature fluctuation, can be realized when the device is normally switched on. However, the device will be irreversibly damaged after 10 μs of the occurrence of short circuit, caused by the on-state of both devices in the upper and lower arms of the application circuit. Moreover, the short-circuit withstand time is crucial for the protection circuit; thus, the short-circuit capability of the device must be carefully considered and evaluated.

3.2.1 Evaluation of Short-Circuit Capability of SiC n-MOSFET

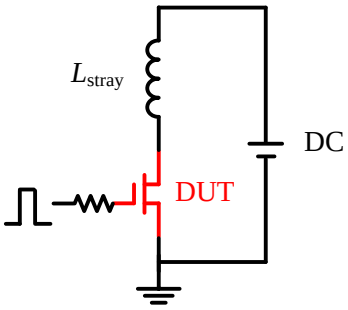


Fig. 3.13. Schematic of short-circuit test for tested SiC MOSFET

The short-circuit capability of the 1200 V SiC MOSFET is evaluated by using the test circuit as shown in Fig. 3.13. The device under test is one chip in the package of TO247 with the rated current of 19 A. The voltage of power supplier ranges from 0 to 600 V. The gate driver with voltages of 18/-5 V to turned on and off the device. Because the effect of gate resistance on the short-circuit capability can be ignored, the gate resistance connected to the gate driver is fixed at 47 Ω.

Figures 3.14(a) and 3.14(b) show the drain current and gate voltage waveforms of the SiC MOSFET with a 400 V power supplier, respectively. It is obvious that the drain current increases promptly at beginning of the transient. Then, the device enters from the linear region to the active region until achieving its peak current at the initial pulse time. After that, the drain current decreases from 117 to 51.6 A due to the degradation of the carrier mobility with the increasing lattice temperature. The drain current becomes horizontal when the device tends to fail during short-circuit transient. Similar with that of the Si IGBT, the tail current of the SiC MOSFET become large if the on-state time is long. The tail current sustains for 4 μs after the device turns off. Moreover, the gate voltage applied in the SiC MOSFET gradually decreases when the on-state time of the device increases.

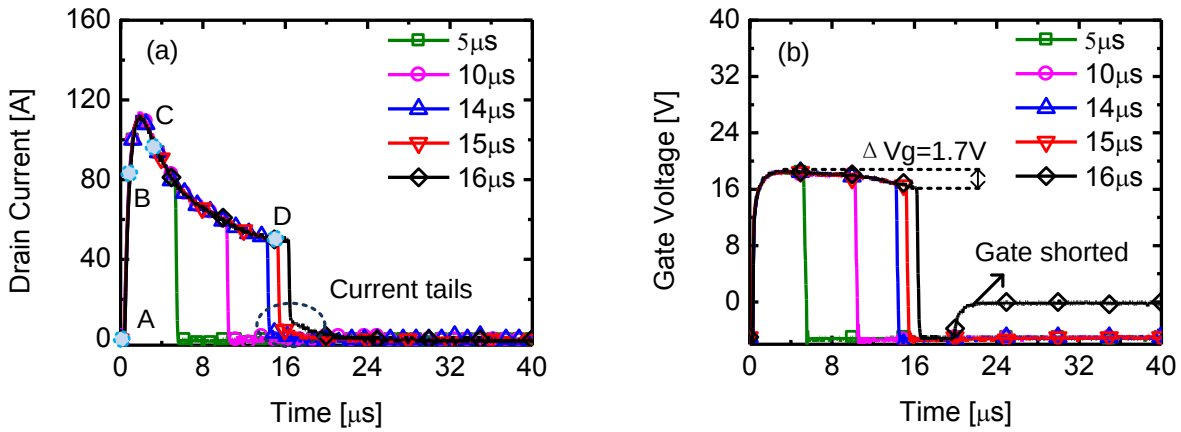


Fig. 3.14. (a) Experimental results of the time dependence of drain current waveforms with maximum short-circuit withstand time of 16 μs and 400 V DC bus. (b) Experimental results of degradation of gate voltage with maximum short-circuit withstand time of 16 μs and 400 V DC bus.

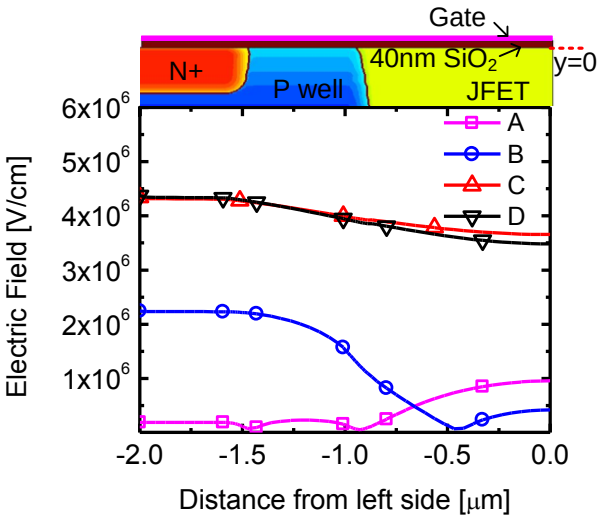
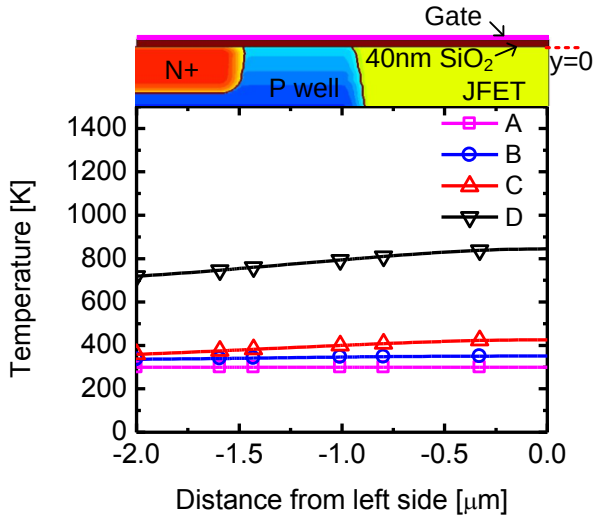


Fig. 3.15. Simulation results of electric field profile in gate oxide at four points of short-circuit transient for SiC MOSFET with gate oxide of 40 nm, maximum short-circuit withstand time of 16 μs, and 400 V DC bus.

Generally, the thickness of the gate oxidation layer in SiC MOSFETs is around 30 to 100 nm. The most prominent oxide degradation in SiC can be deemed the Fowler-Nordheim (FN) tunneling and Poole-Frenkel (PF) emission effect. It can lead to a leakage current at the high gate electric field and lattice temperature. This degradation can be tested by time-dependent dielectric breakdown (TDDB) [28, 29]. It was reported that a large increase in FN current will occurs when the temperature increases to 523 K. At same time, the effective barrier height between SiC and oxide decreases to 2.38 eV when the temperature increase to 573 K. Thus, the high temperature can affect the reliability of gate oxide layer.



(b)

Fig. 3.16. Simulation results of lattice temperature profile at four points of short-circuit transient for SiC MOSFET with gate oxide of 40 nm, maximum short-circuit withstand time of 16 μs, and 400 V DC bus at y=0 μm.

Figs. 3.15 and 3.16 show the simulation results about the electric field in gate oxide and lattice temperature profiles at the interface of SiC and oxide (y=0 μm) at four points of the short-circuit transient as shown in Fig. 3.14(a). When the gate voltage increases from -5 to 18 V, the electric field in gate oxide layer gradually increases to the maximum point, as shown at points A to C in Fig. 3.15. It is obvious that the maximum point of the electric field shifts from the JFET region to the source region. However, there is a small difference in electric field in the JFET region between points C and D even at the same gate voltage bias. This is because the lattice temperature increases as the short-circuit time increases. Therefore, more holes are produced and the carrier concentration increases in the JFET region. This can relieve the electric field in gate oxide at the high lattice temperature. As shown in Fig. 3.16, the ruggedness between the gate and the source terminal cannot be ignored at point D with the high electric field of 4.3 MV/cm and the high lattice temperature of 844 K. This directly explains reason why the gate voltage decrease from 18 to 16.3 V, as shown in Fig. 3.14(b).

The resistance of the three terminals after the device failure between the gate, drain and source (Rgs, Rgd, and Rds) are tested to be 2.6, 8.6 M, and ∞ Ω, respectively. These results indicate that the gate-source terminal of the device is finally shorted and the gate oxide layer is irreversible breakdown. In addition, the breakdown voltage of the failure device remains to be around 1218 V at the drain leakage current of 0.2 mA, as shown in Fig. 3.17. This voltage has been reduced compared with that of the fresh device. This is because the generation of holes induced by large lattice temperature in the top JFET area causes the electric field centralization at the p-well/n drift junction. These results show that failure does not exist in the drain-source terminal, but in the gate oxide layer. The short-circuit energy is calculated to be 12.8 J/cm^2 by the equation during this period:

$$E_{SC} = \int_0^{t_{SC}} VIdt \tag{61}$$

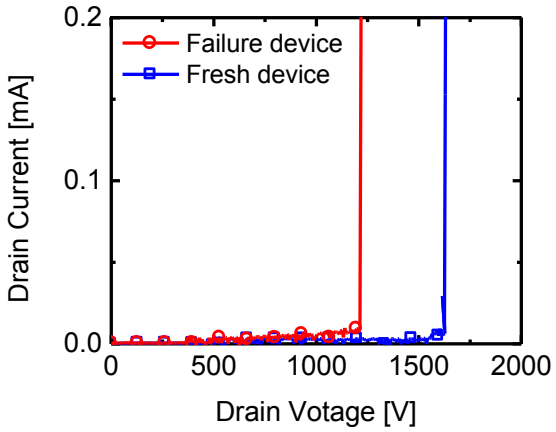


Fig. 3.17. Experimental results of breakdown voltage between gate oxide failure device and fresh device.

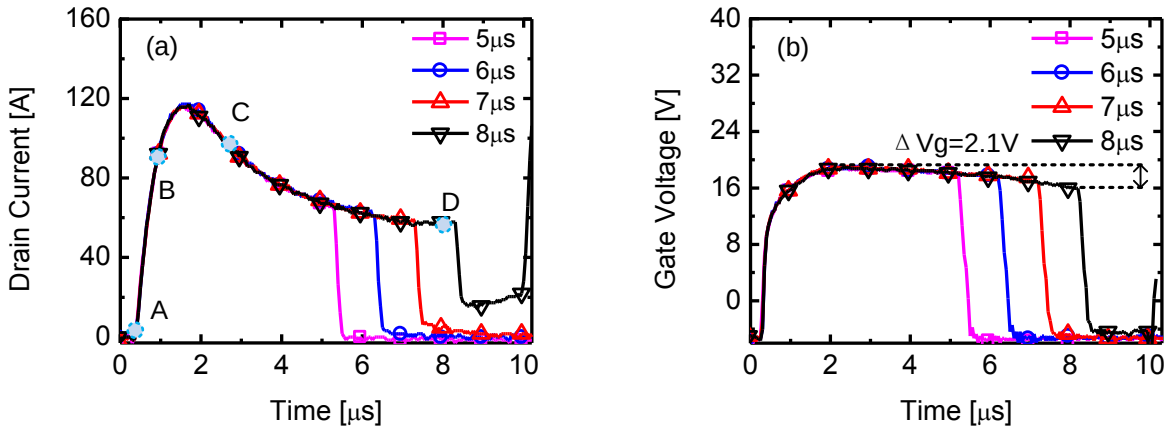


Fig. 3.18. (a) Experimental results of the time dependence of drain current waveforms with maximum short-circuit withstand time of 8 μs and 600 V DC bus. (b) Experimental results of degradation of gate voltage with maximum short-circuit withstand time of 16 μs and 600 V DC bus.

To investigate the device reliability during short-circuit transient, the experiment performs under much harsher condition. Figures 3.18(a) and 3.18(b) show the short-circuit current and gate voltage waveforms as functions of time at room temperature with a 600 V power supplier. Different from the former case, the drain current is not controlled by the gate driver anymore. The thermal runaway eventually occurs when the short-circuit withstand time increases from 5 to 8 μs. The tail current can also be seen after the device switches off, as it can be shown in Fig. 3.18(a). Furthermore, the gate voltage gradually decreases from 18 to 15.9 V. This value is much higher than that of the former case. The short-circuit energy is calculated to be 19.4 J/cm^2.

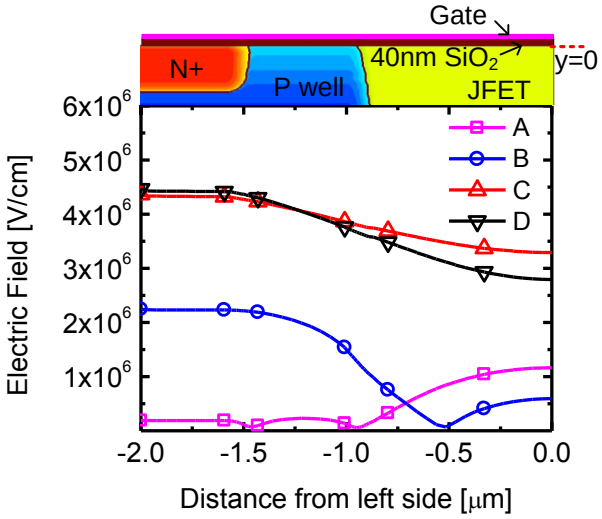


Fig. 3.19. Simulation results of electric field profile in gate oxide at four points of short-circuit transient for SiC MOSFET with gate oxide of 40 nm, maximum short-circuit withstand time of 8 μs, and 600 V DC bus.

In addition, Figs. 3.19 and 3.20 exhibit the simulation results about the electric field in gate oxide and lattice temperature profiles at the interface between SiC and gate oxide layer with a 600 V power

supplier. Different from the former case, the difference in electrical field between points C and D is much larger than that of the device with the 400 V power supplier. This is because the number of hole is dramatically increased by the 1500 K lattice temperature in the top JFET area, as shown in Fig. 3.20. The hole and electron generated by high lattice temperatures in the top JFET and source areas can affect the electric field in the oxide. Furthermore, not only the electric field but also the intrinsic carrier concentration can be effected by the ultrahigh lattice temperature. Therefore, once the electric field and intrinsic carrier exceed the critical safety condition of the device, the failure may occur.

After device failure, the resistances in the three terminals between the gate, drain, and source (Rgs, Rgd, and Rds) are tested. They are 0.2, 0.6, and 0.6 Ω, respectively. It is indicated that the three terminals are completely damaged due to at high lattice temperatures.

As discussed above, the failure modes with different voltage of power supplier are totally different. The gate oxide layer is easier to be damaged with relatively low power supplier after the device turn-off due to a long short-circuit transient. The FN tunneling and PF emission can take responsible for this failure. In addition, if the high voltage of power supplier is implied in the SiC MOSFET, the huge Joule heat can generated and accumulated inner the device, resulting in the thermal runaway. Both two failure modes are related to the lattice temperature. Sometimes, it can be define as the temperatures dependent short-circuit capability.

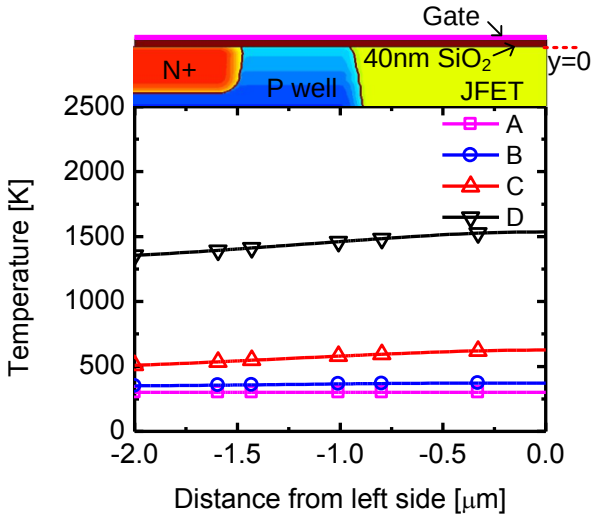


Fig. 3.20. Simulation results of lattice temperature profile at four points of short-circuit transient for SiC MOSFET with gate oxide of 40 nm, maximum short-circuit withstand time of 16 μs, and 400 V DC bus at y=0 μm.

3.2.2 Mathematical Analysis of Lattice Temperature for Two Failure Modes

Because there is no loading component in the circuit when short-circuit mode occur, the drain current is only determined by the saturation current. The short-circuit energy can be wrote by

$$P_{SC} = J_{sat} \cdot V \tag{62}$$

Moreover, the thermal diffusion equation, which indicates the dependence of short-circuit withstand time on coordination and time, is a rigorous thermodynamic model that can be used to obtain the rising

temperature solution during short-circuit transient. In fact, the direction of thermal diffusion is essentially from the surface of the die to the bottom of the case due to the presence of a heat sink. Therefore, the vertical direction of the device is significant to be taken account. The temperature distribution can be expressed by

$$\rho \cdot c \cdot \frac{\partial T_{(z,\, t_{SC})}}{\partial t} = \nabla^2 (\kappa \cdot T) + \frac{P_{SC} t_{SC}}{V_{volume}} \tag{63}$$

where c and κ are the heat capability and thermal conductivity, respectively. V_{volume} is the thermal volume, which includes the parameters of the active area and n drift layer.

The temperature distribution solution based on Eq. (63) can be rewrote as

$$T(z, t_{SC}) = \Delta T e^{-(Z/\sqrt{D_{SiC} t_{SC}})} + T_A \tag{64}$$

$$\Delta T = \frac{E_{SC}}{A V_{volume} \rho c} \tag{65}$$

where T_A is the case temperature at the initial time of short-circuit transient, ρ is the material density for SiC, and Z is the thickness of the device. The parameter A is a fitting value by taking thermal diffusion parameters into account. They are 10.8 and 7.71 for those two failure modes, respectively.

Equations (64) and (65) show that the short-circuit capability of the SiC MOSFET depends not only on thermal properties of the material but also on the dimensional parameters of the device. The short-circuit capability can be greatly improved by increasing the thickness of drift layer and active area of the device.

Finally, the temperature distribution profile along 300 μm wafer thickness is shown in Fig. 3.21. It can be seen that the maximum temperature is located at the device surface with an exponential decay. The maximum temperatures are 848 and 1463 K for two failure modes, which are with power supplier voltages of 400 and 600 V, respectively. The theoretical analysis results are in good agreement with the simulation ones. Therefore, mathematical models can be used to accurately predicted the critical temperature during short-circuit transient, if more device design information are provided.

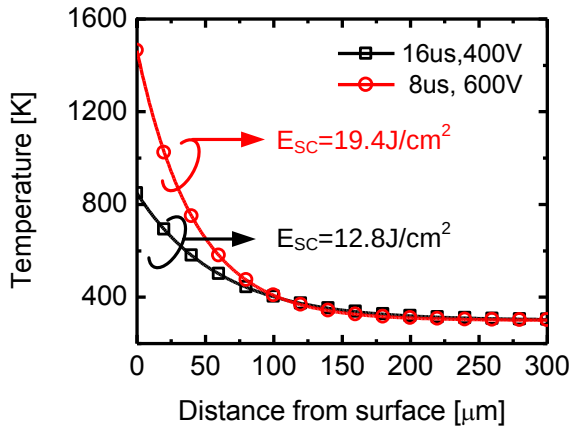


Fig. 3.21. Calculation of the temperature distribution profile for different test conditions.

3.3 Methodology for Enhanced Short-Circuit Capability

In the power inverter circuit, high switching frequency is highly required to downsize the passive component as a result of reducing of the power dispassion to the whole power system. Silicon carbide (SiC) power MOSFETs, without any tail current after the device turns off, are superior candidates that can be wildly used in the inverter system. However, about 1μs of dead time should be set to avoid the short-circuit event of a half bridge in the conventional inverter. Actually, the ultra-high switching frequency could cause the electro-magnetic interference (EMI) to the gate driver, resulting in the on-state of the device even it is switched off. Moreover, when the device on the upper arm of a half bridge turns on, a reverse recovery current from the body diode or the external SBD on the lower arm generates a drain-source voltage to the device on the lower arm. The transient current ($I=Crss \cdot dV/dt$) flows into the gate resistance through the reverse transfer capacitance (Crss), leading to a rising gate voltage. Once this voltage exceeds the gate threshold voltage, the device turns on, and therefore short-circuit event occurs on both the upper and lower arms at the same time. To prevent this unexpected short-circuit event, a valid method is to increase the negative gate bias voltage. However, different from the conventional inverter, the gate switch-on and off voltages controlled by only one gate driver in complementary inverter are 15/-15 and 0 V for the n/p-channel SiC MOSFETs, respectively. The influence of gate switch-off voltage for the device between gate and source cannot be ignored. Owing to the high requirement of stability for the whole application system, thus, it is essential to explore the optimized methods or structures for the SiC MOSFET with much higher short-circuit capability.

In this section, the gate switch-off voltage dependence of short-circuit capability for the SiC MOSFET is presented by the experimental measurement and numerical simulation. In addition to this, the unique failure mechanisms of SiC MOSFETs during the short-circuit state and robustness-enhanced operation are investigated and demonstrated by the experimental and numerical analyses. At last, by preventing the premature degradation of gate oxide layer and further improve the short-circuit capability during the short-circuit transient, a novel structure with L-shaped gate and LDD region is proposed. The proposed structure greatly reduces the electric field in the gate oxide layer and improves the short-circuit capability for the device.

3.3.1 Gate Voltage Dependence

An investigation of short-circuit failure with different DC voltages are very important because the DC input voltage would be frequently changed to control the output AC motor speed. The devices under test are 1.2 kV/10 A SiC MOSFET. Figure 3.22 shows the experimental results of (a) the drain current, (b) drain voltage, (c) short-circuit energy, and (d) gate voltage as functions of short-circuit transient with a DC bus of 600 V at room temperature. The gate switch-off voltages are -5 V and -10 V, respectively. It is obvious that the drain current in Fig. 3.22(a) increases promptly and the device enters from the linear region to the active region until achieving its saturation current at the initial pulse time. After that, the drain current decreases from a peak current of 110 A to 54.6 A due to the degradation of carrier mobility and the slope of drain current become horizontal at the end of

short-circuit transient. From the experimental results, the device fails at the short-circuit transient of 9 us. However, the tail current gradually decreases with a gate switch-off voltage of -10 V when device turns off. On the contrary, the device shows the increase of tail current with a gate switch-off voltage of -5 V. The devices with gate switch-off voltage of -5 V finally damage in not only the junction but gate oxide due to almost zero voltage withstand capability for *pn* junction and gate- source terminals after the device failure, as shown in Fig. 3.22 (b) and (d). The calculated short-circuit energy are 11.7 J/cm^2 during the short-circuit period for the both devices.

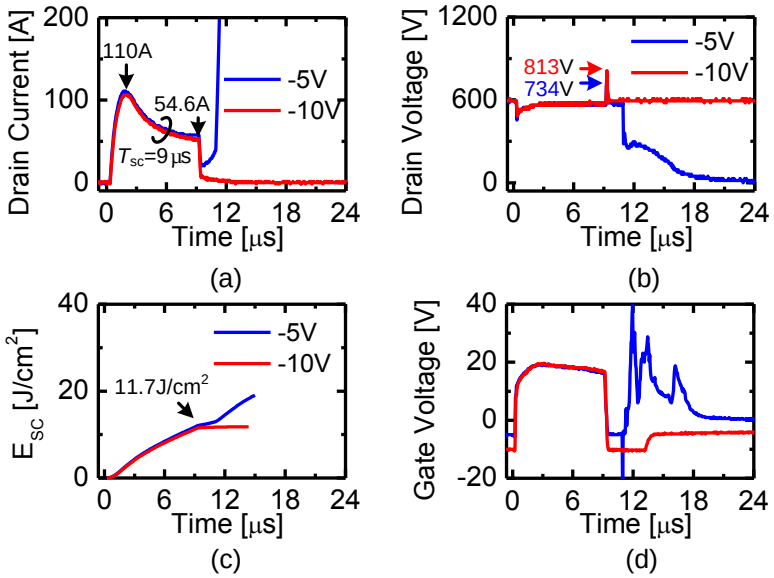


Fig. 3.22. Experimental results of short-circuit waveforms for the 1200V SiC MOSFET at room temperature. (a) the drain current, (b) the drain voltage, (c) the short-circuit energy, and (d) the gate voltage as functions of the short-circuit transient with the DC voltage of 600V and the gate turn-off voltage of -5V and -10V.

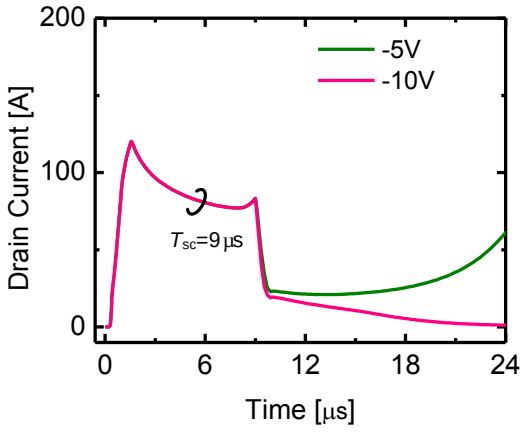


Fig. 3.23. Simulated drain current as a function of the short-circuit transient with the DC voltage of 600V and the gate turn-off voltage of -5V and -10V at room temperature.

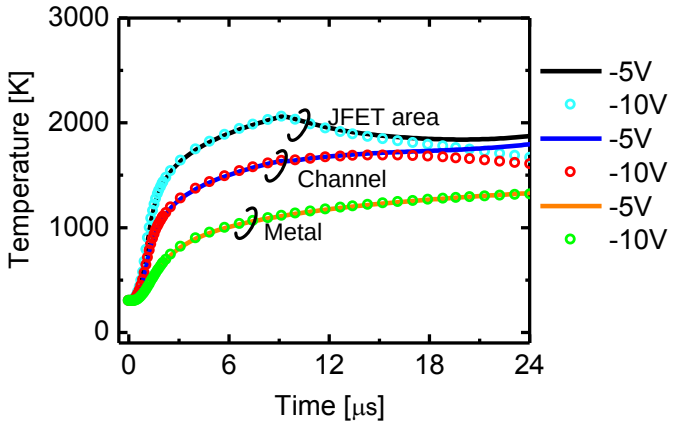


Fig. 3.24 Lattice temperature as a function of the short-circuit transient with the DC voltage of 600V and the gate turn-off voltage of -5V and -10V at room temperature.

As discussed before, two failure mechanisms are recognized for the short-circuit failure. One is that increasing of leakage current produced by the high lattice temperature triggers on-state of the parasitic of *npn* transistor during relatively transitory short-circuit period. The second one is the melting of material or degradation of SiO_2 during relative long short-circuit transient, resulting in the gate shorted between gate and source terminals. The lattice temperature is the main point that takes responsibility for those failures.

In order to further investigate the relationship between the gate switch-off voltages and short-circuit capability, the systematic numerical simulations by using Sentaurus TCAD are implemented. Fig. 3.23 exhibits the simulation results of the drain current for the SiC MOSFET with the gate turn-off voltage of -5 V and -10 V. It should be noted that the simulated current waveforms are in good agreement with the experimental ones and the device fails at the short-circuit transient of 9 us.

Fig. 3.24 shows the simulation results about short-circuit transient dependence of lattice temperature with a DC bus of 600 V and gate turn-off voltage of -5 V and -10 V, respectively. It is obvious that the maximum lattice temperature nearby channel region increases to 1750 K at the switch-off point.

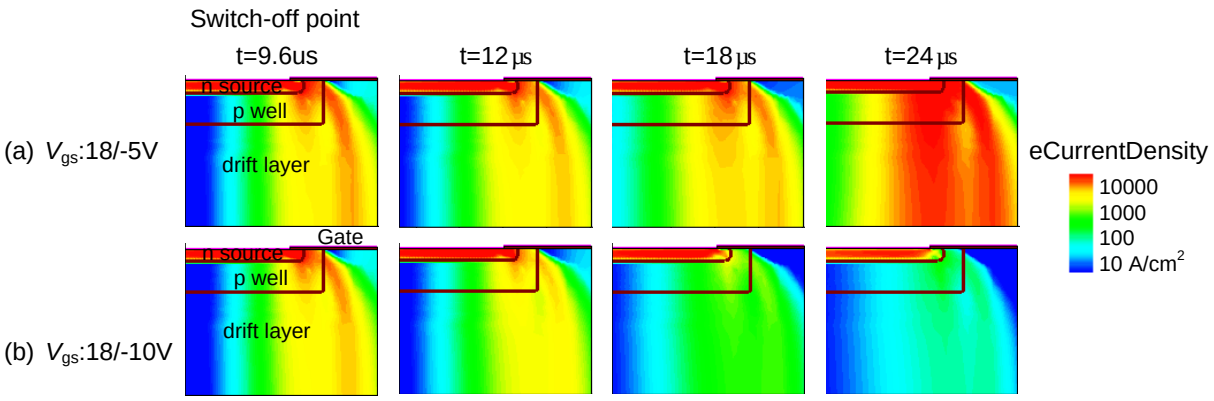


Fig. 3.25. Simulation results of the electron current density distribution with different short-circuit period.

Fig. 3.25 gives the calculated results of the electron current distribution during the short-circuit transient. It is clear that the electron current keeps flowing through the MOS channel after the device switches off at gate turn-off voltage of -5 V.

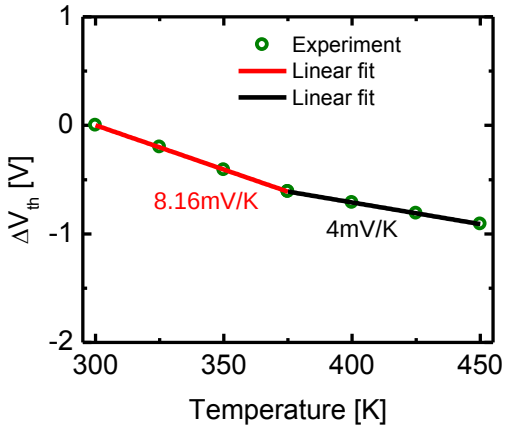


Fig. 3.26. Experimental results of temperature dependence of threshold voltage decrease. The minimum threshold voltage of the device is 2 V at room temperature. ΔV_{th} is equal to -7V when the lattice temperature increases to 1750 K.

Furthermore, Fig. 3.26 shows the experimental and fitting results of temperature dependence of threshold voltage decrease (ΔV_{th}). In order to simply fit the experiment result, only two linear lines (not smooth line) are used. The minimum threshold voltage of the device is 2 V at 298 K and the ΔV_{th} is equal to -7V when the temperature increases to 1750 K. Combined with these results, the authors conclude that the SiC MOSFET is more likely to be destroyed by the uncontrollable gate switch-off. Therefore, the larger gate turn-off voltage can effectively improve the short-circuit capability by reducing the probability of channel normally-on induced by the higher lattice temperature.

3.3.2 Gate Oxide Layer Thickness Dependence

It was reported that the trench MOSFET with thin gate oxide layer suffered from both high electric field and temperature, leading to the gate oxide layer rapture. Figs.3.27 and 3.28 exhibit the comparison of short-circuit waveforms with the DC voltage of 400V between the 1200V SiC trench MOSFETs with thin and thick gate oxide layers. The robustness enhanced MOSFET with the thick gate oxide of 85nm shows the high short-circuit capability even with higher short-circuit energy and longer short-circuit transient. From the measured resistances between all electrodes after the device failure as shown in table 3.3, it is clear that the failure modes of two devices are totally different and the short-circuit capability is successfully improved by thickening gate oxide. Therefore, moderately thick gate oxide layer is required to avoid short-circuit failure related to the gate oxide breakdown in the SiC MOSFETs before the thermal runaway occurs.

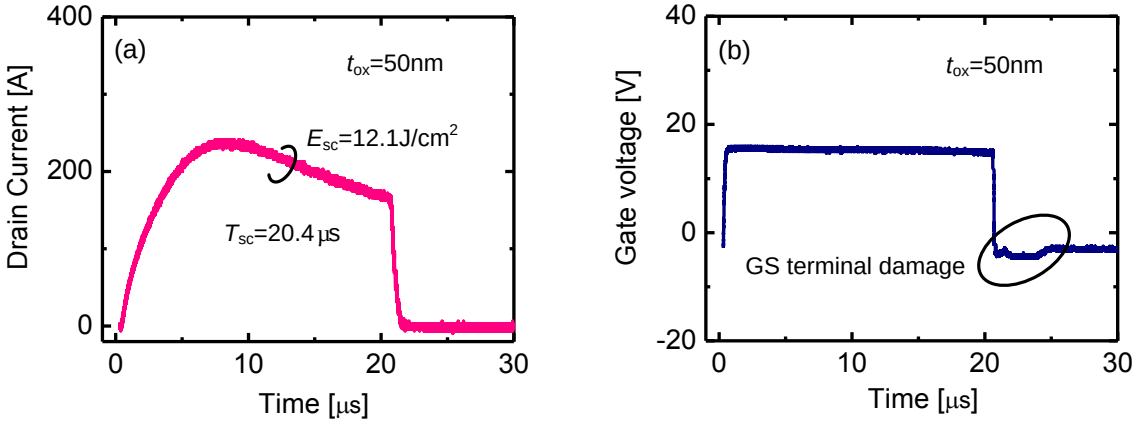


Fig. 3.27. The short-circuit waveforms with the DC voltage of 400V for the SiC trench MOSFETs with SiO_2 thickness of 50nm at room temperature. (a) the drain current, and (b) the gate voltage. The electric field relaxation structures at the trench bottom are applied to the MOSFETs. $R_{on,sp}$ are 2.9mΩcm^2 (50nm) at V_g=20V.

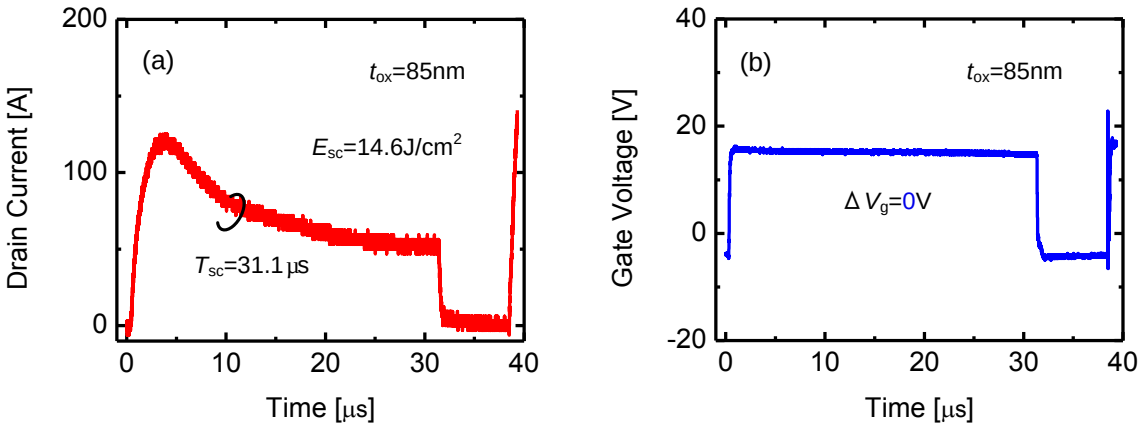


Fig. 3.28 The short-circuit waveforms with the DC voltage of 400V for the SiC trench MOSFETs with SiO_2 thickness of 85 nm at room temperature. (a) the drain current, and (b) the gate voltage. The electric field relaxation structures at the trench bottom are applied to the MOSFETs. $R_{on,sp}$ are 3.88mΩcm^2 (85nm) at V_g=20V.

TABLE 3.3

Impedance test after device failure

Symbol	SiO_2:50nm	SiO_2:85nm
R_{gs}	167 Ω(Shorted)	3.4 Ω (Shorted)
R_{ds}	∞(Blocking)	9.8 Ω(Shorted)
R_{gd}	23 MΩ(Blocking)	10.6Ω(Shorted)

R_{gs}: Resistance between gate and source,

R_{gd}: Resistance between gate and drain,

R_{ds}: Resistance between drain and source.

3.3.3 New Structure Dependence

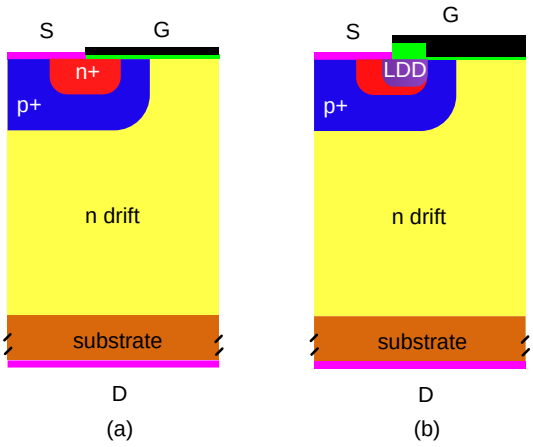


Fig. 3.29 Cross section of 4H SiC MOSFET and (b) the proposed SiC MOSFET.

The new structures with the lightly doped drain (LDD) process in source region and L-shaped gate oxide layer in gate are proposed in this letter to improve the short-circuit capability, as shown in Fig. 3.29(b). The LDD is used to reduce the electric field strength, the hot electron injection effect in the source region. As demonstrated in former section, the much thicker gate oxide layer on the top of source region to prevent the gate oxide degradation and gate shorted caused by Fowler-Nordheim (FN) tunneling and Poole-Frenkel (PF) emission effect at ultra-high lattice temperature.

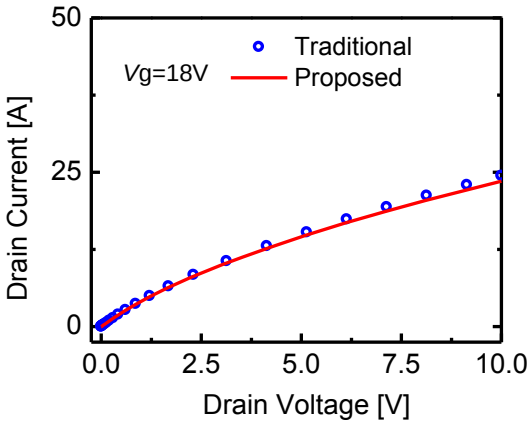


Fig. 3.30. Comparative simulation results for the traditional and proposed structure of on-state characteristic.

From the simulation results, as shown in Fig. 3.30, despite the doping concentration has been reduced in source region, the on-state characteristic of proposed device is similar with that of the traditional SiC MOSFET.

The electric field in gate oxide is dramatically reduced for proposed structure, especially in the source region due to thicker oxide layer upper the n source region, as shown in Fig. 3.31.

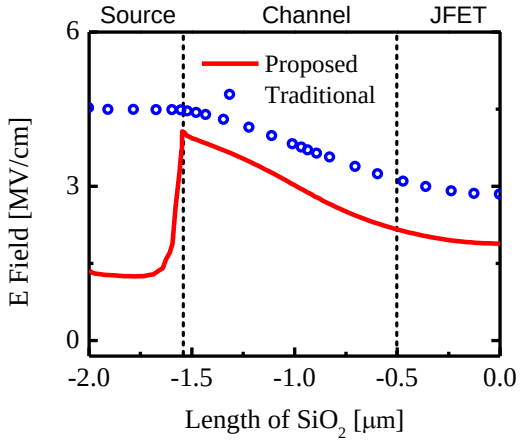


Fig. 3.31. Simulation results for the traditional and proposed structure of electric filed.

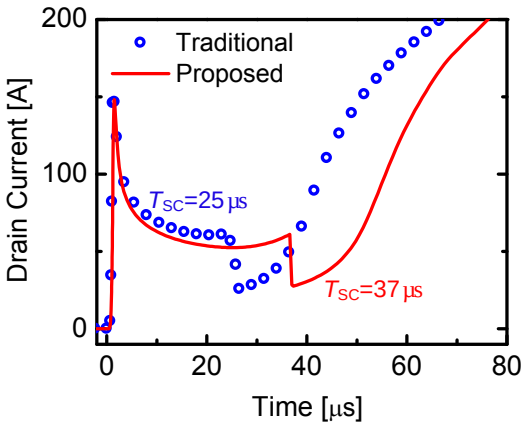


Fig. 3.32 Simulation results for the traditional and proposed structure of short-circuit capability.

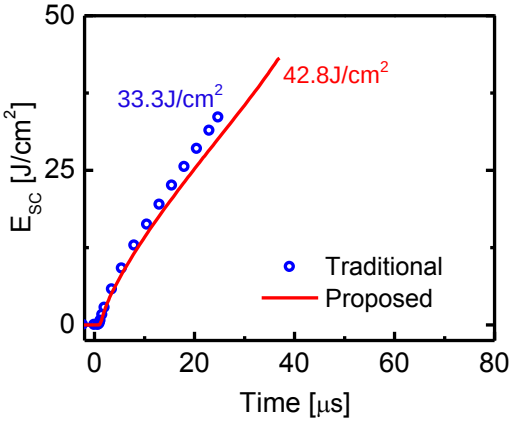


Fig. 3.33. Simulation results for the traditional and proposed structure of short-circuit energy.

Moreover, the short-circuit withstand time and energy of the proposed device are increase by 48% and 28%, as shown in Figs. 3.32 and 3.33, which shows a great advantage compared with those of

traditional device.

3.4 Conclusion

In this chapter, a detailed investigation of avalanche withstanding capability for the 1200 V SiC MOSFET is presented by revealing its avalanche characteristics. Based on the observed avalanche failures, two limitations have been performed in order to estimate their critical lattice temperature under avalanche conditions: a) the avalanche energy limit and b) the peak avalanche current limit. A local burn-out on the surface metallization of the device is discovered when the package is opened. The failure mechanisms have been validated in this study, which are in agreement with theoretical analysis and numerical simulation. In addition, the maximum lattice temperatures for two failure modes based on the short-circuit test for a 1200 V/19 A SiC MOSFET are investigated by experimental and numerical methods. At last, a novel SiC MOSFET with L-shaped gate and LDD region is proposed and studied by the numerical simulation.

The main contributions of this paper are summarized as follows:

(1) The critical lattice temperatures of 1200 V/19 A SiC MOSFET predicted by three proposed evaluation methods are ranging from 937 to 946 K. The post-failure process verifies that the damage in device is due to the failure limit leading into burning up of the metallic electrode pad.

(2) The thermodynamic models associated with simulation method have been developed to explore the critical lattice temperature range during the avalanche event for the SiC MOSFET. The calculated and simulation parameters for dE_{av}/dT_0 to be -0.0115 J/cm^{2}K and -0.012 J/cm^{2}K, respectively, which are in good agreement with the experimental result of -0.0116 J/cm^{2}K.

(3) The avalanche failure mechanisms of the SiC MOSFET are confirmed by the measurements, quantitative models and simulation results, which can be identified as the premature degradation of surface metallization and gate metal electrode resulting in a fusion for the device. The critical temperature for avalanche failure is considered to be $966 \pm 5\%$ K, which can be considered as the main factor taking responsibility for the device failure. Finally, the failure model based on the thermal diffusion equation for the tested SiC MOSFETs is proposed and tested to define the critical temperature range in order to provide a bench mark for the typical avalanche characterization.

(4) Analytical formulas revealed that the short-circuit capability of the SiC MOSFET depends not only on thermal properties of the material but also on the dimensional parameters of the device. Moreover, the maximum lattice temperature is the dominant factor that causes device failure. All the experimental, mathematical, and simulation results show that the SiC MOSFET has a superior thermal reliability and a high quality of short-circuit capability, which make it the best candidate for power application. Consequently, whole analysis models can be used for a bench mark of ruggedness for the SiC MOSFET.

(5) The larger gate turn-off voltage can effectively improve the short-circuit capability by reducing the probability of channel normally-on induced by the higher lattice temperature.

(6) Moderately thick gate oxide layer is required to avoid short-circuit failure related to the gate oxide breakdown in the SiC MOSFETs before the thermal runaway occurs.

(7) A new structure with LDD and L-sharp gate is proposed. It was demonstrated that the short-circuit withstand time and energy of proposed device are increase by 48% and 28% compared with those of the traditional SiC MOSFET. By using those two optimized methods, the short-circuit capability can be greatly improved for the possible application of complimentary inverter.

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4. Robustness Issues for SiC p-channel MOSFET

Due to the superior properties of silicon carbide (SiC) such as high breakdown strength, high thermal conductivity and high carrier drift velocity, the SiC power MOSFET has been regarded as the promising candidate for power electronics applications [1], [2]. Nowadays, owing to the great progress made on the power device fabrication technologies, the n-channel vertical 4H-SiC MOSFET (SiC n-MOSFET) has demonstrated excellent device performance in both static and dynamic characteristics [3]-[5] and is commercially available. On the contrary, little effort has been made to the SiC p-MOSFET and it is still unavailable because of the immaturity in design and fabrication [6]. However, several advantages of the SiC p-MOSFET still make it favorable for some power applications. First, the SiC p-MOSFET can be rugged due to a larger effective barrier height between p type SiC and SiO_2 than that of the n type one [7]. In addition, the SiC p-MOSFET is the key component to realize the SiC-based complementary inverter circuits, which can effectively avoid the dead-time setting and reduce the total harmonic distortion (THD) in output alternating current (AC) waveforms [8].

In this chapter, a high voltage p-channel vertical 4H-SiC MOSFET with double epitaxial growth process that reduces the threshold voltage (V_{th}) and alleviates the SiC/SiO_2 surface roughness is introduced and experimentally demonstrated, achieving a blocking voltage (V_B) of -730 V and a specific on-sate resistance (R_{on}) of 218 mΩ·cm^2 for the possible applications of the complementary inverter. At last, the robustness including short-circuit and avalanche capability is investigated thoroughly.

4.1 Device Fabrication Process

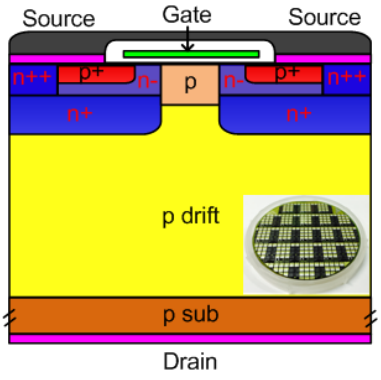

Fig. 4.1. Schematic cross-section view of the fabricated SiC p-MOSFET. The inset shows the overall view of the wafer.

The schematic cross-section view and wafer view of the fabricated SiC p-MOSFET are shown in Fig. 4.1. The device is fabricated based upon the design of the n-IEMOSFET [9]. The hexagonal cell structure for the SiC p-MOSFET is adopted to maximize the packing density [2]. The die size of the SiC p-MOSFET discussed in this letter is 3×3 mm^2. Top view of the bare die and correspondingly enlarged view of the device surface of the fabricated device are shown in Fig. 4.1.

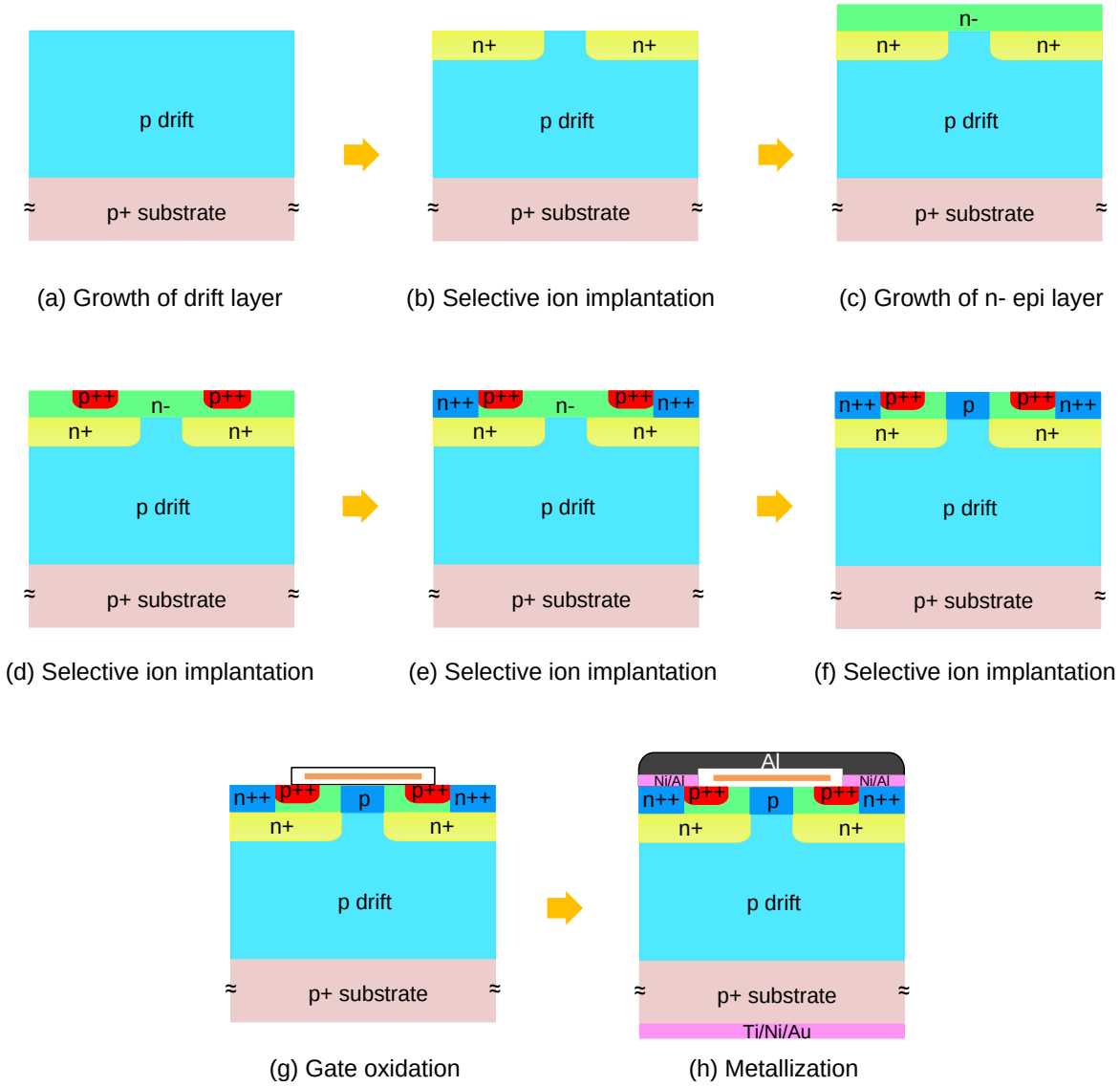

Fig. 4.2. (a)-(h) Process flow line to the fabricated SiC p-MOSFET.

Fig. 4.2 shows the key process steps of the fabricated SiC p-MOSFET, which starts with the epitaxial growth of p drift layer on the 3 inch Si-face p-type 4H-SiC substrate with thickness of 350 μm and resistivity of 2 Ω·cm. The drift layer is 5 μm with doping concentration of 1.6×10^{16} cm^{-3}. On the top of drift layer, the phosphorus ions with the peak doping concentration of 4×10^{18} cm^{-3} are selectively implanted to form the bottom of the n base region. This process aims to prevent punch through in n base region. Then, the 0.5 μm thick n channel region with the doping concentration of as low as 5×10^{15} cm^{-3} is grown on the surface in order to achieve the high channel mobility and relatively small V_{th}. The p+ source and n+ contact region are formed by multiple ion implantations with phosphorus and aluminum, respectively. The JFET area is formed by the aluminum ions implantation with the concentration of 1×10^{17} cm^{-3}. After ion implantation process, high temperature annealing is performed with a carbon cap to suppress the surface roughness. After that, the gate oxide film with a thickness of 50 nm is grown on the surface in dry oxide ambient [10]. Then, the phosphorus-doped polycrystalline silicon (poly-Si) gate electrodes and interlayer dielectric films are formed. At last, Ni/Al and Ti/Ni/Au

stack are deposited and annealed as the source and drain electrodes, respectively.

4.2 Device Characterization and Discussion

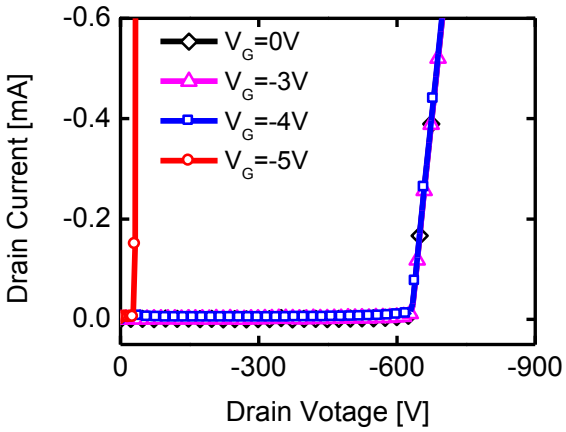

Fig. 4.3. Typical Off-state characteristics for the fabricated SiC p-MOSFET with different gate voltage.

The static characterization of the SiC p-MOSFET is measured using an Agilent B1505A power device analyzer. -730 V blocking is achieved with the drain leakage current at lower than 10 μA at gate-source (V_G) of 0 V, as it can be seen in Fig. 4.3. Furthermore, in spite of the fact that the V_G increases to be -4 V, the SiC p-MOSFET still keeps the blocking state, which exhibits the high immunity for fault turn-on.

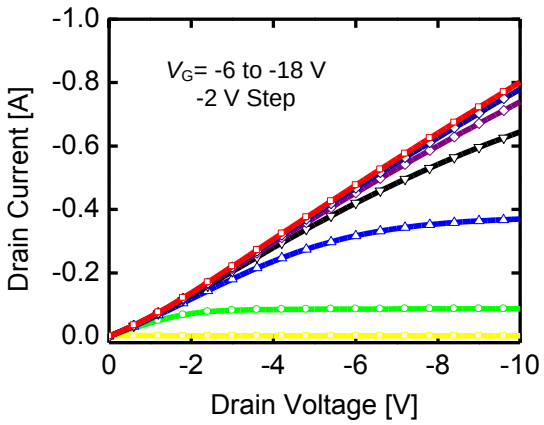

Fig. 4.4. Typical On-state characteristics for the fabricated SiC p-MOSFET.

Fig. 4.4 shows the output characteristics of the fabricated SiC p-MOSFET from V_G = -6 V to -18 V by a step of -2 V. Due to the small doping concentration and epitaxial growth process in channel region, the typical V_{th} obtained from extrapolation of a linear region of the I_d-V_g curve is -5.32 V at room temperature.

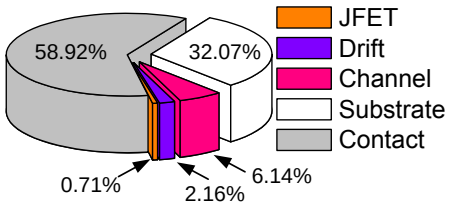

Fig. 4.5. On-state resistance for the fabricated SiC p-MOSFET. The Active area is 5.7 mm^2.

Based on the test results of test elementary devices fabricated with the SiC p-MOSFET on the same wafer and simulation results, the specific on-state resistance $R_{on,sp}$ is 218 $m\Omega \cdot cm^2$ at gate-source voltage V_G = -15 V. As shown in Fig. 4.5, on-state resistance of the fabricated device can be divided as the source and drain contact ($R_{contact}$), channel (R_{ch}), JFET region (R_{JFET}), drift layer (R_{drift}), and substrate (R_{sub}).

The largest components of the on-state resistance are the substrate and metal contact resistances due to the highly specific metal contact resistance (14.7 $m\Omega \cdot cm^2$) and the thick p+ substrate (350 μm, 2 Ω·cm) Thus, the $R_{on,sp}$ can be greatly reduced if the advanced ohmic contact process and better substrate are used.

Fig. 4.6 shows the field-effect mobility as a function of gate voltage for the SiC p-MOSFET. Due to the alleviation of the surface roughness and lower interface state density, the field-effect mobility the p-MOSFET is almost no change when gate voltage is over -12 V, regardless of the drain voltage. Furthermore, the peak field-effect mobility of 8.65 cm^2/V s is 53% higher than that of the reported in [12]. In addition, the channel mobility for the fabricated device is a relatively high value, which is 8.6% of the bulk mobility of hole (about 100 $cm^2/V \cdot s$). This ratio for p-MOSFET is much higher than that for the n-MOSFET (about 2%).

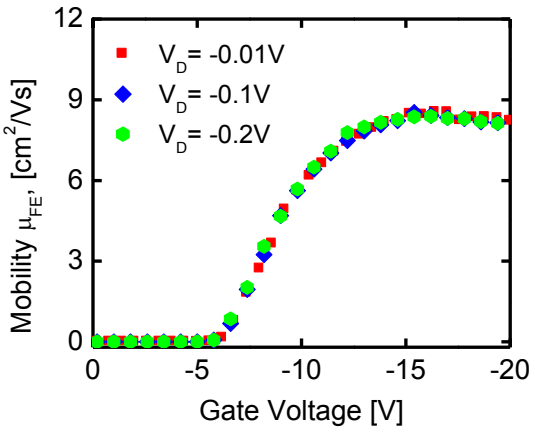

Fig. 4.6. The field-effect channel mobility.

The intrinsic body diode *I-V* characteristic with the ground connection of gate electrode is shown in Fig. 4.7. Under positive drain to source bias, the reverse conduction voltage is around 2.6 V, which is the turn-on voltage of the drift region (*p* type)/base region (*n* type) junction.

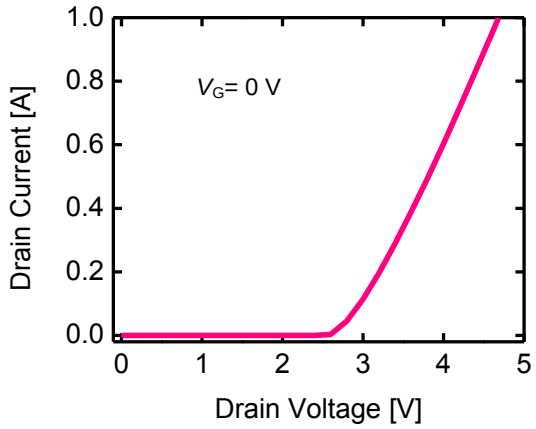

Fig. 4.7. Body diode *I-V* characteristics for the fabricated SiC p-MOSFET.

In addition, Fig. 4.8 shows that the fabricated SiC p-MOSFET body diode has the reverse recovery current of -1.88 A at 12.5 A forward current and 300 V supply. As mentioned previously, the forward and reverse recovery characteristics are highly determined by the minority carrier lifetime which is highly fabrication process dependence [13], [14]. With implantation damage and doping compensation phenomenon in n+ source, the lifetime of highly doped n-type SiC is typical tens of nanoseconds, leading to the relatively high forward voltage (V_F) and the significantly low level of the reverse recovery current.

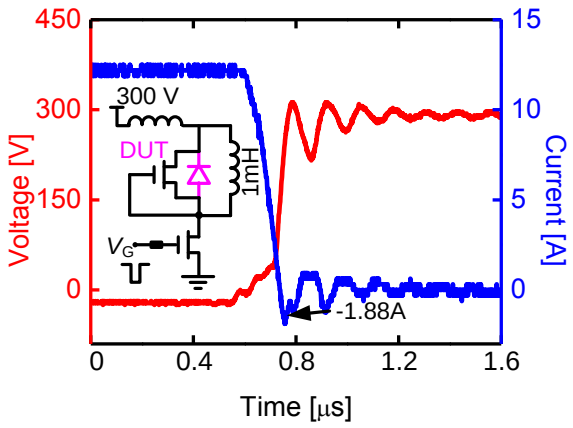

Fig. 4.8. The reverse recovery of the fabricated SiC p-MOSFET body diode at 12.5 A forward current and 300 V supply.

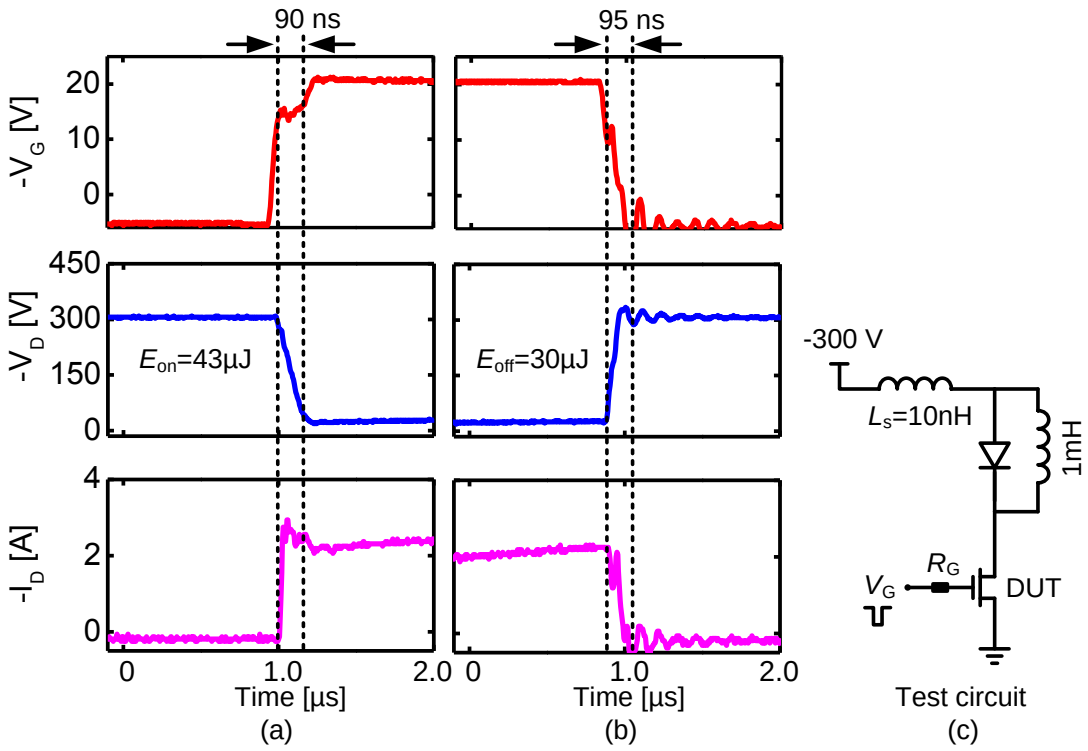

Fig. 4.9. (a) turn-on and (b) turn-off switching waveforms of the fabricated SiC p-MOSFET. (c) test circuit. The gate resistance R_G and the load current are 15 Ω and -2.5 A, respectively. The driving signal is switched between -20 V and 5 V to on and off, respectively.

The switching characteristic of the SiC p-MOSFET at room temperature is shown in Fig. 4.9. A supply voltage of -300 V, drain current (I_D) of -2.5 A and a load inductance of 1 mH are used for this measurement. As a result, the times of turn-on and turn-off are 90 ns and 95 ns, respectively. The total switching loss of the SiC p-MOSFET is 73 μJ. The switching characteristics show a great advantage when compared with the Si IGBT. However, the switching time including the rising and fall time for our fabricated SiC p-MOSFET is larger than the results reported in the n-IEMOFET at same test condition. This is likely because the larger active area for the fabricated device make the resistance of poly-Si become large, resulting in a relatively slow switching time. Therefore, the switching characteristic of the SiC p-MOSFET can be further optimized by decreasing the connected gate resistance.

4.3 Short-Circuit Characteristic for SiC p-/ n-MOSFET

4.3.1 Short-Circuit Capability for SiC p-/ n-MOSFET

Fig. 4.10 shows the waveforms of drain-source current (I_D) and gate-source voltage (V_G) as functions of the times for the SiC p-MOSFET with the power supplier voltage of -300 V (it also can be consider as the -300 V drain voltage (V_D)). The gate voltage is considered as high as -27 V to totally turn on the p-MOSFET. When the short-circuit mode occurs at point A, the I_D swiftly increases and the device enters from linear region to saturation region (point B). Furthermore, the I_D waveform constantly

increases and gradually rises up to the peak current (point C). The drain current shows a 17 μs delay compared with the the peak V_G waveform. This is more likely because the decreasing rate of V_{th} is much larger than the rising rate of $R_{on,sp}$ during this period. After that, the I_D is not changed obviously due to the slightly positive resistance temperature coefficient of the SiC p-MOSFET during the short-circuit mode. According to the experiment results, the device fails at t_{SC} = 90 μs. The short-circuit energy is calculated to be 16.1 J/cm^2. It is worth noting that the degradation of V_G cannot be seen even the high electric field (E_{OX} = 5.4 MV/cm) apply in the gate oxide layer.

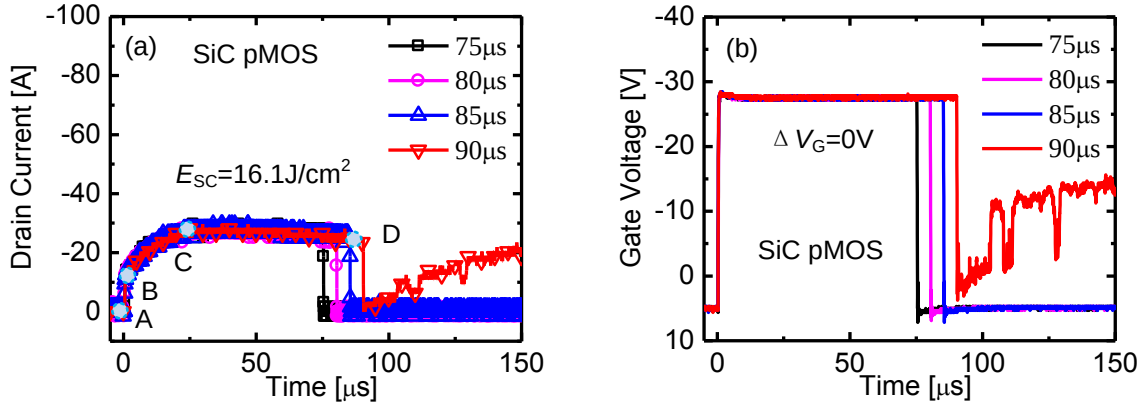

Fig. 4.10. Characteristics of (a) drain-source current, and (b) gate-source voltage as functions of the short-circuit transient for the SiC p-MOSFET when V_D is -300 V at room temperature.

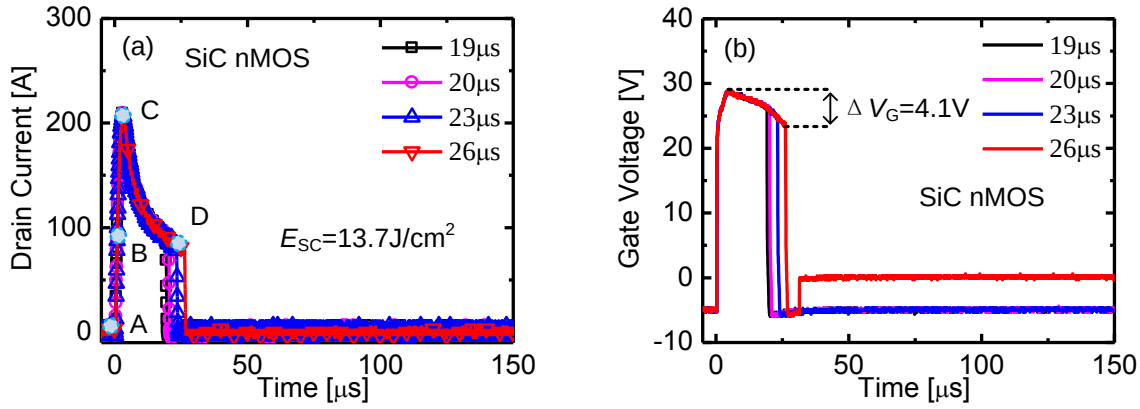

Fig. 4.11. Characteristics of (a) drain-source current, and (b) gate-source voltage as functions of the short-circuit transient for the SiC n-MOSFET when V_D is 300 V at room temperature.

In order to make a comparison, the 650 V SiC n-MOSFET is used. The SiC n-MOSFET has the he die size of 2.8 × 2.8 mm^2 and drift thickness of 8 μm. Fig. 4.11 shows the waveforms of I_D and V_G as functions of the times for the SiC n-MOSFET. Compared with the former case, the SiC n-MOSFET can quickly rise to the peak drain current. It shows the positive resistance temperature coefficient, leading to the fast reduction in I_D during the short-circuit transient. The maximum t_{sc} of the n-MOSFET is 26 μs. It is merely 28% compared with that of the p-MOSFET. Furthermore, the short-circuit energy is calculated to be 13.7 J/cm^2. It is about 85% compared with that of SiC

p-MOSFET. As same with the reported in [14]-[17], the gate voltage of the SiC n-MOSFET gradually decreases by 4.1 V under the test condition.

TABLE 4.1

Impedance test

Symbol	SiC p-MOSFET	SiC n-MOSFET
R_{gs}	30 Ω	0.3 Ω
R_{ds}	∞ Ω	∞ Ω
R_{gd}	1.8 MΩ	14 MΩ

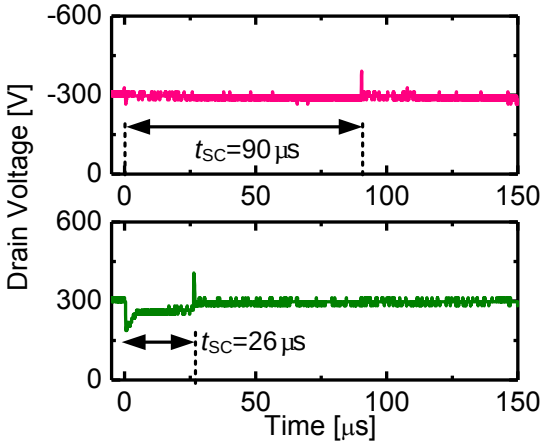

Fig. 4.12. Drain-source voltage as a function of short-circuit transient for the SiC p- and n-MOSFET.

Then the resistances between the three terminals for the failure devices are summarized in table 4.1. The value of R_{gs} shows that the gate-source terminals are completely damaged or shorted in both devices. In addition, the value of R_{ds} exhibits that there is no obvious damage or degradation in the *pn* junction due to the infinite resistance between gate and source for the SiC p- and n-MOSFET. Fig. 4.12 shows the drain voltage as a function of time for both devices. It is obvious that there is no degradation in the drain voltage and the devices can still block the high voltage after the short-circuit transient.

4.3.2 Electro-thermal Models

The thermal diffusion equations (1) and (2) show the dependence of t_{SC} and device parameters on temperature. They are precise thermodynamic models to get the rising temperature during the short-circuit mode. In addition, the temperature can be obtained by the following

$$T(t_{SC}) = \Delta T e^{-(y/\sqrt{D_{SiC} t_{SC}})} + T_A \tag{66}$$

$$\Delta T = \frac{E_{SC}}{A\sigma\rho c} \tag{67}$$

where E_{SC} is the short-circuit energy. The parameters of c and ρ are the heat capability and the material density for SiC, respectively. The σ is the Joule heat region. T_A is room temperature at the initial time

of the short-circuit mode. The constant A is the fitting parameter by taking the t_{SC} and the thermal diffusion parameters into account. They are 47 and 17 for the SiC p- and n-MOSFET, respectively. D_{sic} is the thermal diffusivity. y is the thickness of two devices.

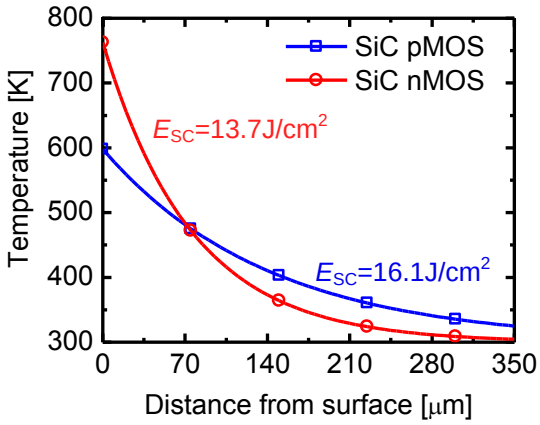

Fig. 4.13. Calculated results of the temperature distribution profile for two type devices with the maximum short-circuit energy.

Fig. 4.13 shows the calculated temperature distribution profile at the end of short-circuit transient, which corresponds to the point D in both Figs. 4.10 and 4.11 From the Fig. 4.13, despite the SiC p-MOSFET has the 15% higher short-circuit energy, the surface temperature is lower compared with that of SiC n-MOSFET. This is due to the relatively longer short-circuit transient, leading to a longer thermal diffusion length and increase the value of the fitting parameter A. Thus, the one with the longer t_{SC} exhibits better short-circuit capability if the devices have similar short-circuit energy. The device can be effectively cooled down without accumulation of Joule heat during a longer time. At same time, the equations (1) and (2) exhibits that the short-circuit capability is determined not only by the thermal properties of material but also by the dimensional parameters of the device. In order to improve the short-circuit capability, it is significant to increase of the drift layer thickness and active area.

4.3.3 Short-Circuit Failure Mechanisms

It is effective to investigate the reliability of gate oxide layer and *pn* junction during the short-circuit mode by using TCAD simulator. The simulation is carried out based on the physical models and related equations [18]. Fig. 4.14 gives the results about the electric field in the gate oxide with 300 V drain voltage at four points of the short-circuit transient in both devices. When the device switches on, the electric field in gate oxide increases gradually. After that, the electric field achieves the maximum point, as shown from point A to C in Fig. 4.10. The maximum point of the electric field gradually shifts from JFET region to source region. In addition, Fig. 4.15 shows the simulation result of the surface temperature at turn-off time (point D). Based on the analytic results, the theoretical temperature in the source region is in good agreement with the simulation one.

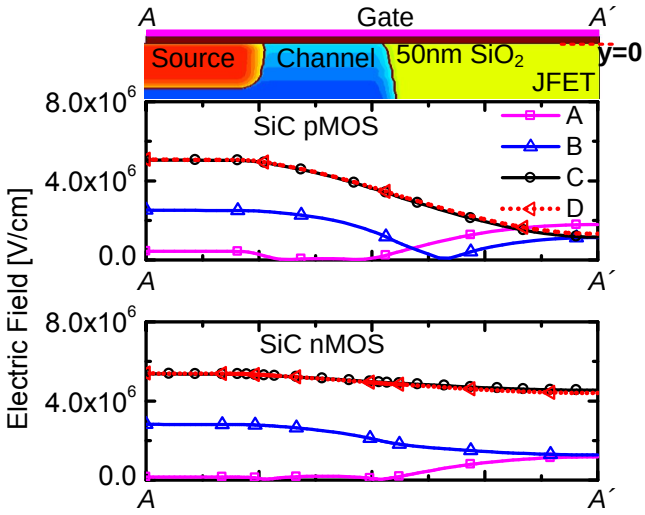

Fig. 4.14. Electric field profiles in gate oxide at four points of short-circuit transient in Figs. 3 and 4 for SiC p- and n-MOSFET with the gate oxidation layer of 50 nm.

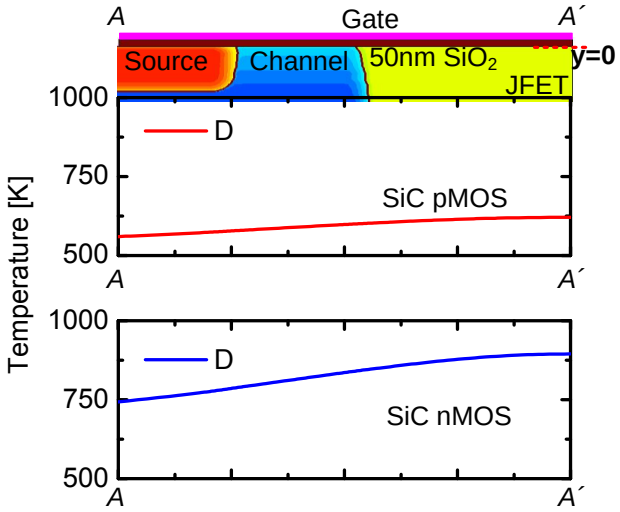

Fig. 4.15. Surface temperature for the SiC p- and n-MOSFET

The oxide degradation mechanism in SiC is considered to be the Fowler–Nordheim (FN) tunneling and Poole–Frenkel (PF) emission effect. These two models can result in a leakage current. It becomes obvious especially at the high gate electric field and lattice temperature, which can be performed by time dependent dielectric breakdown (TDDB) test. Several papers have been reported that a dramatic increase in FN current happens when the temperature rises up to 523 K. Currently, the effective barrier height between n-type SiC and oxide layer decreases to 2.38 eV when the temperature increase to 573 K [19, 20]. The ruggedness problem of the gate oxide layer will be worse due to the existence of the high electric field and the high lattice temperature.

Due to the higher effective barrier height i.e., 3.05 eV between p-type SiC and SiO_2 and relatively smaller lattice temperature, the fabricated SiC p-MOSFET can effectively reduce the possibility of hole injection from SiC to the oxide layer. This can reduce gate leakage current during the short-circuit mode. This indicates the reason why there is no gate voltage degradation in the SiC p-MOSFET. On

the contrary, the larger degradation voltage can be found the SiC n-MOSFET. In addition, similar with reported results [21], despite there is almost no the gate leakage current in the SiC p-MOSFET, the large lattice temperature damage the gate-source terminals.

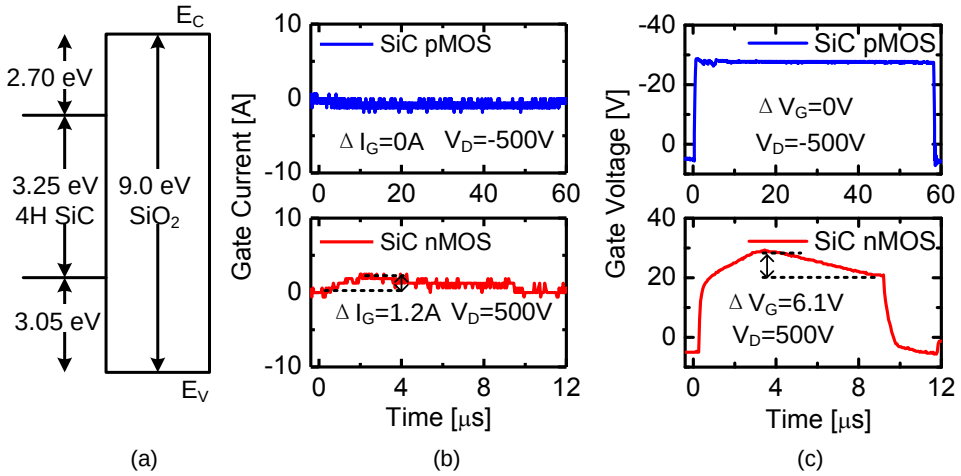

Fig. 4.16. Energy band diagram of 4H-SiC and SiO_2 illustrating barrier heights, (b) (c) gate current waveforms and (c) gate voltage waveforms with $|V_D|$ = 500 V for SiC p- and n-MOSFET.

The drain voltage dependent the gate oxide layer reliability was investigated. Fig. 4.16 shows the experiment results of gate voltage degradation with $|V_D|$ = 500 V for the SiC p-MOSFET and the SiC n-MOSFET during the short-circuit mode. The SiC p-MOSFET has the small gate leakage current and little degradation gate voltage. Thus, the fabricated device shows the advanced in gate oxide reliability compared with its component (ΔV_G= 6.1 V, ΔI_G= 1.2 A).

4.3.4 Avalanche Immunity Property during the Short-Circuit Transient

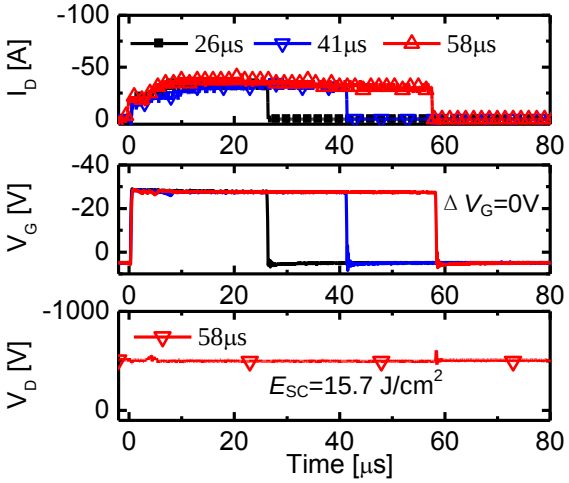

Fig. 4.17. Drain current, gate and drain voltage waveforms with maximum short-circuit withstand time of 58 μs and -500 V drain voltage for the fabricated SiC p-MOSFET.

In order to confirm the avalanche immunity capability of the fabricated device, the drain voltage of

-500 V is used. It is obvious that the fabricated device can safely turn off under the high avalanche condition even in the short-circuit energy of 15.7 J/cm^2, as shown in Fig. 4.17. According to these results, if the short-circuit energy does not beyond the safety limit, the higher drain voltage closing to the breakdown voltage cannot damage the SiC p-MOSFET. Higher avalanche immunity capability is confirmed by the SiC p-MOSFET during the short-circuit mode.

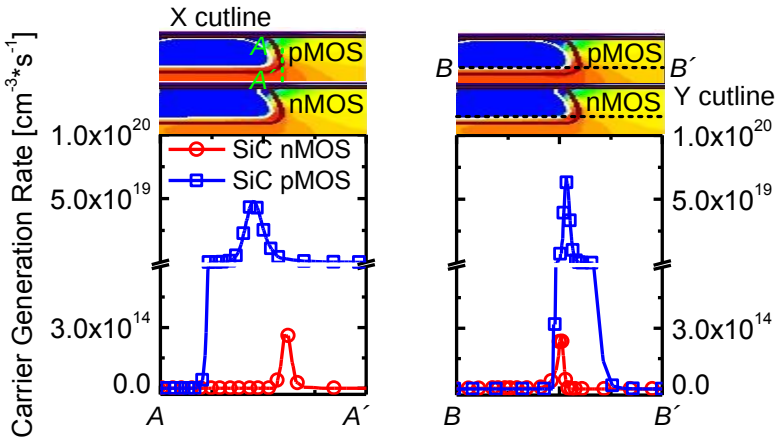

Fig. 4.18. Carrier Generation rate for the SiC p- and n-MOSFET along *A-A´* and *B-B´* cut lines, respectively, at short-circuit transient of point D.

Based on the short-circuit test results at the short-circuit transient of point D, the carrier generation rate by avalanche for two devices is shown in Fig. 4.18. The highest carrier generation rate is located at the corner of body region for both devices. Despite the impact ionization rate for hole is larger than that of the electron, the calculated value of peak carrier generation rate of 6.7×10^{19} cm^{-3}sec^{-1} is much smaller to generate a avalanche breakdown for the SiC p-MOSFET [22]. The simulation result of blocking characteristic of the SiC p-MOSFET suggests that the carrier generation rate is higher than 2×10^{22} cm^{-3}sec^{-1} when device is avalanche breakdown, as shown in Fig. 4.19. However, the generated avalanche leakage current is smaller than 0.026 mA at room temperature.

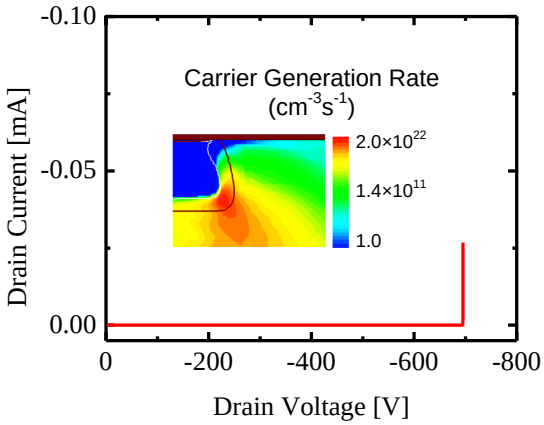

Fig. 4.19. Simulation results of carrier generation rate for the SiC p-MOSFET at avalanche failure point.

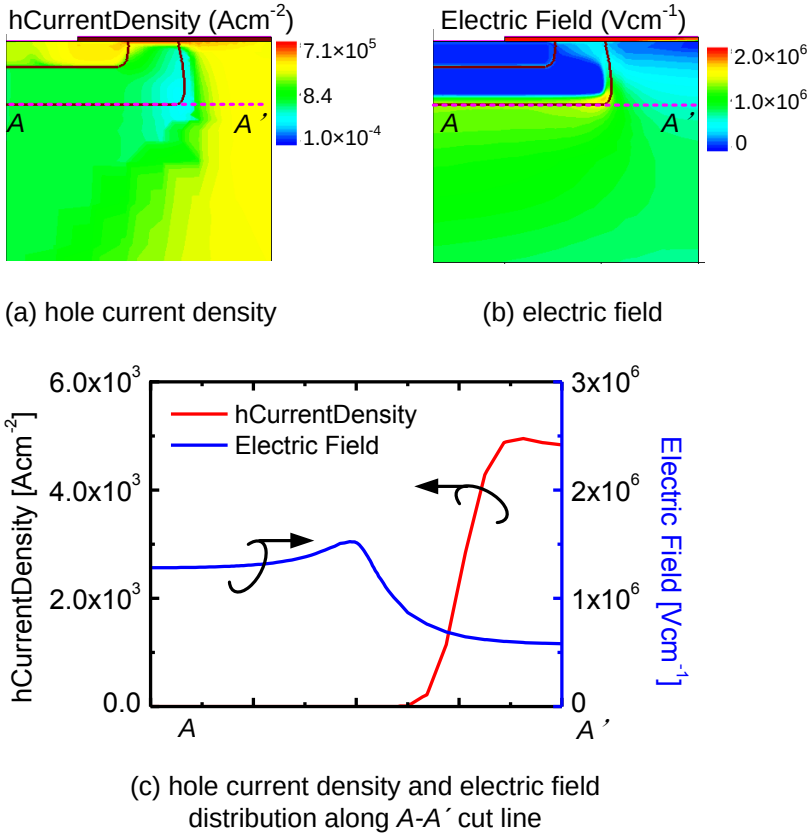

Fig. 4.20. Simulation results of (a) the hole current density, (b) the electric field distribution, and (c) the hole current density and the electric field distribution along *A-A´* cut line for the SiC p-MOSFET at the short-circuit mode of point D.

Fig. 4.20 exhibits the hole current density and electric field distributions along *A-A´* cut line for the SiC p-MOSFET at point D. The carrier generation rate (G) is strongly decided by hole/electron current density (J_p/J_n) and electric field (E) in SiC material. It can be expressed by

$$G = \alpha_n \frac{J_n}{q} + \alpha_p \frac{J_p}{q} \tag{68}$$

where α_n *and* α_p are electron and hole impact ionization coefficient, respectively. The typical models are [23]

$$\alpha_p = (6.3\times10^6 - 1.07\times10^4 \times T)\times\exp\left[-\frac{1.75\times10^7}{E}\right] \tag{69}$$

$$\alpha_n = (1.6\times10^5 - 2.67\times10^2 \times T)\times\exp\left[-\frac{1.72\times10^7}{E}\right] \tag{70}$$

where T is the lattice temperature. From Fig. 4.20, the peaks of hole current density and electric locate at the different region, leading to a small carrier generation rate. In addition, α_n *and* α_p dramatically reduce as increasing of the lattice temperature. Because of those, the avalanche failure is more difficult to happen in the SiC p-MOSFET. The avalanche failure can be ignored in the short-circuit mode. The pn junction safety for the fabricated device also supports these results.

4.4 UIS Characteristic for SiC p-/ n-MOSFET

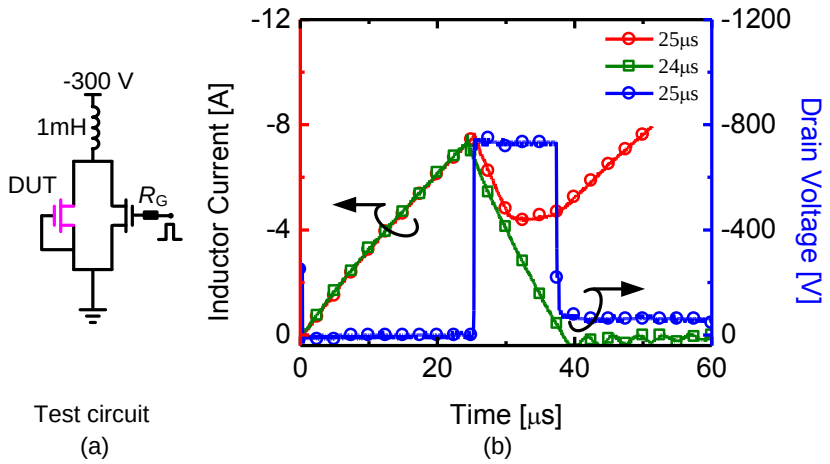

Fig. 4.21. (a) UIS test circuit, and (b) experiment results in the avalanche mode for the SiC p-MOSFET.

The UIS test circuit and experimental waveforms for the fabricated SiC p-MOSFET are shown in Fig. 4.21. In order to ignore the self-heating before the avalanche mode, the 1700 V SiC n-MOSFET paralleled to the tested device. The green line in Fig. 4.21 (b) is obtained when the paralleled device has a turn-on time of 24 μs. It gives the SiC p-MOSFET a peak drain current of 7.3 A with the power supplier of -300 V at room temperature. The load inductance is 1 mH. Furthermore, the SiC p-MOSFET fails when the paralleled device has a turn-on time of 25 μs. In this situation, the peak current in inductor reaches at 7.6 A, as shown in red line in Fig. 4.21(b). In the avalanche transient (t_{av}) of 12.4 μs, the energy stored in the inductor discharges through the p-MOSFET and forces the device work in the avalanche condition. The drain voltage of SiC p-MOSFET reaches at -750 V and the drain current gradually decrease during the avalanche transient. Following, the device is completely damaged by the large power energy due to almost zero drain voltage. In this situation, we can also find that the device lose the blocking capability totally. The avalanche energy is calculated to be 0.93 J/cm^2.

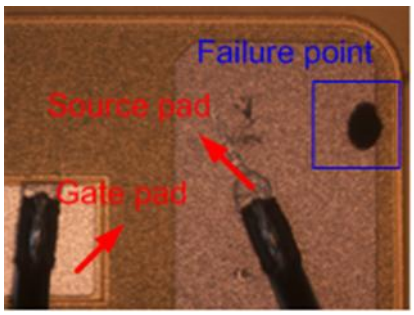

Fig. 4.22. Picture of the failed SiC p-MOSFET.

The resistance between gate and source terminals is tested after the device fails. The resistance is only 19 Ω. It is obvious that the gate and source are nearly shorted and the gate oxide layer is totally

damaged in the avalanche mode.

The picture of failure device is shown in Fig. 4.22. From that, a relatively small damage point is near to the source metallization. Only a smaller region of the SiC p-MOSFET is damaged, perhaps due to the large lattice temperature or thermal runaway inner the device.

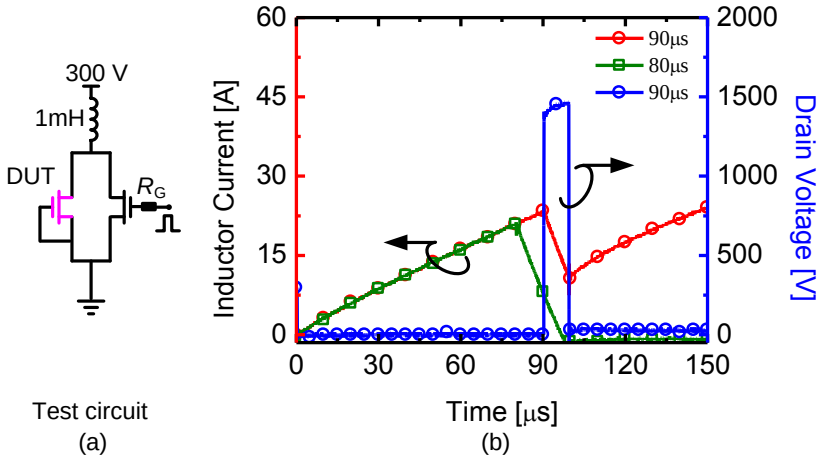

Fig. 4.23. (a) UIS test circuit, and (b) experiment results in the avalanche mode for the SiC n-MOSFET.

The UIS test circuit and experimental waveforms for the available SiC n-MOSFET are shown in Fig. 4.23. Ame with the former test, the 1700 V SiC n-MOSFET is paralleled to the tested device in order to reduce the self-heat before the avalanche mode. The green line in Fig. 4.23 (b) is obtained when the paralleled device has a turn-on time of 80 μs. It gives the SiC n-MOSFET a peak drain current of 20 A with the power supplier of 300 V at room temperature. The peak current for SiC n-MOSFET is much higher than that of the SiC p-MOSFET. This is due to large on-state resistance of SiC p-MOSFET. The load inductance in here is also 1 mH. Furthermore, the SiC n-MOSFET fails when the paralleled device has a turn-on time of 90 μs. The t_{av} of the SiC n-MOSFET is 73% compared with that of the SiC p-MOSFET. However, the drain voltage is higher as 1360 V for SiC n-MOSFET due to the thick drift layer used inner the device. Because of the thicker drift layer, the SiC n-MOSFET can withstand much higher avalanche voltage. The former mathematical model shows that the thicker drift layer shows a great advantage in the avalanche energy if the same active area in different device is same. The avalanche energy is calculated to be 3.97 J/cm^2. This value is larger than that of SiC p-MOSFET.

Same with the aforementioned results in the SiC p-MOSFET, the resistance between gate and source terminals is only 1.1 Ω. It reveals that the gate oxide layer is totally damaged. Thus, the gate oxide reliability should be greatly improved in the avalanche mode for both devices.

4.5 Conclusion

In this chapter, the SiC p-MOSFET with the typical threshold voltage of -5.32 V, the breakdown voltage of -730 V and the on-resistance of 218 mΩ·cm^2 is successfully fabricated for the first time.

(1) The highly field-effect channel mobility of 8.65 cm^2/V s for the SiC p-MOSFET is achieved by the double epitaxial growth process of channel region. Reverse recovery current of the SiC p-MOSFET

body diode at 12.5 A forward current shows a significantly lower level of the reverse recovery current. Furthermore, the fast switching capability with turn-on time of 90 ns, turn-off time of 95ns, and switching loss of 73 μJ is demonstrated.

(2) According to the evaluation results of short-circuit capability for SiC p/n-MOSFET, the p type one has the 15% higher short-circuit energy than that of the n type one. In order to study the critical lattice temperature during short-circuit mode, the mathematical model is built by taking the device parameters and the thermal properties of SiC material into account. It is also demonstrated that avalanche immunity of the SiC p-MOSFET is confirmed by experiment results. Theoretical direction to improve the device avalanche capability is provided at last.

The target of this chapter is to evaluate the actual safety area of the SiC p-MOSFET for complementary inverter circuit in the future. Currently, it also provides a bench mark to the SiC p-MOSFET device technologies in the future.

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5. Conclusions and Future Work

Conclusions

Because of the outstanding properties of silicon carbide (SiC), SiC power devices outperform silicon (Si) counterpart in many regards, including the higher breakdown voltage, the lower on-state resistance, the faster switching and the higher maximum operating temperature. With the rapid development of power device technologies, the high voltage SiC MOSFET and SiC Schottky Barrier Diode (SBD) have been widely put into practical use in transportation applications, such as hybrid electric vehicle (HEV), traction control system, etc.

The research work presented in this thesis is mainly based on the experiment, mathematical model and simulation to investigate the unclamped inductive switching and short-circuit characteristics for SiC n/p-channel MOSFETs. Physic models combined with fitting parameters used in simulator have been introduced. TCAD simulation has been performed to put the physical insight into device when analyze the rubustness issues for SiC MOSFETs (n/p channel). The mathematical models used in this thesis give a direction to improve the unclamped inductive switching and short-circuit characteristics for SiC MOSFETs. The conclusions derived from this research work have been divided into two important sections as follows:

1. The UIS failure mechanisms of the SiC MOSFET are confirmed by the measurements, quantitative models and simulation results, which can be identified as the premature degradation of surface metallization and gate metal electrode resulting in a fusion for the device. The critical temperature for avalanche failure is considered to meet the melting point of metal, which can be considered as the main factor taking responsibility for the device failure. In addition, two failure modes have been considered in short-circuit failure for SiC MOSFET. Analytical formulas revealed that both UIS capability and short-circuit capability of the SiC MOSFET highly depends not only on thermal properties of the material but also on the dimensional parameters of the device. In order to improve UIS and short-circuit characteristics, the higher drift layer can be used. Besides, larger gate turn-off voltage, moderately thick gate oxide layer and LDD+Lgate structure can effectively improve the short-circuit capability and reduce the gate oxide layer degradation.

2. In order to realize the application of SiC-based complementary inverter circuits and reduce the number of gate driver, the SiC p-MOSFET has been successfully fabricated for the first time. High performances in the static characteristics are experimental demonstrated. At last, robustness issues for SiC p-MOSFET are systematically analyzed compared with SiC n-MOSFET. It is shown that SiC p-MOSFET the p-MOSFET can tolerate more out-of-SOA energies than the n one.

All the experimental, mathematical, and simulation results show that the SiC MOSFETs has a superior thermal reliability and a high quality of short-circuit capability, which make it the best candidate for power application. Consequently, whole analysis models can be used for a bench mark of ruggedness for the SiC MOSFETs. This thesis also provides theoretical direction to the device engineer how to boost the device robustness capability.

Future Work

This work has been performed by the experiment, compact models and simulation to analyze the robustness issues for SiC MOSFETs. However, the fabricated SiC p-MOSFET show a large contact resistance, which needs to be dramatically reduced by advanced process in the future. At that time, further research work on the comparison of robustness issues between SiC n and p MOSFETs is still essential to explore the potential property for SiC power devices.

Research Achievements

Award

IEEE EDS Japan Chapter Student Award (2017)

Papers (Journal)

1. **Junjie An**, Masaki Namai, and Noriyuki Iwamuro, "Experimental and Theoretical Analyses of Gate Oxide and Junction Reliability for 4H-SiC MOSFET under Short-Circuit Operation," *Japanese Journal of Applied Physics*, Vol. 55, pp. 124102-1~4, 2016

2. **Junjie An**, Masaki Namai, Hiroshi Yano, and Noriyuki Iwamuro, "Investigation of Robustness Capability of -730 V P-Channel Vertical SiC Power MOSFET for Complementary Inverter Applications," *IEEE Transaction on Electron Devices*, Vol. 64, No. 10, pp. 4219-4225, 2017

3. 安俊傑、生井正輝、岡本大、矢野裕司、只野博、岩室憲幸、"Unclamped Inductive Switching 試験による 4H-SiC MOSFET の最大接合温度の評価"、電気学会論文誌 C、137 巻 2 号 C 分冊、pp.216-221、2017

4. **Junjie An**, Masaki Namai, Dai Okamoto, Hiroshi Yano, Hiroshi Tadano, and Noriyuki Iwamuro, "Investigation of Maximum Junction Temperature for 4H-SiC MOSFET during Unclamped Inductive Switching Test," *Electronics and Communications in Japan*, vol.101, no.1, pp.24-31, 2018

Papers (General Magazine)

1. **Junjie An**, Masaki Namai, Mikiko Tanabe, Dai Okamoto, Hiroshi Yano, and Noriyuki Iwamuro, "Making a debut: the p-type SiC MOSFET", *Compound Semiconductor*, June, 2017

Papers (International Conference)

1. **Junjie An**, Masaki Namai, Mikiko Tanabe, Dai Okamoto, Hiroshi. Yano, and Noriyuki Iwamuro, "Experimental Demonstration of -730V Vertical SiC p-MOSFET with High Short Circuit Withstand Capability for Complementary Inverter Applications," *IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 272-275 (IEEE EDS Japan Chapter Student Award)

2. **Junjie An**, Masaki Namai, Dai Okamoto, Hiroshi Yano, and Noriyuki Iwamuro, "Evaluation of Maximum Junction Temperature for 4H-SiC MOSFET during Unclamped Inductive Switching Test," *International Conference on Electrical Engineering* (ICEE), ID 90276, 2016

3. **Junjie An**, Masaki Namai, Hiroshi Yano, and Noriyuki Iwamuro, "Methodology for Enhanced Short-Circuit Capability of SiC MOSFETs," *IEEE in Proceedings of International Symposium on Power Semiconductor Devices & ICs (ISPSD)*, 2018

4. Masaki Namai, **Junjie An**, Hiroshi Yano and Noriyuki Iwamuro, "Experimental and Numerical Demonstration and Optimized Methods for SiC Trench MOSFET Short-Circuit Capability," *IEEE in Proceedings of International Symposium on Power Semiconductor Devices & ICs (ISPSD)*, 2017, pp. 363-366.

Papers (Domestic Conference)

1. **安俊傑**, 生井正輝, 岡本大, 只野博, 矢野裕司, 岩室憲幸, “Electrothermal Evaluation of SiC MOSFETs during Unclamped Inductive Switching,” 平成 28 年電気学会全国大会, 東北大学　川内北キャンパス, 2016
2. 生井正輝, **安俊傑**, 岡本大, 只野博, 矢野裕司, 岩室憲幸,“SiC-MOSFET の UIS 耐量評価,” 平成 28 年電気学会全国大会, 東北大学　川内北キャンパス, 2016
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Junjie An

February 2018

Tsukuba, Japan