Advanced solid-phase crystallization for high-hole mobility (450 cm^2/Vs) Ge thin film on an insulator

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The hole mobility of the solid-phase-crystallized Ge layer is significantly improved by controlling the deposition temperature of Ge (50–200 °C) and the Ge thickness (50–500 nm) and by applying post annealing at 500 °C. The resulting hole mobility, 450 cm^2/Vs, is the highest value to date among that of semiconductor layers directly formed on glass. The mechanism of the mobility enhancement is discussed from the perspective of three carrier scattering factors: grain boundary scattering, interface scattering, and impurity scattering. The high-hole mobility Ge layer formed by the simple fabrication process will be useful for high-speed thin-film transistors.

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Ge has attracted attention as the most promising candidate for post-Si material because it has higher carrier mobility than Si and is compatible with conventional Si process. Effective mobilities in Ge metal-oxide-semiconductor field-effect-transistors (MOSFETs) have exceeded those in Si-MOSFETs thanks to the development of device technologies including gate stacks.[1–6] Ge on insulator (GOI) technology has been widely studied for lowering the fabrication cost and improving the device performance of Ge-MOSFETs. Researchers have developed many techniques for GOIs, such as mechanical transfer,[7] oxidation-induced condensation,[8–10] epitaxial growth on Si on insulator,[11,12] and rapid-melting growth.[13–16] Although these techniques are attractive for achieving high quality GOIs, the direct low-temperature formation (< 600 °C) of Ge on arbitrary substrates is desired for lowering the process costs and expanding the device application. Polycrystalline Ge (poly-Ge) thin films have been directly formed on glass or plastic substrates at low temperatures using solid-phase crystallization (SPC),[17–22] laser annealing,[23–26] chemical vapor deposition,[27,28] flash lamp annealing,[29] and metal-induced crystallization.[30–34] The performance of the Ge thin film transistors (TFTs), however, has been no match for that of Si-MOSFETs.[20,21,26,29,34] This is attributed to the fact that the carrier mobilities of the Ge layers are still low (≤ 200 cm^2/Vs). In addition, the Ge layers are highly p-doped (> 10^{17} cm^{-3}) because of point defects generating holes,[35] which restricts device application. To further improve Ge-TFTs, one needs to study not only device technology but also crystallization techniques.

Toko *et al*. reported that post annealing (PA) at 500 °C is effective to reduce the point defects and then the hole concentration of SPC-Ge,[17] which allows for the hole mobility of 140 cm^2/Vs. On the other hand, Sadoh *et al*. reported that a thicker film allows for the higher hole mobility in SPC-GeSn.[36] Very recently, we improved the hole mobility of SPC-Ge from 140 cm^2/Vs to 340 cm^2/Vs by preparing an amorphous Ge (a-Ge) precursor with heating the substrate.[37] This hole mobility was the highest ever recorded for a thin film formed on

insulators at temperatures below the melting point of Ge (937 °C). In this study, we investigated the effects of both film thickness and PA on the SPC-Ge and broke the record with a hole mobility of 450 cm^2/Vs. The process temperature was 500 °C, making it possible to fabricate devices on glass substrates.

In the experiment, the Ge precursors were deposited on SiO_2 glass substrates using the Knudsen cell of a molecular beam deposition system (base pressure: 5×10^{-7} Pa). The deposition rate was 1.0 nm/min where the sample substrate was not heated. The thickness of the a-Ge layer, t, ranged from 50 to 500 nm. The substrate temperature during the deposition, T_d, ranged from 50 to 200 °C. We note that T_d spontaneously rises from room temperature to 50 °C without heating the substrate because of the heat radiation from the Knudsen cell. The samples were then loaded into a conventional tube furnace in a N_2 (99.9%) atmosphere and annealed at 450 °C for 5 h to induce SPC. After that, we performed PA at 500 °C for 5 h to enhance the electrical properties. To avoid sublimation of Ge by reaction with oxygen,[17] PA was performed in a lamp heating furnace in a high-purity Ar (99.9999%) atmosphere.

The as-deposited Ge layers, precursors for SPC, were evaluated using X-ray reflectivity (XRR) and Raman spectroscopy (spot size 20 μm, wavelength 532 nm). Figure 1(a) shows that the relationship between the film density of the precursor and T_d is different for different t. This behavior can be explained as follows. As the migration of Ge atoms reaching the substrate becomes more active, the film density increases and approaches the crystal. Since Ge is difficult to adhere to SiO_2,[28] migration is active on the SiO_2 substrate. In contrast, because Ge easily adhere to each other, migration is not active on the Ge film. Reflecting these phenomena, the film density becomes higher as the film becomes thinner for T_d = 50 °C (Fig. 1(a)). The higher T_d, the more the migration is promoted and the film density approaches the crystal, as seen for t = 100 and 200 nm. Meanwhile, for t = 50 nm, the film density does not approach that of crystalline Ge. This behavior is not completely understood, but possibly due to residual strain

in a thin film. In the case of the a-Ge film on a SiO_2 substrate, the tensile strain due to the film formation is more remarkable in the thinner film.[38,39] We speculate that the effect of tensile strain is dominant for t = 50 nm, resulting in a constant density with respect to T_d. Figure 1(b) shows broad peaks near 275 cm^{-1} corresponding to a-Ge, while Fig. 1(c) shows the sharp peaks near 300 cm^{-1} corresponding to crystalline Ge for all samples. These results indicate that the crystalline Ge nuclei start to form in the a-Ge layer for T_d > 150 °C.

After annealing for SPC, the grown Ge layers were evaluated using electron backscattering diffraction (EBSD) analysis. The EBSD images in Fig. 2(a) show that the grains are randomly oriented and the grain size strongly depends on both T_d and t. Figure 2(b) shows that there are optimum values for both T_d and t. For each t, the grain size expands with the increase of T_d, then turns to shrink. As a result, the grain size reaches the highest value at around $100 \leq T_d \leq 150$ °C. The behavior at $T_d \geq 150$ °C can be explained by nucleation during deposition of the precursor.[37] On the other hand, the cause of the behavior at $T_d \leq 100$ °C is not yet clear, but the process of nucleation and growth may depend on the atomic density of the a-Ge precursor. In order to verify the speculation, further studies to quantitatively determine the activation energies and frequency factors for nucleation and growth are strongly needed. For t = 50 nm, the grain size is relatively low over the whole T_d. For $t \geq 100$ nm, the T_d for achieving the maximum grain size value shifted to higher T_d with thicker t. Assuming that the grain size depends on the precursor density, these behaviors are consistent with the results in Fig. 1(a). For $t \geq 100$ nm, the grain size became smaller with increasing t. This result likely reflects the increase of bulk nucleation with the increasing t.[36,40] As a result of these phenomena, the maximum grain size value is 3.8 μm for the sample with T_d = 100 °C and t = 100 nm.

The electrical properties of the SPC-Ge layers before PA were evaluated using Hall effect measurements. All samples showed p-type conduction, similar to conventional non-doped poly-Ge.[17,27,29,34] This is because point defects in Ge provide shallow acceptor levels and then

generate holes at room temperature.[35] There are three possible locations of point defects: the interface between Ge and SiO_2, Ge grain boundaries, and within Ge grains. Figure 3(a) shows that hole concentration decreases with increasing t for T_d = 50 °C. This behavior is the same as the previous study on the SPC of GeSn[36] and considered to arise from point defects located at the interface between Ge and SiO_2. For t = 50 and 100 nm, the hole concentrations are reduced for T_d > 50 °C. These make the t dependence of the hole concentration small for T_d > 50 °C. These behaviors suggest that the point defects located at the interface between Ge and SiO_2 are reduced by the heating deposition of the precursor. For T_d > 50 °C, the hole concentration increases as T_d increases for each t. This behavior can be explained from the perspective of the point defects located at grain boundaries and within grains. Since the grain boundary decreases as the grain size increases, point defects due to grain boundaries decrease. Reflecting the change in grain size with respect to T_d (Fig. 2(b)), point defects due to grain boundaries are the lowest at around T_d = 125 °C. On the other hand, in crystal growth, as the growth rate increases, vacancies are more easily taken into the grain. Since the growth rate increases with increasing T_d,[37] higher T_d likely provides more vacancies in the Ge grains. As a result of the balance between the defects in the grain boundary and grain, the hole concentration behaves as shown in Fig. 3(a) with respect to T_d (> 50 °C).

Figure 3(b) shows that the hole mobility of the SPC-Ge layer strongly depends on T_d, except t = 50 nm. For $t \geq$ 100 nm, the high hole mobilities (> 250 cm^2/Vs) at the high-density amorphous regime (100 ≤ T_d ≤ 150 °C) are attributed to both the large grain size and low potential barrier height of grain boundaries.[37] The thicker t tends to provide the higher hole mobility despite the grain becoming smaller (Fig. 2(b)). These results suggest that the higher hole mobility with the thicker Ge layer arises from the reduction of the interface scattering. The highest hole mobility of the SPC-Ge layer before PA is 380 cm^2/Vs obtained for T_d = 150 °C and t = 300 nm. For this sample, the limiting factors of hole mobility were discussed as follows.

From the Matthiessen's rule, the hole mobility of the Ge layer μ (= 380 cm^2/Vs) is expressed by the following equation:

$$\frac{1}{\mu} = \frac{1}{\mu_{\mathrm{P}}} + \frac{1}{\mu_{\mathrm{I}}} + \frac{1}{\mu_{\mathrm{others}}} \ , \qquad (1)$$

where μ_{P}, μ_{I}, and μ_{others} are the hole mobilities limited by phonon scattering, impurity scattering, and the other scattering factors, respectively. According to the Irvin's curve,[41] μ_{P} and μ_{I} are determined to be 1900 cm^2/Vs and 770 cm^2/Vs, respectively. Therefore, from the equation (1), μ_{others} is determined to be 1230 cm^2/Vs. These results indicate that the hole mobility in this sample is dominantly limited by impurity scattering. Therefore, the reduction of the hole concertation is necessary to further improve the hole mobility.

PA was performed for the samples of the highest hole mobility with each t. Figure 4(a) shows that the hole concentration decreases by approximately 30% for all samples. This result suggests that Ge atoms migrated by thermal diffusion and passivated point defects, generating holes, in the Ge layers. Figure 4(b) shows that the hole mobility increases for all samples. The improvement of the hole mobility is up to 100 cm^2/Vs, though the improvement rate is relatively small for t = 50 nm. The effect of PA on the electrical properties of 50-nm-thick SPC-Ge agrees with the previous study.[17] Considering the Irvin's curve and the equation (1), the hole mobility for t = 50 nm is limited by grain boundary and/or interface scattering, whereas it is dominantly limited by impurity scattering for t > 50 nm. These facts account for the t dependence of the PA effect (Fig. 4(b)). Thus, the reduction of the hole concentration by PA led to the hole mobility of as high as 450 cm^2/Vs for t = 400 nm. This Ge layer will be suitable for application to junctionless type multiple gate FETs including FinFETs.[6,29]

In conclusion, we further improved the hole mobility of the SPC-Ge layer by controlling T_{d} (50–200 °C) and t (50–500 nm) and applying PA (500 °C, 5 h). The resulting hole mobility, 450 cm^2/Vs, is the highest value to date among that of semiconductor layers directly formed on

glass. This achievement is likely attributed to the reduction of the carrier scattering factors: (i) the interface scattering was reduced by thickening SPC-Ge; (ii) the impurity scattering was reduced by PA passivating vacancy defects. These results open up the possibility for developing high-speed complimentary metal-oxide-semiconductor transistors leading to advanced system-in-displays and three-dimensional integrated circuits.

This work was financially supported by the JSPS KAKENHI (No. 26709019), the Iketani Science and Technology Foundation, and the Nanotech CUPAL. The authors are grateful to Prof. T. Sakurai at the University of Tsukuba for assistance with the Hall effect measurement. Some experiments were conducted at the International Center for Young Scientists in NIMS.

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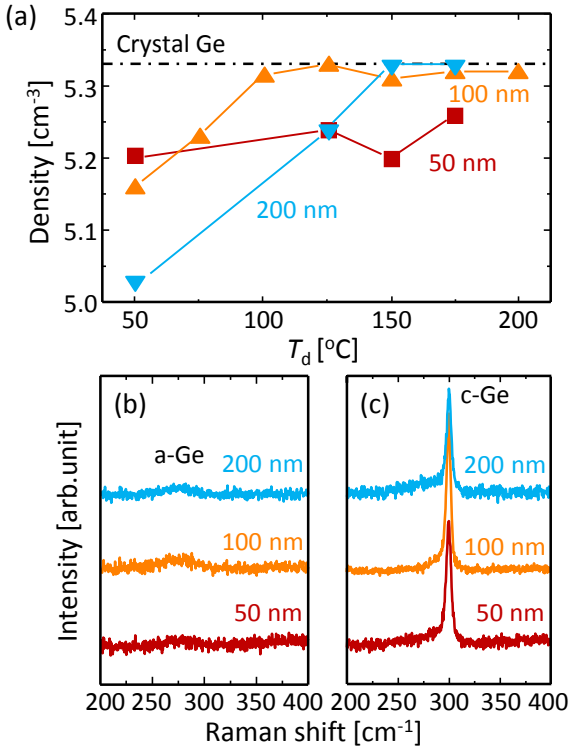

FIG. 1. Characteristics of the as-deposited Ge layers before SPC obtained by XRR and Raman measurement. (a) Density of precursor Ge as a function of T_d for t = 50, 100, and 200 nm. The data for crystalline Ge are shown by the dotted line. (b),(c) Raman spectra for the samples with T_d = (b) 150 °C and (c) 200 °C.

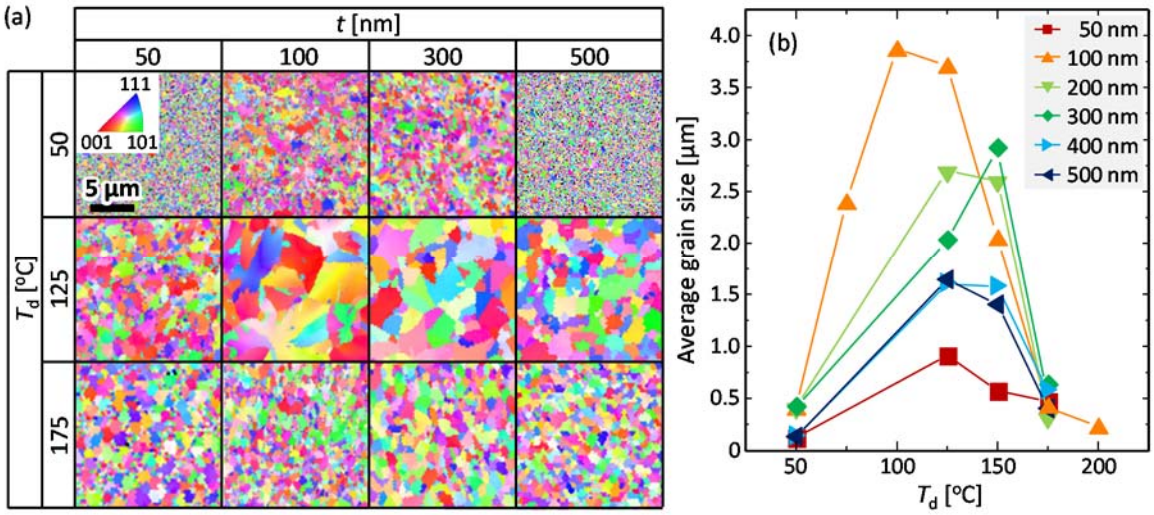

FIG. 2. Grain size of the SPC-Ge layers. (a) EBSD images of SPC-Ge summarized as the matrix composed of T_d (50, 125, and 175 °C) and t (50, 100, 300, and 500 nm). The colors indicate the crystal orientation, according to the inserted color key. (b) T_d dependence of the average grain size calculated from the EBSD images for t = 50–500 nm.

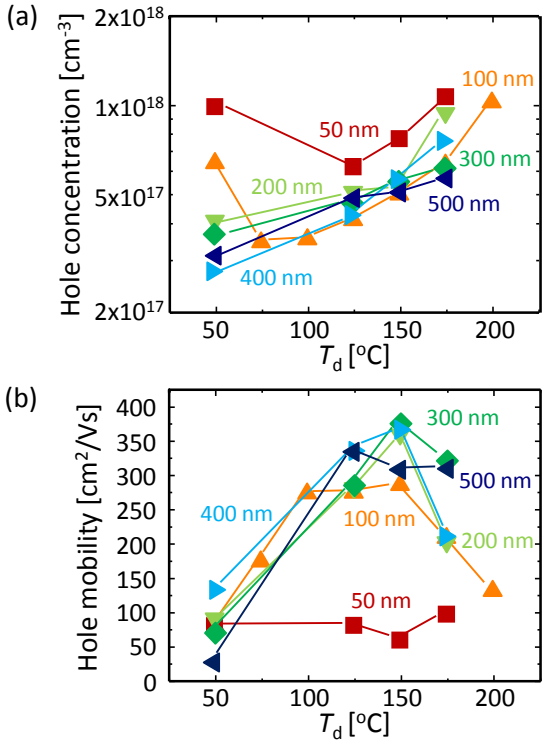

FIG. 3. Electrical properties of the SPC-Ge layers before PA for t = 50–500 nm, obtained by Hall effect measurement with the van der Pauw method. (a) Hole mobility and (b) hole concentration as a function of T_d.

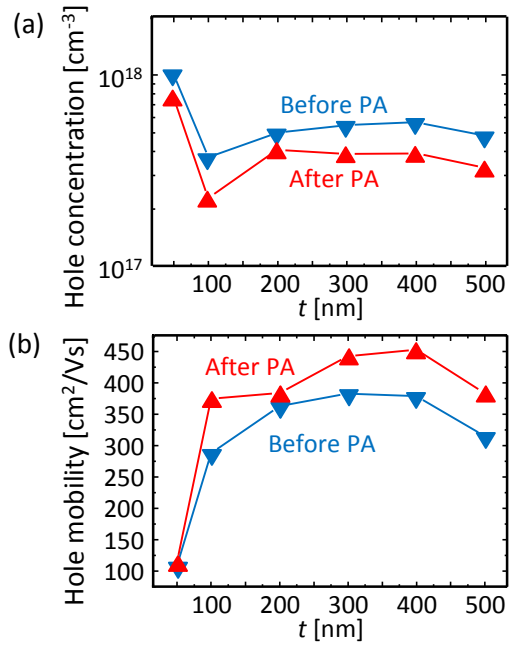

FIG. 4. Electrical properties of the SPC-Ge layers for t = 50–500 nm before and after PA at 500 °C for 5 h. (a) Hole mobility and (b) hole concentration as a function of t.