Studies on Transmitting and Receiving Device Technologies in High-speed Access Network Equipment

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Atsushi Kanda

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Graduate School of Systems and Information Engineering

University of Tsukuba

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Abstract

This dissertation presented research results regarding technologies to attain or improve transmitting and receiving devices in next-generation advanced high-speed access network equipment. The explosive growth of data traffic due to the spread of the Internet has been accelerating the demand for larger data transmission capacity in access network systems. Wired and wireless access network systems co-exist according to their applications. For the access network equipment, not only data transmission speed but also size and cost are important factors to be considered. In wireless access, increasing the carrier frequency to the millimeter-wave region is one of the key technologies for higher data transmission speeds. On the other hand, in wired access, especially optical access, faster optical modulation is required for increasing data transmission capacity. Besides, since the optical access networks are widely used today, optical access systems of different speeds have to co-exist on the same existing optical distribution network. However, conventional device technologies have three main problems that must be addressed to achieve advanced transmitting and receiving devices in high-speed access network equipment. (1) The size and cost of millimeter-wave circuits for high-speed wireless access network equipment, especially millimeter-wave local oscillators, could not be sufficiently reduced by using a conventional oscillation stabilizing technique. (2) For optical modulator drivers used in fiber-optic communication equipment, it is difficult to achieve high-speed and large-output-amplitude performance due to the incompatibility between device speed and breakdown voltage of the transistors. (3) There is need for small and cost-effective optical modules consisting of three optical components in one package for dual-rate optical access systems, such as the co-existence of GE-PON and 10G-EPON in one fiber-link.

In this study, to solve these problems, the following three technologies were established. (1) An MMIC technology for reducing size and cost of a 60-GHz full-monolithic phase-locked oscillator using a GaAs MMIC sampling phase detector. (2) A circuit technology—a series-connected voltage-balancing pulse driver with direct-coupled current switch architecture, which achieves compatibility between high-speed operation and high output amplitude for an optical modulator driver. (3) A module assembly technology for reducing size and cost of an optical module consisting of three optical components for dual-rate optical access systems by a light collection system with a low-magnification long-focus lens and a low-cost design of optical the components.

In chapter 2, circuit technology for reducing size and cost of a 60-GHz full-monolithic phase-locked oscillator (PLO) chip set for millimeter-wave wireless access network equipment was

proposed. The uniplanar structure reduced the circuit size drastically, and the use of a GaAs MMIC SPD made the PLO simple and compact. Consequently, all the circuits could be integrated into as few as three chips, and the chip area was 5.5 mm^2 for the oscillator and 3.0 mm^2 for the SPD, which contributes to reducing material cost and assembly cost. The oscillator stabilized at 56.0–60.0 GHz in a phase-locked condition. The SSB phase noise in the loop bandwidth was suppressed to the noise floor of the PLL, and it was as low as −90 dBc/Hz at 1-MHz offset from 60.0 GHz in spite of the low Q full-monolithic circuitry.

In chapter 3, circuit technology for achieving compatibility between high-speed operation and high output amplitude for an optical modulator driver was proposed. A series-connected voltage-balancing configuration can output a high voltage proportional to the number of series-connected transistors by sharing the voltage among the transistors. Novel direct-coupled current switch architecture suppresses undershooting in gate-drain voltage during switching and prevents the FETs from exceeding the gate-drain breakdown voltage. The fabricated driver core circuit using 0.1-μm InP HEMTs showed 3.7-Vpp single output with clear eye opening for 10-Gb/s data patterns. Moreover, a series-connected voltage-balancing pulse driver with a high-driving-capability input buffer improved the performance drastically. With the input buffer, the −3 dB limiting bandwidth of the driver increased from 11 to 30 GHz. The decreases in rise and fall times much improved the waveform of the 10-Gb/s eye opening with an output voltage swing of 3.6 Vpp. The driver showed a sufficient speed margin for 10 Gb/s and potential for higher bit rate operation

In chapter 4, module assembly technology for reducing size and cost of an optical module consisting of three optical components for dual-rate optical access systems was proposed. A small and low-cost optical triplexer module was successfully developed for 10G-EPON applications. Reducing optical path length by means of a light collection system with a low-magnification long-focus coupling lens made the triplexer the smallest without degradation of optical coupling efficiency. A low-material-cost design for the EADFB-LD transmitter and eliminating lenses yielded cost reduction. The 10G/1G dual-rate burst-mode TIA with feedback AGC provides superior receiver sensitivity. As a result, excellent performance has been achieved that complies with the IEEE 802.3av PR30, 802.3av PRX30, and 802.3ah PX20 standards.

The above research results provide fundamental data regarding technologies that can attain or improve transmitting and receiving devices in next-generation advanced high-speed access network equipment.

Contents

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Chapter 1

Introduction

1. Introduction

1.1. Background

This chapter describes the background and the aim of this study. Technical issues associated with transmitting and receiving devices used in the high-speed wireless and optical access network equipment are discussed. The dissertation's organization is shown at the end of this chapter.

Today, communications networks have expanded all over the world and have become indispensable to our daily lives. The current communications network hierarchy in Japan is illustrated in Fig. 1.1 [1.1]. A communications network mainly consists of core networks that connect inter-areas, metro networks that connect inner-city areas, and access networks that connect backbone (core and metro) networks to end-users. Early access networks started as a part of the public telephone network and the subsequent Integrated Services Digital Network (ISDN) [1.2]. As the Internet became popular, data traffic increased explosively and exceeded phone traffic, resulting in the emergence of new technologies to increase data transmission capacity. To support the demand for higher transmission speeds for access networks so that the end-users could handle more data traffic, the backbone networks also evolved.

At present there are basically two different types of broadband access network systems: wired access networks and wireless access networks. A wired broadband access network includes digital subscriber lines (DSLs) [1.3], cable television (CATV) [1.4], and an optical access system known as fiber-to-the-home (FTTH) [1.5]. On the other hand, a wireless broadband access network includes wireless local area networks (LANs) or Wi-Fi, cellular phones (including those of the third-generation (3G) [1.6][1.7], long term evolution (LTE) [1.8], and personal handy-phone system (PHS) [1.9]), fixed wireless access (FWA) [1.10], and mobile wireless access other than cellular phones. Wired and wireless access networks have co-existed according to their applications. A wireless access system should provide a mobile and flexible network configuration; therefore, downsizing the equipment is essential. On the other hand, wired access, especially optical access, should optimize long-distance and large-capacity transmission capability.

The demand for access network infrastructure with larger data transmission capacity has accelerated. Fig. 1.2(a) and (b) show the trends in the number of subscribers for fixed and mobile broadband access infrastructures in Japan from 2010 to 2016 [1.11]. As shown in Fig. 1.2(a), the number of FTTH subscribers continues to increase drastically, and it reached more than 25 million in 2016. Furthermore, as shown in Fig. 1.2(b), the number of subscribers to cellular phone service

and services in other wireless access network systems has reached approximately 200 million in 2016. It should be noted that not only the number of cellular phone subscribers but also the number of subscribers with other wireless access network systems keep growing steadily. Fig. 1.3 shows the trends in the amount of Internet traffic for fixed and mobile access network systems in Japan from 2007 to 2016 [1.12]. The download traffic of fixed access network systems reached approximately 7 Tb/s in 2016, and it continues to increase at an explosive pace due to the spread of broadband applications such as video-streaming. The download traffic of mobile access network systems also continues to increase, though at a far slower pace than fixed access network systems.

In order to meet the demand for enlarging data transmission capacity, advanced technologies for access networks have been developed.

In wireless access systems, following solutions have been introduced or considered to enlarge data transmission capacity while taking full advantage of mobility and flexibility for network configurations:

1. Increasing carrier frequency
    - from microwave radio frequency (300 MHz–30 GHz) to millimeter-wave radio frequency (30–300 GHz), especially a bandwidth categorized as “V-band” (40–75 GHz)
2. (Multilevel) modulation technology
    - QPSK (quadrature phase shift keying) modulation [1.13]
    - 16-, 64-QAM (quadrature amplitude modulation) [1.13]
3. Improving frequency utilization efficiency
    - OFDM (orthogonal frequency division multiple access) wireless system [1.14]
    - MIMO (multiple input multiple output) transmission technique [1.15]
    - Interference compensation technique

Among them, increasing the carrier frequency to the millimeter-wave region is considered one of key technologies for higher data transmission speeds. Millimeter-wave radio travels straight by line-of-sight and has high atmospheric attenuation. Conversely, since the radio interference is less strong, it is useful for short-range communications up to a few kilometers. Using millimeter-wave signal as the carrier frequency had been restricted to special applications such as military radars for a long time, as the device technology at the time was too crude for consumer millimeter-wave communications equipment. Nowadays, however, we can now exploit the wide frequency bandwidth in the millimeter-wave region, which is promising for the application of high-speed short-reach data transmission and communications among buildings. During the 1990s and the

2000s, 60-GHz-band wireless communications systems were studied extensively to realize wireless local area network and personal area network applications [1.16][1.17]. Recently the millimeter-wave carrier frequency has come under the spotlight again. IEEE 802.11ad, also known as “WiGig” [1.18], which is a next-generation wireless LAN system using 60-GHz-band radio, has been standardized, and is expected to be applied extensively.

On the other hand, in optical access systems, the following solutions have been introduced or considered to enlarge data transmission capacity by making best use of the optical-fiber’s capability of long-distance and large-capacity transmission:

1. Increasing the optical modulation rate (bit rate):
   - from 1 Gb/s (at present) to 10 Gb/s (next generation), or to 40 or 100 Gb/s (future)
2. (Multilevel) modulation technology
   - from binary modulation (on-off-keying) to PAM-4 (4-level Pulse Amplitude Modulation) [1.19]
3. Multiplexing technology
   - combined use of Wavelength Division Multiplexing (WDM) and Time Division Multiplexing (TDM)

Meanwhile cost-effective optical access systems have become more widespread by utilizing Ethernet hardware and protocol technologies and by adopting passive optical network (PON) technologies [1.20].

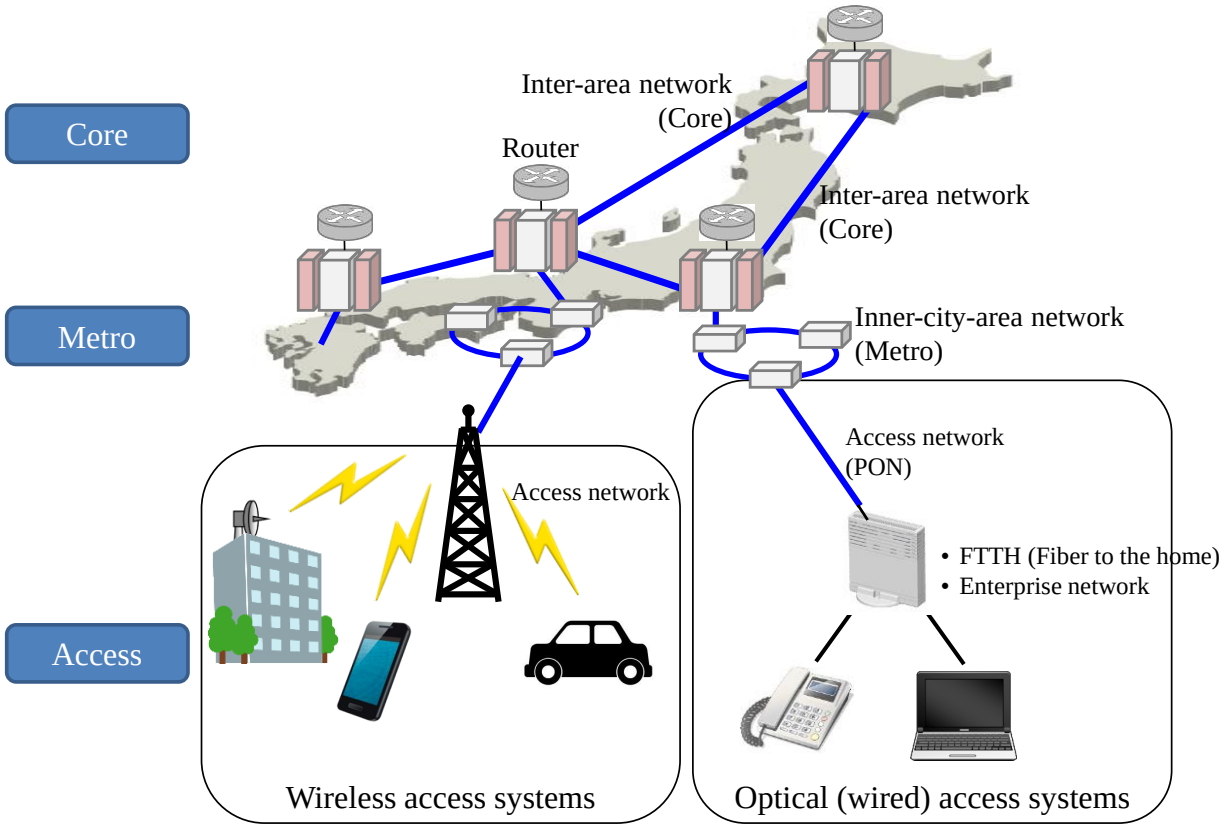
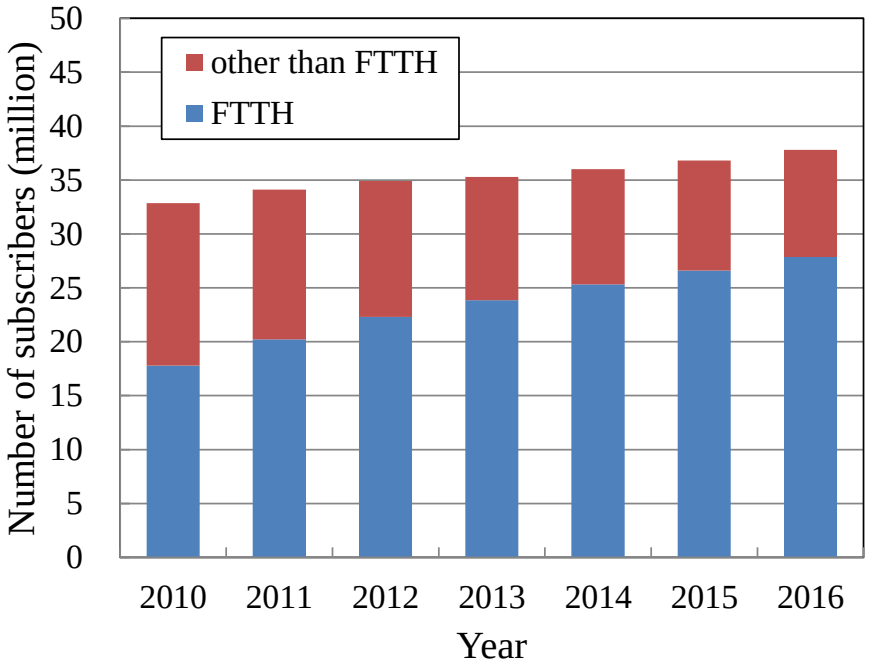
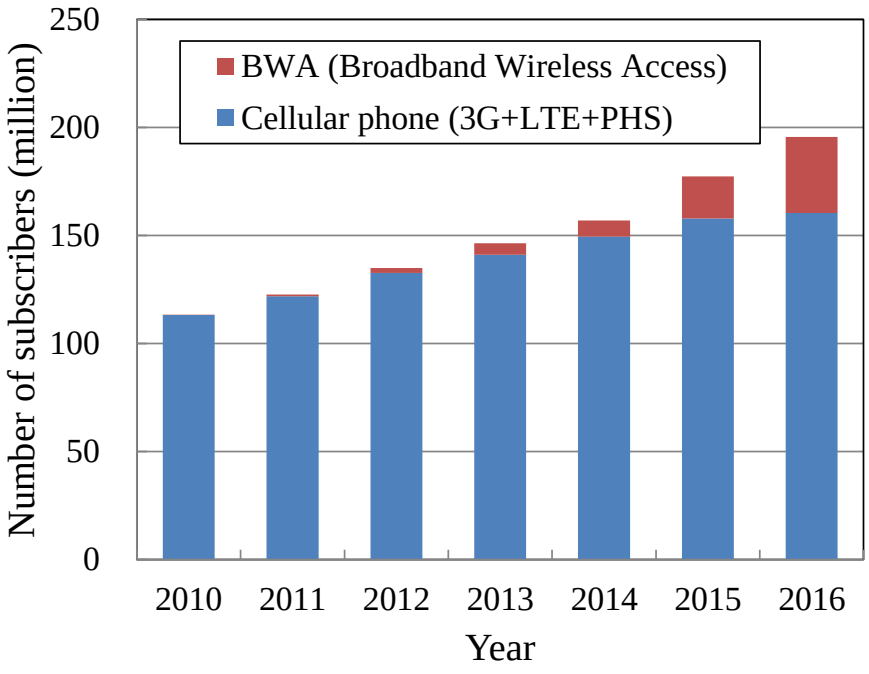


Fig. 1.1 Communications network hierarchy in Japan.



(a) Fixed broadband access networks



(b) Mobile broadband access networks

Fig. 1.2 Trends in number of subscribers for fixed and mobile broadband access network infrastructure in Japan [1.11].

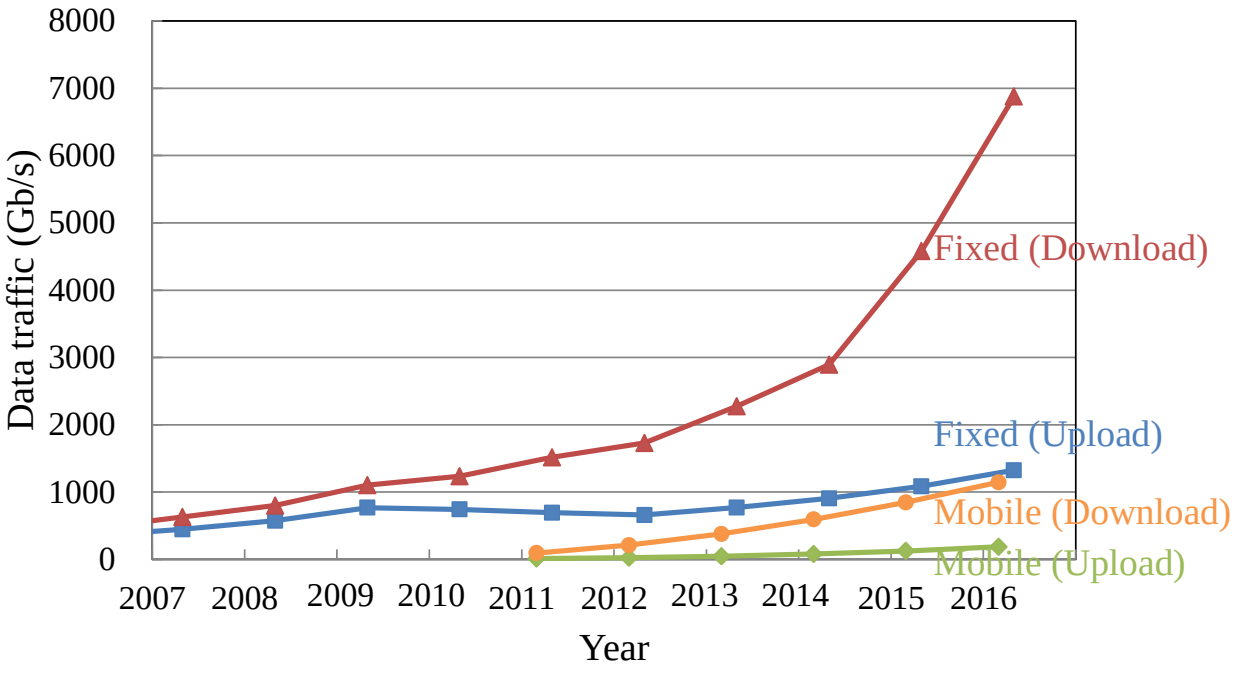


Fig. 1.3 Trends in the amount of Internet traffic for fixed and mobile access network systems in Japan [1.12].

1.2. Technical Issues in Transmitting and Receiving Device Technologies for High-speed Access Networks

1.2.1. Devices for Wireless Access Networks

To take full advantage of wireless' properties offering a mobile and flexible network configuration, wireless access network equipment has to be portable and easy to install in the system. For that purpose, the miniaturization of wireless access network equipment is crucial. In particular, downsizing the transmitting and receiving circuits is of high priority, because they are difficult to integrate on a large scale, unlike digital LSIs.

Fig. 1.4 shows a simplified diagram of a typical configuration of transmitting and receiving circuits in wireless access network equipment. Among the circuits, a local oscillator (LO)—a key device in almost all microwave and millimeter-wave communications systems—converts intermediate frequency (IF) baseband signals to and from radio-frequency (RF) carrier waves. Low phase noise and high stability are required for microwave and millimeter-wave LO's to enlarge data transmission capacity. Low cost is also important for access network equipment. However, as the LO is composed of an oscillator circuit part and a stabilization circuit part, it is the most complex among the transmitting and receiving circuits, which makes reducing its size and cost difficult.

The conventional technique for stabilizing oscillation of the LO used in microwave wireless access network equipment is to couple a dielectric resonator (DR) to it or use a phase-locked loop (PLL) with frequency dividers. However, there are some difficulties in applying these techniques to LOs used in millimeter-wave wireless access network equipment. A millimeter-wave LO coupled with a DR can never be made smaller than the DR itself. Moreover, the oscillation frequency is determined by the material and the dimensions of the DR, while stability is determined by the distance between the DR and the oscillating circuit. Therefore, those dimensions and the distance become critical for precise millimeter-wave oscillation, which leads to poorer yields and higher costs. In a millimeter-wave LO using a PLL with frequency dividers, on the other hand, even the fastest commercially available frequency dividers are not fast enough. The millimeter-wave LO has to be used in combination with a lower frequency phase-locked oscillator (PLO) and multiple frequency multipliers, which leads to larger dimensions and higher costs.

By assessing these problems, the requirement becomes clear: Another oscillation stabilizing technique that is more appropriate for millimeter-wave LO's has to be developed in place of the conventional ones.

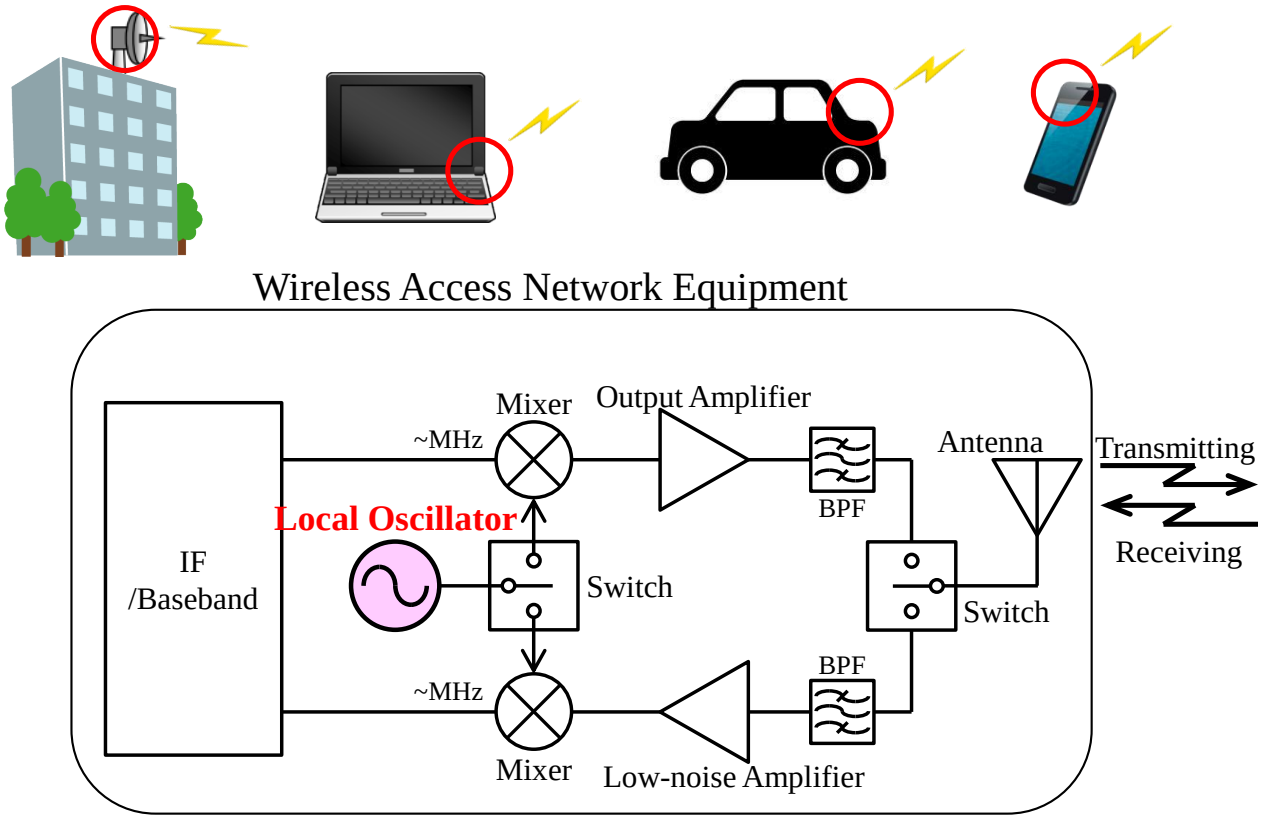


Fig. 1.4 Typical configuration of transmitting and receiving circuits in wireless access network equipment.

1.2.2. Devices for Optical Access Networks

As discussed in subsection 1.1, increasing the optical modulation rate (bit rate) is a potent way to enlarge data transmission capacity. Among optical and electrical devices for transmitter and receiver in high-speed fiber-optic communication equipment, there are some key ones for increasing the optical modulation rate. With regard to electronic devices, a driver circuit for optical modulation is one of the most important components in high-speed fiber-optic communications equipment.

Fig. 1.5 shows the basic architecture of a fiber-optic communication system and the driver circuit for the optical modulator used in the optical transmitter [1.21]. In the optical transmitter, electrical signals are converted into optical signals by biasing a distributed feedback laser diode (DFB-LD) directly or supplying electrical signals to an external optical modulator. Therefore, the optical driver circuit, as well as the DFB-LD or the optical modulator, needs faster operation to increase the optical modulation rate. In addition, the optical driver needs a large amplitude in order to enhance the contrast between the "1 (bright)" level and "0 (dark)" level of the light and improve signal-to-noise ratio (S/N ratio) of the optical signals. These requirements are not limited to access network equipment; they are also applicable to backbone network equipment.

Considering a basic current switch as a driver circuit, the maximum output amplitude the driver can achieve depends on the breakdown voltage of the transistors used in the current switch. Faster transistors are required for faster operation of the driver. However, breakdown voltage generally decreases as transistor speed increases. This makes it difficult to develop a high-speed large-voltage-amplitude driver circuit.

Focused on optical access networks, fiber-to-the-home (FTTH) systems such as the gigabit Ethernet passive optical network (GE-PON) are widely used today. For larger transmission capacity, the 10-gigabit Ethernet passive optical network (10G-EPON) has been considered as a promising candidate. In the process of substituting 1G with 10G EPON, 1G and 10G will co-exist on the same existing optical distribution network [1.22], as shown in Fig. 1.6, because GE-PON systems have already been widely deployed. Therefore, with regard to optical devices, the optical transmitter and receiver modules in optical line terminal (OLT) equipment in a symmetric 10G-EPON system must have the function of the 1G-transmitter and receiver for GE-PON optical network units (ONUs), in addition to the function of the 10G-transmitter and receiver for 10G-EPON ONUs.

In order to reduce the size and cost of OLT equipment, a dual-rate optical transmitting and receiving sub-assembly with three optical components (10G-transmitter, 1G-transmitter, and

10G/1G-receiver) and wavelength division multiplexing (WDM) filters in one module, what is called an optical triplexer, has been developed [1.23]. With the introduction of new 10G-EPON systems in the near future, there is a need for smaller and cheaper optical access equipment. However, as the number of the optical components increases, the module assembly technologies become challenging and tend to become incompatible with size and cost reducing technologies.

By assessing these problems, the requirement becomes clear: With regard to electrical transmitting and receiving devices for high-speed optical communication equipment, circuit technology achieving compatibility between high-speed operation and high output amplitude for an optical modulator driver is required for increasing the optical modulation rate. With regard to optical transmitting and receiving devices, module technology to assemble these many optical components in a small and inexpensive package is required for next-generation optical access network equipment.

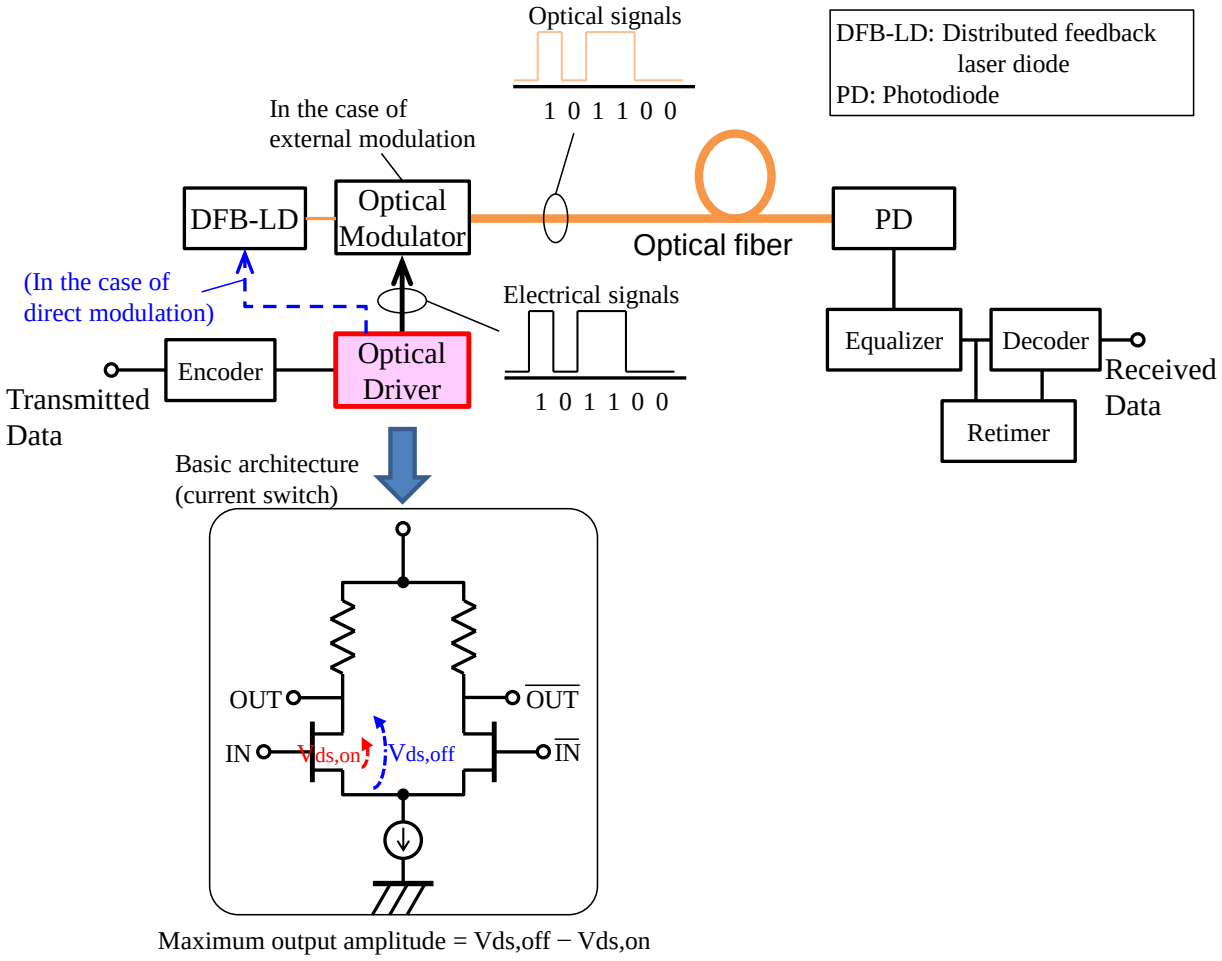


Fig. 1.5 Basic architecture of fiber-optic communication system (intensity modulation with direct detection (IM/DD) scheme) and driver circuit for the optical modulator used in the optical transmitter.

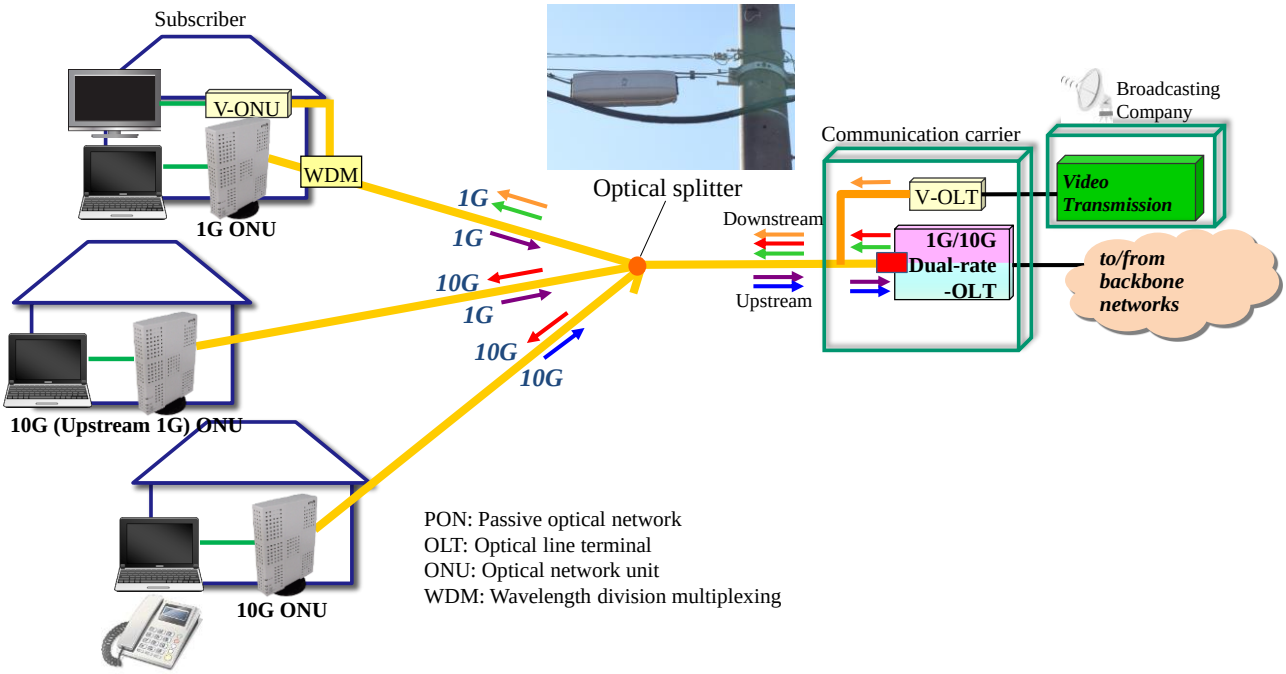


Fig. 1.6 Typical architecture of current PON optical access network system.

1.3. Aim of Studies

Considering the background, there are three main aims in this dissertation.

1. Clarify the circuit technology reducing the size and cost of a millimeter-wave phase-locked local oscillator for high-speed wireless access network equipment.
2. Clarify the circuit technology achieving compatibility between high-speed operation and high output amplitude for an optical modulator driver in fiber-optic communications systems.
3. Clarify the assembly technology reducing the size and cost of an optical module consisting of multiple optical components in one package for dual-rate optical access systems.

Accomplishing these aims will be useful when designing advanced transmitting and receiving devices in high-speed access network equipment. Moreover, the each device technology will contribute to shortening the time and reducing the resources for actualizing access systems.

1.4. Organization of Dissertation

The organization of this dissertation is shown in Fig. 1.7. This dissertation consists of five chapters.

Chapter 2 proposes circuit technology that overcomes the problems associated with conventional oscillation stabilizing technique for millimeter-wave wireless access network equipment. The circuit configuration and design of a newly developed 60-GHz full-monolithic phase-locked oscillator (PLO) chipset is described. The measured performance of each circuit composing the oscillator chipset is shown. The total performance, such as the oscillation spectrum and phase noise characteristics of the PLO with free-running state and phase-locked state, confirms the feasibility of the proposed configuration.

Chapter 3 proposes circuit technology that overcomes the problems associated with conventional optical modulator driver architecture for high-speed optical communications equipment. The basic concept, circuit design, and experimental evaluation are shown for a newly developed series-connected voltage-balancing pulse driver with direct-coupled current switch architecture. Further, the challenge associated with achieving higher driver operation speed by using

a high-driving-capability input buffer is described. The circuit design and improved performance of the driver with the input buffer are also shown. The results demonstrate the higher-speed operation potential of the proposed series-connected voltage-balancing pulse driver architecture.

Chapter 4 proposes module technology that overcomes the problems associated with the conventional assembly technique for optical modules for next-generation optical access network equipment. The configuration and the design of an optical triplexer —a dual-rate optical module with multiple optical components in one package for optical access network equipment in 10G/1G co-existing 10G-EPON systems— are presented. The focus is on the design of the optical system and design of optical components, such as the 10G transmitter, 1G transmitter, and 10G/1G receiver. The measured 10G-transmitting, 1G-transmitting, and 10G-/1G-dual-rate receiving performance of the triplexer complies fully with the 10G-EPON and GE-PON standards.

Chapter 5 describes the conclusions reached and summarizes the performance of the technologies proposed in this dissertation.

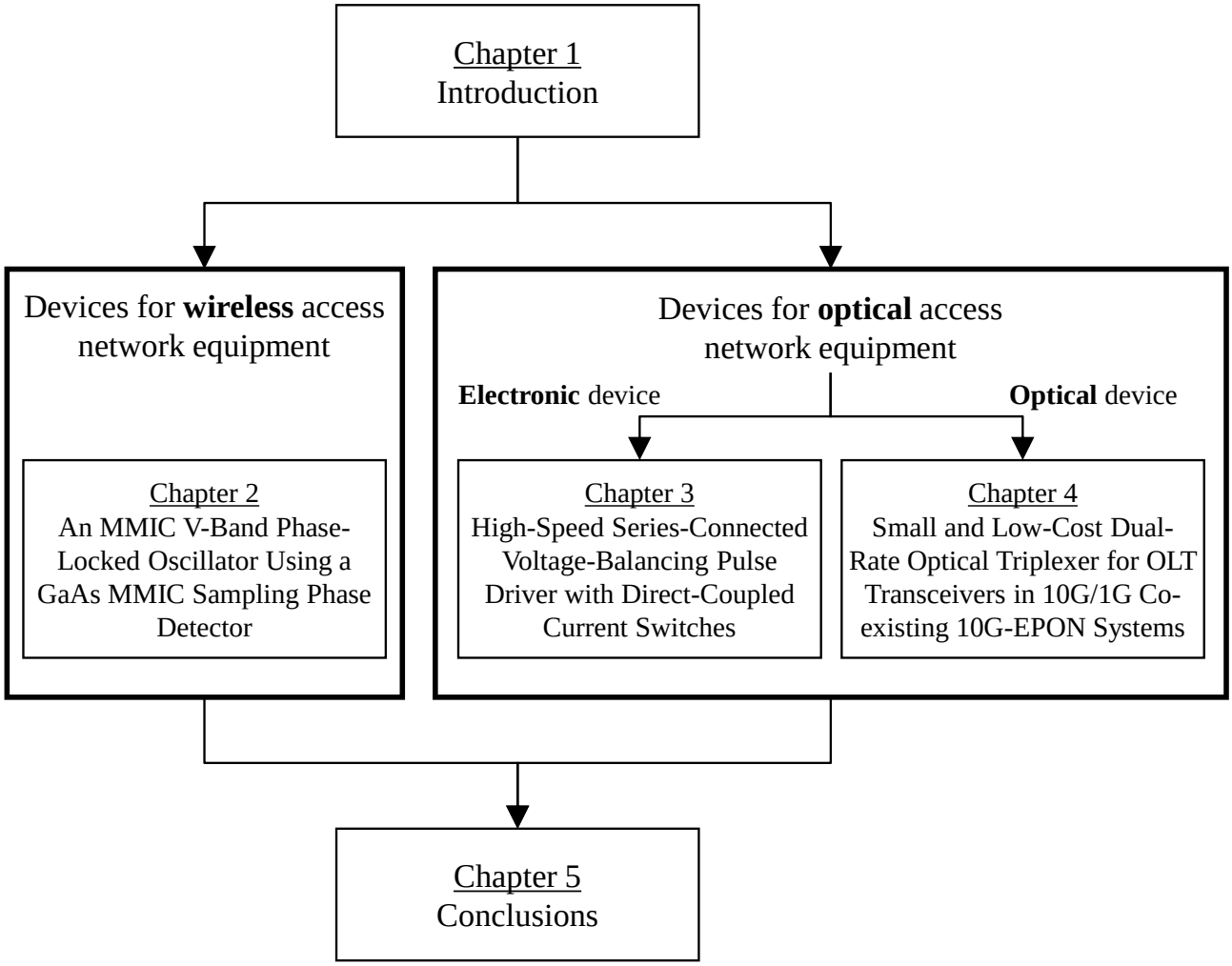


Fig. 1.7 Organization of this dissertation.

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Chapter 2

An MMIC V-Band Phase-Locked Oscillator Using a GaAs MMIC Sampling Phase Detector

2. An MMIC V-Band Phase-Locked Oscillator Using a GaAs MMIC Sampling Phase Detector

2.1. Introduction

The local oscillator (LO) is the key device for frequency conversion in all microwave and millimeter-wave communication systems. Many systems need frequency synthesis for precise and fast frequency switching. As the demand for higher data transmission speeds increases, the radio frequency (RF) will have to be increased, meaning millimeter-wave LO's will become more important. IEEE 802.11ad (WiGig) [2.1], a wireless LAN system that uses 60-GHz-band radio, has been recently standardized and is expected to be extensively applied.

A very effective way to miniaturize wireless access network equipment is to integrate RF components in monolithic microwave integrated circuit (MMIC) form. MMIC's are not used in many applications, however, because the combined cost of the chips and assembly make them expensive. Therefore, chip size should be reduced to lower chip cost and MMIC's should be integrated as highly as possible to reduce assembly costs. Higher integration will also prevent performance degradation caused by inter-chip connections.

Low phase noise and high stability are especially required for LO's in millimeter-wave communication systems. Coupling the oscillator with a dielectric resonator (DR) [2.2] is an easy way to reduce phase noise, but the oscillator could never be made smaller than the DR. Some reported millimeter-wave MMIC oscillators use a phase-locked loop (PLL) for stabilization [2.3], [2.4]. In a phase-locked oscillator (PLO), the oscillation frequency is divided or sampled in a feedback path and then compared with a reference signal. The frequency division scheme is used in most MMIC PLO's. But above the millimeter-wave region, the oscillation frequency is too high to be directly divided, and problems such as phase noise, spurs, and increased power consumption arise.

This chapter proposes the design and performance of a very compact V-band (60-GHz) full-monolithic PLO that uses a GaAs MMIC sampling phase detector (SPD). Size is reduced by: 1) making maximum use of lumped-constant elements such as meander inductors, spiral inductors, and metal-insulator-metal (MIM) capacitors and 2) densely integrating the whole circuit using a uniplanar MMIC structure. The use of the compact MMIC SPD simplifies the PLO configuration and makes the phase noise of the PLO lower than that of PLL's using frequency dividers, which are now used in most MMIC PLO's.

2.2. Concept of Millimeter-wave MMIC PLO's

A millimeter-wave oscillator can be achieved either by oscillation at a high fundamental frequency itself or by oscillation obtained from a low fundamental frequency oscillation by means of frequency multipliers. The former approach makes the oscillator smaller and simpler, but high-performance active devices such as high electron mobility transistors (HEMT's) or HBT's are needed for millimeter-wave oscillation. Moreover, a PLL cannot be used because of the speed limitation of the frequency dividers. In the latter approach, many phase-noise and spurious-signal-reduction techniques can be applied. Circuit scale tends to be large, however, because a large number of frequency multipliers are required to obtain the desired frequency. Thus, a high level of integration is important.

MMIC oscillators generally require an oscillation stabilizing technique because MMIC's have a poor quality factor Q. As summarized in Fig. 2.1, there are two effective ways to stabilize millimeter-wave oscillators: either the loaded Q (QL) of the oscillators can be increased by coupling them to high Q external DR's or a PLL can be used.

Adding high Q (unloaded Q, Qu, is normally 1000–10000) ceramic DR's is common in millimeter-wave oscillators. When the DR is arranged in the vicinity of the transmission line (e.g. microstrip line) of the oscillator, magnetic coupling occurs between the transmission line and the DR, and the Q-value of the feedback circuit (resonance circuit) in the oscillator is increased. As a result, the phase noise of the oscillation decreases. The oscillation frequency is determined by the material, the dimensions of the DR, and surrounding shields, while stability is determined by the coupling coefficient of the DR and oscillating circuit, which depends on the distance between them. Those dimensions and the coupling coefficient become critical for precise millimeter-wave oscillation as the wavelength becomes shorter. Therefore, a lot of attention must be given to the DR assembly processes, and this leads to poor yields and higher costs. Since the oscillation stability comes from the resonance, DR's are used for fixed-frequency oscillators or for narrow-band oscillators even if the frequency is tunable. Therefore, DR oscillators (DRO's) in millimeter-wave communication are usually only used in LO's or in modulation sources in a single channel.

Using a PLL in millimeter-wave oscillators is not yet popular, but this approach is superior to adding DR's in that it provides long-term stability and reduces phase noise within the loop bandwidth. It also has the advantage of widening the frequency band.

PLL's can be categorized into two types: those that use a frequency division scheme and those that use a sampling phase detection scheme. MMIC PLO's with frequency dividers have been

emphasized because it is easy to develop PLO's into synthesizers with programmable division ratios. In the millimeter-wave frequency range, however, even the fastest commercially available frequency dividers are not fast enough, so lower frequency PLO's must be used in conjunction with frequency multipliers [2.3][2.4]. The larger the order of multiplication is, the larger the dimension of circuit becomes. In addition, the faster the frequency dividers operate, the more power they consume of the order of several watts.

The SPD scheme has the potential to provide compact millimeter-wave MMIC PLO's with low phase noise and low power consumption without the use of any frequency dividers. But there has been some difficulty in developing MMIC SPD's because: 1) the step recovery diodes for the pulse generator cannot be fabricated using the GaAs MMIC process and 2) the conventional SPD dissipates a lot of driving power. So the development of millimeter-wave MMIC PLO's has had to wait for the GaAs MMIC SPD to get over those weaknesses.

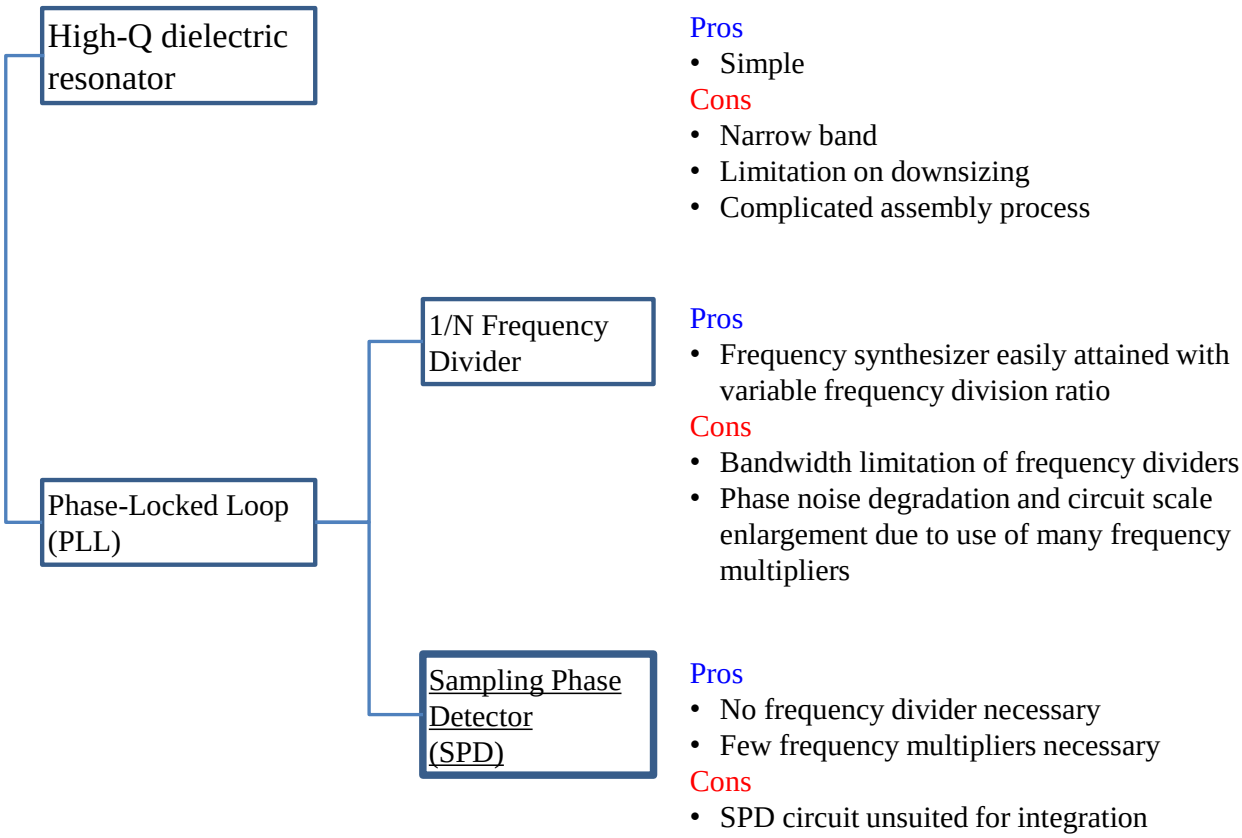
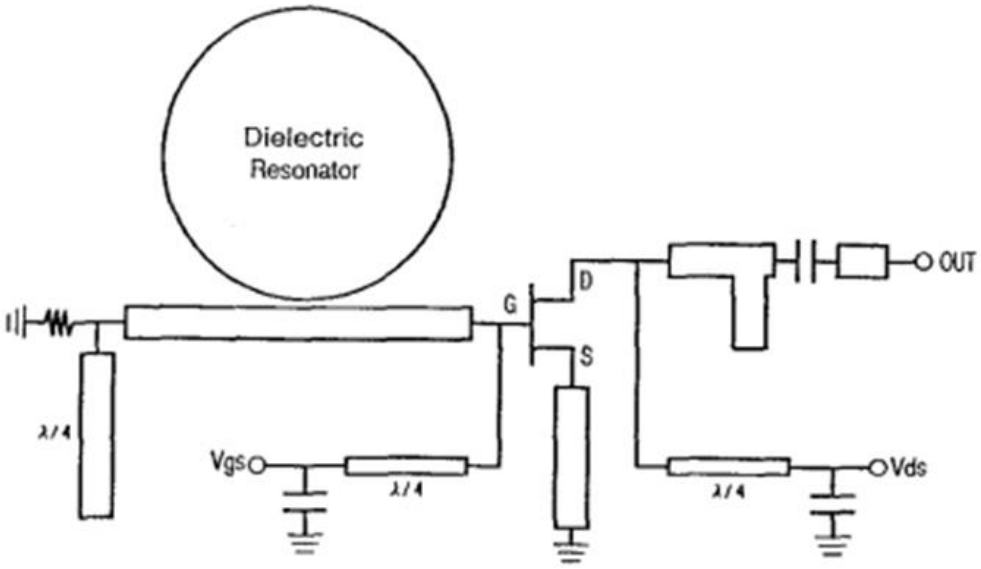
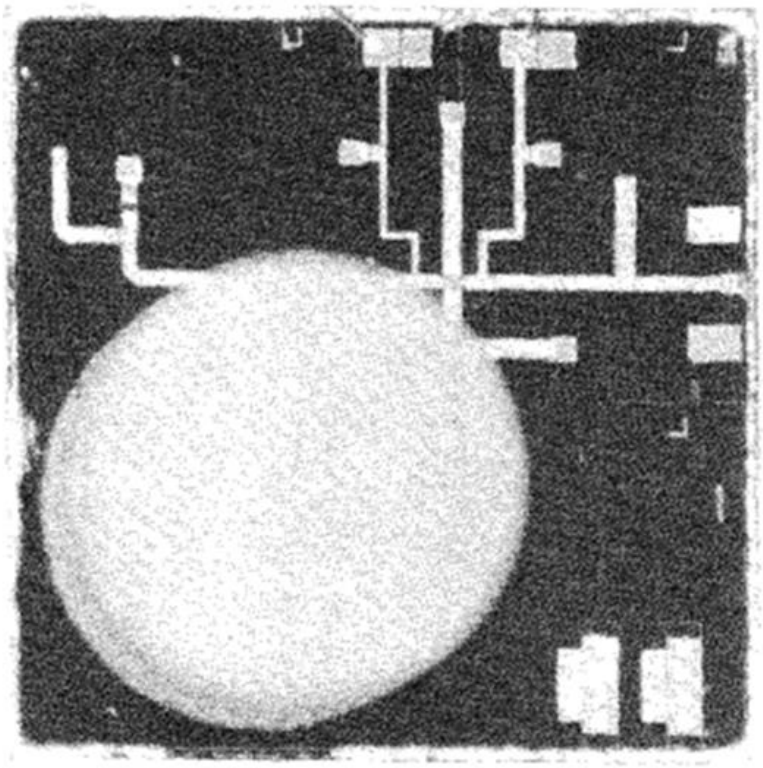


Fig. 2.1 Comparison of oscillation stabilizing techniques for millimeter-wave oscillators.



(a)



(b)

Fig. 2.2 (a) Circuit diagram. (b) Photograph of a millimeter-wave dielectric resonator oscillator [2.2]. Chip size is 2.22×2.22 mm^2.

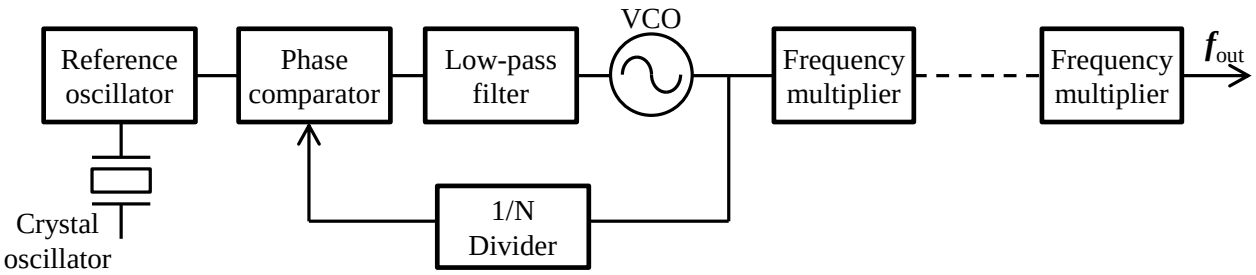


Fig. 2.3 A typical configuration of millimeter-wave PLO with a frequency divider.

2.3. Configuration and MMIC Design

A block diagram of the MMIC PLO is shown in Fig. 2.4. It mainly consists of the oscillator chip set (two MMIC chips), the SPD circuit (one MMIC chip), and an external analog adder. A conventional signal generator was used for the PLL reference oscillator in the performance measurement.

2.3.1. The Oscillator Chip Set

The colored areas in Fig. 2.4 show the MMIC oscillator chip set [2.5]. The 30-GHz oscillator chip (see Fig. 2.5) was fabricated with a high-yield 0.3-μm self-aligned ion-implanted MESFET process [2.6]. The FET devices have a cutoff frequency (fT) of 20 GHz, maximum oscillation frequency (fmax) of 70 GHz, and dc transconductance (Gm) of 200 mS/mm. The chip includes a 15-GHz voltage-controlled oscillator (VCO), a 15–30-GHz balanced frequency doubler, and a 30-GHz output cascode amplifier [2.7]. The circuit area is only 2.2 × 1.3 mm^2, due to the maximal use of lumped-constant elements, i.e., meander inductors, spiral inductors, and MIM capacitors. The VCO employs a Clapp-oscillator configuration (a variation of a Colpitts oscillator) utilizing LC resonance and positive feedback amplified by transistors. The resonance circuit consists of one inductor and three capacitors, two of which constitute a voltage divider and determine the feedback voltage applied to the input of the FET. The oscillation frequency is tuned by a 240-μm gate-width FET working as a varactor (variable capacitor) diode. The output of the VCO is split by a dual-output amplifier [2.8]. One of the amplifier outputs is for the PLL and the other is fed to the frequency doubler. The two outputs are sufficiently isolated from each other owing to the isolation of the amplifier. The 600-μm-thick substrate does not need polishing for proper circuit operation due to the use of the uniplanar structure.

The other chip, the 30–60-GHz doubler shown in Fig. 2.6, was fabricated with a 0.1-μm pseudomorphic (PM) low-noise AlGaAs/InGaAs/GaAs HEMT process. The PM HEMT devices have a cutoff frequency (fT) higher than 70 GHz, maximum oscillation frequency (fmax) higher than 110 GHz, and typical dc transconductance (Gm) of 400 mS/mm. The chip includes a buffer amplifier, a 30–60-GHz frequency doubler, and a 60-GHz amplifier. The wide use of coplanar waveguides reduces the circuit area to 2.9 × 0.9 mm^2. The buffer amplifier weakens the influence of significant changes in the input impedance of the frequency doubler. The frequency doubler has a single gate configuration and an open stub is used at the output of the PM HEMT to suppress the

30-GHz signal. The HP-Root model [2.9] was employed to optimize the nonlinear design of the frequency doubler. Precise device modeling and uniplanar element libraries yield a high conversion gain.

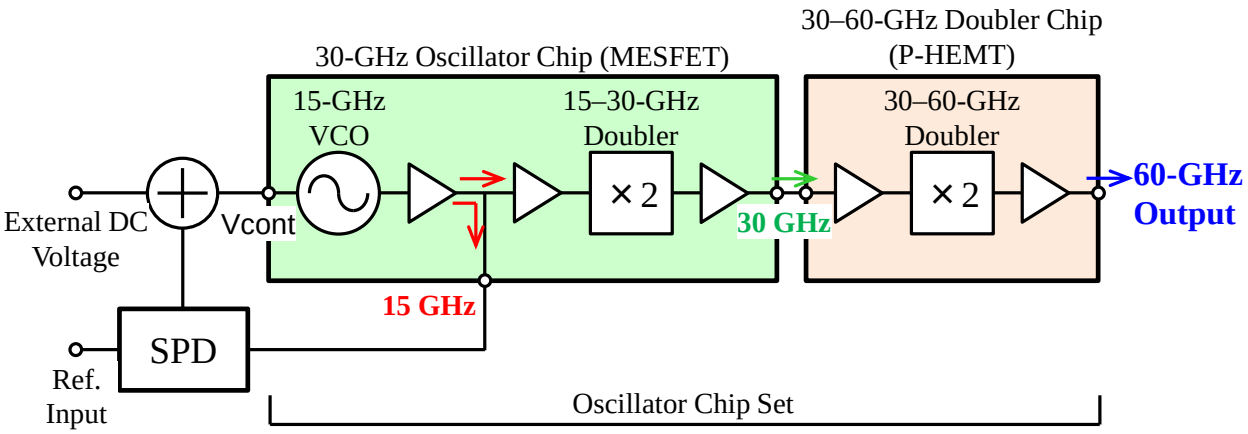
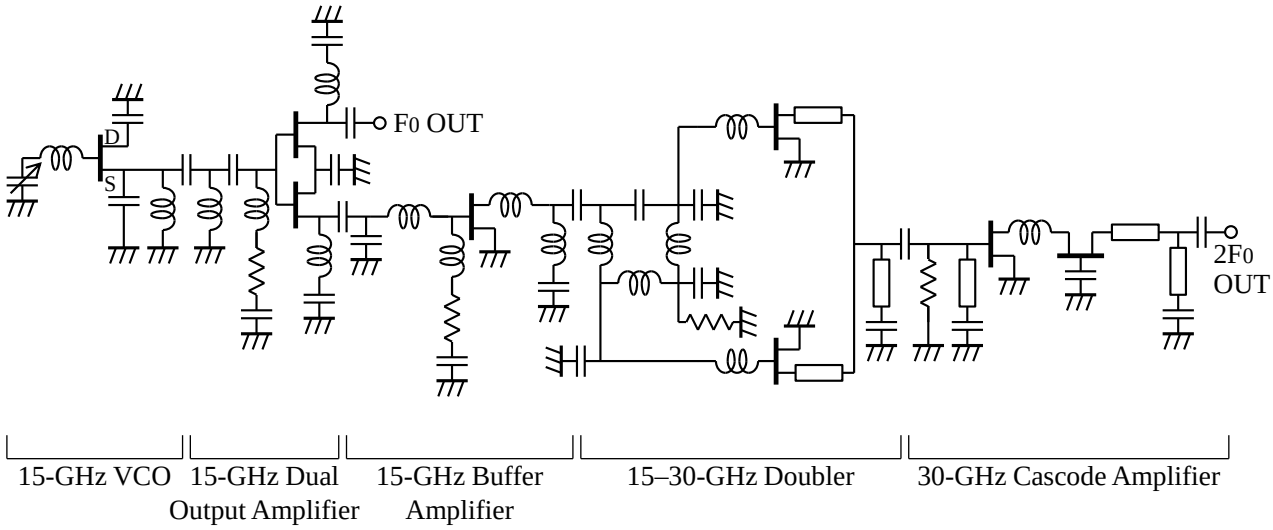
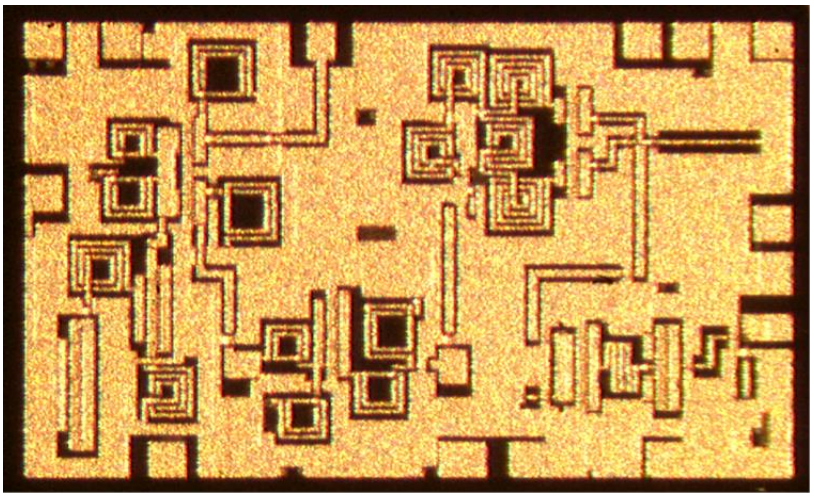


Fig. 2.4 A functional block diagram of the MMIC 60-GHz PLO.

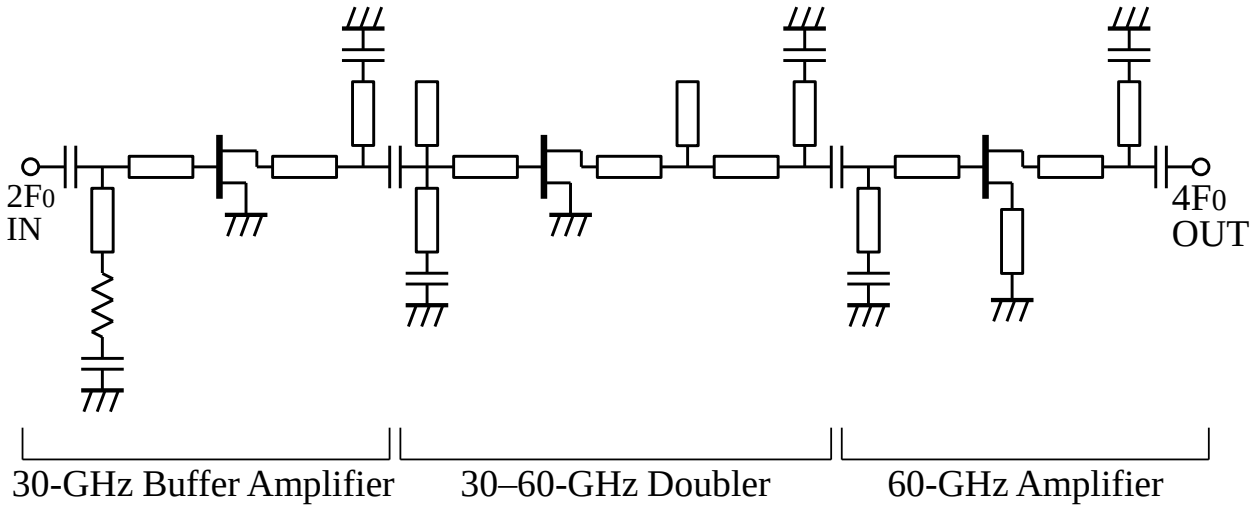


(a)

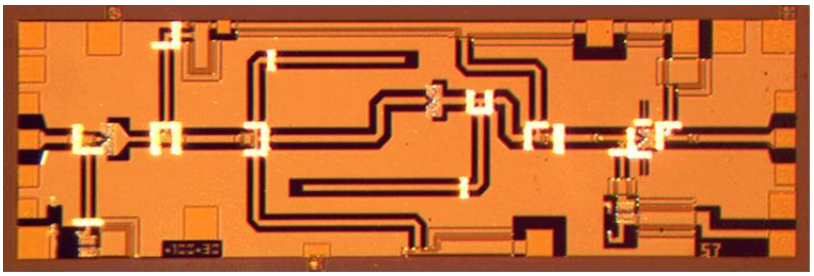


(b)

Fig. 2.5 (a) Circuit diagram. (b) Photograph of the 30-GHz oscillator chip. Chip size is 2.2 × 1.3 mm^2.



(a)



(b)

Fig. 2.6 (a) Circuit diagram. (b) Photograph of the 30–60-GHz doubler chip. Chip size is 2.9 × 0.9 mm^2.

A photograph of the oscillator chip set as a unit is shown in Fig. 2.7. The two chips are connected by 20-μmϕ Au wires. The wire inductance causes insertion loss, which degrades the output return loss of the 30-GHz oscillator chip and the input return loss of the 30–60-GHz doubler chip. To mitigate the effect of the wire inductance, all circuit parameters were optimized by simulating the total performance, including the wire inductance. The uniplanar structure allows a high level of integration and thus reduces the chip size. Integration leads to a decrease in the number of wires. Moreover, the small chip size helps to avoid undesired parasitic resonance caused by the cavity around the IC in a package.

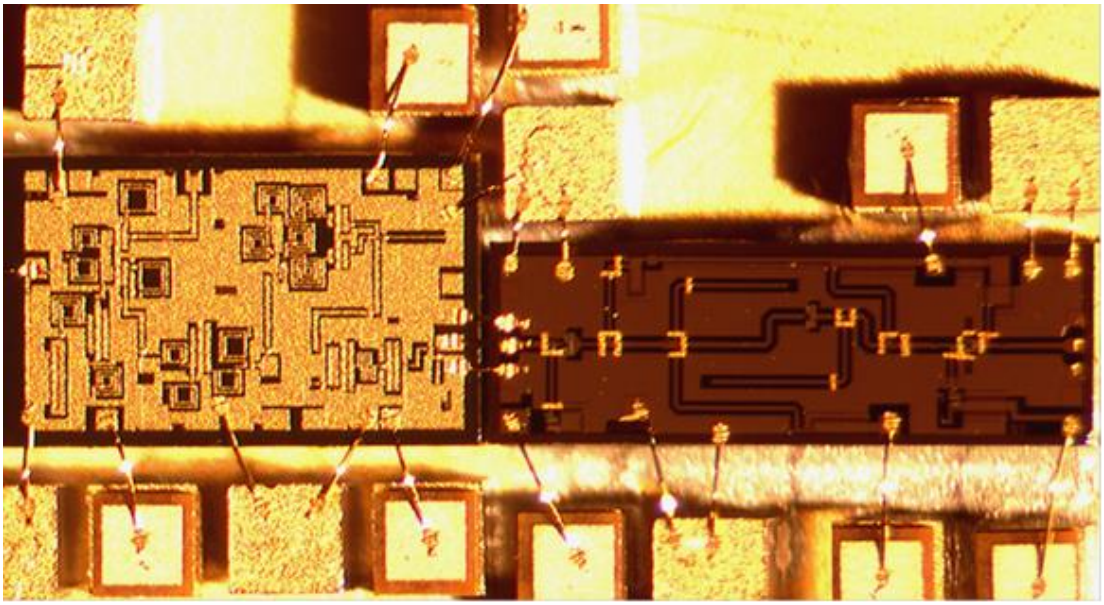


Fig. 2.7 Photograph of the oscillator chip set. The two chips are connected with Au wires.

2.3.2. The SPD Circuit

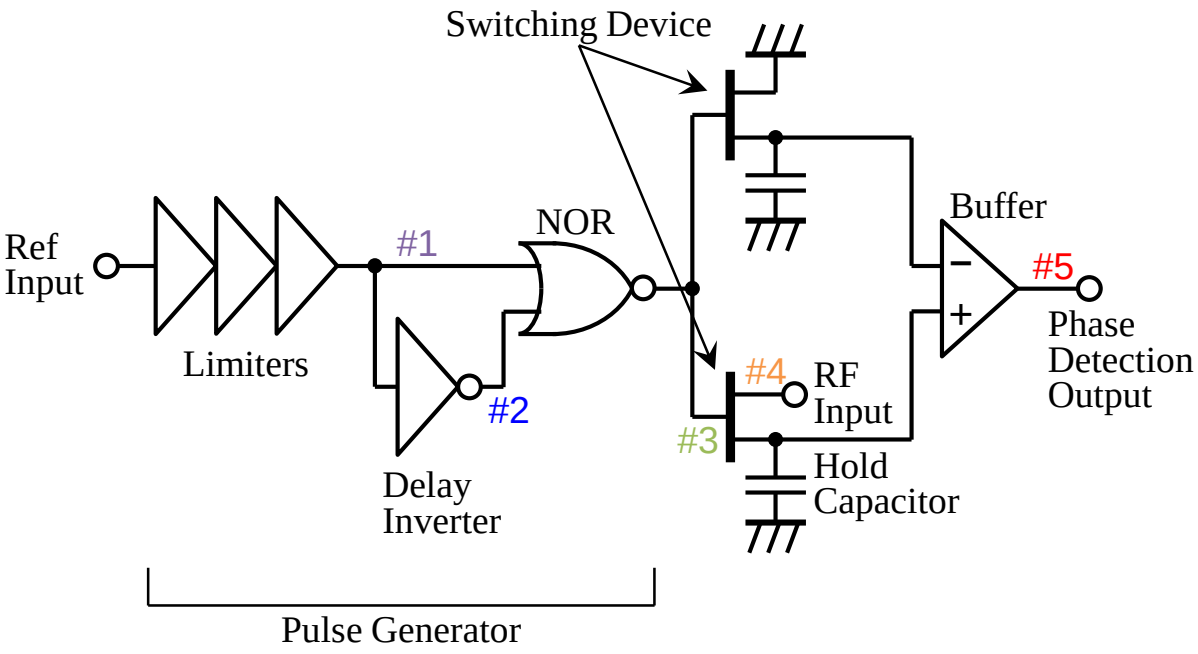
The configuration and principles of the SPD [2.10] are shown in Fig. 2.8. The pulse generator consists of limiters, a delay inverter, and a NOR gate. The switching devices are transfer-gate FETs. Two FET's are arranged in a balanced-like configuration to suppress the leakage of the sampling pulses, which are canceled at the following buffer amplifier. The reference input sinusoidal wave is shaped into a square wave by the limiters. The wave is then split in two with one part going to the NOR gate directly and the other passing through the delay inverter. Thus, narrow pulses synchronized to the reference signal are obtained at the NOR gate output, as schematically shown in Fig. 2.8. The RF signal input to the drain port of one FET is then sampled by these narrow pulses. Therefore, a sampled phase-detection output is obtained at the FET source and held on the capacitor.

These circuits were simulated using SPICE. Because this SPD does not need the step recovery diode that is used in ordinary SPD's as a pulse generator, it can operate at a low driving power of 0 dBm.

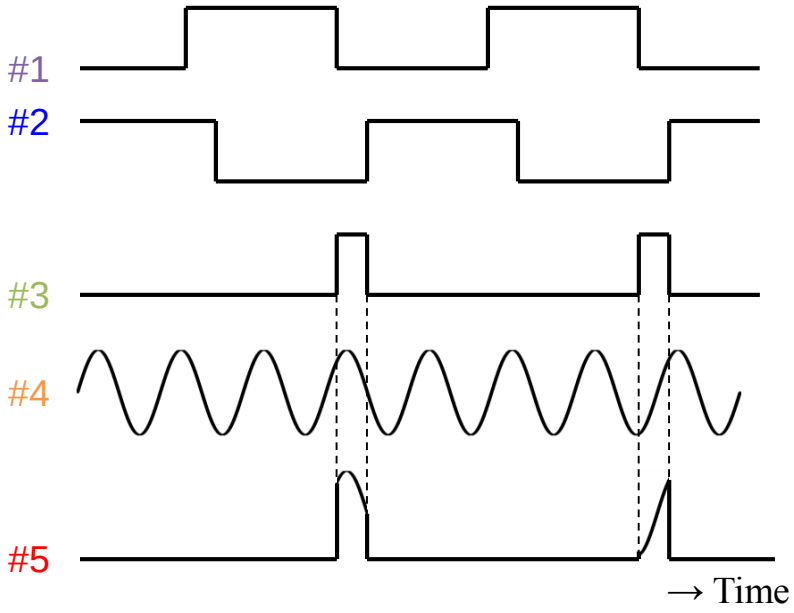
A photograph of the SPD is shown in Fig. 2.9. The circuit size is only 2.0×1.5 mm^2. It was fabricated with the same monolithic high-yield MESFET process used to fabricate the 30-GHz oscillator chip. This implies that the MMIC SPD can also be integrated into the 30-GHz oscillator chip.

2.3.3. External Components

An analog adder built with a commercially available IC is used for the DC offset of the phase-detection output voltage. No loop filter is applied to control the PLL bandwidth. Instead, a variable resistor after the SPD is used here to optimize it.



(a)



(b)

Fig. 2.8 (a) Configuration. (b) principle of the MMIC SPD.

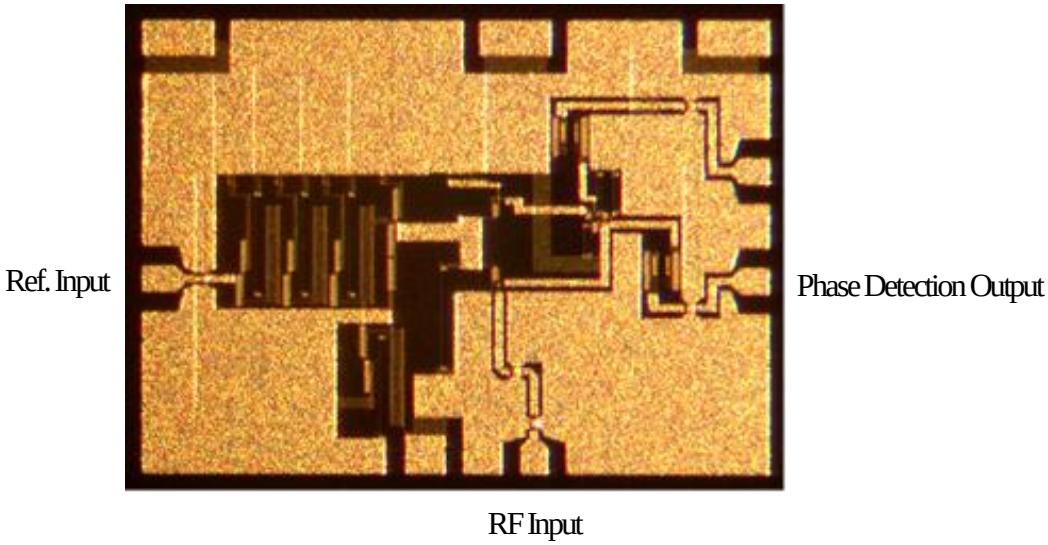


Fig. 2.9 Photograph of the MMIC SPD. Chip size is 2.0 × 1.5 mm^2.

2.4. Measured Performance

2.4.1. Oscillator Free-Running Characteristics

Fig. 2.10 shows the frequency and output power of the 30-GHz oscillator chip versus tuning voltage across the varactor. Output power of 12.5 dBm ±0.7 dB is obtained throughout the frequency range. A large signal is, therefore, fed into the frequency doubler, which uses harmonics caused by nonlinearity. The fundamental frequency oscillation for the PLL is also shown. Output power of 6.7 dBm ±1.4 dB is supplied to the SPD, which is sufficiently large for the driving power.

The frequency responses of the 30–60-GHz doubler chip at low input power are shown in Fig. 2.11. The conversion gain is 14 dB with an input frequency of 29.2 GHz. Gain is decreased when the input signal is large. Consequently, a fairly stable output level is achieved over a wide frequency range for a large signal input, as also shown in Fig. 8.

Fig. 2.12 shows the frequency and output power of the oscillator chip set versus the tuning voltage across the varactor. The frequency can be tuned smoothly from 55.6 to 60.3 GHz as the tuning voltage is changed from 0 to −7.7 V. Output power of 3.5 dBm ±1.5 dB is obtained throughout the frequency range. This is near the output saturation of a 60-GHz amplifier fabricated with a low noise PM HEMT, and is sufficient for a local oscillator signal for a millimeter-wave active frequency converter. The single-sideband (SSB) phase noise of free-running oscillation at the V-band was measured with a spectrum analyzer (Fig. 2.13). It is less than −80 dBc/Hz at 1-MHz offset when the tuning voltage is set to −5 V.

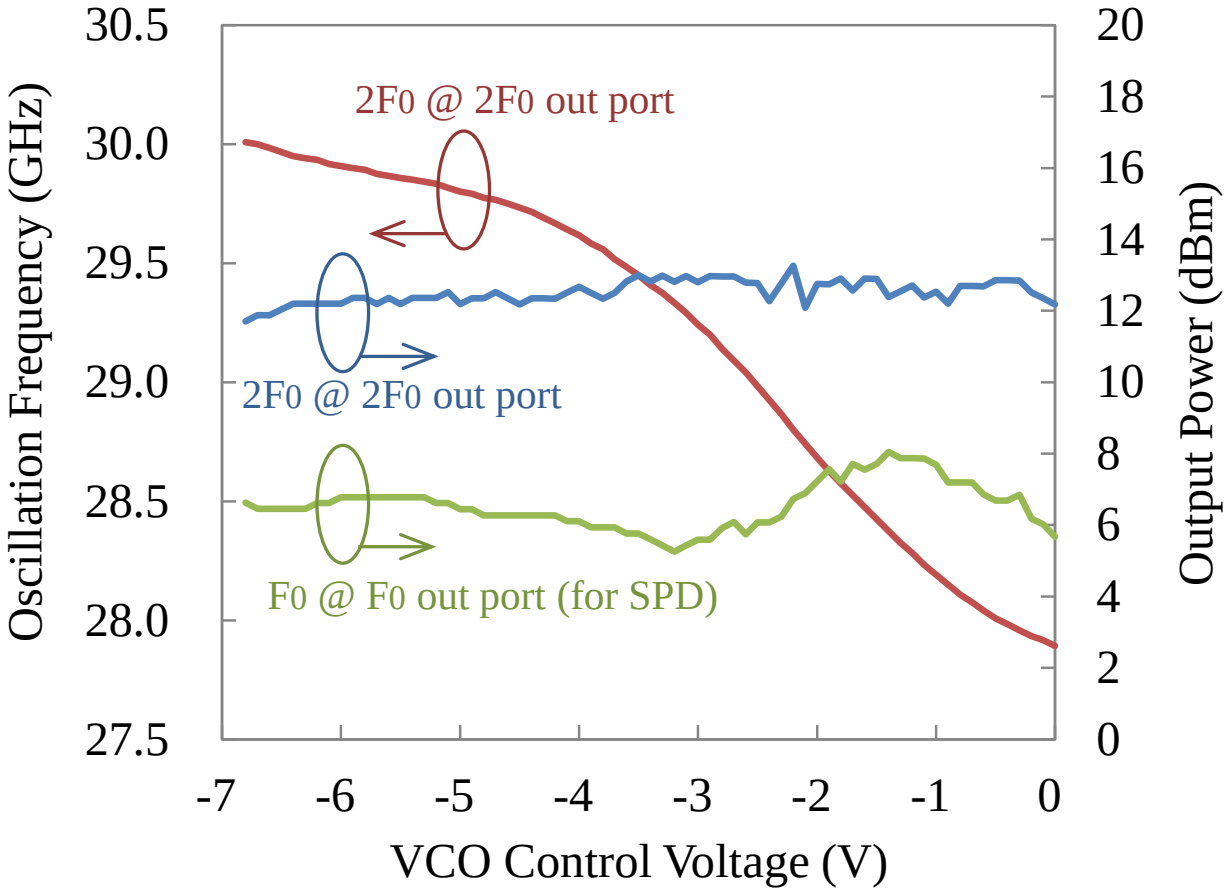


Fig. 2.10 The tuning characteristic for the 30-GHz oscillator chip.

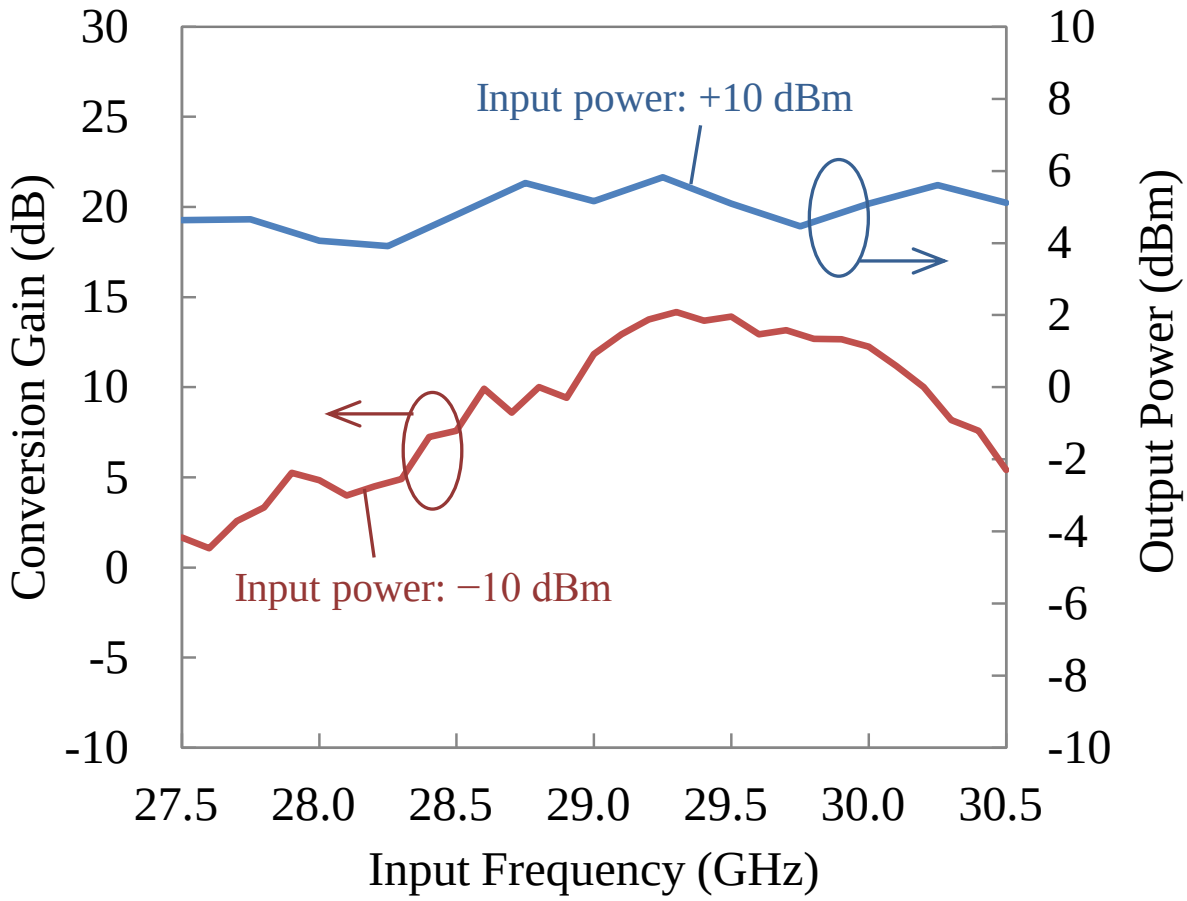


Fig. 2.11 The conversion gain at low input power and saturated output at high input power for the 30–60-GHz doubler chip.

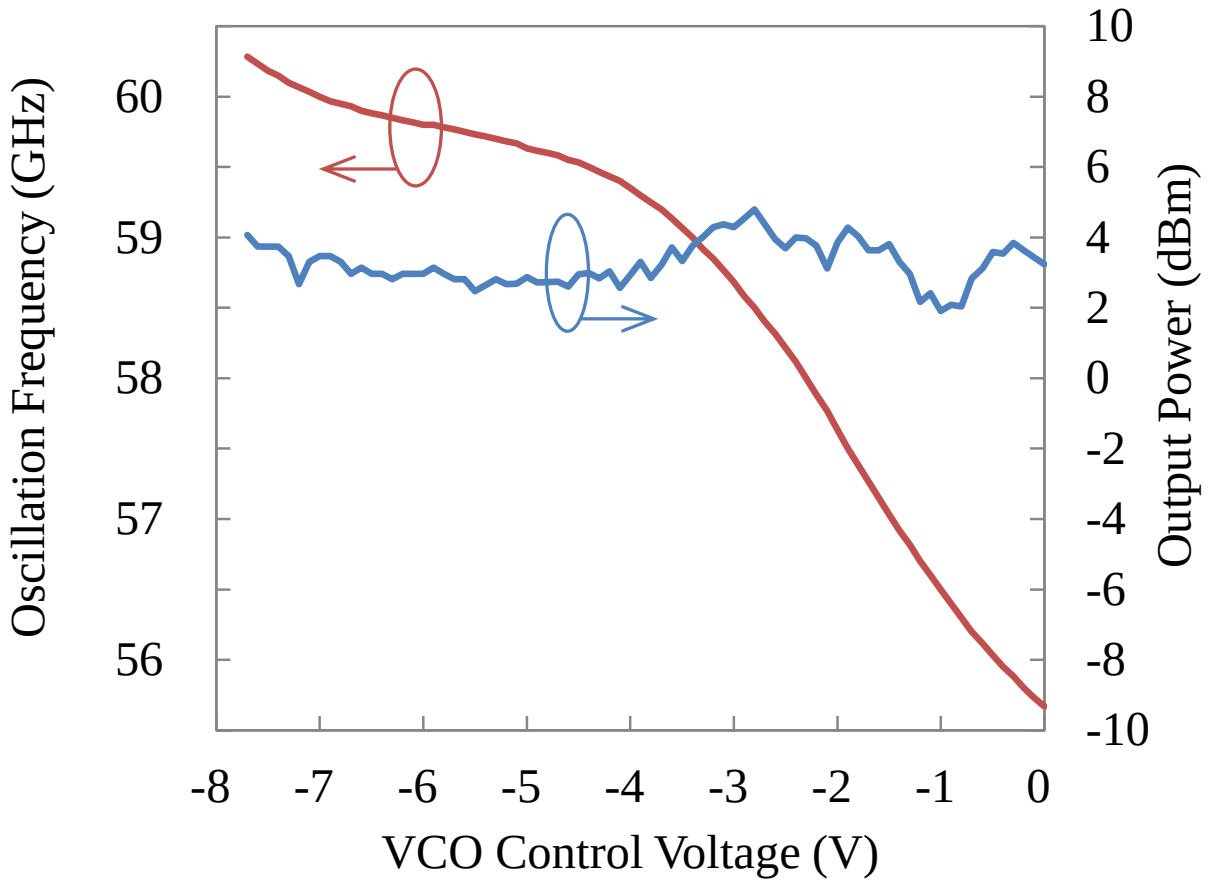


Fig. 2.12 The tuning characteristic for the oscillator chip set.

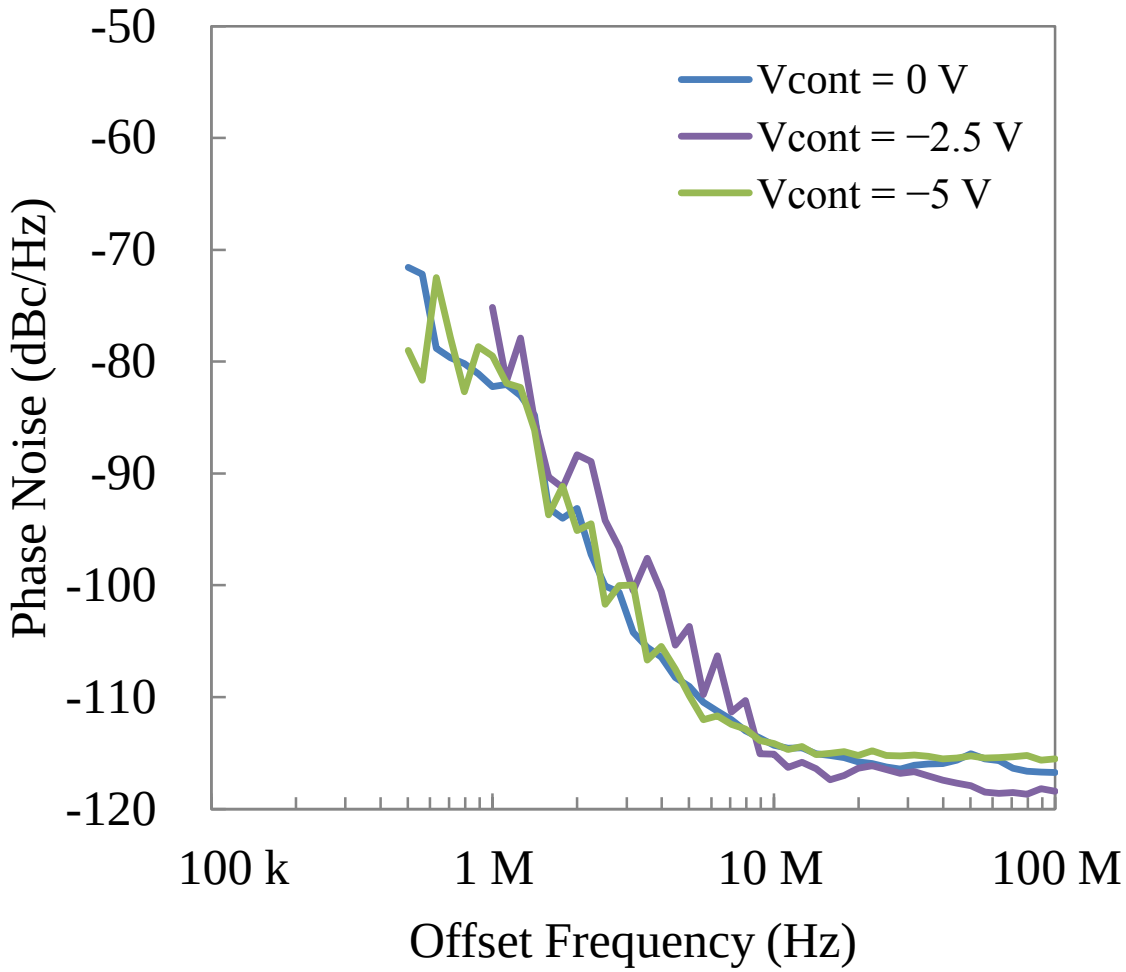


Fig. 2.13 The SSB phase noise for the oscillator chip set (free-run).

2.4.2. SPD and PLO Performance

Fig. 2.14 shows the measured phase detection output voltage of the SPD versus RF input frequency. An output of more than 100 mVpp above 15 GHz is obtained with a 100-MHz, 0-dBm reference signal.

This SPD was applied to the oscillator. Phase-locking was achieved with 800-MHz steps from 56.0 to 60.0 GHz when the reference frequency was 200 MHz. An example of the observed phase-locked spectrum at 60.0 GHz is shown in Fig. 2.15(a). The free-running spectrum near 60 GHz is shown in Fig. 2.15(b) for comparison. Note that the frequency spans in these two figures are quite different. Fig. 2.15(c) shows the panoramic wide span PLO spectrum of Fig. 2.15(a). The two traces in Fig. 2.15(c) were obtained using two alternating spectrum analyzer mixer modes. No spurs can be seen except for the fundamental 15.0-GHz signal and harmonic 30.0- and 45.0-GHz signals. For V-band use, the loss of the cable between the output terminal and spectrum analyzer is more than 6 dB around 60 GHz, and it is far more than the loss of the cable below the V-band. Thus, these undesired harmonics are actually suppressed further than can be seen in the figure. Because these signals are far from the desired 60-GHz signal, they can be easily eliminated by a simple high-pass filter. The measured SSB phase noise for phase-locked oscillation at 60.0 GHz is shown in Fig. 2.16. The phase noise is −64 dBc/Hz at 10-kHz offset and −90 dBc/Hz at 1-MHz offset from the carrier. For a local oscillator used in the 60-GHz-band IEEE 802.15.3c WPAN (Wireless Personal Area Network) standard [2.11], the phase noise characteristic of −90 dBc/Hz or less at 1-MHz offset is required in 16 QAM for high-speed wireless communications [2.12]. Although my circuit configuration cannot be applied directly as the local oscillator stipulated in IEEE 802.15.3c, it can be evaluated as a reference for the phase noise characteristic of the consideration.

The total power consumption of the PLO is about 2100 mW; 350 mW for the 30-GHz oscillator chip, 60 mW for the 30–60-GHz doubler chip, and 850 mW for the SPD.

Compared to the V-band PLO of the previous study [2.3], the size of the circuit excluding the dielectric resonator is reduced by 57% in this research. In addition, while all PLOs in previous studies are composed of high-performance technologies such as HEMTs and HBTs, we have introduced a high-yield MESFET process in part of this research.

For the PLO scheme proposed in this chapter, the fundamental oscillation frequency is determined by the operation bandwidth of the SPD; besides, oscillating frequency of the whole PLO output is limited by the operation bandwidth of the frequency multipliers. Therefore, frequency multipliers with higher operation speed afforded by using faster transistors are needed to speed up

the PLO oscillation frequency. Moreover, this PLO scheme has the potential to achieve several-hundred gigahertz operation using the state-of-the-art fastest transistors. However, a higher fundamental oscillation frequency is also needed to avoid increasing the number of frequency multipliers in practice. The operation speed of the SPD will have to be improved.

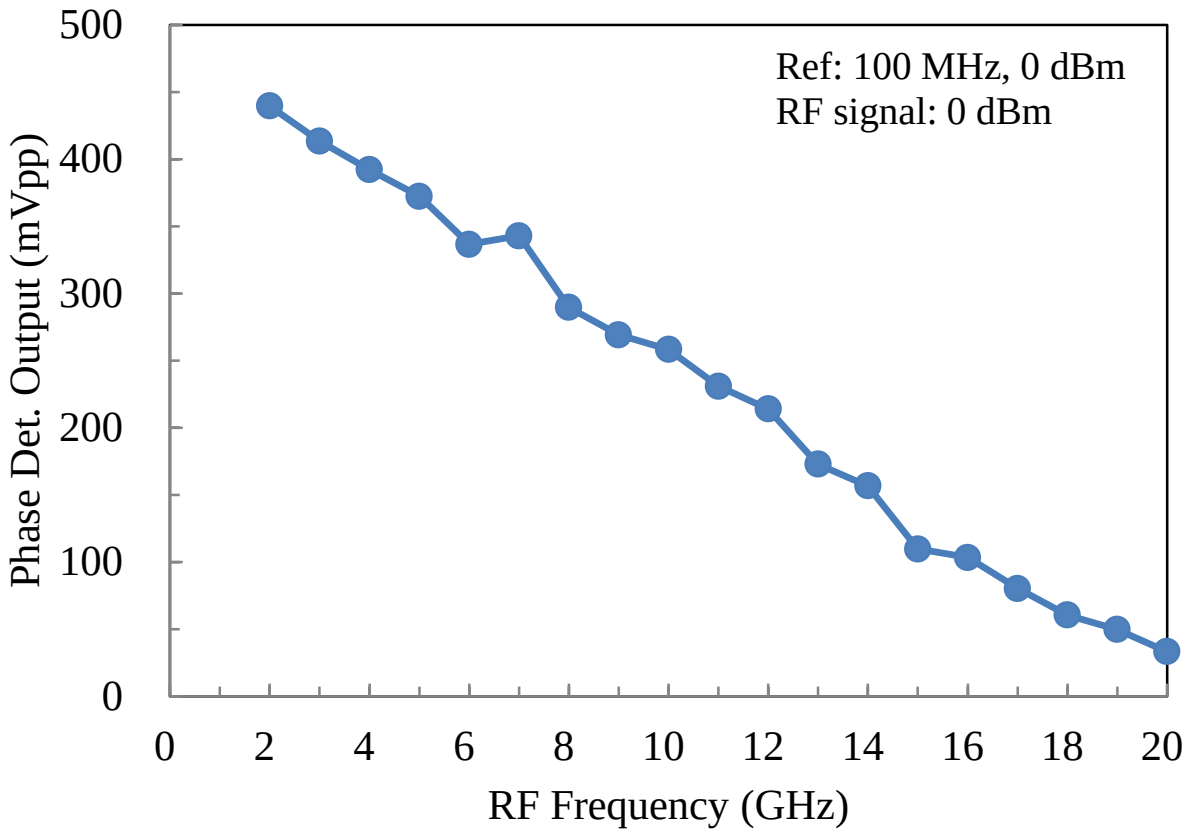
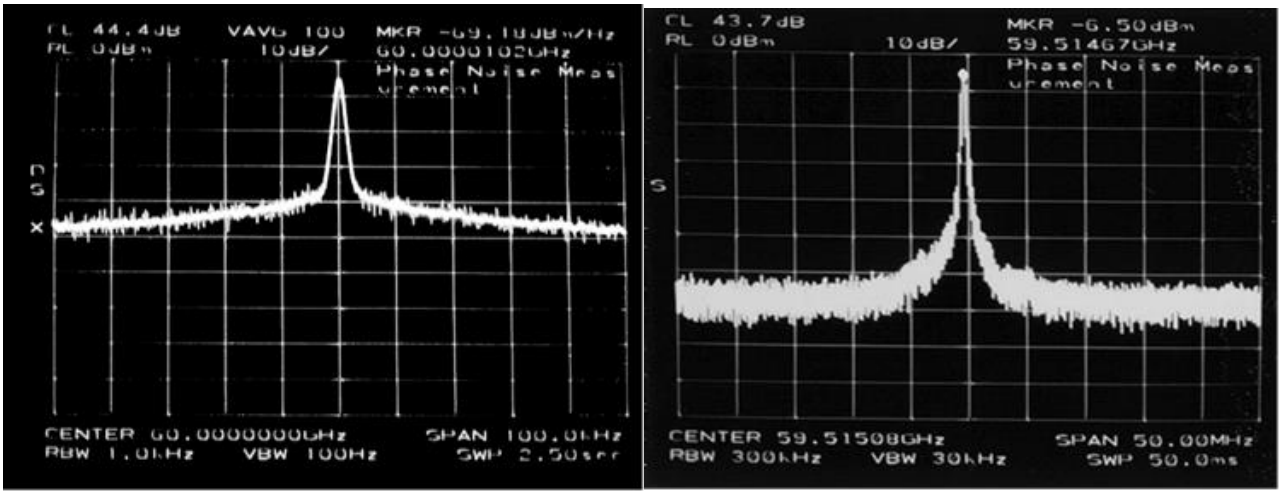
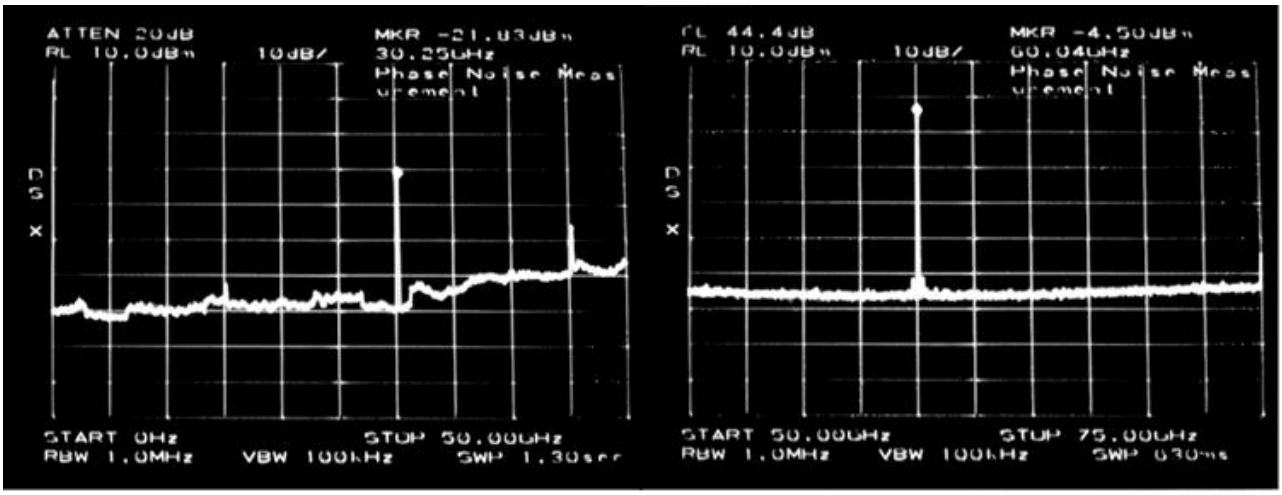


Fig. 2.14 The output voltage of the MMIC SPD as a function of RF input frequency.



(a) (b)



(c)

Fig. 2.15 PLO output spectra.

(a) Near a carrier with locked state, H: 10 kHz/div, V: 10 dB/div, RBW: 1 kHz.

(b) Near a carrier with free-run (Vcont = −5 V), H: 5 MHz/div, V: 10 dB/div, RBW: 300 kHz.

(c) Panoramic view, H: DC–50 GHz (left), 50–75 GHz (right), V: 10 dB/div, RBW: 1MHz.

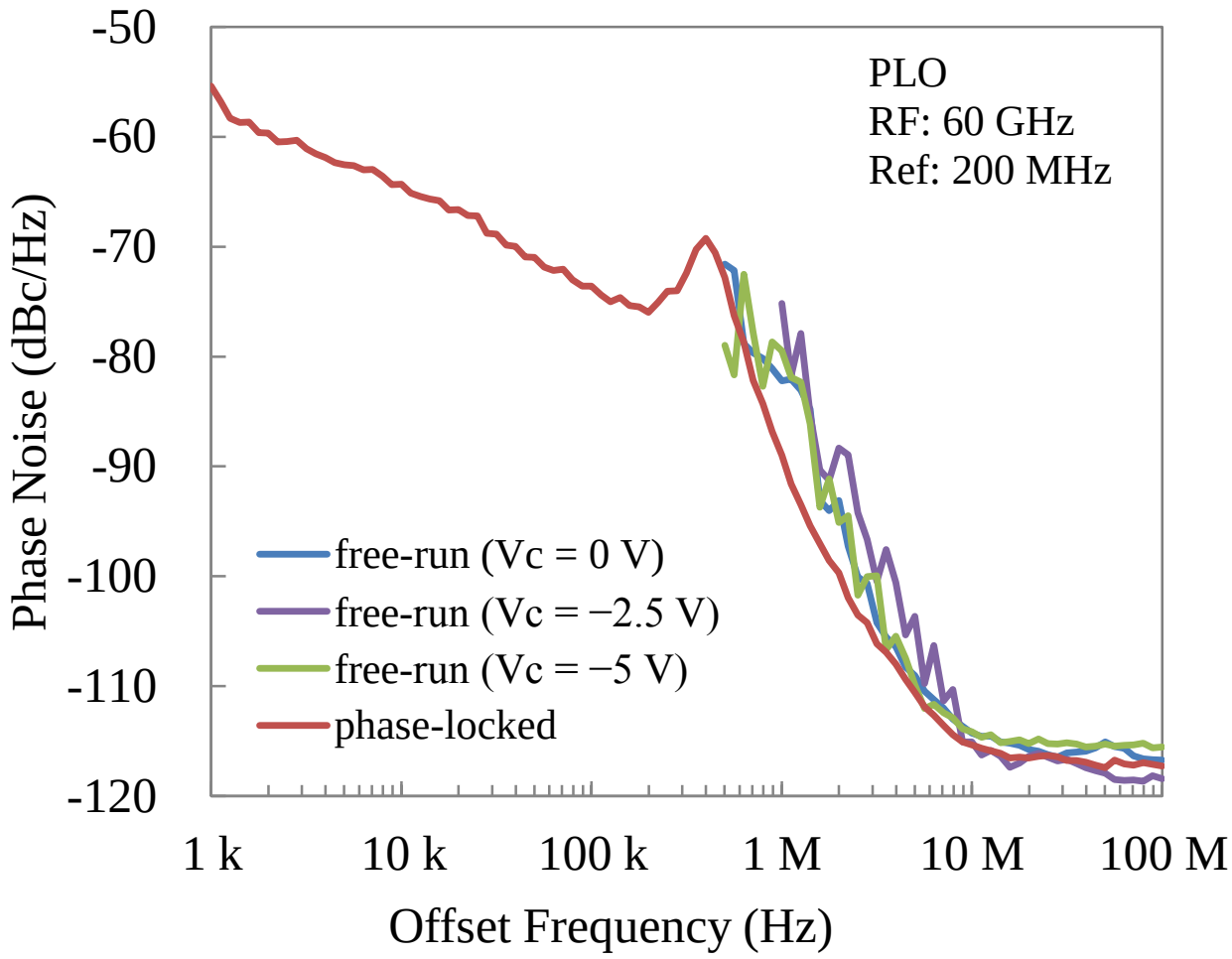


Fig. 2.16 The SSB phase noise for the 60-GHz SPD PLO.

2.5. Summary

This chapter has described a V-band full-monolithic PLO chip set that, to my knowledge, is the most compact one ever developed. The uniplanar structure reduces the circuit size drastically and the use of a GaAs MMIC SPD makes the PLO simple and compact. Consequently, all the circuits can be integrated into as few as three chips, and the chip area is 5.5 mm^2 for the oscillator and 3.0 mm^2 for the SPD. The oscillator stabilized at 56.0–60.0 GHz in a phase-locked condition with a step four times the size of the PLL reference frequency. The SSB phase noise in the loop bandwidth is suppressed to the noise floor of the PLL, and it is as low as −64 dBc/Hz at 10-kHz offset and −90 dBc/Hz at 1-MHz offset from 60.0 GHz in spite of the low Q full-monolithic circuitry. This approach will surely contribute to the development of small and simple V-band MMIC PLO's for communication equipment.

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Chapter 3

High-Speed Series-Connected Voltage-Balancing Pulse Driver with Direct-Coupled Current Switches

3. High-Speed Series-Connected Voltage-Balancing Pulse Driver with Direct-Coupled Current Switches

3.1. Introduction

The optical modulator driver is a key component for high-speed fiber-optic communications systems. Though faster transistors are required for faster operation of the driver, the breakdown voltage generally decreases as the transistor speed increases. This makes it difficult to develop a high-speed large-voltage-swing driver circuit.

One solution to this problem is to employ a distributed-amplifier configuration combined with rather-low-speed high-breakdown-voltage transistors [3.1][3.2]. Nevertheless, the transistors used in these ICs cannot be applied to digital circuits at the same bit rate as the ICs operate because of the shortage of device speed. In addition, the group delay characteristics of the distributed amplifier degrade at frequencies considerably lower than the cutoff frequency of the amplifier.

InP HEMTs show excellent high-speed and high-frequency performance. However, they generally have lower breakdown voltages than GaAs HEMTs because of their larger impact ionization and gate leakage [3.3], which originates from the properties of the InAlAs/InGaAs/InP material system. Therefore, high-voltage pulse drivers, such as optical modulator drivers, which need transistors with high breakdown voltages, largely employ GaAs HEMTs [3.4].

To integrate digital functional blocks with high-output-voltage drivers, circuit technology that enables large output voltage swing using high-speed transistors with rather low breakdown voltage is required. For this purpose, series-connected voltage-balancing circuit configuration is promising. This configuration has been developed and been used in power electronics for low-speed high-voltage switching [3.5]–[3.7] where the difficulty is in keeping voltage balance during switching. If the voltage balance breaks, one transistor may exceed the breakdown voltage and burn out. Therefore, many practical high-voltage switches employ protection devices, such as Zener diodes, in parallel to the transistors [3.7]; however, these devices decrease the operating speed and, accordingly, cannot be adopted in high-speed pulse driver circuits. In addition, delay between sequential switching of series-connected transistors might distort the eye-pattern when the circuit is applied to signal transmission. Thus, this type of circuit has not been applied to high-speed signal transmission circuits, such as optical modulator drivers until recently. In 1997, the first trial for a modulator driver was done by T. K. Woodward, et al. [3.8], which used series connected CMOS. However, the maximum operating speed remained only 155 Mb/s due to the limitations of the

circuit configuration and device speed. By employing current switch configuration, such as source-coupled FET logic (SCFL), high-speed operation will be possible because the transistor can operate in the saturation region of the transistor I-V curves. The operating speed can be boosted by using high-speed transistors with rather low breakdown voltages.

This chapter proposes a series-connected voltage-balancing pulse driver in novel direct-coupled current switch architecture. The architecture solves the problem of voltage balancing between series-connected FETs during switching. By employing high-speed SCFL circuits and high-speed but rather low-breakdown-voltage transistors, high-speed operation of the driver is achieved. A data transmission experiment demonstrates that this type of driver can transmit signals with sufficiently good waveform qualities.

3.2. Basic Concept of the Driver

3.2.1. Circuit Design

Fig. 3.1 illustrates the principle of voltage-balancing operation of series-connected FETs when two FETs are used for the balancing. The key point is that during the operation the gate-source voltages (Vgs) of the two FETs (lower: T1, upper: T2) are applied equally so as to keep the drain-source voltage (Vds) of the two FETs equal. This operation divides the voltage applied between the source of T1 and the drain of T2 equally. Consequently, the output voltage (Vout) swing is the sum of the change of the Vds's of T1 and T2, and it can be twice as much as the swing that can be output by a single FET.

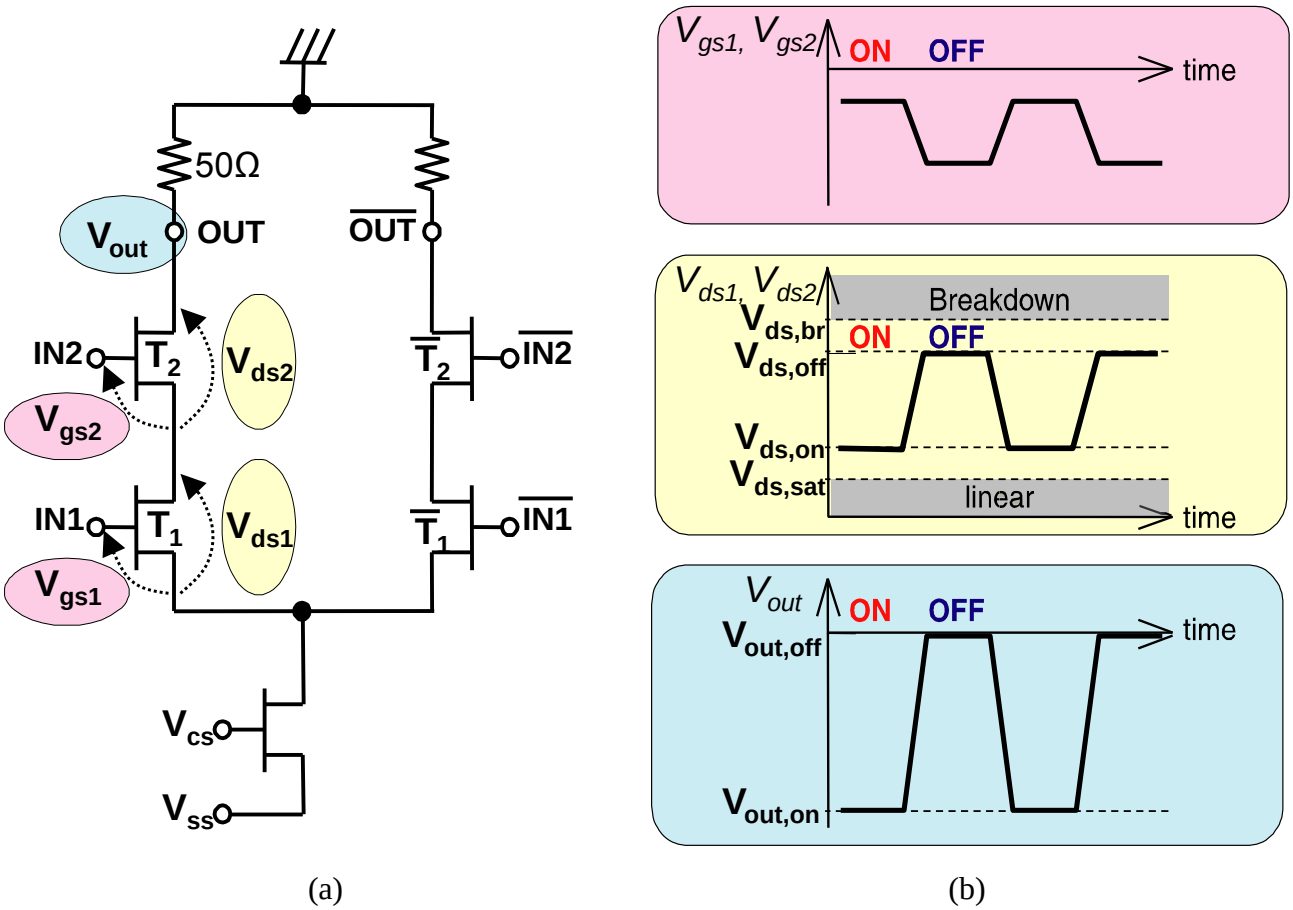
Though the concept of the series-connected voltage-balancing operation is simple, the difficulty lies in the control sequence of series-connected FETs. That is, if the control timing between gate and source of the upper FET differs during switching, the FET tends to suffer exceeding the breakdown voltage and will be damaged.

Fig. 3.2 shows how the waveform of Vgs, Vds and the gate-drain voltage (Vgd) of the upper series-connected transistor, T2, (Vgs2, Vds2, and Vgd2) differs when the control timing of the gate and source voltage of the same FET (Vg2 and Vs2) changes. The ON / OFF signals input to the IN1 and IN2 terminals are inverted in this configuration to avoid exceeding the breakdown voltages for Vgs2, Vds2, and Vgd2. Fig. 3.2(a) and (b) are the waveforms when Vin1 and Vin2 (i.e. Vg2) are controlled simultaneously. Large undershoots in Vgs2, Vds2 and Vgd2 are observed at the

beginning of the transition at a time of around 100 ps, which corresponds from ON to OFF for T2, and at the beginning of the transition at a time of around 200 ps, which corresponds from OFF to ON for T2. The undershoot in Vgd2 is especially serious because the voltage breakdown of an FET is limited in Vgd for normal compound semiconductor FETs. These undershoots are caused by the control timing difference between Vg2 and Vs2. Due to the delay from the input of T1 (IN1) to the source of T2, the control timing of Vg2 is approximately 6-ps earlier than that of Vs2 when Vin1 and Vin2 are controlled simultaneously.

This problem can be solved by adding an appropriate delay to the control timing at IN2 so as to synchronize the control timing of Vg2 and Vs2. By adding 6-ps delay to the control timing at IN2, the undershoots for the transition at a time of around 100 ps and 200 ps are much reduced as shown in Fig. 3.2(c) and (d). The undershoot in Vds2 still remains to some extent because it is inherent for this type of sequential switching from T1 to T2. This inherent undershoot originates from the delay between the switching of T1 and T2, which breaks the voltage balance in Vds during the time that T1 becomes ON and T2 is still OFF. Nevertheless, this is not serious because the maximum output voltage swing is limited not by Vds but Vgd. Fortunately, the remained undershoot in Vgd2 is slight after the control-timing synchronization between Vg2 and Vd2.

To include the control-timing synchronization in the design of series-connected voltage-balancing driver circuit, we employed novel direct-coupled current switch architecture as shown in Fig. 3.3. In this architecture, the gate of T1 is controlled directly from the input signal at terminal IN, while the gate of T2 is controlled through the current switch without a source-follower circuit. In this architecture, the delay from terminal IN to the gate of T2 (path A) is designed to be approximately the same as the delay from terminal IN to the source of T2 (path B) to suppress undershoots in Vgd for T2. In this configuration, it is necessary to invert the ON / OFF signals input to T1 and T2. The direct-coupled current switch configuration also provides the phase inversion of signals input to IN2, as well as adding 6-ps delay to the control timing at IN2.



(a) (b)

Fig. 3.1 Principle of voltage-balancing operation by series-connected FETs (T1, T2) when two FETs are used for the balancing.

(a) Series-connected current switch.

(b) Illustrated time transition of gate-source voltage (Vgs1, Vgs2), drain-source voltage (Vds1, Vds2), and output voltage (Vout) when the left side of the current switch is on and off.

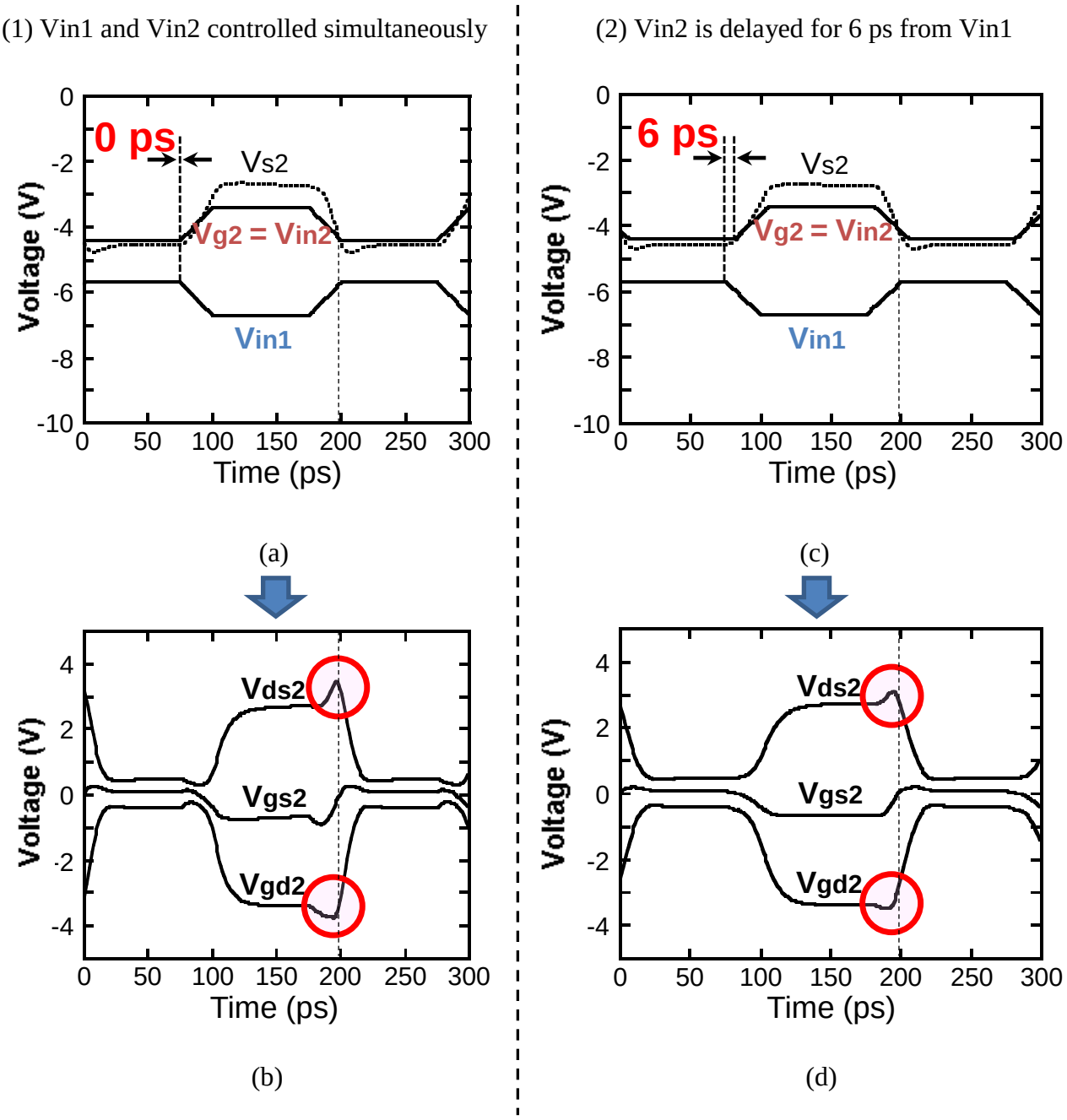


Fig. 3.2. Impact of control timing between IN1 and IN2 on Vgs2, Vds2 and Vgd2 of upper series-connected FET (T2) by circuit simulation.

(a) Waveforms at IN1 (Vin1), IN2 (Vin2), and source voltage (Vs2) of T2 when Vin1 and Vin2 are controlled simultaneously.

(b) Waveforms of Vgs2, Vds2 and Vgd2 of T2 when the input voltages are as shown in (a).

(c) Vin1, Vin2 and Vs2 of T2 when Vin2 is delayed for 6 ps from Vin1.

(d) Vgs2, Vds2 and Vgd2 of T2 when the input voltages are as shown in (c).

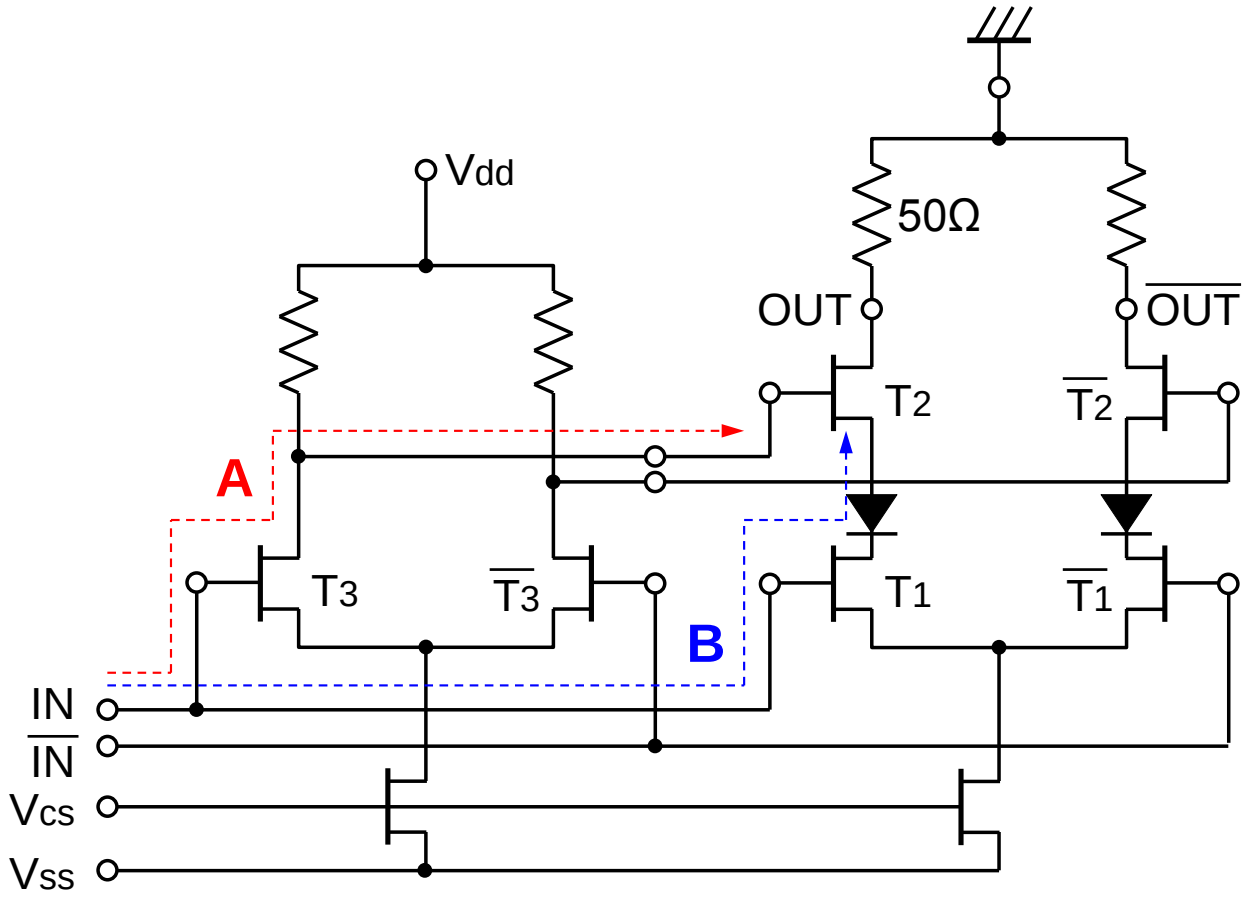


Fig. 3.3 Circuit diagram of series-connected voltage-balancing pulse driver in novel direct-coupled current switch architecture. The delays though path A and path B are approximately the same.

3.2.2. Experimental Evaluation

The driver circuit shown in Fig. 3.3 was fabricated using 0.1-μm InP HEMT process [3.9] with a gm of 1.05 S/mm, a Vt of −0.53 V, and an fT of 165 GHz. In the design, the Vds at the off-state is set to 2.7 V so as not to exceed a tentative Vgd limit for the design of −4 V. By setting Vds at the on-state to 0.55 V, the output voltage swing of single FET is 2.15 Vpp. Because the voltage swing decrease due to the level shift diode is 0.3 Vpp, the designed output voltage swing of the driver is 4 Vpp. A gate width of 200 μm is used for the FETs.

Fig. 3.4 shows a photomicrograph of the fabricated driver chip. The chip size is 1.12 × 1.84 mm^2. Power supply voltages for Vss, Vcs and Vdd are respectively −7.3 V, −7.3 V and −3.4 V and the power dissipation is 0.96 W.

The signal transmission was experimented on wafer using an Anritsu MP1761B 12.5-Gb/s pulse pattern generator and a Hewlett-Packard HP54750A digitizing oscilloscope mainframe with an HP54752A 50-GHz module. Figure 5 shows the output waveforms for the input of 10-Gb/s pseudorandom bit stream (PN $2^{31}-1$). A clear eye opening with the output voltage swing of 3.7 Vpp was observed. Considering that the measured output voltage swing value does not include the voltage drop caused by the insertion loss of the coaxial cable and an on-wafer RF probe used in the test, the measured data agreed well with the designed output voltage swing of 4 Vpp. This result proves that the degradation in transmission quality by nonlinear limiting operation due to sequential switching of series-connected FETs is sufficiently allowable for 10-Gb/s non-return-to-zero (NRZ) data.

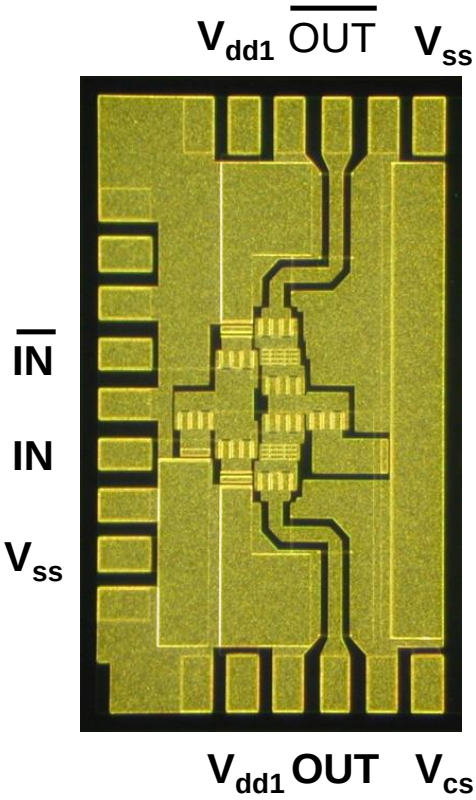


Fig. 3.4 Photomicrograph of fabricated driver IC. Chip size is 1.12 × 1.84 mm^2.

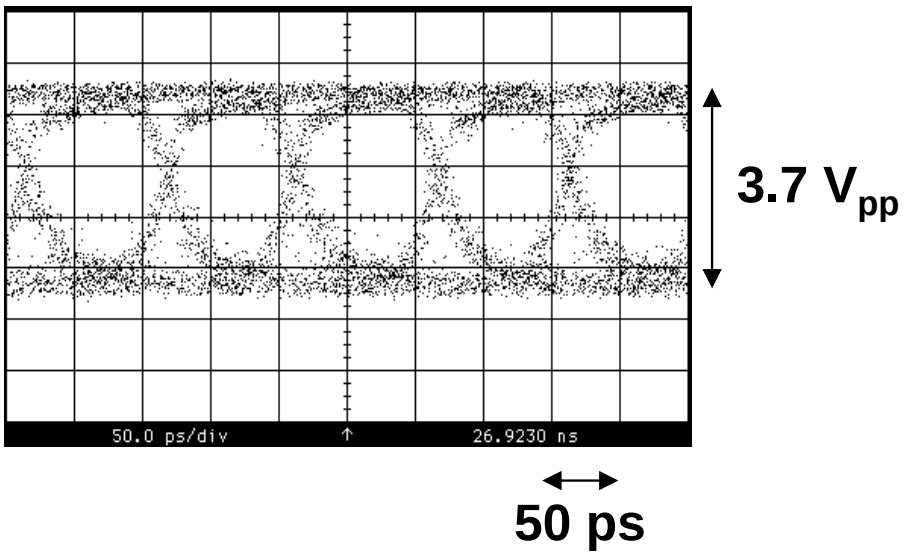


Fig. 3.5 10-Gb/s output waveform of the driver. The input signal is 10-Gbit PN $2^{31}-1$ pseudorandom bit stream.

3.3. Challenges in Achieving Higher Operation Speeds by Employing High-Driving-Capability Input Buffer

3.3.1. Considerations for Faster Operation of the Driver

A series-connected voltage-balancing circuit configuration can output a voltage proportional to the number of series-connected transistors by sharing the voltage among the transistors. The architecture suppresses undershooting in gate-drain voltage (Vgd) during switching and prevents the FETs exceeding gate-drain breakdown voltage. Therefore, the architecture is promising for applying high-speed but low-break-down voltage transistors to high-amplitude pulse drivers. In fact, 10-Gb/s operation with the high amplitude of 3.7 Vpp was exhibited using of this type of driver core with novel direct-coupled current switch architecture using InP HEMTs (see Fig. 3.5). However, the CR time constant between the signal source impedance and the input capacitance of the driver core limits the bandwidth and prevents the intrinsic high-speed operation of the driver core.

In this section, faster operation of the driver core enhanced by a high-driving-capability input buffer is proposed. The buffer decreases the CR time constant at the input of the driver core and enables the driver core to show its intrinsic high-speed operation. The fabricated driver shows a wider bandwidth, faster rise and fall times, and clearer eye opening at 10 Gb/s.

3.3.2. Circuit Design

Fig. 3.6 shows the whole block diagram of the driver proposed in this section. The driver core, which is the same configuration as in Fig. 3.3, employs the direct-coupled current switch architecture to synchronize the gate and source control timing of the upper FET of the series-connected FETs. This synchronization suppresses under-shooting in Vgd during switching and, accordingly, prevents the FETs exceeding gate-drain breakdown voltage and ensures high-speed operation. The gate width of the FETs in the output stage was designed to be 200 μm to output a voltage swing of 4 Vpp with 50 Ω load. The gate width of the current switch in the driving stage is also 200 μm to synchronize the control timing between the gate and source of upper FETs. Consequently, the total gate width at the input of the driver core is 400 μm.

For lumped-element high-speed large-swing pulse driver cores, the CR time constant (the product of the signal source impedance (Zs) and the input capacitance (Ci) of the driver core) is

often so large that it limits the bandwidth of the driver. Fig. 3.7 shows how the time constant affects the bandwidth. The Zs affects the limiting −3 dB cutoff frequency ($f_{-3\,dB}$) of the driver core when 1-Vpp differential sinusoidal signal sources are input. The $f_{-3\,dB}$ increases from 8 to 26 GHz by reducing Zs from 50 to 4 Ω. The driver core in the previous section was directly driven by 50 Ω signal source, so faster operation is expected by reducing Zs to 4 Ω.

For this reason, an input buffer with high driving capability is added to reduce Zs against the driver core to reduce the ZsCi product. Fig. 3.8 shows the input buffer, which comprises three-stage SCFL current switches with source-follower level shifters. To reduce Zs to approximately 4 Ω, the gate width of the output stage of the input buffer is set to 260 μm. As a result, the number of fan-out between the input buffer and the driver core becomes approximately 1.6. The same number of fan-out is applied between the stages of the input buffer. Accordingly, the gate widths of the first and second stage of the input buffer are 100 and 160 μm, respectively. Since the ZsCi product for the input of the first stage is sufficiently small, the number of stages is decided to three.

The driver, whose block diagram is shown in Fig. 3.6, comprises the voltage-balancing driver core and the input buffer. The three-stage input buffer also increases the gain of the driver. The designed DC gain of the driver is over 20 dB, which is high enough for it to be driven directly by digital ICs. The input is AC-coupled using external capacitors, internally biased and terminated with 50 Ω. The outputs are DC-coupled open-drains to external 50 Ω loads. The power supply voltages for Vss, Vcs, Vdd1 and Vdd2 are −6.6, −6.6, −2.7 and −3.4 V, respectively. The power dissipation is 3.5 W.

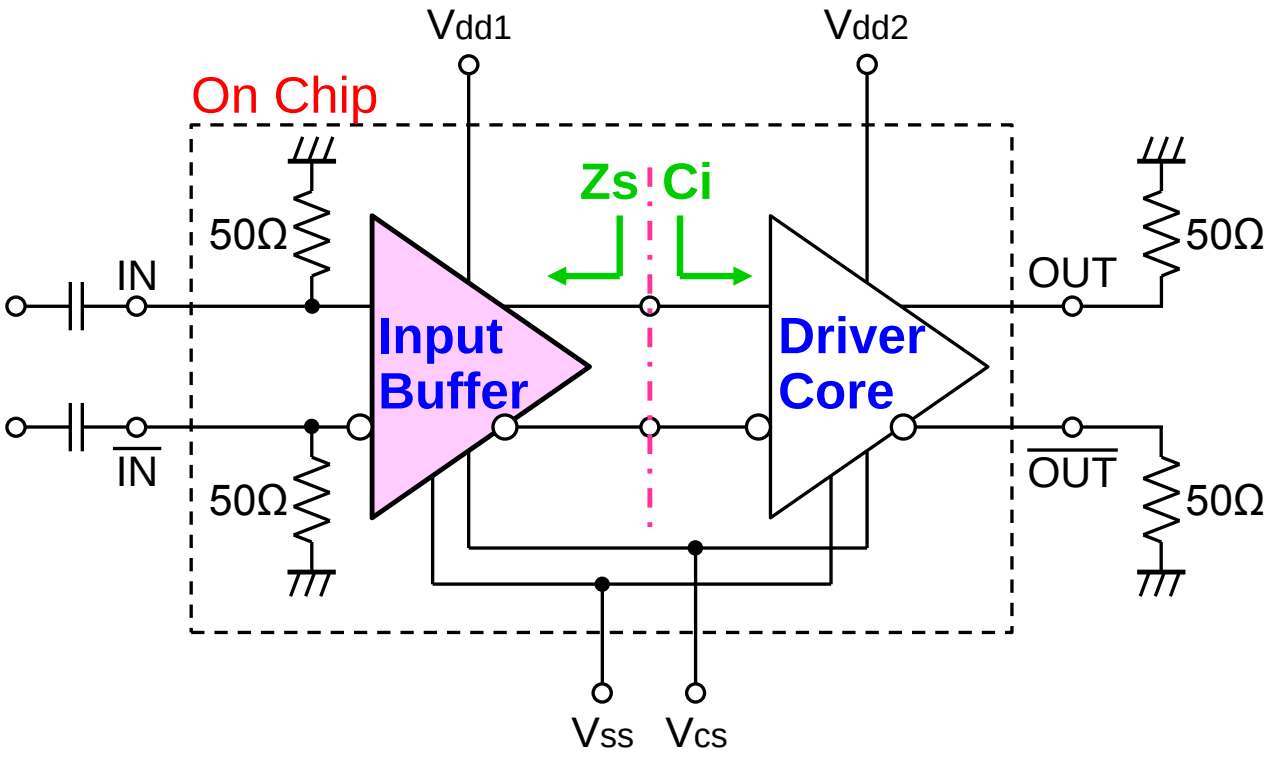


Fig. 3.6 Block diagram of the series-connected voltage-balancing pulse driver with the three-stage input buffer.

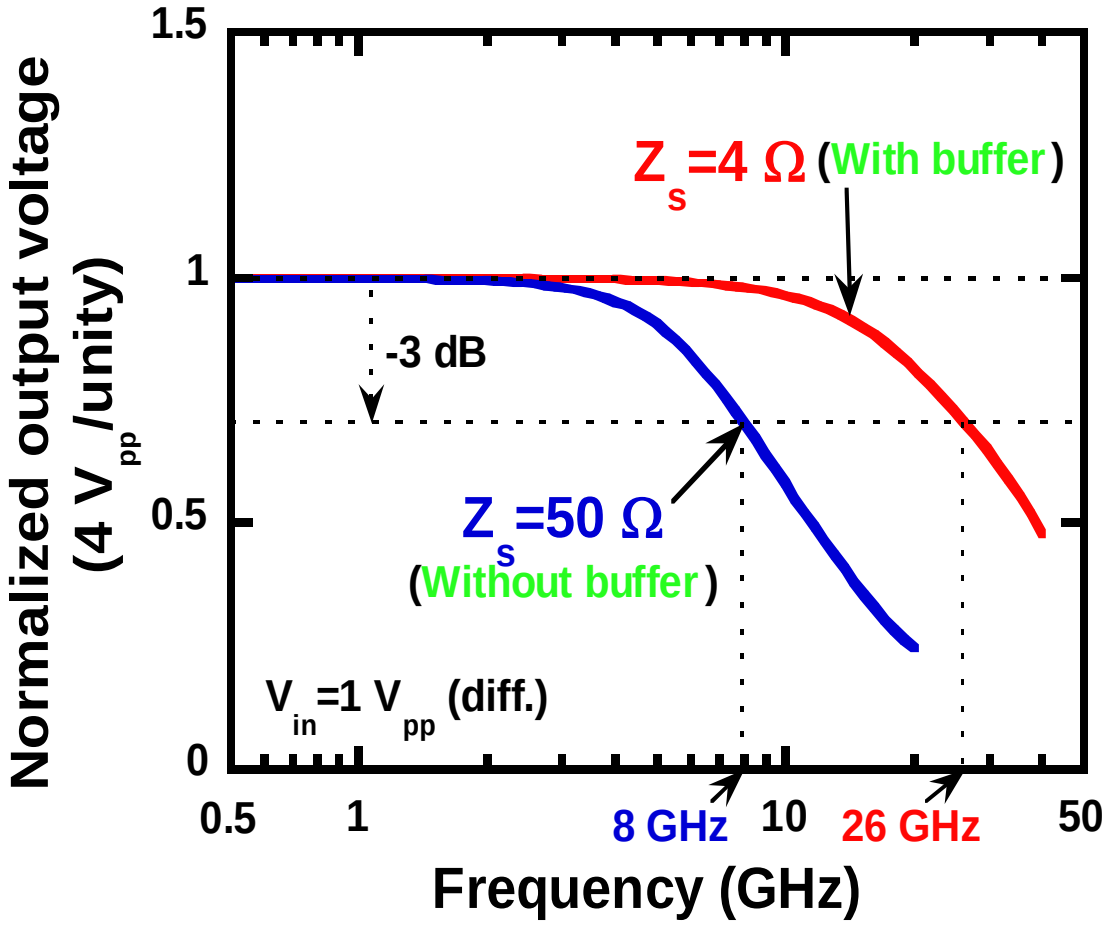


Fig. 3.7 Simulated frequency dependence of normalized output voltage of driver core with signal source impedance (Zs) as a parameter. The vertical unit is 4 0 Vpp for simulated data.

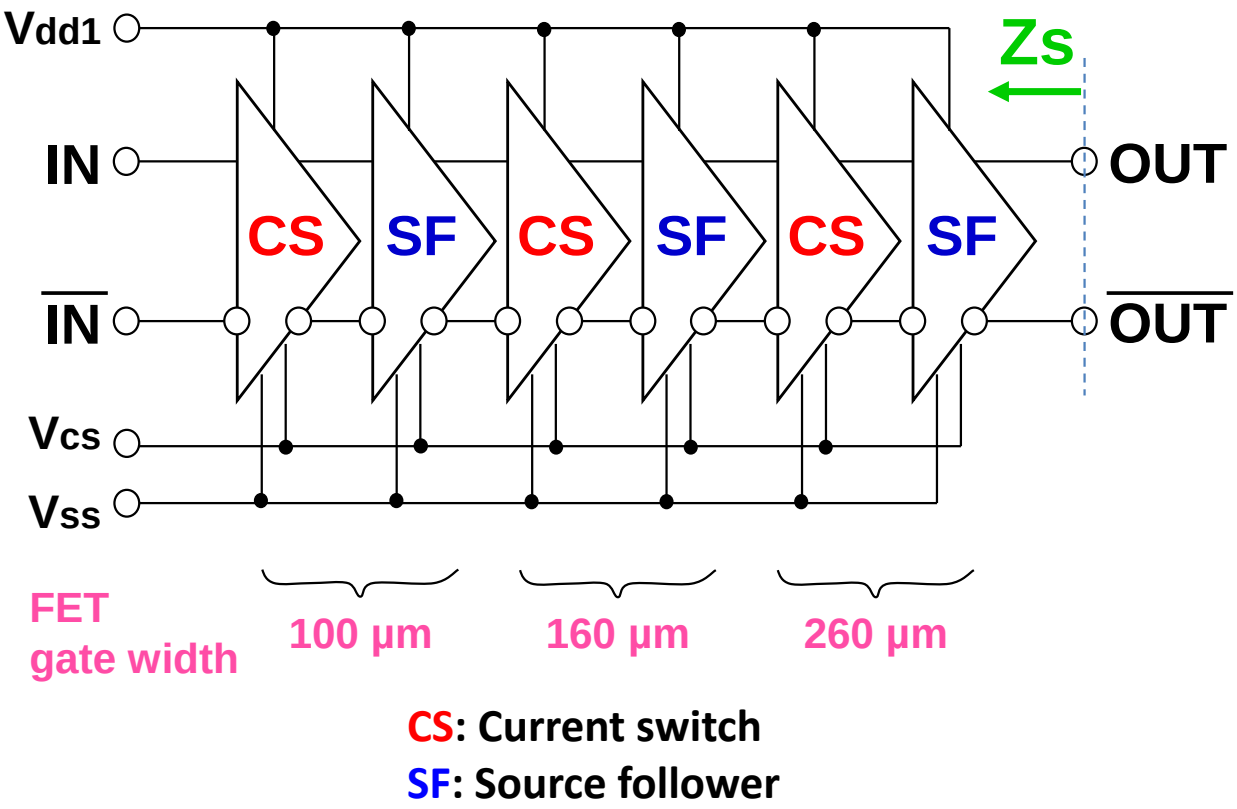


Fig. 3.8 Circuit diagram of the input buffer. Zs represents the output impedance.

3.3.3. Experimental Evaluation

The driver was fabricated using a 0.1-μm InP HEMT process [3.9] developed for high-speed digital and analog ICs. The transconductance (gm), threshold voltage, and current-gain cutoff frequency (fT) are 1.15 S/mm, −0.49 V, and 183 GHz, respectively. Fig. 3.9 shows a photomicrograph of the fabricated chip. The chip size is 1.84×1.84 mm^2.

The limiting bandwidth was measured on-wafer using 65 GHz Cascade Microtech multi-contact air-coplanar probes for IC probing. The 1-Vpp single-ended sinusoidal signal was input from an Agilent 83640A synthesized sweeper to the driver and the output voltages were measured using a Tektronix CSA8000B oscilloscope mainframe with a Tektronix 80E06 70+-GHz sampling module. Solid lines in Fig. 3.10 show measured frequency dependence of the output voltage swing of the driver core for the approximately 1-Vpp differential inputs that were outputs from the input buffer for 1-Vpp single-ended input. The measured f_{-3dB}'s for a Zs of 50 and 4 Ω are 11 and 30 GHz, respectively, which agree well with the simulated values.

Output waveforms for 10-Gb/s $2^{31}-1$ pseudorandom bit stream (PRBS) data input were measured using the same setup as that for the bandwidth measurement except that an Anritsu MP 1778A pulse pattern generator was used as a signal source. Fig. 3.11(a) and (b) show output waveforms for the PRBS data input for the driver core with and without the input buffer, respectively. The output voltage swings for these configurations are both 3.6–3.7 Vpp. This is 1.6–1.7 times as high as the 2.2 Vpp for the conventional configuration that uses one transistor for output, which is limited by the maximum drain-source voltage of 2.7 V and knee voltage of 0.5 V. The rise and fall times (20−80%) are remarkably shortened, from 33 to 16 ps and from 37 to 16 ps, respectively, by employing the input buffer. This demonstrates the high-speed operation capability of the series-connected voltage-balancing pulse driver.

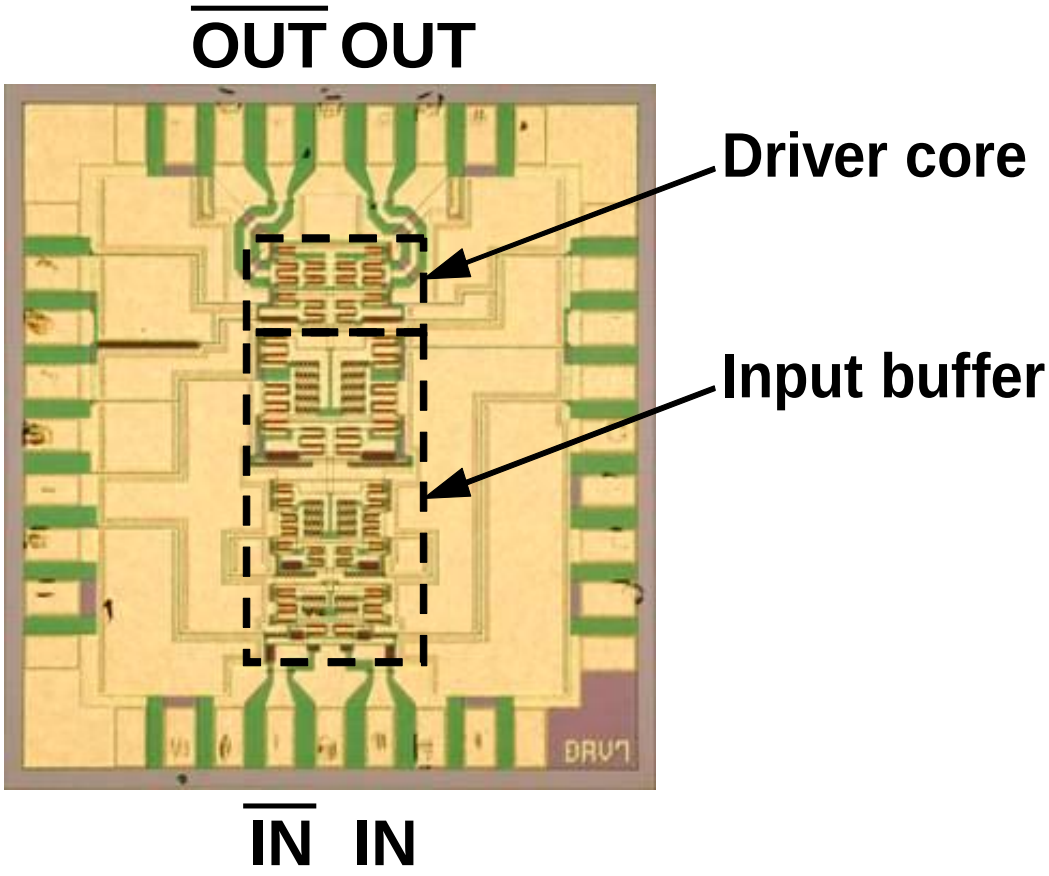


Fig. 3.9 Photomicrograph of fabricated pulse driver. Chip size is 1.84 × 1.84 mm^2.

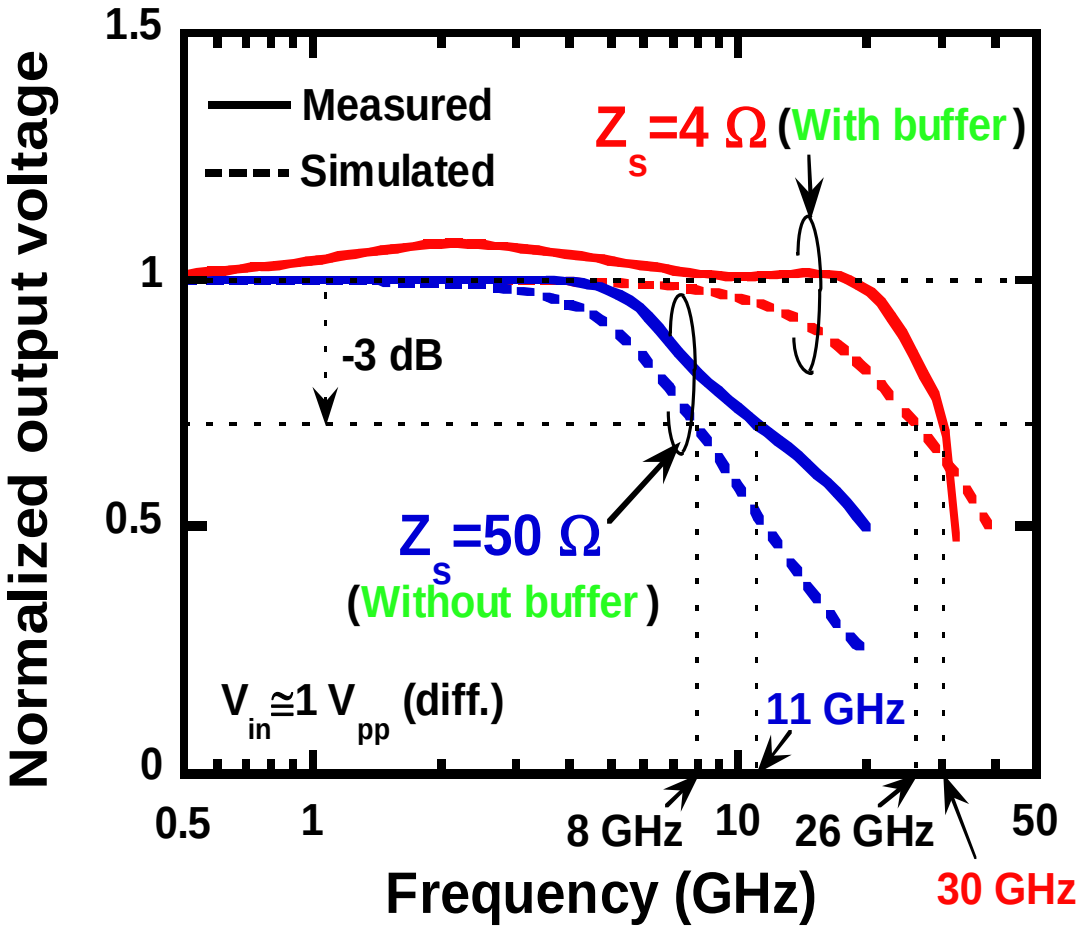
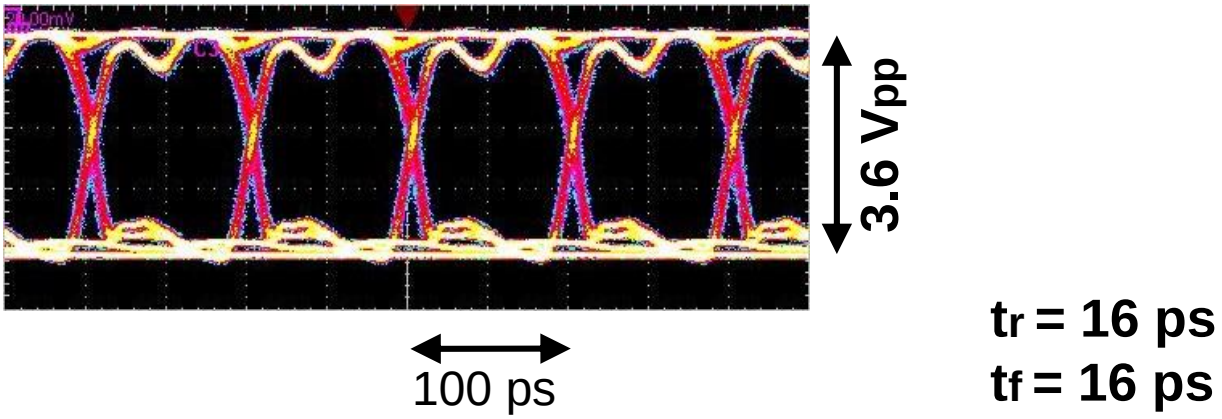
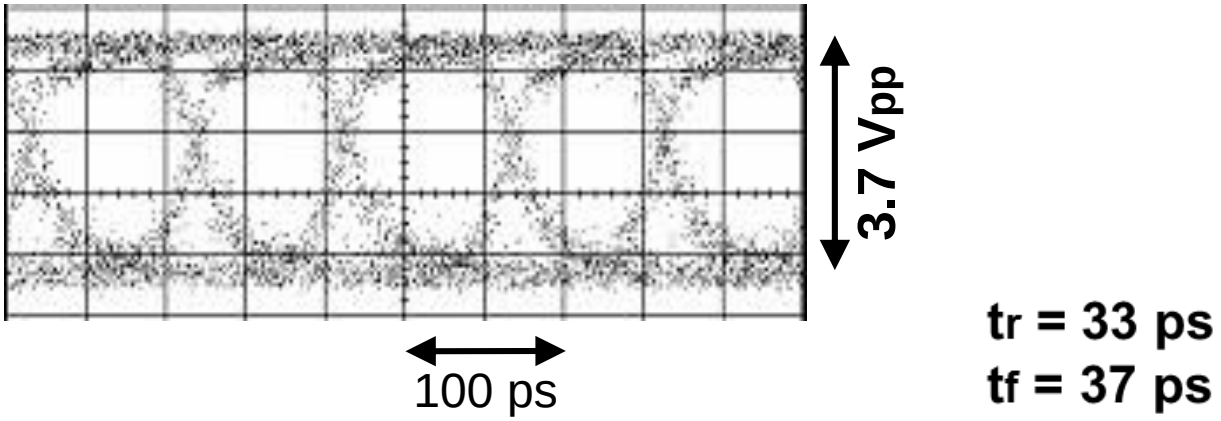


Fig. 3.10 Frequency dependence of normalized output voltage of driver core with signal source impedance (Zs) as a parameter. The unit is 3.6–3.7 and 4 0 Vpp for measured and simulated data, respectively.



(a)



(b)

Fig. 3.11 Output waveform for 10 Gb/s $2^{31}-1$ PRBS data input.
(a) with the input buffer.
(b) without the input buffer (the same waveform as Fig. 3.5).

3.4. Summary

A novel architecture using direct-coupled current switches for a series-connected voltage-balancing pulse driver is described. This architecture provides the phase inversion of signals input to the upper series-connected FET in order to avoid exceeding the breakdown voltages. This architecture also synchronizes the gate and source control timing of the upper FET of series-connected FETs. This synchronization suppresses the undershoot in Vgd that occurs when the gates of both series-connected FETs are controlled simultaneously and consequently prevents exceeding the gate-drain breakdown voltage. This results in a substantial increase of output voltage swing by decreasing the surplus margin for Vgd. An on-wafer measurement experiment showed that the fabricated driver IC has 3.7-Vpp single output and 7.4-Vpp differential output with clear eye opening for 10-Gb/s PN $2^{31}-1$ data patterns. The driver also demonstrated that the series-connected voltage-balancing circuit in the direct-coupled current switch architecture can be applied to the optical modulator driver for high-speed fiber-optic communications systems.

In addition to that, higher-speed operation was demonstrated for a series-connected voltage-balancing pulse driver with direct-coupled current switch architecture using 0.1-μm InP HEMTs and a high-driving-capability input buffer. With the input buffer, the −3-dB limiting bandwidth of the driver increased from 11 to 30 GHz, and rise and fall times decreased from 33 to 16 ps and from 37 to 16 ps, respectively. These decreases in rise and fall times much improve the waveform of the 10-Gb/s eye opening with an output voltage swing of 3.6 Vpp. The driver demonstrates a sufficient speed margin for 10 Gb/s and shows potential for higher-bit-rate operation.

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Chapter 4

Small and Low-Cost Dual-Rate Optical Triplexer for OLT Transceivers in 10G/1G Co-existing 10G-EPON Systems

4. Small and Low-Cost Dual-Rate Optical Triplexer for OLT Transceivers in 10G/1G Co-existing 10G-EPON Systems

4.1. Introduction

The explosive growth of internet traffic has been accelerating the use of fiber-to-the-home (FTTH) access systems such as the gigabit Ethernet passive optical network (GE-PON). For providing larger traffic capacity, the 10-gigabit Ethernet passive optical network (10G-EPON) is a promising candidate. In the process of substituting 1G with 10G EPON, 1G and 10G will co-exist on the same existing optical distribution network [4.1], as shown in Fig. 4.1, because GE-PON systems have already been widely deployed. Therefore, optical line terminal (OLT) transceivers in a symmetric 10G-EPON system must have the function of the 1G-transmitter and receiver for GE-PON optical network units (ONUs), in addition to the function of the 10G-transmitter and receiver for 10G-EPON ONUs.

In order to downsize OLT equipment and decrease the number of fiber cords, hence reducing troubles associated with fiber management, a dual-rate optical sub-assembly for the OLT transceivers with these three optical components (10G-transmitter, 1G-transmitter, and 10G/1G-receiver) and wavelength division multiplexing (WDM) filters in one module, what is called an optical triplexer, has been developed [4.2], [4.3]. With the introduction of new 10G-EPON systems in the near future, there is need for smaller and cheaper optical transceivers. Thus, reducing the size and cost of the optical triplexer used in the transceiver has been one of the largest issues.

This chapter proposes a novel small and low-cost optical triplexer for use in 10G-EPON applications. Owing to the use of a light collection system and by reducing optical path length with a low-magnification long-focus lens, the number of lenses has been successfully decreased, and the triplexer has been ultimately miniaturized for installation in 10-gigabit small form factor pluggable (XFP) transceivers, without sacrificing its performance.

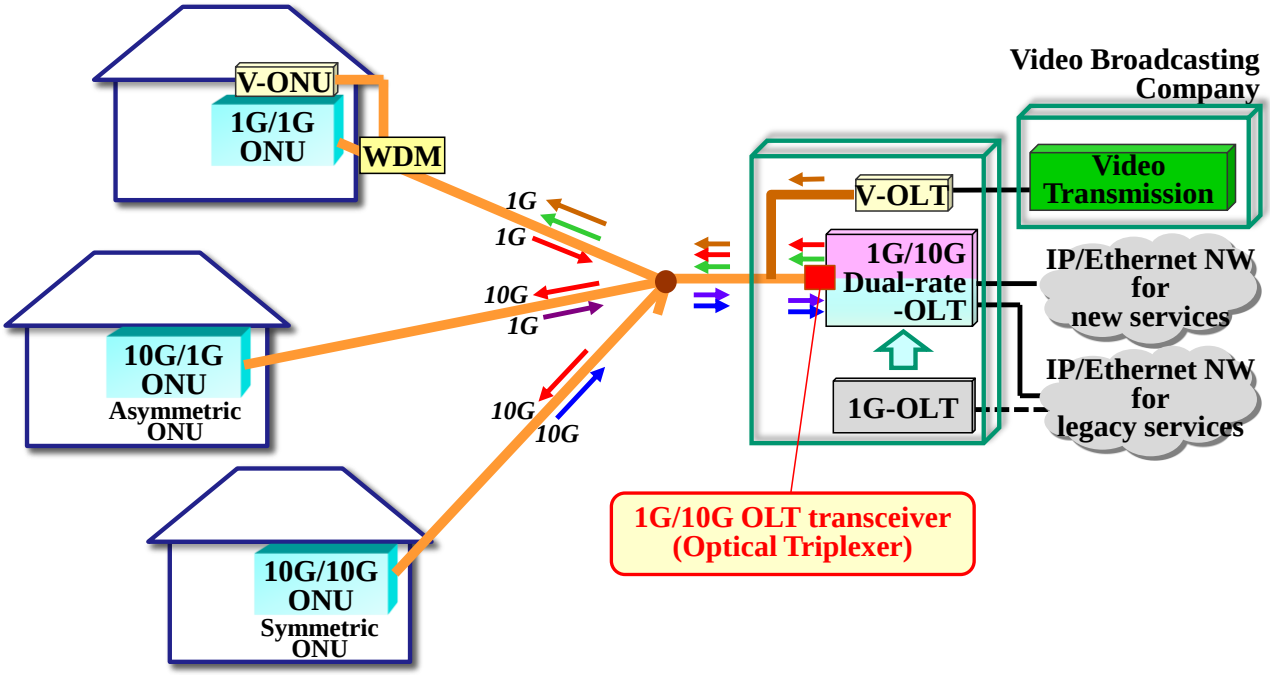


Fig. 4.1 10G-EPON system architecture with 1G/10G co-existing.

4.2. Design of Triplexer

4.2.1. Configuration

Fig. 4.2 and 4.3(a) show a photograph and the configuration of the developed optical triplexer. The total size of the triplexer is 20 × 14 × 7.2 mm^3, which is 57% smaller than a previously reported one [4.3]. The triplexer consists of two laser diode (LD) transmitters, an avalanche photodiode (APD) receiver, an isolator, two WDM filters, an optical bandpass filter (BPF), and a chassis. The two LD's are a 1577-nm electro-absorption modulator integrated distributed feedback laser diode (EADFB-LD) for 10G downstream and a 1490-nm distributed feedback laser diode (DFB-LD) for 1G downstream, respectively.

4.2.2. Design of Optical System

4.2.2.1. Comparison of Optical Systems

Two optical systems can be used to compactly align two LD outputs and one APD input with the same optical fiber, as shown in Fig. 4.3.

One is collimating optics [Fig. 4.3(b)], which uses two collimating lenses to change a diffuse optical beam from a laser or fiber into a collimated beam and has been generally used because of its high coupling efficiency, flexible optical design, and low tracking error.

The other is a light collection system, which is used in this work [Fig. 4.3(a)]. A light collection system, which uses a single coupling lens to focus a diffuse optical beam from a laser or fiber, requires fewer lenses and simplifies the optical alignment process. However, the optical coupling efficiency can be easily degraded with a light collection system. Besides, a light collection system allows little space for passive optical devices such as an isolator, WDM filters, and optical BPFs. The tracking error also tends to be larger than that for collimating optics. For these reasons, a light collection system had never been used in an optical triplexer for OLT transceivers. However, a light collection system is often employed in bidirectional optical sub-assemblies (BOSA's) with a transmitter and receiver [4.6]–[4.8] in ONU transceivers, whose size and cost are the highest priority.

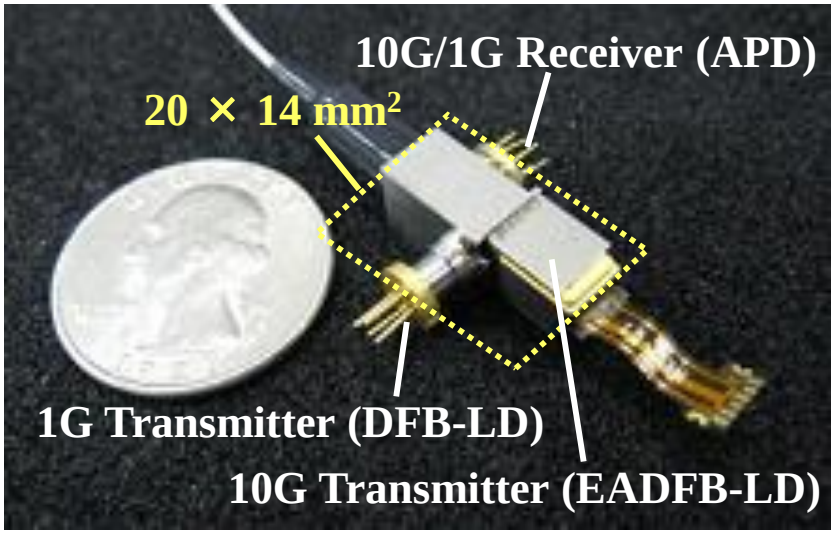
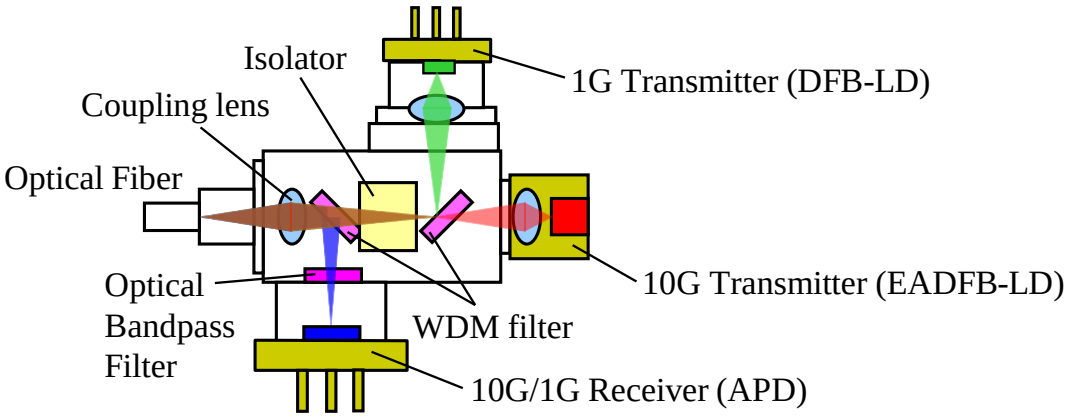
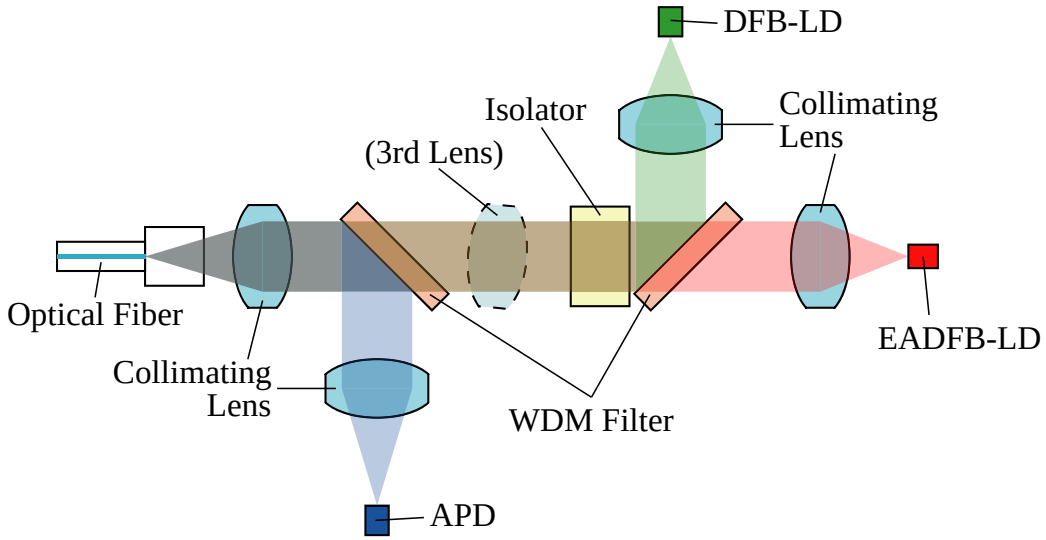


Fig. 4.2 Photograph of the optical triplexer.



(a) This work (light collection system)



(b) Collimating optics (general)

Fig. 4.3 Configuration of our optical triplexer and comparison of optical systems.

4.2.2.2. Design and Feasibility Evaluation of the Light Collection System

In the optical design of the triplexer, the relationship between the tolerance of optical coupling efficiency and the size of the optical system has been considered.

In collimating optics, the tolerance of optical coupling efficiency and the size of the optics are independent of each other, and the minimal size is limited by length of the optical devices.

In a light collection system, on the other hand, magnification, focal length, and working distance determine the tolerance of optical coupling efficiency and the size of the system. There exists an upper limit of the magnification, because the optical coupling efficiency becomes less tolerant as the magnification becomes larger. There also exist lower and upper limits of the focal length: a focal length that is too small reduces the space available for passive optical devices; one that is too large results in enlarging the optical path length. Accordingly, I designed the focal length of the coupling lens and the working distance between each device, so that the image magnifications between the fiber and 10-Gb/s EADFB-LD and between the fiber and 1-Gb/s DFB-LD are 4-power and 3-power, respectively.

Thus, the problems of optical-coupling-efficiency degradation and the lack of space for passive optical devices have been solved by using a coupling lens with low magnification and large focal length for the light collection system.

The optical system has been evaluated through simulations and measurements. Fig. 2.4 shows a tolerance simulation of optical coupling efficiency between the fiber and 10-Gb/s EADFB-LD, which is of primary concern. Owing to the low magnification, less degradation due to misalignments is achieved. The efficiency is more than 50% with a fiber offset within ±100 μm, and the degradation of optical coupling efficiency is kept to the minimum, as small as that for collimating optics [4.2], over the wide range of fiber offset. Fig. 4.5(a) shows the measured optical coupling efficiency between the fiber and 10-Gb/s EADFB-LD and between the fiber and 1-Gb/s DFB-LD. For the fiber and 10-Gb/s EADFB-LD, the optical configuration was the same as for the simulation in Fig. 4.4 except with alignment along the z-axis omitted for miniaturization. The efficiency is 10% less than for our previous device employing collimating optics [4.2], primarily due to the lack of alignment along the z-axis. However, the reduced efficiency is equivalent to a drop in output power of only 0.5 dB. For the fiber and 1-Gb/s DFB-LD, the efficiency is also around 10% less than for our previous device [4.2], because here I used such a 1-Gb/s LD CAN that the image magnifications between the fiber and 1-Gb/s DFB-LD is 2-power, with the aim of

enlarging tolerance of the optical coupling efficiency. However, the 1-Gb/s DFB-LD has a sufficient margin for the output power to comply with the IEEE 802.3ah standard [4.5]. Fig. 4.5(b) shows the measured optical coupling efficiency of the receiver in terms of receiver responsivity. The coupling efficiency is 4% less than that for collimating optics, which is equivalent to a drop of only 0.2 dB in the minimum sensitivity.

On the other hand, the large focal length yields enough space to align passive optical devices. Moreover, as shown in Fig. 4.3(b), collimating optics usually needs an additional third lens for the beam-angle correction to achieve high coupling efficiency for two LD's simultaneously [4.3]. However, there is no need for an additional lens to achieve high coupling efficiency with the light collection system because the beam angles can be varied easily. As a result, compared to the previous work with collimating optics [4.2], the optical path length can be reduced by half and the volume of the chassis by 60%. Two aspherical lenses can be also eliminated, which reduces material costs.

These results show that the light collection system provides size and cost reductions as well as good optical coupling efficiency.

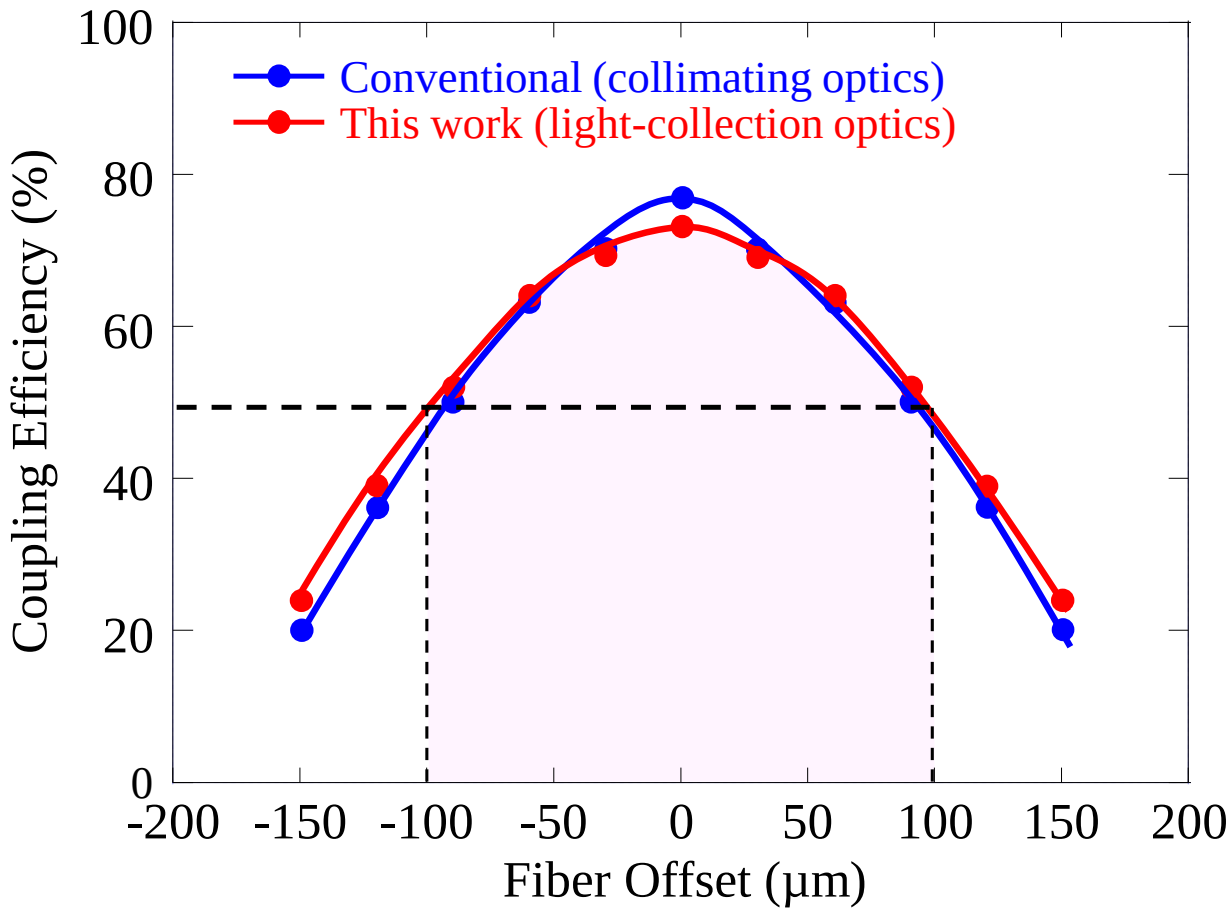
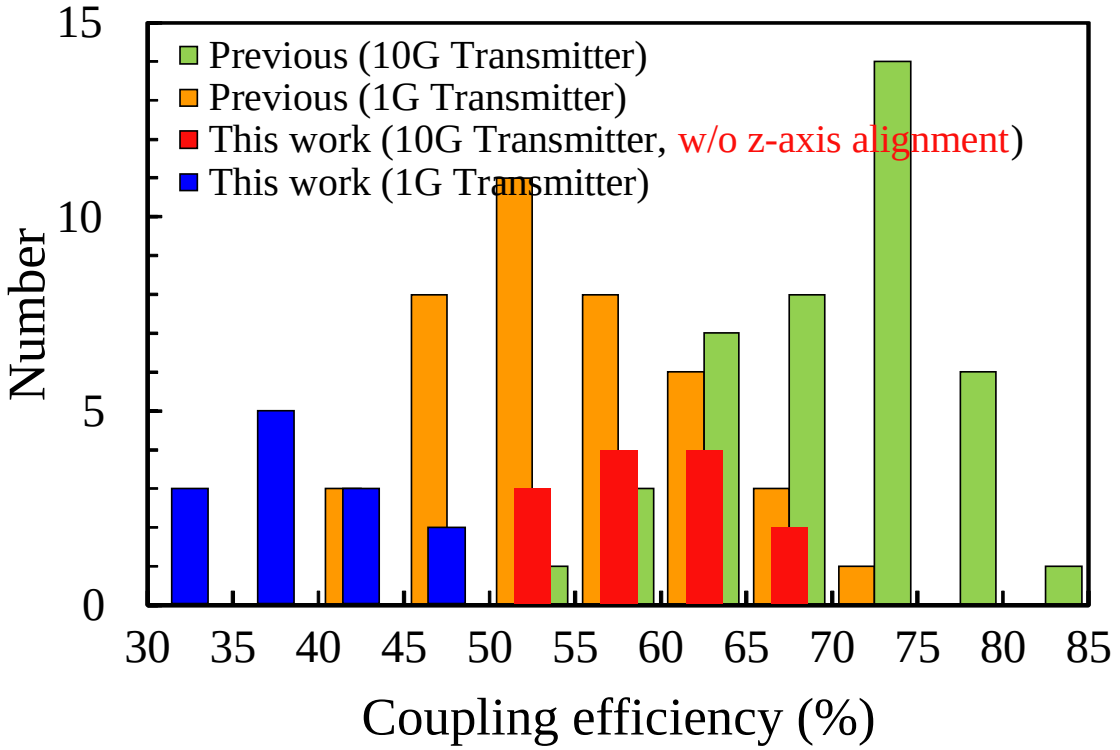
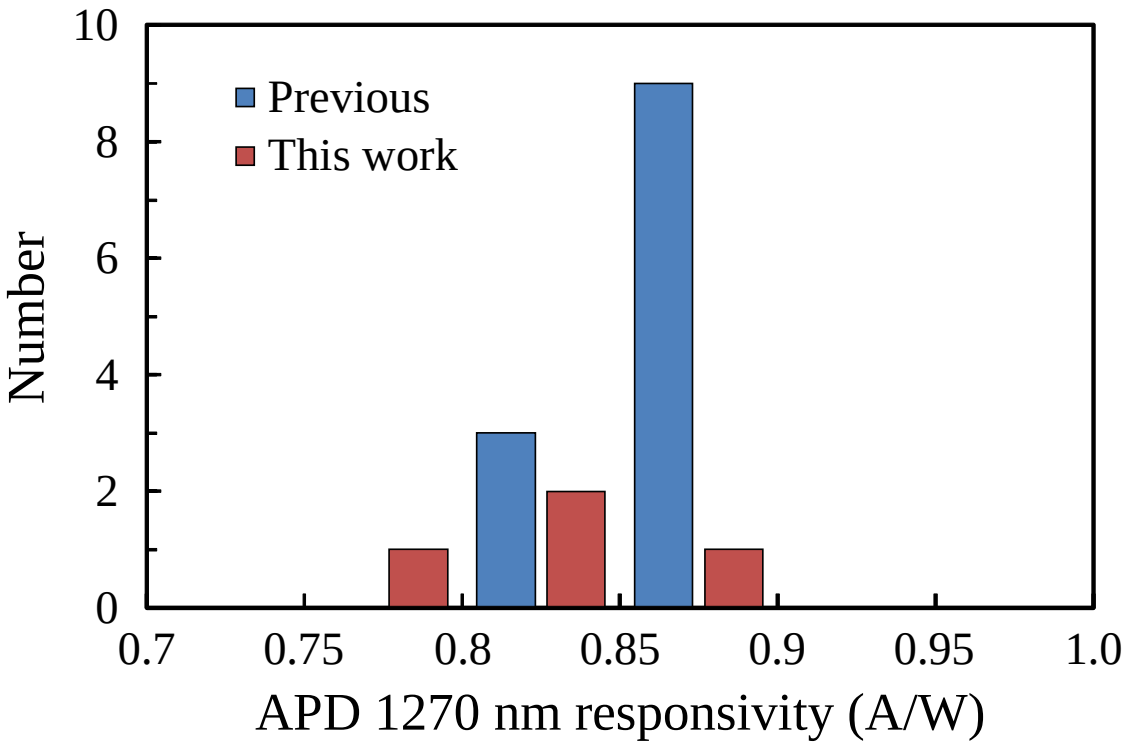


Fig. 4.4 Simulated optical-coupling-efficiency tolerance between the fiber and 10-Gb/s EADFB-LD, with z-axis alignment.



(a) Between the fiber and 10-Gb/s EADFB-LD: between the fiber and 1-Gb/s DFB-LD.



(b) Receiver responsivity.

Fig. 4.5 Measured optical coupling efficiency.

4.2.3. Design of Optical Sub-Assemblies

4.2.3.1. EADFB-LD and DFB-LD Transmitters

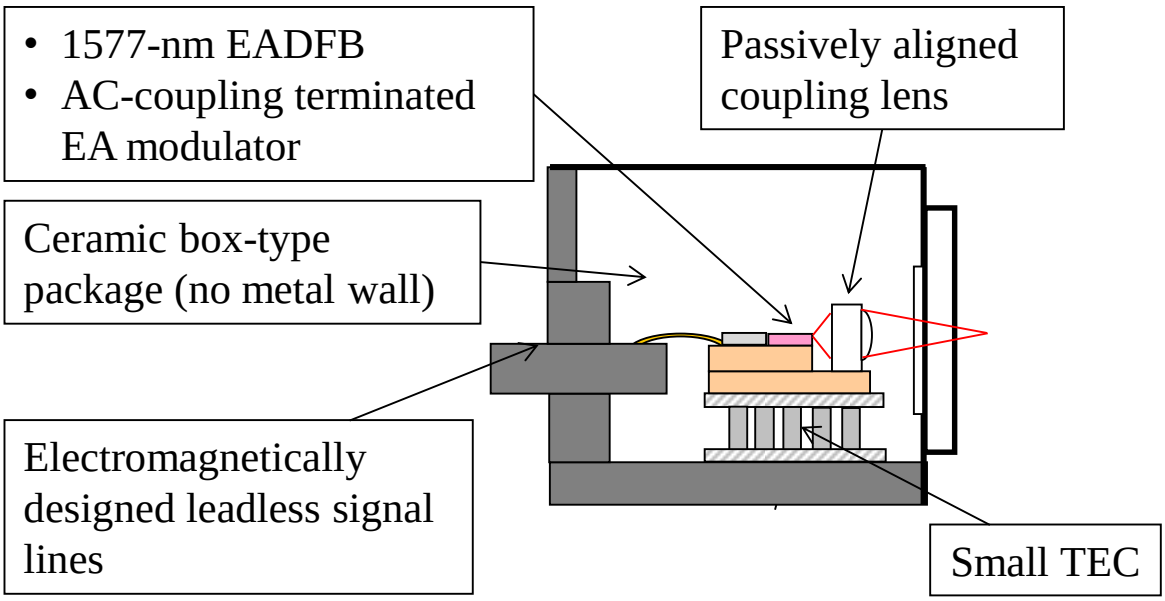
Since the cost of an EADFB-LD transmitter module accounts for a significant part of a triplexer's total cost, a low-cost ceramic box-type package with no metal wall has been developed. Fig. 4.6 shows the configuration of the 10G EADFB-LD transmitter module. The signal lines fed through the ceramic wall were designed on the basis of an electro-magnetic analysis to avoid degradation of electrical transmission performance. AC-coupling termination of the EA modulator reduces power consumption, thus making it possible to downsize the thermoelectric cooler of the transmitter. Consequently, I have succeeded in reducing the material cost and also reducing the size of the transmitter by 20% in depth without degrading its performance.

A commercially available TO-56 (Transistor-Outline type 5.6 mmϕ) DFB-LD-CAN was used for the 1490-nm transmitter.

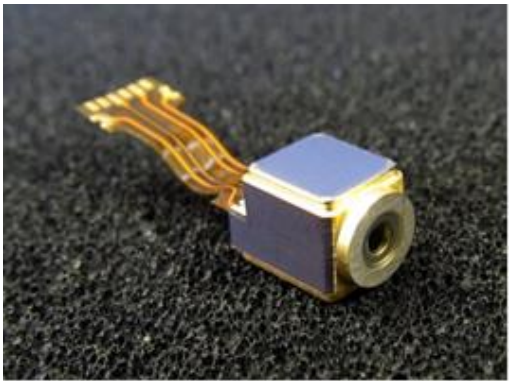
4.2.3.2. APD Receiver

A TO-CAN (Transistor Outline CAN) APD receiver module was also developed, in which a 10-Gb/s InP/InGaAs APD [4.4] operates in an electron-injection mode. For this triplexer, a SiGe BiCMOS 10G/1G dual-rate burst-mode transimpedance amplifier (TIA) was designed. Fig. 4.7 shows the configuration of the APD receiver and the 10G/1G dual-rate burst-mode TIA. The TIA operates with no reset signals. This is advantageous for decreasing the number of CAN-package pins necessary for an APD receiver, which contributes to reducing material and assembly costs. Whether the TIA bandwidth is 10G or 1G depends on the feedback resistor switched according to the input rate-select signals. Feedback-type automatic gain control (AGC) provides a wide dynamic range. The time constant value of the AGC feedback was set so that the AGC can respond to the input burst signals.

A customized thin cap with a flat window reduces the TO-CAN receiver height to less than 3 mm.



(a)



(b)

Fig. 4.6 (a) Configuration. (b) Photograph of 10G EADFB-LD transmitter module.

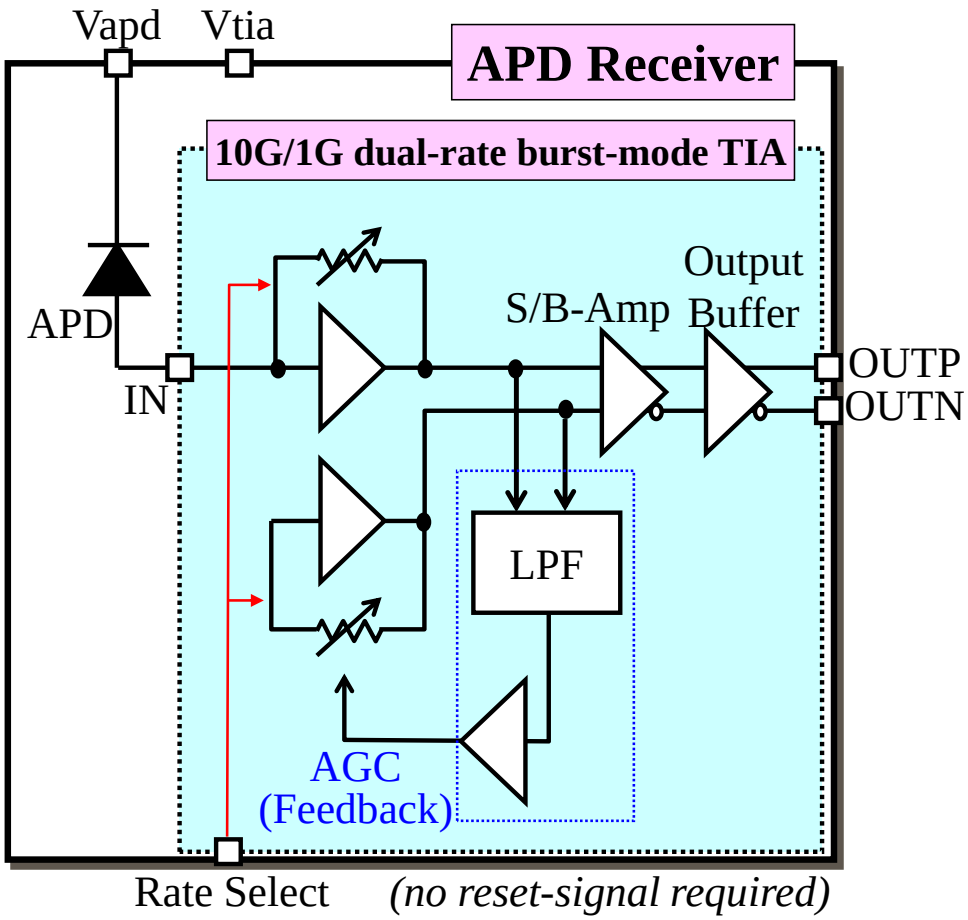


Fig. 4.7 Configuration of TO-CAN burst APD receiver module and 10G/1G dual-rate burst-mode TIA.

4.3. Performance of Triplexer

4.3.1. 10.3-Gb/s and 1.25-Gb/s Transmitters

The transmitter in the optical triplexer is evaluated under conditions close to those in the actual system.

Fig. 4.8 shows measured 10.3-Gb/s transmit optical waveforms of PRBS $2^{31}-1$ with a fourth-order Bessel-Thomson filter at case temperatures (Tc) from −5 to 75˚C. The 10.3-Gb/s EADFB-LD operating temperature is maintained at 45˚C. Fig. 4.9 also shows measured 1.25-Gb/s transmit optical waveforms of PRBS $2^{7}-1$ with a fourth-order Bessel-Thomson filter at case temperatures from −5 to 75˚C. For both transmitters, clear eye openings are observed over the wide temperature range with the mask margin of 35% (10.3 Gb/s) and 45% (1.25 Gb/s). The optical output power, extinction ratio, tracking error, and the dispersion penalty after 25-km transmission are +3 dBm, 9.6 dB, less than 1 dB, and 0.5 dB for 10.3 Gb/s transmitter and +5.2 dBm, 15.8 dB, less than 1dB, and less than 0.1 dB for 1.25 Gb/s transmitter, respectively. This performance complies fully with IEEE 802.3av PR30 (10.3 Gb/s) and IEEE 802.3ah PX20 (1.25 Gb/s) standards [4.1][4.5].

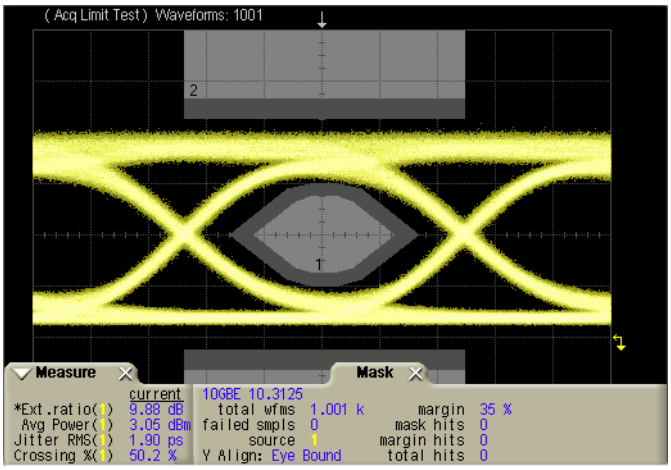
4.3.2. 10.3-Gb/s / 1.25-Gb/s Receiver

The receiver is also evaluated under conditions close to those the actual system, where two optical signals are alternately input to the receiver with different powers and only one ONU at a time is allowed to transmit data in an actual PON system. Receiver instantaneous response to the burst input signals is evaluated, as shown in Fig. 4.10. The first and second input burst signals have optical powers of –6 and −28 dBm, respectively, and have a data rate of 10.3 Gb/s PRBS $2^{31}-1$ with the guard time of 10 ns and a preamble of 800 ns, as shown in Fig. 4.10(b). Received electrical waveforms measured at the output of an external limiting amplifier following the receiver are shown in Fig. 4.10(a). Clear eye opening is observed for a very weak optical burst signal of −28 dBm instantaneously, and a high-speed response to the burst input signal of less than 800 ns as a preamble time is obtained.

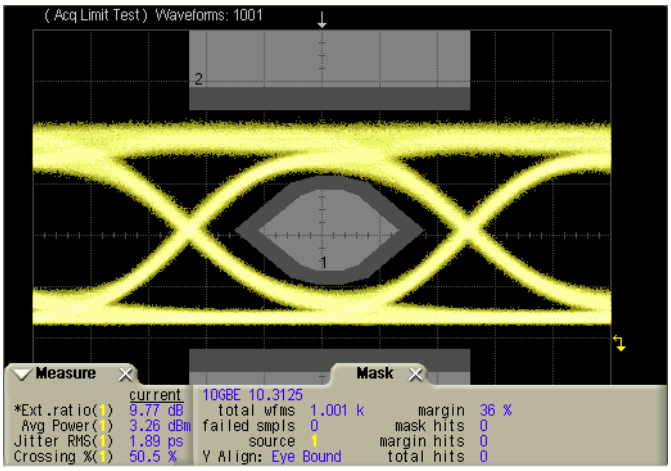
Receiver BER performance measured at case temperatures from −5 to 75˚C is shown in Fig. 4.11. The input optical format is also shown in Fig. 4.11(a). In the 10.3-Gb/s receiver, the minimum sensitivity, defined at BER=10^{-3}, of less than −28 dBm and overload of more than −6 dBm are

achieved over the whole temperature range. These results were obtained under full-duplex operation (the 10.3-Gb/s and 1.25-Gb/s transmitters were on) with ±5% power-supply fluctuation, 15 dB of optical return loss, polarization scrambling, and an out-of-band light for optical maintenance. In the 1.25-Gb/s receiver, the minimum sensitivity, defined at BER=10^{-12}, is less than −33.7 dBm and the overload is more than −6 dBm under the same conditions. This performance also complies fully with IEEE 802.3av PR30 and PRX30 standards [4.1].

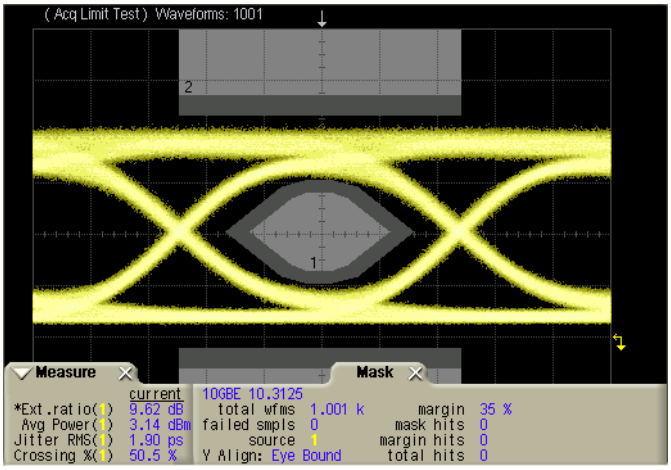
Table 4.1 summarizes all of the measurement results, which show that the optical triplexer using our light collection system performs well enough to meet FTTH requirements.



(a) Tc = −5˚C

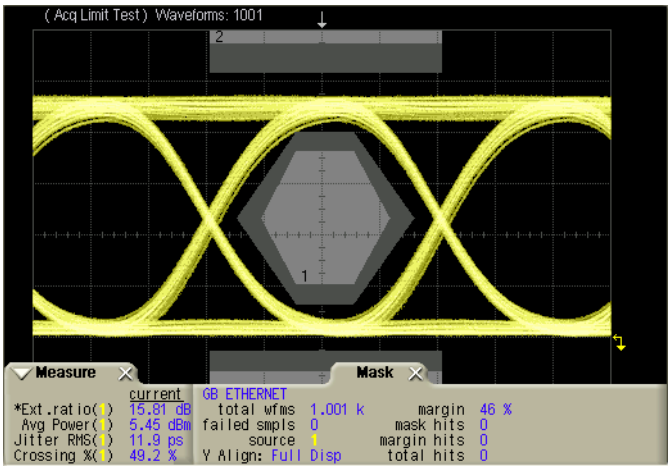


(b) Tc = 25˚C

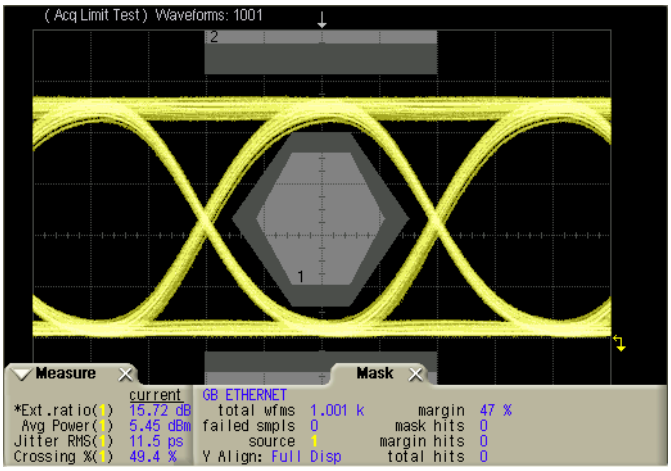


(c) Tc = 75˚C

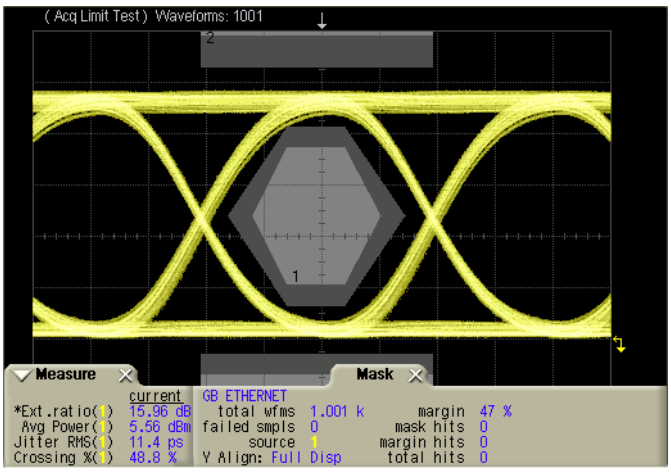
Fig. 4.8 Optical waveforms of 10.3-Gb/s transmitter in the triplexer.



(a) Tc = −5˚C

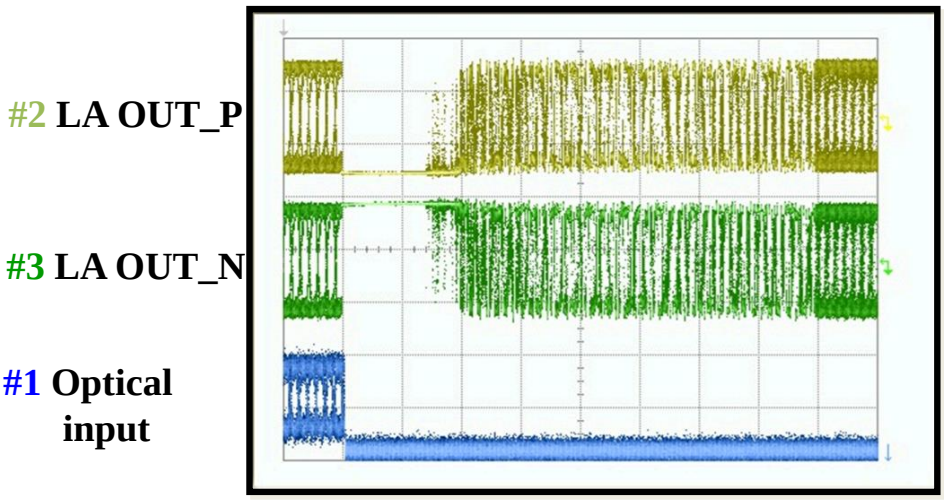


(b) Tc = 25˚C



(c) Tc = 75˚C

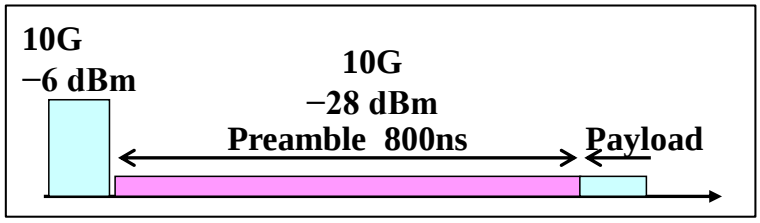
Fig. 4.9 Optical waveforms of 1.25-Gb/s transmitter in the triplexer.



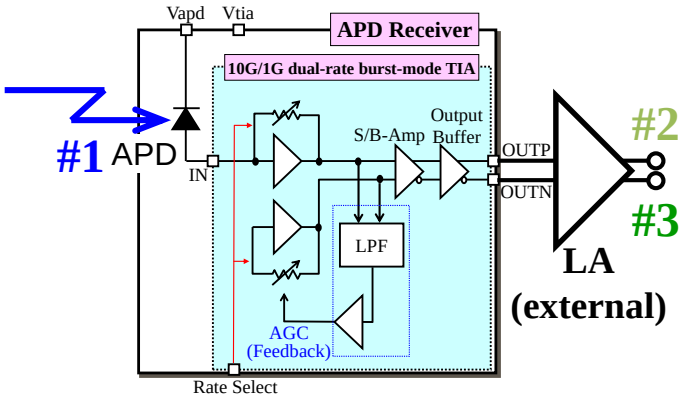
(a) Waveforms of the burst 10.3-Gb/s receiver in the optical triplexer.

#1: Burst-mode optical waveform input to the receiver.

#2, #3: Electrical positive and negative waveforms output from an external limiting amplifier (LA) following the receiver (see Fig (c)).

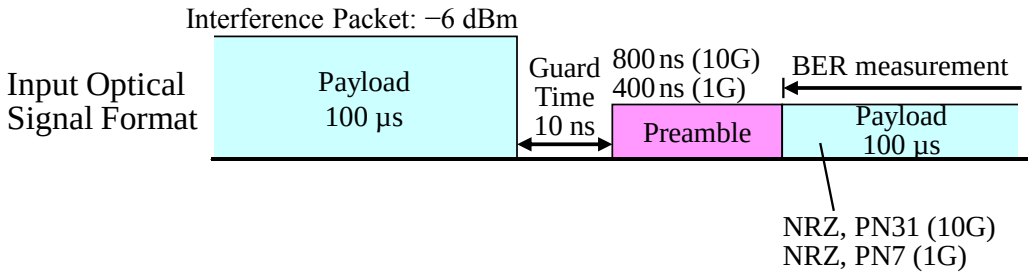


(b) Input optical format.

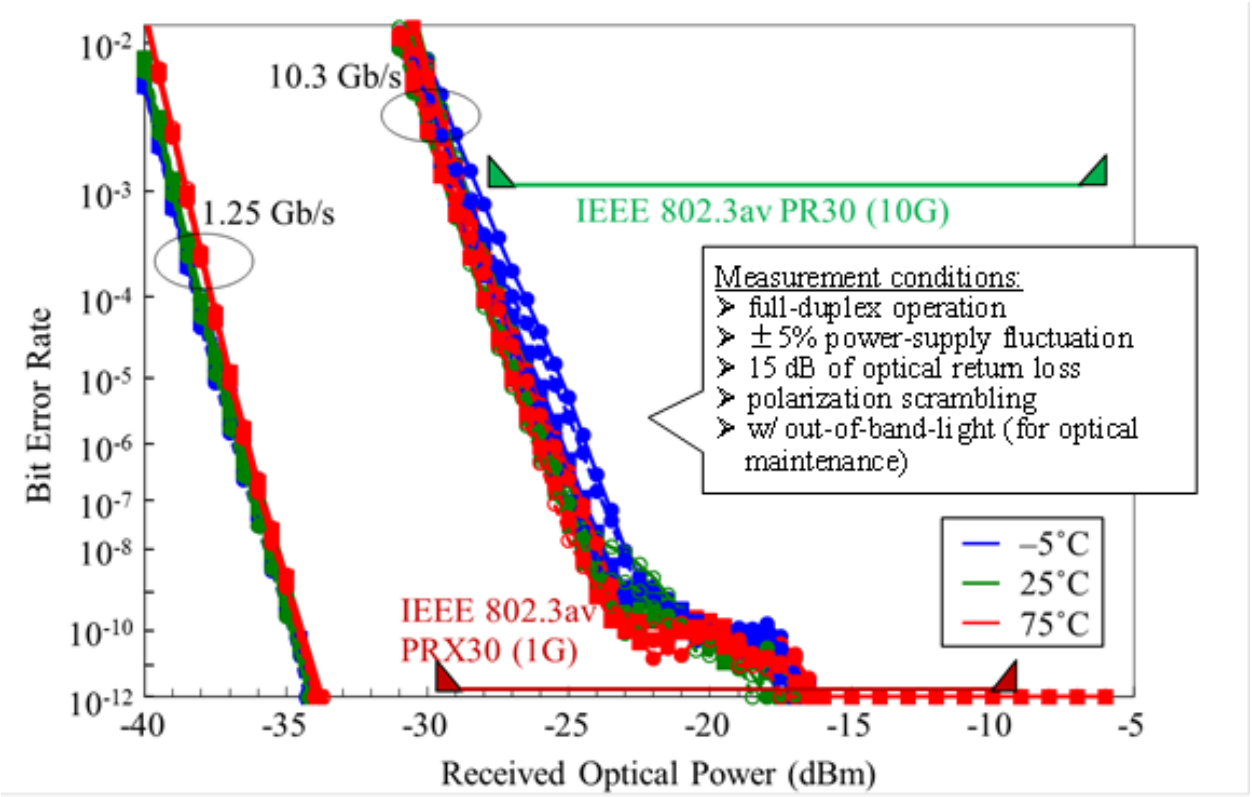


(c) Configuration of the burst APD receiver and an external limiting amplifier (LA), with observation points of waveforms shown in Fig (a).

Fig. 4.10 Response waveforms of the burst APD receiver in the triplexer.



(a) Input optical format.



(b) BER measurement results.

Fig. 4.11 BER performance of the burst 10.3-Gb/s/1.25-Gb/s receiver in the triplexer.

Table 4.1 Measured characteristics

(a) 10.3-Gb/s transmitter

Parameter	10.3 Gb/s			
Case temperature (˚C)	802.3av PR30 spec.	−5	25	75
Output power (dBm)	+2–+5	+3.0	+3.2	+3.1
Tracking error (dB)	–	−0.2		
Extinction ratio (dB)	> 9 (6*)	9.9	9.8	9.6
$RIN_{15}OMA$ (dB/Hz)	< −128	−143	−144	−145
Mask margin (%)	–	33	34	33
Dispersion penalty (dB)	< 1.5	0.5	0.5	0.5

* Higher output power is required for extinction ratio = 6 dB.

(b) 1.25-Gb/s transmitter

Parameter	1.25 Gb/s			
Case temperature (˚C)	802.3ah PX20 spec.	−5	25	75
Output power (dBm)	+2–+7	5.1	5.2	5.2
Tracking error (dB)	–	−0.1		
Extinction ratio (dB)	> 6	15.8	15.8	16.0
$RIN_{15}OMA$ (dB/Hz)	< −115	−145	−145	−145
Mask margin (%)	–	45	47	46
Dispersion penalty (dB)	< 2.3	−0.3	−0.2	−0.4

(c) 10.3-Gb/s / 1.25-Gb/s receiver

Parameter	10.3 Gb/s			
Case temperature (˚C)	802.3av PR30 spec.	−5	25	75
Minimum sensitivity (dBm)	−28 [a]	−28.6	−28.7	−28.8
Overload (dBm)	> −6 [a]	> −6	> −6	> −6
Parameter	1.25 Gb/s			
Case temperature (˚C)	802.3av PRX30 spec.	−5	25	75
Minimum sensitivity (dBm)	−29.78 [b]	−34.0	−34.0	−33.8
Overload (dBm)	> −9.38 [b]	> −6	> −6	> −6

[a] BER = 10^{-3}, [b] BER = 10^{-12}.

4.4. Summary

A small and low-cost optical triplexer module was developed for 10G-EPON applications. Reducing optical path length by means of a light collection system with a low-magnification long-focus coupling lens makes the triplexer as small as 20 × 14 × 7.2 mm^3, without degrading optical coupling efficiency. A low-material-cost design of the EADFB-LD transmitter and eliminating lenses yields cost reduction. The 10G/1G dual-rate burst-mode TIA with feedback AGC provides superior receiver sensitivity. As a result, excellent performance has been achieved that complies with the IEEE 802.3av PR30, 802.3av PRX30, and 802.3ah PX20 standards.

To the best of my knowledge, this is the smallest dual-rate optical triplexer for symmetric 10G-EPON OLT transceivers.

References for Chapter 4

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Chapter 5

Conclusions

5. Conclusions

This dissertation presented research results regarding technologies to attain or improve transmitting and receiving devices in next-generation advanced high-speed access network equipment.

The explosive growth of data traffic due to the spread of the Internet has been accelerating the demand for larger data transmission capacity in access network systems, as well as in backbone network systems. Wired and wireless access network systems co-exist according to their applications. For the access network equipment, not only data transmission speed but also size and cost are important factors to be considered.

In wireless access, increasing the carrier frequency to the millimeter-wave region is one of the key technologies for higher data transmission speeds. On the other hand, in wired access, especially optical access, faster optical modulation is required for increasing data transmission capacity. Besides, since the optical access networks are widely used today, optical access systems of different speeds have to co-exist on the same existing optical distribution network.

However, conventional device technologies have three main problems that must be addressed to achieve advanced transmitting and receiving devices in high-speed access network equipment.

1. The size and cost of millimeter-wave circuits for high-speed wireless access network equipment, especially millimeter-wave local oscillators, could not be sufficiently reduced by using a conventional oscillation stabilizing technique.
2. For optical modulator drivers used in fiber-optic communication equipment, it is difficult to achieve high-speed and large-output-amplitude performance due to the incompatibility between device speed and breakdown voltage of the transistors.
3. There is need for small and cost-effective optical modules consisting of three optical components in one package for dual-rate optical access systems, such as the co-existence of GE-PON and 10G-EPON in one fiber-link.

In this dissertation, to solve these problems, the following three technologies were established.

(1) An MMIC V-band phase-locked oscillator using a GaAs MMIC sampling phase detector.

(2) A high-speed series-connected voltage-balancing pulse driver with direct-coupled current switches.

(3) A small and low-cost dual-rate optical triplexer for OLT transceivers in 10G/1G co-existing 10G-EPON systems.

The following summarizes the results obtained in this study.

In chapter 2, circuit technology for reducing size and cost of a 60-GHz full-monolithic PLO chip set for millimeter-wave wireless access network equipment was proposed. The uniplanar structure reduced the circuit size drastically, and the use of a GaAs MMIC SPD made the PLO simple and compact. Consequently, all the circuits could be integrated into as few as three chips, and the chip area was 5.5 mm^2 for the oscillator and 3.0 mm^2 for the SPD, which contributes to reducing material cost and assembly cost. The oscillator stabilized at 56.0–60.0 GHz in a phase-locked condition with a step four times the size of the PLL reference frequency. The SSB phase noise in the loop bandwidth was suppressed to the noise floor of the PLL, and it was as low as −90 dBc/Hz at 1-MHz offset from 60.0 GHz in spite of the low Q full-monolithic circuitry.

In chapter 3, circuit technology for achieving compatibility between high-speed operation and high output amplitude for an optical modulator driver was proposed. High-speed operation was demonstrated for a series-connected voltage-balancing pulse driver with direct-coupled current switch architecture using 0.1-μm InP HEMTs. A series-connected voltage-balancing configuration can output a high voltage proportional to the number of series-connected transistors by sharing the voltage among the transistors. Novel direct-coupled current switch architecture suppresses undershooting in gate-drain voltage during switching and prevents the FETs from exceeding the gate-drain breakdown voltage. In an on-wafer measurement experiment, the fabricated driver core circuit showed 3.7-Vpp single (7.4-Vpp differential) output with clear eye opening for 10-Gb/s data patterns. Moreover, a series-connected voltage-balancing pulse driver with a high-driving-capability input buffer improved the performance drastically. With the input buffer, the −3 dB limiting bandwidth of the driver increased from 11 to 30 GHz, and rise and fall times decreased from 33 to 16 ps and from 37 to 16 ps, respectively. These decreases in rise and fall times much improved the waveform of the 10-Gb/s eye opening with an output voltage swing of 3.6 Vpp. The driver showed a sufficient speed margin for 10 Gb/s and potential for higher bit rate operation. The driver demonstrated that the series-connected voltage-balancing driver with direct-coupled current switches is a promising candidate for an optical modulator driver in high-speed fiber-optic communications systems.

In chapter 4, module assembly technology for reducing size and cost of an optical module consisting of three optical components for dual-rate optical access systems was proposed. A small

and low-cost optical triplexer module was successfully developed for 10G-EPON applications. Reducing optical path length by means of a light collection system with a low-magnification long-focus coupling lens made the triplexer as small as 20 × 14 × 7.2 mm^3, without degradation of optical coupling efficiency. A low-material-cost design for the EADFB-LD transmitter and eliminating lenses yielded cost reduction. The 10G/1G dual-rate burst-mode TIA with feedback AGC provides superior receiver sensitivity. As a result, excellent performance has been achieved that complies with the IEEE 802.3av PR30, 802.3av PRX30, and 802.3ah PX20 standards.

The above research results provide fundamental data regarding technologies that can attain or improve transmitting and receiving devices in next-generation advanced high-speed access network equipment. These results will contribute to promoting the actualization of transmitting and receiving devices in advanced high-speed access network equipment. Finally, it is my sincere hope that this dissertation will aid in actualizing future access network systems.

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List of Publications

1. Works Regarding This Dissertation

1.1. Papers

(J-1) Atsushi Kanda, Tadao Nakagawa, Tetsuo Hirota, Hiroshi Okazaki, and Masaru Nakamae, "An MMIC V-band phase-locked oscillator using a GaAs MMIC sampling phase detector," IEEE Trans. Microwave Theory Tech., vol. 45, no. 5, pp. 659–665, May 1997.

(J-2) Atsushi Kanda, Yohtaro Umeda, and Takatomo Enoki, "10 Gbit/s series-connected voltage-balancing pulse driver with direct-coupled current switches," Electronics Letters, vol. 39, no. 12, pp. 908–909, June 2003.

(J-3) Yohtaro Umeda, Atsushi Kanda, Kimikazu Sano, Koichi Murata, and Hirohiko Sugahara, "10 Gbit/s series-connected voltage-balancing pulse driver with high-speed input buffer," Electronics Letters, vol. 40, no. 15, pp.934–935, July 2004.

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(P-1) Atsushi Kanda, Tetsuo Hirota, Hiroshi Okazaki, and Masaru Nakamae, "An MMIC chip set for a V-band phase-locked local oscillator," IEEE GaAs IC Symp. Dig., San Diego, CA, USA, pp. 259–262. Oct. 1995.

(P-2) Yohtaro Umeda, Atsushi Kanda, and Takatomo Enoki, “Novel direct-coupled current switch architecture for a series-connected voltage-balancing pulse driver,” IEEE MTT-S Int. Microwave Symp. Dig., Philadelphia, PA, USA, pp. 2265–2268, June 2003.

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2. Related Works

2.1. Papers

(1) Masashi Nakatsugawa, Atsushi Kanda, Hiroshi Okazaki, Kenjiro Nishikawa, and Masahiro Muraguchi, “Line-loss and size reduction techniques for millimeter-wave RF front-end boards by using a polyimide/alumina–ceramic multilayer configuration,” IEEE Trans. Microwave Theory Tech., vol. 45, no. 12, pp. 2308–2315, Dec. 1997.

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(10) Masashi Nakatsugawa, Atsushi Kanda, Hiroshi Okazaki, Kenjiro Nishikawa, and Masahiro Muraguchi, "Line-loss and size-reduction techniques for millimeter-wave RF front-end boards by using a polyimide/alumina–ceramic multilayer configuration," IEEE MTT-S Int. Microwave Symp. Dig., Denver, CO, USA, pp. 509–512, June 1997.

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