Resistance change phenomenon in Ta_2O_5/TiO_2 stacked structure and its application to non-volatile memory

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Resistance change phenomenon in Ta_2O_5/TiO_2 stacked structure and its application to non-volatile memory

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Preface

This thesis is submitted to the Graduate School of Pure and Applied Sciences at the University of Tsukuba, Japan, in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy in Science. The present study found its origins in a research program on emerging nonvolatile memory which took place from October 2008 to March 2010 in Device platforms research laboratory of NEC Corporation.

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Yokkaichi, February 2017

List of Publications

In the thesis, the references listed below are referred.

Publications Related to Thesis

[1] Y. Sakotsubo, M. Terai, S. Kotsuji, T. Sakamoto and H. Hada, "Physical model for reset state of Ta_2O_5/TiO_2-stacked ReRAM", *41th International Conference on Solid State Devices and Material*, *Technology Digest of Technical Papers*, (2009) 1204-1205.

[2] Y. Sakotsubo, M. Terai, S. Kotsuji, T. Sakamoto and H. Hada, "Physical Model for Reset State of Ta_2O_5/TiO_2-stacked Resistance Random Access Memory", *Japanese Journal of Applied Physics* **49**, (2010) 04DD19

[3] M. Terai, Y. Sakotsubo, Y. Saito, S. Kotsuji and H. Hada, "Effect of Bottom Electrode of ReRAM with Ta_2O_5/TiO_2 Stack on RTN and Retention", *2009 International Electron Device Meeting*, Technology Digest of Technical Papers, (2009) 775-778.

[4] M. Terai, Y. Sakotsubo, S. Kotsuji, and H. Hada, "Resistance Controllability of Ta_2O_5/TiO_2 Stack ReRAM for Low-Voltage and Multilevel Operation", *Electron Device Letters* **31**, (2010) 204-206.

[5] M. Terai, Y. Sakotsubo, Y. Saito, S. Kotsuji, and H. Hada, "Memory-State Dependence of Random Telegraph Noise of Ta_2O_5/TiO_2 Stack ReRAM", *Electron Device Letters* **31**, (2010) 1302-1304.

[6] Y. Sakotsubo, M. Terai, S. Kotsuji, Y. Saito, M. Tada, Y. Yabe, and H Hada, "A New Approach for Improving Operating Margin of Unipolar ReRAM using Local Minimum of Reset Voltage", *2010 Symposium on VLSI*, Technology Digest of Technical Papers, (2010) 87-88.

[7] M. Terai, M. Saitoh, T. Nagumo, Y. Sakotsubo, Y. Yabe, K. Takeda and T Hase, "High Thermal Robust ReRAM with a New Method for Suppressing Read Disturb", *2011 Symposium on VLSI*, Technology Digest of Technical Papers, (2011) 50-51.

[8] Y. Sakotsubo, “NONVOLATILE SEMICONDUCTOR OTHER PUBLICATIONS MEMORY DEVICE AND MANUFACTURING METHOD THEREOF”, US 8,598,564 (2013).

[9] Y. Sakotsubo, M. Terai, M. Tada, Y. Yabe, and Y. Saito, “SEMICONDUCTOR DEVICE WITH VARIABLE RESISTANCE ELEMENT AND METHOD FOR MANUFACTURING THE SAME”, US 8,766,233 (2014).

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Chapter 1. Introduction

Today's highly information-oriented society is carried by the data processing which is implemented by pyramidal hierarchical structure shown in Figure 1-1(a) of memories and storage devices [1]. To improve the data processing further, reducing the latency gaps is important. Traditionally, improvement of data processing speed and capacity is most interested in the product development for each memory and storage classes. Although the latency gap between dynamic random access memory (DRAM) and hard-disc drive (HDD) had not been bridged by the efforts [2], solid-state drive (SSD) composed of NAND flash memory device appeared into the gap recently, and the SSD dramatically reduced the gap and improved the data processing speed. And now, the SSD is replacing HDD market through the effort of cost reduction rapidly as shown in Figure 1-1 (b). However, the SSD does not fully bridge the gap fundamentally, because the device composed of NAND flash memory cannot be accessed randomly like a DRAM. So, the "non-volatile memory (NVM)" bridging the latency gap is highly required [3].

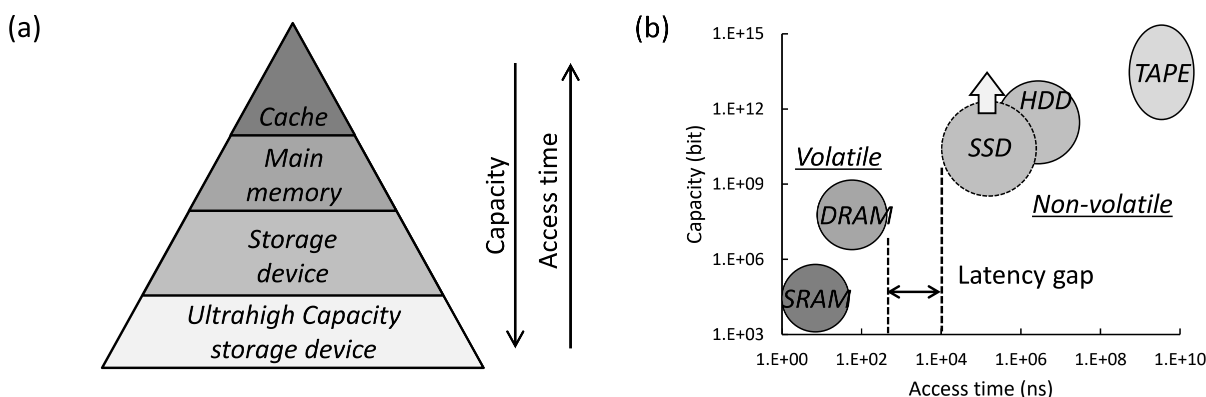

Figure 1-1 (a) Pyramidal hierarchical structure. (b) Positioning for memories and storages.

Now, transition metal oxide (TMO) -based resistance change device is attracting attention as a candidate of the bridging device between main memory and storage device [3-11]. The cell structure of the device is a simple Metal-TMO-Metal stack, and well-known materials such as hafnium oxide and titanium oxide are used for the TMO layer. The zero-bias conductivity of the cell is changed by only applying the voltage to the cell. This device is characterized by three features [3-11]. Firstly, this device has long retention time which is enough longer than the access times. Secondly, this device works with ultra-high speed less than 100ns. These two features satisfy the demand for "non-volatile memory" bridging the latency gap. Thirdly, the material and process are highly compatible with CMOS process, and one does not need additional dedicated facility and process optimization for fabricating the structure because these material and process are already used in a current product line. Thus, TMO-base resistance change device is the most promising candidate among emerging non-volatile memory devices such as phase change device and magnetic change device [3].

Resistance change phenomenon in the TMO materials has not yet been elucidated. For example, it is not clear why the state changes by applying the voltage and why the changed states keep long time. The resistance change behavior is different for each TMO material, and a variety of resistance change models have been proposed to explain it [3]. In this sense, basic research is indispensable to the

development of the resistance change memory. We will introduce the background easily in the following.

1- 1 Resistance change phenomena in Transition metal oxide

In 1962, T. W. Hickmott observed a hysteresis loop in current-voltage characteristic of Metal-Insulator-Metal (MIM) structure with oxide insulator such as titanium oxide, zirconium oxide and silicon oxide for the first time [12]. Since then, resistance change phenomena have been found and studied in various binary and multi-nary oxide [15-18] such as , Ag/NiO/Ni [13], Al/TiO_2/Ti [14], Ti/Cu_2O/Cu [7], Pt/$Pr_{0.7}Ca_{0.3}MnO_3$(PCMO)/Pt [19] and Pt/PZT/Pt [20, 21] before the late 2000s. This phenomenon was called "Colossal electro-resistance (CER)" because the resistance is changed by electrical stimulation [22].

The resistance change behaviors are classified into two types, bipolar- and unipolar- (nonpolar-) type, depending on the materials composing the cell. Typical current-voltage characteristics for each type are shown in Figure 1-2. The cell has two states, high resistance state (HRS) and low resistance state (LRS), and the state is changed by applying the voltage to the cell. An operation changing the cell from LRS to HRS is called RESET, while opposite operation is called SET in the both type cells. In the bipolar-type cells, initial state (as-fabricated pristine state) is usually LRS, and the resistance can be changed by bipolar-type operation [Fig. 1-2(a)]. On the other hand, in the unipolar-type cells, initial state is usually insulating, and the resistance can be changed by unipolar-type operation of either polarity [Fig. 1-2(b)]. The both types of the cells can be also operated with pulsed voltage. Although essential pulse width for SET and RESET operations depends on the pulse height, resistance change phenomena occur in ultra-short pulse less than 10ns [9-11, 19].

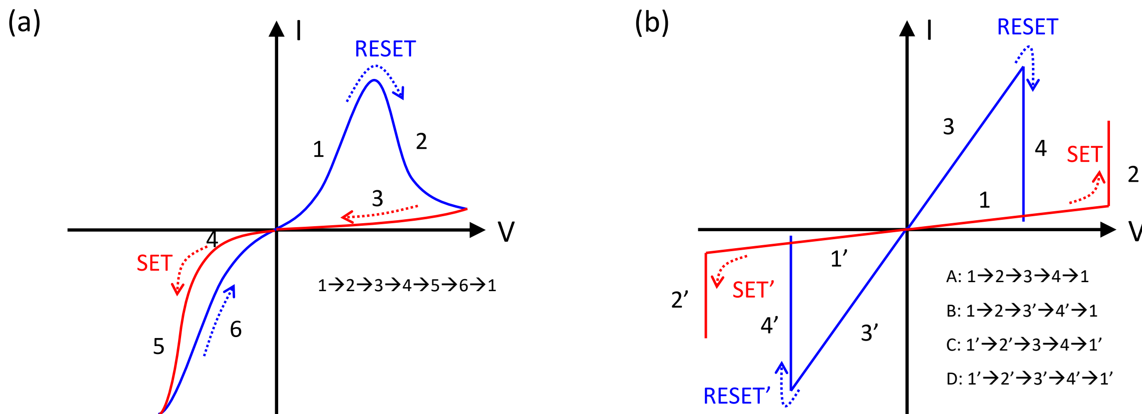

Figure 1-2 Schematics of resistance change phenomena. (a) I-V characteristics in bipolar-type cell. Single hysteresis loop is observed. (b) I-V characteristics in unipolar- (nonpolar-) type cell. RESET and SET phenomena are observed in either polarities as indicated by A to D.

1-2 Resistance change model for transition metal oxide

There have been proposed several models for resistance change phenomena in particular class of materials and structure with electrical conduction model. They include the ferroelectricity-based model [23-25], insulator-metal transition (IMT) -based model [26-28], charge-trap-based model [29-31], and V_O cohesion-isolation transition-based model [32-34]. The ferroelectricity-based model was proposed to described the resistance change in ferroelectric materials such as Cr-doped $SrZrO_3$ [21], Cr-doped $SrTiO_3$ [35], $Pt/Pb(Zr_{0.52}Ti_{0.48})O_3$ /$SrRuO_3$ hetero-structure [36], and is based on the reversal of electric polarization that causes a change in tunnel barrier or the Schottky barrier [23-25]. The IMT-based model deals the resistance change in materials such as Cr-doped $SrZrO_3$ [21], and $Ag/CeO_2/La_{0.67}Ca_{0.33}MnO_3$ [37], and the strong electron correlation in these materials are thought to be essential for the resistance change [26-28]. The charge-trap-based model is a model for $Pt/Pr_{0.7}Ca_{0.3}MnO_3$ [29-31]. The V_O cohesion-isolation transition is caused by carrier injection/removal. This model is a generalized resistance change mechanism in binary oxides such as TiO_2 [32, 33], NiO [33] and HfO_2 [34].

As for the simple binary TMO-base resistance change devices, the features such as the cell area dependence and the switching polarity differ among devices, and are currently discussed by two types of model, i.e., the interface switching model [38] and the filamentary switching model [3, 15, 38]. Main features of both models are summarized in Table 1-1, which we will explain briefly in the following.

Table 1-1 General understanding for TMO-based switching devices [3]

	Interface switching devices	Filamentary switching devices
Switching polarity	Bipolar	Unipolar (Nonpolar)*
Switching model	Redox reaction (Reduction & Oxidation)	Thermal reaction (Conductive path formation & rupture)
Physical model	Schottky barrier height (LRS: Low, HRS: High)	LRS: Ohmic conductor HRS: Tunnel barrier
Typical cell structure	SW layer: Non-stoichiometric TMO Electrode: Inert electrode	SW layer: Stoichiometric TMO Electrode: N/A

Note: *In this devices, “unipolar” has the same meaning as “nonpolar”. SET/RESET phenomena are observed in either polarity.

i Interface switching model for bipolar-type cell

Interface switching model was proposed for explaining bipolar-type resistance change phenomenon (Fig. 1-2(a)). It is expected that the resistance change occurs at the interface of the electrode and the TMO layer owing to movement of oxygen vacancies/ions or trapping/de-trapping of electrons or holes under the applied electric field [38]. The resistance is usually proportional to the cell area.

In 2008, Wei et al. investigated composition profile of Pt/TaOx/Pt structure by Hard X-ray Photoemission Spectroscopy (HX-PES), and found that the ratio of $TaO_{2-\beta}/Ta_2O_{5-\delta}$ increases from HRS to LRS, indicating that the $Ta_2O_{5-\delta}$ component of HRS is reduced to the $TaO_{2-\beta}$ component of

LRS [39, 40]. The origin of the resistance change was attributed to the changing of the barrier height between the anode and TaO_X caused by the redox reaction.

To achieve stable resistance change, the device should be composed of non-stoichiometric TMO layer sandwiched between the inert metal electrodes, and the oxygen profile of the un-stoichiometric TMO layer should have gradient to control the resistance change region. Moreover, high work-function material for anode electrode achieves stable RESET operation. The interface resistance increases with increasing the Schottky barrier height caused by the oxygen atoms segregation at the anode/oxide interface. Based on these experimental evidences, device model, which could explain well the resistance change behavior, was constructed [41, 42]. By this breakthrough, mass-production of new non-volatile memory with the interface-type cell in 2012.

ii Filamentary switching model for unipolar-type cell

Filamentary switching model is proposed to explain another type of devices, where the initial state is a HRS, resistance can be changed by unipolar-type operation of either polarity (see Fig. 1-2(b)), and resistance of both LRS and HRS does not depend on cell area [43-51]. The operation changing from an initial HRS to a LRS is especially called FORMING. By a FORMING operation, filamentary thin conductive path is postulated to be formed perpendicular to the resistance change layer [3]. The region other than the filament is still unchanged in the initial state. This filamentary-conductive-path hypothesis is supported by the fact that the resistance of both LRS and HRS is almost constant irrespective of the cell area [48-51].

ii- 1 Filamentary conductive path in transition metal oxide

In the early studies, it was speculated that resistance change occurs at grain boundaries which role filamentary ion channel of the polycrystalline TMO layers [12-15, 47], and similar mechanism as the interface switching was supposed [43-46]. In 2000s, the resistance change phenomena were found even in grain boundary-less stoichiometric binary TMO layer such as HfO_2 and NiO formed by the atomic-layer deposition (ALD) method and the epitaxial growth method [43, 49]. Moreover it was reported that the resistance can be changed not only by the bipolar-type operation but also by the unipolar- (nonpolar-) type operation [43-51]. Thus, we understood that the resistance change mechanism in these devices is different fundamentally from that in the interface switching devices [3].

The change during the FORMING is very similar to the dielectric breakdown of gate oxide (e.g. SiO_2, HfO_2) in the MOS transistor. Defects are generated randomly in the bulk by electrical stress-induced Si-O/Hf-O bond breaking [52]. The defect generation rate is given by following expression,

$$P_E \propto exp\left(-\frac{E_a-\beta E_{OX}}{k_B T}\right), \qquad (1\text{-}1)$$

where E_a is the activation energy for Si-O/Hf-O bond breaking, β is the contribution of the bond polarization to the local electric field, E_{OX} is average electrical field in the oxide, k_B is the Boltzmann constant, and T is the temperature [52]. Leakage current through the oxide increase with increasing defects. Finally, the generated defects complete a percolation path that bridges the

two electrodes across the oxide, eventually [53-55]. The current through the path increases significantly and causes lateral growth of the path. It is noted that isolated defect (typically oxygen vacancy) in the oxide behaves as an electron trap.

These percolation paths composed of generated defects are formed in the filamentary switching devices after FORMING operation [54]. When the percolation path has an Ohmic current-voltage characteristics, this conductive path is called “filament”. Thus, it is believed that the filaments are locally formed in the TMO layer. In 2005, B. J. Choi showed the evidence of localized conductive path in the TiO_2 thin film grown by ALD by using conductive atomic force microscope (CAFM) (see Figure 1-3(a)) [43]. Since 2010, studies of direct observation of the conductive filaments in single TiO_2 layer cell by analyzing crystal structure using a transmission electron microscope (TEM) have been reported [56-59]. According to D.H. Kwon et al., Magnéli phases (Ti_4O_7) was confirmed in the TiO_2 layer after FORMING [56]. As Ti_4O_7 shows metallic conduction at room temperatures, Ti_4O_7 region bridging the electrodes is regarded as the conducive filament. Moreover, it was confirmed that the Magnéli phases is disappeared in the middle region between the electrodes after RESET operation [56].

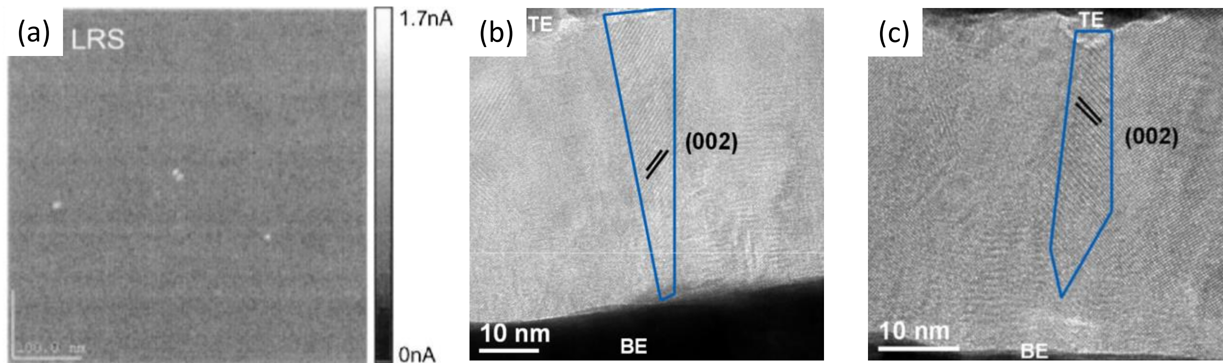

Figure 1-3 Evidences of a filamentary conductive path in TiO_2 film. (a) Conductivity mapping results of the low resistance state TiO_2 films, using atomic force microscopy systems with conductive tips(CAFM) [42]. The bright spots represent the conducting spots. (b) High-resolution TEM image of the low resistance state TiO_2 films [56]. (c) High-resolution TEM image of the high resistance state TiO_2 films [56].

ii- 2 Thermal reaction-based resistance change model

Unipolar switching shown in Figure 1-2(b) of filamentary switching device is obviously not explained by the redox reaction-based resistance change model for the interface switching. Most promising resistance change model for the *RESET* is the thermal reaction-based model which was provided by the linear temperature dependence of the RESET voltage [8, 60-65].

In 2006, Fang et al. investigated temperature dependence of LRS retention property, and found transition to HRS from LRS after thermal stress [8]. The critical temperature for the LRS-HRS transition increases as the LRS resistance decreases as reprinted in Figure 1-4(a). Moreover, it is confirmed that RESET power decreases as the ambient temperature [Figure 1-4(b)] [8, 63]. These results strongly implied that RESET mechanism in the filamentary switching device is caused by the thermal reaction.

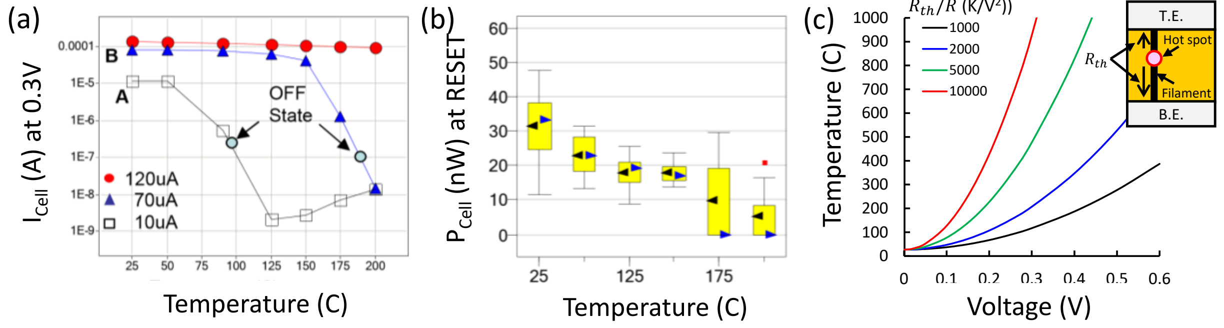

Figure 1-4 (a) Thermal stability of LRS in $Cu/Cu_2O/Ni$ memory cells [8]. The critical temperature for a LRS-HRS transition increases as the LRS resistance decreases. (b) RESET power dependence on ambient temperature [8]. RESET power decreases as the ambient temperature. The box shows the data range and the triangle indicates the mean and median. (c) Calculated filament temperature dependence on the ratio of thermal resistance to filament resistance [63-65]. R_{th} is equivalent thermal resistance of filament describing the heat loss from the hot spot on the filament toward the top and bottom electrodes as shown in inset of (c).

In 2008, Cagli et al. proposed the joule heating model which was considered that the defects composing the filament are relaxed to stable states by thermally acceleration [64, 65]. The relaxation probability is described in following equation,

$$\nu \propto exp\left(-\frac{E_a}{k_B T}\right), \qquad (1\text{-}2)$$

where E_a is the activation energy for the relaxation, k_B is the Boltzmann constant, and T is the local temperature. The local temperature depends on power consumption on the filament and thermal conductivity of the filament;

$$T = T_0 + \frac{R_{th}}{R} V^2, \qquad (1\text{-}3)$$

where T_0 is the ambient temperature and R_{th} is the equivalent thermal resistance of the filament describing the heat loss from the hot spot on the filament toward the top and bottom electrodes as shown in inset of Figure 1-4(c). The filament temperature just depends on the voltage across the filament [Fig. 1-4(c)], and the relaxation probability significantly increases with the voltage. Therefore, the defect states composing conductive filament decrease during the RESET operation, and the conductive filament is ruptured, finally.

1- 3 Filamentary resistance change devices for non-volatile memory application

Nowadays, conventional DRAM and NAND flash memory developments face the serious challenges which exist in the tradeoff between READ/WRITE latencies, WRITE/ERASE immunity, data retention and scalability, and the filamentary resistance change devices are expected to be able to overcome the tradeoff relation, fundamentally. Requirements for achieving the non-volatile memory (NVM) are

1. Low READ/WRITE latencies,
2. Highly WRITE/ERASE immunity (i.e. cycle endurance),
3. Highly non-volatility (i.e. data retention under thermal and electrical stresses).

i Advantages of filamentary resistance change devices

In the filamentary resistance change devices, the LRS (On-state) composed of the conductive filament bridging the electrodes is the most important state for the retention properties such as non-volatility and disturb immunity. If we use the result of simulation with Eq. 1-2 and Eq. 1-3, the retention time of the LRS depends strongly on the applied voltage, and the retention time at READ bias (~0.1V) is about 10^{12} times longer than that at RESET bias (~0.5V) although sufficient cell current can be obtained in low voltage due to the ohmic property of LRS in filamentary switching device. So, the state can be sensed with short integration time compared to the interface switching device which has nonlinear property of LRS. These facts mean that filamentary switching devices make both highly non-volatility and low READ/WRITE latencies happen at once.

The filamentary resistance change devices have two other significant advantages over other candidates such as the TMO-based interface switching devices, the phase change devices and the magnetic change devices in terms of the process integration feasibility in a chip fabrication plant (FAB). First one is the fact that the materials such as stoichiometric TMO is already introduced in the FAB. These materials are used for the gate insulator of a field effect transistor. The other one is that the materials can be deposited with atomic layer deposition (ALD) method. This means that the device is applicable to three dimensional (3D) structure which realize the both high density and high cost performance at once. Moreover it is expected to be able to be scaled the cell size to the filament size level. Thus, filamentary resistance change devices are the most promising candidate for the next-generation nonvolatile memories.

ii Challenges and the solutions

Filamentary switching devices have a challenge in the SET/RESET cycle endurance. Generally, cell current of both LRS and HRS increases as the SET/RESET cyclings advance. Most frequent failure is RESET failure, which is classified into two types shown in Figure 1-5(a) and (b). In Type-A failure mode, the reduction of the cell current after RESET operation is not large enough to meet the HRS specification. In Type-B failure, the cell current get stuck on the LRS because the switching current for RESET becomes larger than drivability of voltage source. Both failures are caused by increase of

total cross-sectional area of the filaments, which is originated from filament number [Fig. 1-5(d)] and/or thickness [Fig. 1-5(e)] [43].

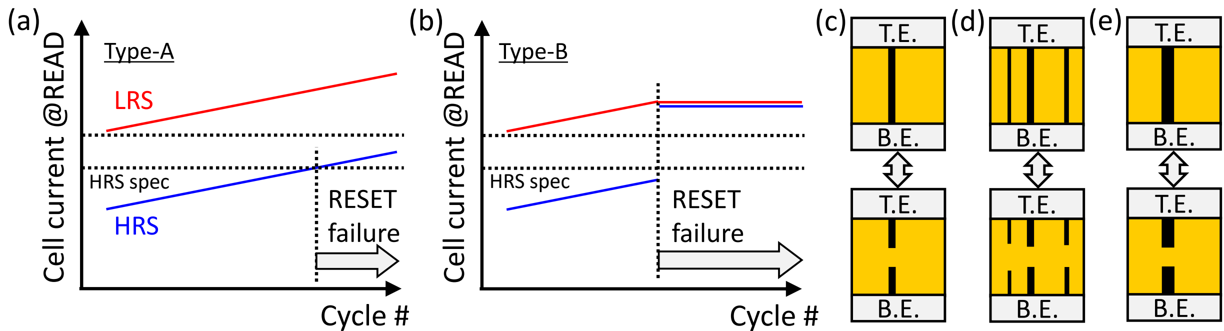

Figure 1-5 Schematics of RESET failure modes. Cell currents of both LRS and HRS increase with increasing cycling number. (a) Type-A failure mode: Cell current does not reach the HRS criteria. (b) Type-B failure mode: Cell current get stuck on the LRS. (c) Schematics of the filament in initial cycling stage. (d) Schematics of the filament in aged cells. (e) Schematics of the filament with large SET current.

So, to suppress the additional filament formation is a key to improve the cycle endurance, and the process had been studied in details by R. Degraeve [66]. The risk of additional filament formation during SET operation is higher than that during RESET operation, because the electrical stress such as electrical field is larger in SET operation. In order to reduce the stress at the SET operation, we have two methods [67]: One is the cutoff of the stress just after SET by using series transistor. The other one is the reduction of the effective electrode size to the filament size by stacking relatively stable TMO layer in series.

ii- 1 1T-1R type device

In 2004, usefulness of 1T-1R type device structure was introduced by I. G. Baek et al. [5]. Transistor (FET) controlling the operating current was incorporated in series with the memory cell as shown in Figure 1-6(a). Because of current limiting feature of FET, the voltage across the memory cell decreases instantaneously after SET occurs, as shown in Figure 1-6(c). Thus, additional filament formation risk is significantly reduced [54-55]. Oneness of the conductive filament formed on the 1T-1R configuration was shown in several literatures. I. G. Baek et al. and H. Shima et al. reported that resistance of LRS does not depend on the cell area [5, 61]. In addition, K. Kinoshita reported that one of the divided cells after FORMING operation is always high resistive state although another one showed the low resistance that agreed with LRS before being divided [68].

1T-1R type device is also useful to control the filament thickness [69-72]. K. Kinoshita et al. reported that the RESET current depends on the compliance current at SET operation [71]. Type-B RESET failure is dramatically reduced by using 1T-1R type device structure.

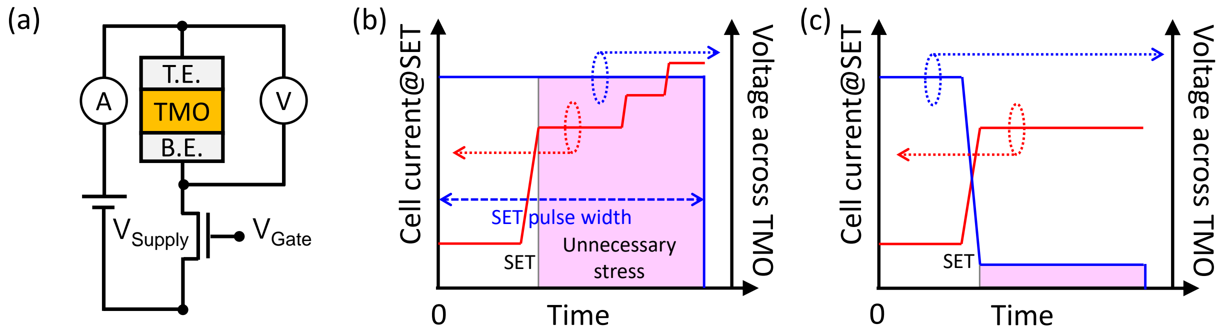

Figure 1-6 Schematics of SET operation on 1T-1R device. (a) Schematic circuit diagram of 1T-1R device. Transistor is incorporated in series with the memory cell. (b) SET operation on 1R device. Large electrical stress is applied continuously to the TMO layer during SET operation. (c) SET operation on 1T-1R device. Electrical stress is decreased significantly after SET.

ii- 2 Heterogeneous TMO stacked structure for the memory cell

In the early days, filamentary switching devices were composed of single layer of polycrystalline TMO (Figure 1-7(a)) [5, 6, 11-14, 45-48]. The cycle endurance of such devices was poor, because filaments easily increases in domain boundaries (DBs) of the polycrystalline film during the cycling. A simple solution is to apply single crystalline film as the TMO layer, but it is not easy to fabricate a perfect film [43, 49, 73].

Kinoshita et al. proposed heterogeneous polycrystalline TMO stacked cell (Figure 1-7(c)) [68]. In this memory cell, higher isolative initial state and lower switching current were observed. They speculated that number of filament bridging the two electrodes was suppressed in the heterogeneous TMO stacked cell, and relatively stable filaments in the TiO_2 layer acts as an electrode. If we believe this hypothesis, the switching current can be reduced by using single stable filament as the electrode.

In 2008, Terai et al. proposed a novel cell structure which is composed of amorphous Ta_2O_5 (a-Ta_2O_5)/polycrystalline TiO_2 (p-TiO_2) stacked layers (Figure 1-7(d)) [74]. They were inspired by two fact, that is,

- The amorphous structure is homogeneous and isotropic, and there is no weak structure like grain boundaries or lattice defects, and
- Single Ta_2O_5 layer does not show any switching properties.

These facts suggest that un-switchable stable conductive filament is formed in the a-Ta_2O_5 layer by FORMING operation, while the p-TiO_2 stacked on a-Ta_2O_5 acts as typical resistance change material. Based on it, they speculated that resistance change phenomena occur in limited area of TiO_2 by apex of the stable filament formed in a-Ta_2O_5 layer. Additional fact that

- FORMING voltage in the a-Ta_2O_5/p-TiO_2 stack can be controlled by the a-Ta_2O_5 thickness, and

- SET/RESET voltages are enough lower than the FORMING voltage,

suggest that the probability of the stable conductive filament formation in a-Ta_2O_5 is very small during the cycling [54, 55]. Thus, the RESET failures of both Type-A and Type-B are expected to be significantly reduced in this structure, however highly SET/RESET cycle endurance was not demonstrated in the literature although data retention properties dependence on thermal and electrical stresses were examined.

Terai et al. also reported distributions of SET/RESET voltages in the Ta_2O_5/TiO_2 stacked cell, and pointed out that the distributions depend on the HRS/LRS resistances [74]. However, physical origin of the variations was not discussed because detail parametric analysis and in-depth understanding of the states were lacked in the study. It is noted that Terai et al. had reported that the RESET phenomenon was observed only with single polarity like a bipolar operation in the literature [74]. As a result of additional experiments, it has been found that unipolar (nonpolar) operation is possible as long as sufficient current is supplied in RESET operation [75].

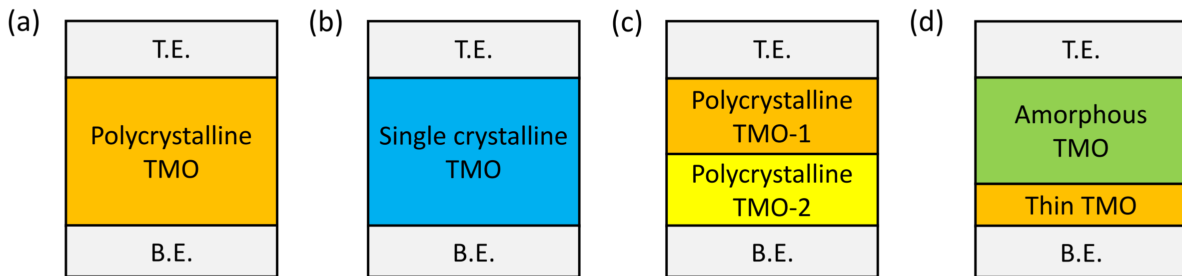

Figure 1-7 Schematic cell structures of filamentary switching device. (a) Conventional polycrystalline TMO cell, (b) Single crystalline TMO cell, (c) Heterogeneous polycrystalline TMO stacked cell, (d) Amorphous TMO and ultra-thin polycrystalline TMO stacked cell.

1-４ Purposes of this study

As described in the preceding section, the Ta_2O_5/TiO_2 stacked resistance change device proposed by Terai et al. was expected to have superior performance in the cycle endurance. Although the resistance change phenomena and non-volatility were already reported [74], the resistance change mechanism and the transport mechanism were not discussed. In this study, we examined the transport properties of this device in details to understand following three issues.

i Resistance change phenomenon in Ta_2O_5/TiO_2 stacked structure

In reference 69, Terai et al. speculated that the resistance change in the Ta_2O_5/TiO_2 stacked device occurs by the redox reaction in TiO_2 layer. However, the model cannot explain the unipolar switching in the device. In this study, we analyze the switching parameters in details to know the mechanism of the resistance change.

ii Physical model for high resistance state of Ta_2O_5/TiO_2 stacked structure

Microscopic understanding of the HRS is important to discuss the risk of unnecessary filament formation during switching operations and to construct the reliability model for the SET/RESET cycle endurance. In this study, we show the physical model for the HRS based on the detail analysis of the electrical properties of HRS at low temperatures.

iii Non-volatile memory performance of Ta_2O_5/TiO_2 stacked structure

Most important function is the SET/RESET cycle endurance for achieving the non-volatile memory application. However SET/RESET cycle endurance in the Ta_2O_5/TiO_2 stacked cell was still not demonstrated although data retention properties dependence on thermal and electrical stresses were examined. In this study, we demonstrate the cycle endurance of Ta_2O_5/TiO_2 stacked cell on 1kbits memory cell array.

1-5 Outline of this thesis

This thesis is organized in six chapters. In the Chapter 1, we introduced a background of this study at first. The resistance change phenomena and models for the phenomena were described to give a purpose of this study. In Chapter 2, we explain the experimental details such as sample preparation and electrical evaluation method.

Main subjects are described in Chapters 3, 4 and 5.

In Chapter 3, we investigate the resistance change phenomenon in the Ta_2O_5/TiO_2 stacked cell. As a result, we understand that the resistance change phenomenon is originated from rupture and re-connection of the conductive filament in the TiO_2 layer, which is induced by the joule heating of the conductive filament.

In Chapter 4, we investigate the conduction mechanism of the HRS by analyzing the I-V characteristics at low temperatures, and discuss the detail process of the conduction by comparing the data with a simple conduction model on the picture of the ruptured filament. As a result, we realize that the conduction in the HRS composed of not only the direct tunneling but also the trap-assisted tunneling.

In Chapter 5, we demonstrate the memory function of Ta_2O_5/TiO_2 stacked cell on 1kbits memory cell array. From the investigation in chapter 3, we find the SET occurrence is influenced by parameters in RESET operation, and vice versa. We show the decision making process of the operating parameters such as the target LRS/HRS specs and the operating voltages for reducing the risk of unnecessary additional or thicker filament formation at switching operations. We understand that the compliance current (I_{COMP}) at SET operation and the pulse height in RESET operation are keys for reliable operation. Then, we show the memory function with optimized switching parameters on 1kbits array. We confirm an excellent cycle endurance with single pulse operation, and a good retention property in 100 degrees C.

In Chapter 6, we summarized this thesis.

1-6 Reference

[1] D. A. Patterson and J. L. Hennessy, "Computer Organization and Design: The Hardware/Software Interface", Fifth edition, *Morgan Kaufmann* (2013).

[2] International technology roadmap for semiconductors, http://www.semiconductors.org/main/2015_international_technology_roadmap_for_semiconductors_itrs/, (2016).

[3] D. Ielmini and R. Waser, "Resistive switching from fundamentals of nanoionics redox processes to memristive device applications" *WILEY-VCH* (2016).

[4] W. W. Zhuang, W. Pan, B. D. Ulrich, J. J. Lee, L. Stecker, A. Burmaster, D. R. Evans, S. T. Hsu, M. Tajiri, A. Shimaka, K. Inoue, T. Naka, N. Awaya, K. Sakiyama, Y. Wang, S. Q. Liu, N. J. Wu, and A. Ignatiev, "Novell Colossal Magnetoresistive Thin Film Nonvolatile Resistance Random Access Memory (RRAM)", *IEDM Tech. Dig.*, pp. 193-196 (2002).

[5] I. G. Baek, M. S. Lee, S. Seo, M. J. Lee, D. H. Seo, D.–S. Suh, J. C. Park, S. O. Park, H. S. Kim, I. K. Yoo, U.-In Chung and J. T. Moon, "Highly Scalable Non-volatile Resistive Memory using Simple Binary Oxide Driven by Asymmetric Unipolar Voltage Pulses," *IEDM Tech. Dig.*, pp. 587-590 (2004).

[6] I. G. Baek, D. C. Kim, M. J. Lee, H.-J. Kim, E. K. Yim, M. S. Lee, J. E. Lee, S. E. Ahn, S. Seo, J. H. Lee, J. C. Park, Y. K. Cha, S. O.Park, H. S. Kim, I. K. Yoo, U-In. Chung, J. T. Moon, and B. I. Ryu, "Multi-layer cross-point binary oxide resistive memory (OxRRAM) for post-NAND storage application", *IEDM Tech. Dig.*, pp. 769-762 (2005).

[7] A. Chen, S. Haddad, Y.-C. Wu, T.-N. Fang, Z. Lan, S. Avanzino, S. Pangrle, M. Buynoski, M. Rathor, W. Cai, N. Tripsas, C. Bill, M. VanBuskirk, and M. Taguchi, "Non-Volatile Resistive Switching for Advanced Memory Applications", *IEDM Tech. Dig.*, pp. 746-749 (2005).

[8] T.-N. Fang, S. Kaza, S. Haddad, A. Chen, Y.-C. Wu, Z. Lan, S. Avanzino, D. Liao, C. Gopalan, S. Choi, S. Mahdavi, M. Buynoski, Y. Lin, C. Marrian, C. Bill, M. VanBuskirk and M. Taguchi, "Erase Mechanism for Copper Oxide Resistive Switching Memory Cells with Nickel Electrode", *IEDM Tech. Dig.*, pp. - (2006).

[9] Y. Hosoi, Y. Tamai, T. Ohnishi, K. Ishihara, T. Shibuya, Y. Inoue, S. Yamazaki, T. Nakano, S. Ohnishi, N. Awaya, I. H. Inoue, H. Shima, H. Akinaga, H. Takagi, H. Akoh, and Y. Tokura, "High Speed Unipolar Switching Resistance RAM (RRAM) Technology", *IEDM Tech. Dig.*, pp. 1-4 (2006).

[10] K. Tsunoda, K. Kinoshita, H. Noshiro, Y. Yamazaki, T. Jizuka, Y. Ito, A. Takahashi, A. Okano, Y. Sato, T. Fukano, M. Aoki, and Y. Sugiyama, "Low Power and High Speed Switching of Ti-doped NiO ReRAM under the Unipolar Voltage Source of less than 3 V", *IEDM Tech. Dig.*, pp. 767-770 (2007).

[11] C. Yoshida, K. Tsunoda, H. Noshiro, and Y. Sugiyama, "High speed resistive switching in Pt/TiO_2/TiN film for nonvolatile memory application", *Appl. Phys. Lett.*, **91**, 223510 (2007).

[12] T. W. Hickmott, "Low-frequency negative resistance in thin anodic oxide films", *J. Appl. Phys.*, **33**, 2669–2682 (1962).

[13] J. F. Gibbons and W. E. Beadle, “Switching properties of thin NiO films”, *Solid State Electronics Pergamon Press*, **7**, 785-797 (1964).

[14] F. Abgall, “Switching phenomena in titanium oxide thin films”, *Solid-State Elrctronics Pergamon Press*, **11**, 535-541 (1968).

[15] G. Dearnaley, A. M. Stoneham, and D. V. Morgan, “Electrical phenomena in amorphous oxide films”, *Rep. Prog. Phys.*, **33**, 1129–1191 (1970).

[16] Y. Hirose and H. Hirose, “Polarity-dependent memory switching and behavior of Ag dendrite in Ag-photo-doped amorphous As2S3 films”, *J. Appl. Phys.*, **47**, 2767–2772 (1976).

[17] D. P. Oxley, “Electroforming, switching and memory effects in oxide thin films”, *Electrocomponent Sci. Technol. UK*, **3**, 217–224 (1977).

[18] H. Pagnia and N. Sotnik, “Bistable switching in electroformed metal-insulator-metal devices”, *Phys. Status Solidi*, **108**, 11–65 (1988).

[19] A. Asamitsu, Y. Tomioka, H. Kuwahara, and Y. Tokura, “Current switching of resistive states in magnetoresistive manganites”, *Nature*, **388**, 50–52 (1997).

[20] M. N. Kozicki, M. Yun, L. Hilt and A. Singh, “Applications of programmable resistance changes in metal-doped chalcogenides”, *Pennington NJ USA: Electrochem. Soc.*, 298–309 (1999).

[21] A. Beck, J. G. Bednorz, C. Gerber, C. Rossel and D. Widmer, “Reproducible switching effect in thin oxide films for memory applications”, *Appl. Phys. Lett.*, **77**, 139–141 (2000).

[22] D. S. Kim, Y. H. Kim, C. E. Lee, and Y. T. Kim, “Colossal electroresistance mechanism in a Au/Pr0.7Ca0.3MnO3/Pt sandwich structure: evidence for a Mott transition”, *Phys. Rev. B*, **74**, 174430 (2006).

[23] L. Esaki, R. B. Laibowitz, and P. J. Stiles, “Polar Switch”, *IBM Tech. Discl. Bull.*, **13**, 2161 (1971).

[24] H. Kohlstedt, N. A. Pertsev, J. R. Contreras, and R. Waser, “Theoretical current–voltage characteristics of ferroelectric tunnel junctions”, *Phys. Rev. B*, **72**, 125341 (2005).

[25] E. Y. Tsymbal, and H. Kohlstedt, “Tunneling across a ferroelectric”, *Science*, **313**, 181–183 (2006).

[26] M. J. Rozenberg, I. H. Inoue, and M. J. Sanchez, “Nonvolatile memory with multilevel switching: a basic model”, *Phys. Rev. Lett.*, **92**, 178302 (2004).

[27] M. J. Rozenberg, I. H. Inoue, and M. J. Sanchez, “Strong electron correlation effects in nonvolatile electronic memory devices”, *Appl. Phys. Lett.*, **88**, 033510 (2006).

[28] I. H. Inoue, M. J. Rozenberg, S. Yasuda, M. J. Sanchez, M. Yamazaki, T. Manago, H. Akinaga, H. Takagi, H. Akoh and Y. Tokura, “Strong electron correlation effects in non-volatile electronic memory devices”, *Non-Volatile Memory Technology Symposium Tech. Dig.*, pp. 131-136 (2005).

[29] A. Odagawa, H. Sato, I. H. Inoue, H. Akoh, M. Kawasaki, Y. Tokura, T. Kanno and H. Adachi, “Colossal electroresistance of a $Pr_{0.7}Ca_{0.3}MnO_3$ thin film at room temperature”, *Phys. Rev. B*, **70**, 224403 (2004).

[30] S. Tsui, A. Baikalov, J. Cmaidalka, Y. Y. Sun, Y. Q. Wang, Y. Y. Xue, C. W. Chu, L. Chen and A. J. Jacobson, "Field-induced resistive switching in metal-oxide interfaces", *Appl. Phys. Lett.*, **85**, 317-319 (2004).

[31] T. Harada, I. Ohkubo, K. Tsubouchi, H. Kumigashira, T. Ohnishi, M. Lippmaa, Y. Matsumoto, H. Koinuma, and M. Oshima, "Trap-controlled space-charge-limited current mechanism in resistance switching at Al/$Pr_{0.7}Ca_{0.3}MnO_3$ interface", *Appl. Phys. Lett.*, **92**, 222113 (2008).

[32] K. Kamiya, M. Y. Yang, S.-G. Park, B. M.-Köpe, Y. Nishi, M. Niwa, and K. Shiraishi, "ON-OFF switching mechanism of resistive–random–access–memories based on the formation and disruption of oxygen vacancy conducting channels", *Appl. Phys. Lett.*, **100**, 073502 (2012).

[33] B. M.-Köpe, S.-G. Park, H.-D. Lee, Y. Nishi, "First principles calculations of oxygen vacancy-ordering effects in resistance change memory materials incorporating binary transition metal oxides", *J. Mater. Sci.*, **47**, 7498–7514 (2012)

[34] K. Kamiya, M. Y. Yang, T. Nagata, S.-G. Park, B. M.-Köpe, T. Chikyow, K. Yamada, M. Niwa, Y. Nishi, and K. Shiraishi, "Generalized mechanism of the resistance switching in binary-oxide-based resistive random-access memories", *Phys. Rev. B.*, **87**, 155201 (2013).

[35] Y. Watanabe, J. G. Bednorz, A. Bietsch, C. Gerber, D. Widmer, A. Beck, and S. J. Wind, "Resistive switching in metal–ferroelectric–metal junctions", *Appl. Phys. Lett.*, **78**, 3738–3740 (2001).

[36] J. R. Contreras, H. Kohlstedt, U. Poppe, R. Waser, C. Buchal and N. A. Pertsev, "Resistive switching in metal–ferroelectric–metal junctions", *Appl. Phys. Lett.*, **83**, 4595–4597 (2003).

[37] Rickard Fors, Sergey I. Khartsev, and Alexander M. Grishin, "Giant resistance switching in metal-insulator-manganite junctions: Evidence for Mott transition", *Phys. Rev. B*, **71**, 045305 (2005).

[38] A. Sawa, "Resistive switching in transition metal oxides", *Mater. Today*, **11**, 28-36 (2008).

[39] Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Kawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Iijima, T. Mikawa, T. Ninomiya, R. Miyanaga, Y. Kawashima, K. Tsuji, A. Himeno, T. Okada, R. Azuma, K. Shimakawa, H. Sugaya, and T. Takagi, R. Yasuhara, K. Horiba, H. Kumigashira, and M. Oshima, "Highly Reliable TaOx ReRAM and Direct Evidence of Redox Reaction Mechanism", IEDM Tech. Dig., pp. 293-296 (2008)

[40] Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, S. Muraoka, S. Mitani, S. Fujii, K.Katayama, T.Ninomiya, and T. Takagi, "Switching Mechanism of TaOx ReRAM", *SSDM Tech. Dig.*, pp1202-1203 (2009).

[41] S. Kim and Y.-K. Choi, "A Comprehensive Study of the Resistive Switching Mechanism in Al/TiOx/TiO2/Al-Structured RRAM", *Electron Devices*, **56**, 3049-3054 (2009).

[42] J. H. Hur, M.-J. Lee, C. B. Lee, Y.-B. Kim, and C.-J. Kim, "Modeling for bipolar resistive memory switching in transition-metal oxides", *Phys. Rev. B*, **82**, 155321 (2010).

[43] B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot and R. Waser, B. Reichenberg, and S. Tiedke, "Resistive switching mechanism of TiO_2 thin films grown by atomic-layer deposition" *J. Appl. Phys.*, **98**, 033715 (2005).

[44] K. M. Kim, B. J. Choi, Y. C. Shin, S. Choi, and C. S. Hwang, “Anode-interface localized filamentary mechanism in resistive switching of TiO_2 thin films”, *Appl. Phys. Lett.*, **91**, 012907 (2007).

[45] K. Kinoshita, T. Tamura, H. Aso, H. Noshiro, C. Yoshida, M.Aoki, Y. Sugiyama and H. Tanaka, “New Model Proposed for Switching Mechanism of ReRAM”, *Non-Volatile Semiconductor Memory Workshop Tech. Dig.*, pp. - (2006).

[46] K. Kinoshita, T. Tamura, M. Aoki, Y. Sugiyama and H. Tanaka, “Bias polarity dependent data retention of resistive random access memory consisting of binary transition metal oxide,” *Appl. Phys. Lett.*, **89**, 103509 (2006).

[47] G.-S. Park, X.-S. Li, D.-C. Kim, R.-J. Jung, M.-J. Lee, and S. Seo, “Observation of electric-field induced Ni filament channels in polycrystalline NiO_x film”, *Appl. Phys. Lett.*, **91**, 222103 (2007).

[48] K. M. Kim, B. J. Choi, Y. C. Shin, S. Choi, and C. S. Hwang, “Anode-interface localized filamentary mechanism in resistive switching of TiO_2 thin films” *Appl. Phys. Lett.*, **91** 012907 (2007).

[49] K. M. Kim, B. J. Choi, and C. S. Hwang, “Localized switching mechanism in resistive switching of atomic-layer-deposited TiO_2 thin films”, *Appl. Phys. Lett.*, **90**, 242906 (2007).

[50] H. D. Lee, B. M.-Köpe, and Y. Nishi, “Model of metallic filament formation and rupture in NiO for unipolar switching”, *Phys. Rev. B*, **81**, 193202 (2010).

[51] J.S. Lee, S.B. Lee, S.H. Chang, L.G. Gao, B.S. Kang, M.-J. Lee, C.J. Kim, T.W. Noh, and B. Kahng, “Scaling Theory for Unipolar Resistance Switching”, *Phys. Rev. Lett.* **105**, 205701 (2010).

[52] G. Bersuker, A. Korkin, L. Fonseca, A. Safonov, A. Bagatur’yants, and H. R. Huff, “The role of localized states in the degradation of thin gate oxides”, *Microelectronic Engineering*, **69**, 118–129 (2003).

[53] M. A. Alam, “A Study of Soft and Hard Breakdown-Part I: Analysis of Statistical Percolation Conductance”, *Electron Devices*, **49**, 232-238 (2002). “A Study of Soft and Hard Breakdown-Part II: Principles of Area, Thickness, and Voltage Scaling”, *Electron Devices*, **49**, 239-246 (2002).

[54] J. Sune, “New physics-based analytic approach to the thin oxide breakdown statistics”, *Elec. Dev. Lett.*, **22**, 296-298 (2001).

[55] E. Wu and J. Sune, “Power-law voltage acceleration: a key element for ultra-thin gate oxide reliability”, *Microelectronics reliability*, **45**, 1809-1834 (2005).

[56] D.-H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X.-S. Li, G.-S. Park, B. Lee, S. Han, M. Kim, and C. S. Hwang, “Atomic structure of conducting nano-filaments in TiO_2 resistive switching memory”, *Nature Nanotechnology*, **5**, 148 (2010).

[57] J. P. Strachan, M. D. Pickett, J. J. Yang, S. Aloni, A. L. David Kilcoyne, G. Medeiros-Ribeiro, and R. Stanley Williams, “Direct identification of the conducting channels in a functioning memristive device”, *Advanced Materials*, **22**, 3573 (2010).

[58] K. Szot M. Rogala, W. Speier, Z. Klusek, A. Beshmehn, and R. Waser, “TiO_2-a prototypical memristive material”, *Nanotechnology*, **22**, 254001 (2011).

[59] F. Miao, J. P. Strachan, J. J. Yang, M. –X. Zhang, I. Goldfarb, A. C. Torrezan, P. Eschbach, R. D. Kelley, G. Medeiros-Ribeiro, and R. S. Williams, "Anatomy of a Nanoscale Conduction Channel Reveals the Mechanism of a High-Performance Memristor", *Advanced Materials*, **23**, 5633 (2011).

[60] D. C. Kim, S. Seo, et al., "Electrical observations of filamentary conductions for the resistive memory switching in NiO films", *Appl. Phys. Lett.*, **88**, 202102 (2006).

[61] H. Shima, F. Takano, H. Akinaga, Y. Tamai, I. H. Inoue, H. Takagi, "Resistance switching in the metal deficient-type oxides: NiO and CoO", *Appl. Phys. Lett.*, **91**, 012901 (2007).

[62] Y. Sato, K. Kinoshita, M. Aoki, and Y. Sugiyama, "Consideration of switching mechanism of binary metal oxide resistive junctions using a thermal reaction model", *Appl. Phys. Lett.*, **90**, 033503 (2007)

[63] U. Russo, D. Jelmini, C. Cagli, A. L. Lacaita, S. Spigat, C. Wiemert, M. Peregot and M. Fanciullit, "Conductive-filament switching analysis and self-accelerated thermal dissolution model for reset in NiO-based RRAM", *IEDM Tech. Dig.*, pp.775-778 (2007)

[64] C. Cagli, D. Ielmini, F. Nardi and A. L. Lacaita, "Evidence for threshold switching in the set process of NiO-based RRAM and physical modeling for set, reset, retention and disturb prediction", *IEDM Tech. Dig.*, pp.301-304 (2008).

[65] C. Cagli, F. Nardi, and D. Ielmini, "Modeling of Set/Reset Operations in NiO-Based Resistive-Switching Memory Devices", *Electron Devices*, **56**, 1712-1720 (2009).

[66] R. Degraeve, P.H. Roussel, L. Goux, D. Wouters, J. Kittl, L. Altimime, M. Jurczak, and G. Groeseneken, "Generic learning of TDDB applied to RRAM for improved understanding of conduction and switching mechanism through multiple filaments", *IEDM Tech. Dig.*, pp. 633-636 (2010).

[67] M. A. Alam, "Statistically independent soft-breakdown redefine oxide reliability specifications", *IEDM Tech. Dig.*, pp. 151-154 (2002).

[68] K. Kinoshita, T. Tamura, M. Aoki, Y. Sugiyama and H. Tanaka, "Lowering the Switching Current of Resistance Random Access Memory Using a Hetero Junction Structure Consisting of Transition Metal Oxides", *Jpn. J. Appl. Phys.*, **45**, L991–L994 (2006).

[69] C. Rohde, B. J. Choi, D. S. Jeong, S. Choi, J.-S. Zhao, and C. S. Hwang, "Identification of a determining parameter for resistive switching of TiO_2 thin films", *Appl. Phys. Lett.*, **86**, 262907 (2005).

[70] K. Kinoshita, T. Tamura, M. Aoki, Y. Sugiyama and H. Tanaka, "Lowering the Switching Current of Resistance Random Access Memory Using a Hetero Junction Structure Consisting of Transition Metal Oxides", *Jpn. J. Appl. Phys.*, **45**, L991-994 (2006).

[71] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, and Y. Sugiyama, "Reduction in the reset current in a resistive random access memory consisting of NiOx brought about by reducing a parasitic capacitance", *Appl. Phys. Lett.*, **93**, 033506 (2008).

[72] H. Shima, F. Takano, H. Muramatsu, H. Akinaga, Y. Tamai, I. H. Inoue, and H. Takagi, "Voltage polarity dependent low-power and high-speed resistance switching in CoO resistance random access memory with Ta electrode", *Appl. Phys. Lett.*, **93**, 113504 (2008).

[73] K. M. Kim, B. J. Choi, B. W. Koo, S. Choi, D. S. Jeong, and C. S. Hwang, "Resistive Switching in Pt/Al_2O_3/TiO_2/Ru Stacked Structures", *Electrochemical and solid-state Letters*, **9**, G343-G346 (2006).

[74] M. Terai, S. Kotsuji, H. Hada, N. Iguchi, T. Ichihashi, and S. Fujieda, "Effect of ReRAM-Stack Asymmetry on Read Disturb Immunity", *IRPS Tech. Dig.*, pp. 134-138 (2009).

[75] In the early papers [70], they reported that the RESET phenomenon was observed only at the voltage with polarity opposite to the SET voltage like a bipolar operation. Later, however, it became clear that unipolar operation in either polarity is also possible as long as sufficient current is supplied in RESET operation (see Figure 2-8(b)).

Chapter 2. Experimental

In this chapter, experimental techniques and methods are described. At first, formation methods of stoichiometric TMO layers, which is important to achieve the filamentary switching, are explained. After that, device structure and switching operation method are shown briefly. Finally, measurement systems and evaluated samples are summarized.

2-1 Ta_2O_5/TiO_2 stacked memory cell

Tantalum oxide (Ta_2O_5)/Titanium oxide (TiO_2) stacked memory cells, the concept of which was proposed by M. Terai et al. [1, 2], were used for our study. When the stacked structure is operated as the filamentary switching device, the Ta_2O_5 layer and the TiO_2 layer are expected to act as the stable layer and the switching layer, respectively [1]. As we wrote in section 1-2, the non-stoichiometric TaO_x and TiO_x show another type, i.e., the interface type resistance change [3, 4]. So, stoichiometric composition for both layers is very important to achieve the filament type memory cell (Figure 2-1(a)). In this study, we optimized the deposition process conditions for achieving stoichiometric composition. The results of composition and crystallinity characterization of both layers are given in this section. The cell integration and process optimization were done on 8-inch processing R&D line at Device platforms research laboratory of NEC Corporation.

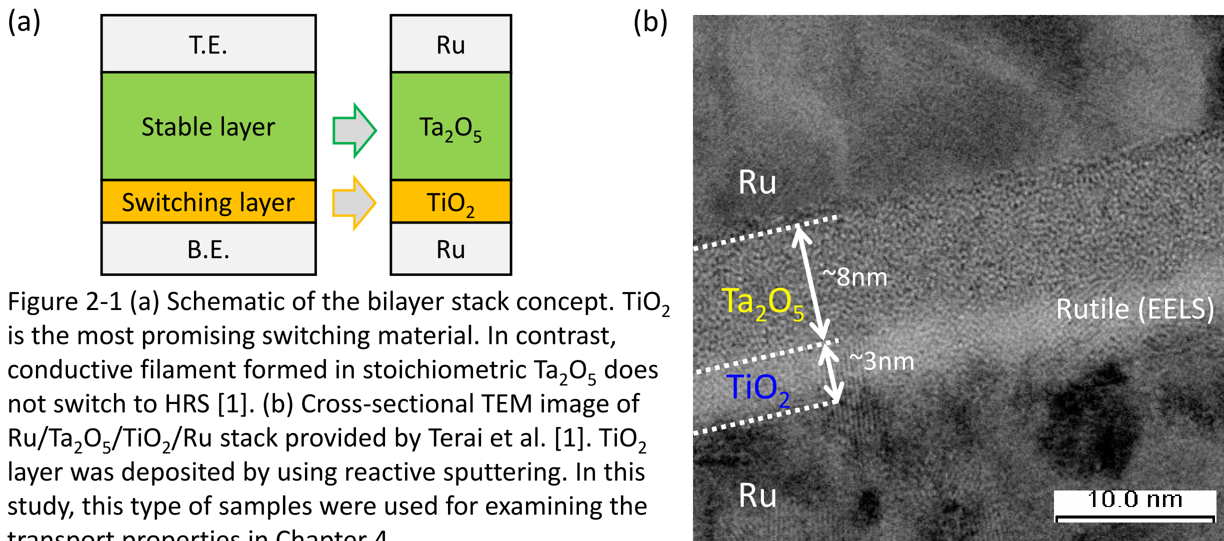

Figure 2-1 (a) Schematic of the bilayer stack concept. TiO_2 is the most promising switching material. In contrast, conductive filament formed in stoichiometric Ta_2O_5 does not switch to HRS [1]. (b) Cross-sectional TEM image of $Ru/Ta_2O_5/TiO_2/Ru$ stack provided by Terai et al. [1]. TiO_2 layer was deposited by using reactive sputtering. In this study, this type of samples were used for examining the transport properties in Chapter 4.

i TiO_2 layer

In reference 1, Terai et al. used a reactive sputtering method to make TiO_2 layer on bottom electrode. The deposited TiO_2 they obtained is polycrystalline with rutile structure, which was confirmed by the electron diffraction and the electron energy loss spectroscopy (EELS) [1], and the grain size is larger than TiO_2 layer thickness as shown in the Figure 2-1(b). This means that grain

boundaries penetrate the layer. As it is widely accepted that grain boundaries behave high mobility path for oxygen ion, unintended degradation of the resistive state can easily occur in such films [5].

In our study, we chose an alternative method to form the TiO_2 layer on bottom electrode, that is, deposition of thin titanium film followed by the oxidation [2].

At first, the ruthenium bottom electrode 20 nm thick was sputtered on a Si substrate. Then, thin titanium layer was deposited physically on bottom electrode by sputtering a titanium target. Deposition rate was about 0.04 nm/sec, that was evaluated from process time for thicker film formation as shown in Figure 2-2(a). Continuous thin film was obtained with low Ar-gas flow (20 sccm) and dc-power (0.5 kW) conditions at room temperature.

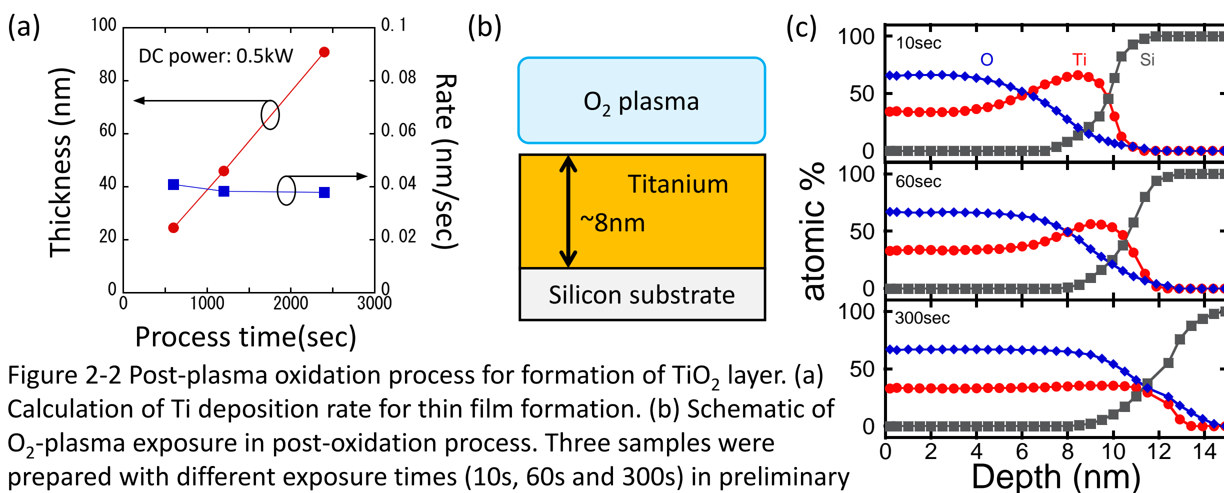

Figure 2-2 Post-plasma oxidation process for formation of TiO_2 layer. (a) Calculation of Ti deposition rate for thin film formation. (b) Schematic of O_2-plasma exposure in post-oxidation process. Three samples were prepared with different exposure times (10s, 60s and 300s) in preliminary experiment. (c) Depth profile of TiO_2 composition which was investigated by RBS technique.

Post-oxidation was done by using plasma-enhanced method at 250 degrees C. In order to get stoichiometric TiO_2, we made preliminary experiments, and optimum O_2-plasma exposure time was determined with fixed dc-power and O_2-gas flow (2800sccm). Three sample were prepared with different exposure times (10 s, 60 s and 300 s) to 8nm-thickness titanium film on silicon substrate as shown in Figure 2-2(b), and the depth profile of TiO_2 composition was investigated by High Resolution Rutherford Backscattering Spectrometry (HR-RBS). The results are shown in Figure 2-2(c). Atomic O/Ti ratio near the surface is almost 2, which means that TiO_2 layer was formed at the surface by O_2-plasma exposure. The TiO_2 layer thickness increased with the exposure time, and after 300 s exposure TiO_2 layer reached 8nm thick, which means that 5 nm-titanium region from the surface was fully oxidized in this case.

Stoichiometry of O_2-plasma exposed 5 nm-titanium on ruthenium was investigated by X-ray photoelectron spectroscopy (XPS). Figure 2-3(a) shows the spectrum near the Ti-2P peaks. We found that Ti-2p peaks was shifted to higher binding energy by the O_2-plasma exposure. Position of the peaks is similar to that of reactive sputtered TiO_2. The difference between plasma-oxidized TiO_2 and reactive-sputtered TiO_2 is existence of small shoulder near 457eV. This means that TiO_{2-x} exists

in interface between fully oxidized TiO_2 layer and ruthenium bottom electrode when O_2-plasma exposure time is not long enough.

It should be noted that surplus longer exposure time also causes oxidation of the ruthenium bottom electrode. Figure 2-3(c) shows XPS spectrum near the Ru-3d peak from the O_2-plasma exposed sample which was processed to 2 nm-thick titanium film on ruthenium bottom electrode. Additional peaks caused by forming RuO_2 to the interface between TiO_2 layer and ruthenium bottom electrode were observed in case with longer process time condition than 1 min.

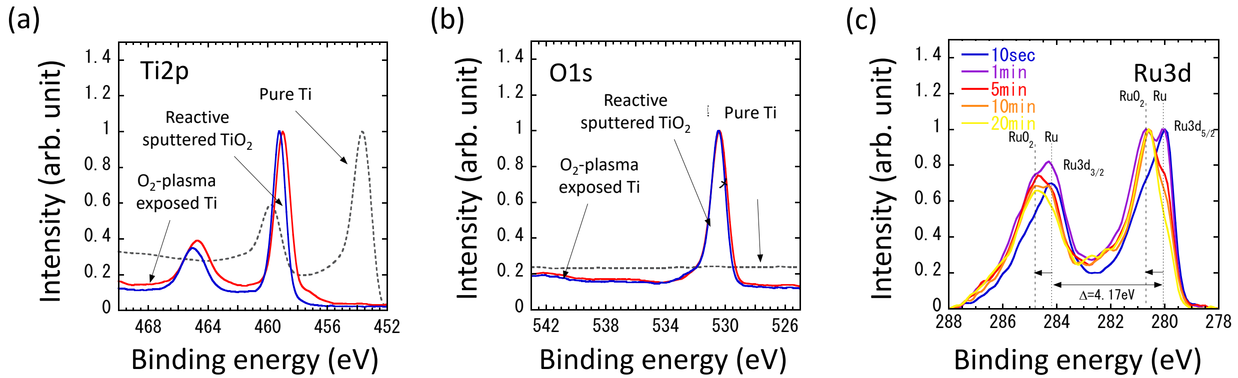

Figure 2-3 XPS spectra from O_2-plasma exposed 5nm-titanium on ruthenium [2] (a) Spectrum near the Ti-2p peaks (Red solid line: O_2-plasma exposed titanium, Blue solid line: Reactive sputtered TiO_2, Black dashed line: Pure titanium). (b) Spectrum near the O-1s peak. (c) Spectra near the Ru-3d peaks. The spectra is different in the oxidation time.

ii Ta_2O_5 layer

Ta_2O_5 layer was deposited on TiO_2 layer by RF sputtering using Ta_2O_5 target. Process conditions such as Ar/O_2 flow ratio and temperature were tuned for achieving isolative Ta_2O_5.

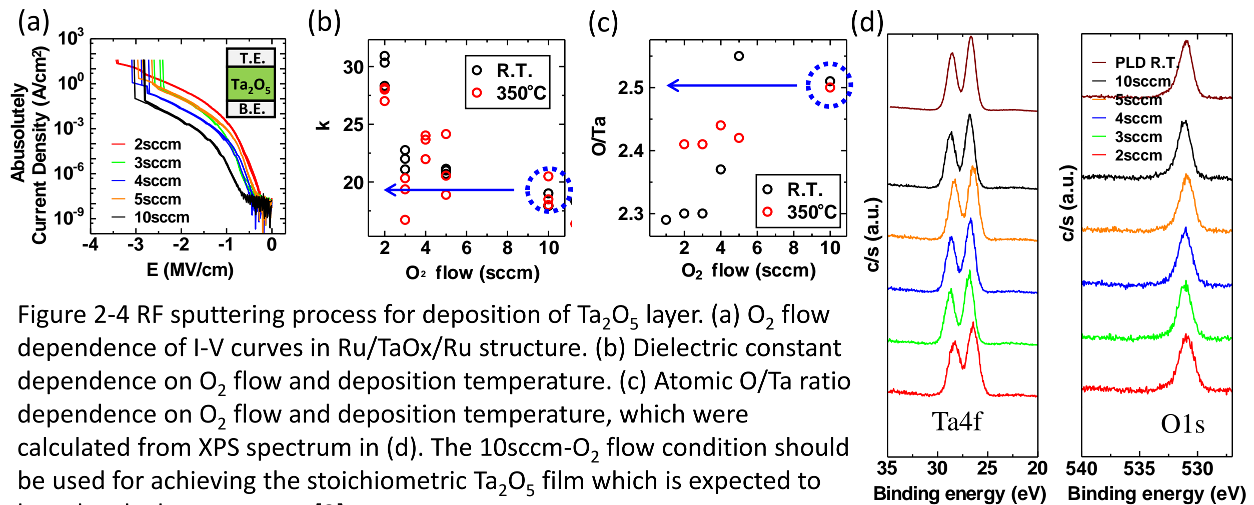

Figure 2-4 RF sputtering process for deposition of Ta_2O_5 layer. (a) O_2 flow dependence of I-V curves in Ru/TaOx/Ru structure. (b) Dielectric constant dependence on O_2 flow and deposition temperature. (c) Atomic O/Ta ratio dependence on O_2 flow and deposition temperature, which were calculated from XPS spectrum in (d). The 10sccm-O_2 flow condition should be used for achieving the stoichiometric Ta_2O_5 film which is expected to have low leakage property[3].

Figure 2-4(a) shows the leakage current as a function of the applied electric field for five films made at different O_2 flow rates. We understand that high oxygen flow rate gives preferable isolation. We also measured the dielectric constant and XPS spectrum of the films, from which atomic O/Ta ratio was determined (Figure 2-4(b) ~ (d)). We found desirable parameters were obtained with small cell-to-cell variation in higher oxygen flow condition. From these results, we decided the Ar/O_2 flow ratio to 40/10sccm with 2.0kW-rf-power. The temperature was aligned to maximum temperature in the integration process (350 degrees C). Deposition rate of Ta_2O_5 is about 0.15nm/sec.

2-２ Device structure and switching operation

Based on the conductions obtained in the previous section, we fabricated $Ru/Ta_2O_5/TiO_2/Ru$ stacked memory devices. Control of current through the memory cell at the switching operations is very important to achieve reproducible switching in the filamentary switching device [6], and we employed 1T-1R type device structure mentioned in section 1-3. In this section, we show the structure of the integrated 1T-1R memory device at first. After that, operation methods of 1T-1R type device are described for both unipolar and bipolar switching.

ｉ Memory cell integration to 1T-1R type device

$Ru/Ta_2O_5/TiO_2/Ru$ stacked memory cell was integrated to the 1T-1R type devices on 6-inch wafer with conventional 0.35um-node CMOS process. An n-channel field-effect transistor (n-FET) is incorporated in series with a memory cell. Cross-sectional schematic of the device is shown in Figure 2-5(a) [1, 2]. Memory cell was placed directly on the drain contact to reduce the parasitic capacitance. Effective memory cell size is defined by top electrode area.

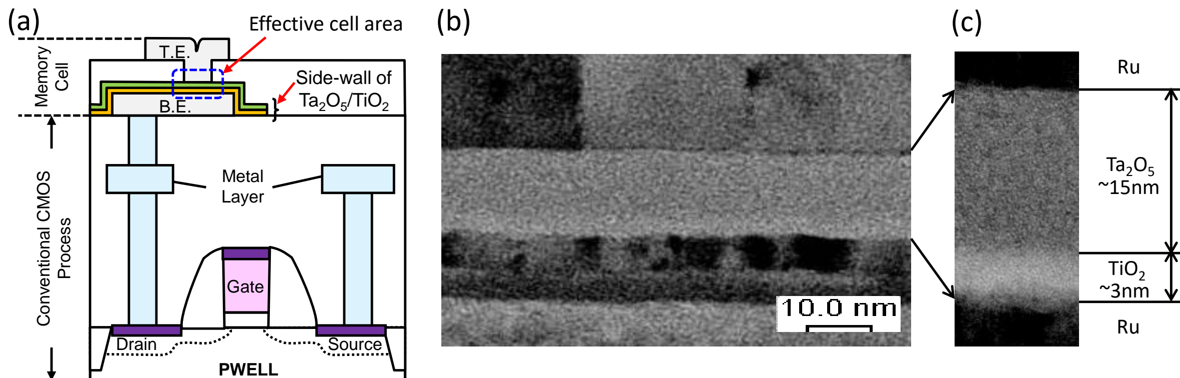

Figure 2-5 (a) Cross-sectional schematic of integrated 1T-1R device. Memory cell module was placed just above drain contact for reducing the parasitic capacitance. Effective memory cell size is defined by the top electrode area. (b) Cross-sectional TEM image of $Ru/Ta_2O_5/TiO_2/Ru$ stacked memory cell. (c) Magnified TEM image shows that both Ta_2O_5 layer and TiO_2 layer are amorphous.

Cross-sectional TEM image of the memory cell is shown in Figure 2-5(b) and (c). It is composed of a ruthenium bottom electrode (BE), a 3nm-thick titanium oxide layer (TiO_2), a 15nm-thick tantalum

oxide layer (Ta_2O_5), and a ruthenium top electrode (TE). The TiO_2 layer was formed by oxidizing 2nm-thick titanium metal by O_2-plasma. The maximum temperature in memory cell integration process is sufficiently lower than the crystallization temperature of Ta_2O_5 and TiO_2 [2], and we ascertain the both layers are amorphous.

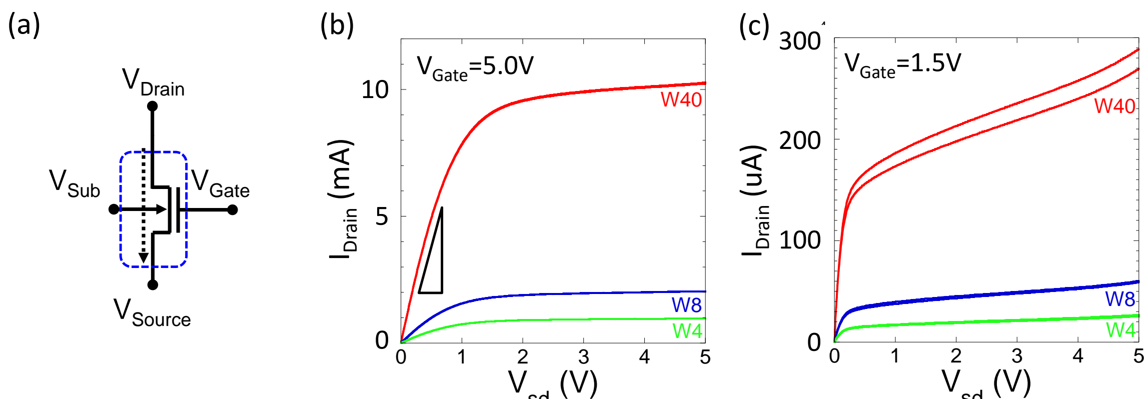

Figure 2-6 (a) Schematic of the n-FET. In the 1T-1R type devices, the drain terminal is connected to the the bottom electrode of the memory cell as shown in the Figure 2-5 (a). (b) Drain current dependence on bias voltage between source and drain with some channel width variations in case of $V_{Gate} = 5.0\text{V}$. (c) Drain current dependence on bias voltage between source and drain with some channel width variations in case of $V_{Gate} = 1.5\text{V}$.

Figure 2-6(b) and (c) show the electrical characteristics of the integrated transistors. Drain current as a function of bias voltage between source and drain is given for three devices with different channel width (W). The saturation current and the ON-conductance is proportional to the channel width as summarized in Table 2-1. As we will see in the next chapter, RESET characteristics and apparent LRS resistance are influenced by the ON-resistance of the FET. Thus, we have to consider the effects in analysis of the resistance change parameters.

Table 2-1 Device parameters of series transistors

Name	W(um)	Saturation current @Vg=5.0V	ON-resistance @Vg=5.0V	Saturation current @Vg=1.5V	Series resistance in 1T-1R type device
T1	4	1mA	1000Ω	30μA	
T2	8	2mA	500Ω	60μA	~28Ω
T3	40	10mA	100Ω	300μA	

Note: These values come from transistor only devices. Series resistance in 1T-1R type device is estimated by adding contact resistance to the ON-resistance.

ii Unipolar and bipolar switching operation

The $Ru/Ta_2O_5/TiO_2/Ru$ stacked memory cell is a unipolar-type device, and basically it works in either polarity of voltage. As for our 1T-1R device, however, FORMING and SET operations must be done with positive bias, i.e., to apply a positive voltage to the top Ru electrode while the source of the

FET being grounded. In this case, the current flowing the cell is kept smaller than the saturation current of the FET even after the sudden resistance drop takes place. If we apply negative voltage to the top electrode, however, a larger current can flow directly from the Si substrate, because it is grounded to stabilize the FET characteristics (see Figure 2-7(b)).

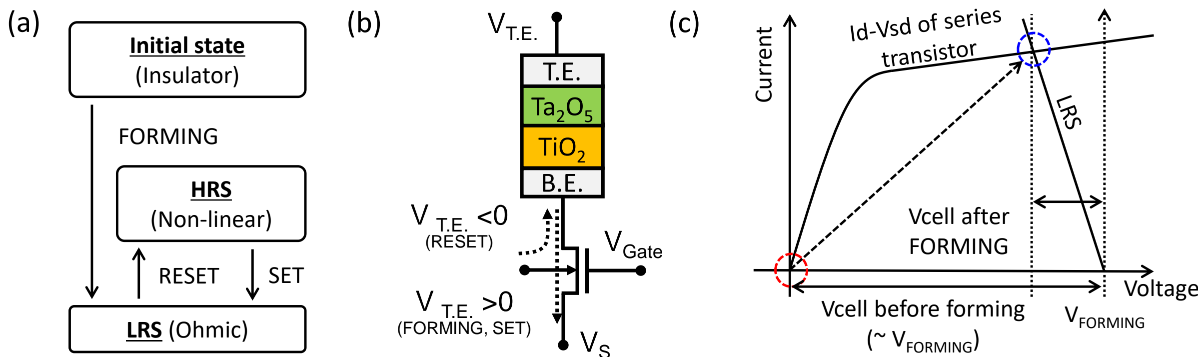

Figure 2-7 (a) Switching operation flow. (b) Schematic of 1T-1R type device configuration. Current compliance is possible only in positive drain bias condition. Drain current includes the current from the substrate in negative drain bias condition. (c) Schematic load curve of 1T-1R type device at FORMING and SET operations.

In our early experiments [1], we did the measurement by bipolar operation. Figure 2-8(a) shows an example of the bipolar operation with dc sweep method. Black solid line shows the FORMING: applying positive voltage to the top electrode causes the resistance of the memory cell to decrease suddenly at around 4 V. At this time, the current flowing the cell is bounded by the saturation current of the FET. Black dashed line shows the RESET: applying negative voltage to the top electrode causes the resistance of the memory cell to increase suddenly at around 1 V. This high resistive state defines the “off-state” or “high resistance state (HRS)”. Blue solid line shows the SET: applying positive voltage to the top electrode caused the resistance of the memory cell to decrease suddenly at around 3 V. At this time, current is limited by FET in common with the FORMING operation. This low resistive state defines the “on-state” or “low resistance state (LRS)”. The limit current in FORMING and SET operation is called the “compliance current”. The compliance current is controllable by the gate voltage.

In this research, we mainly used the unipolar operation. Figure 2-8(b) shows an example of the unipolar operation with dc sweep method. Black solid line shows the FORMING: applying positive voltage causes a sudden resistance drop at around 4 V. After that, the current is limited to the compliance current. Black dashed line shows the RESET: applying positive voltage to the top electrode with Vg=5V causes a jump to the HRS at around 1 V. Generally, in RESET operation we have to apply the current larger than the compliance current at SET operation. To do this, we set the gate voltage at Vg = 5 V, where the saturation current of the FET is much higher than compliance current at SET. Blue solid line shows the SET: applying positive voltage caused a jump to the LRS at around 3 V. The compliance current is an important control parameter.

Figure 2-8(c) shows compliance current dependence of LRS conductance in our 1T-1R type devices. LRS conductance can be changed by the compliance current. This means that the compliance current can control the conductance of single conductive filament formed in the Ta_2O_5/TiO_2 stacked cell. By using this controlling method, we investigate resistance change characteristics dependence on the LRS conductance in Chapter 3.

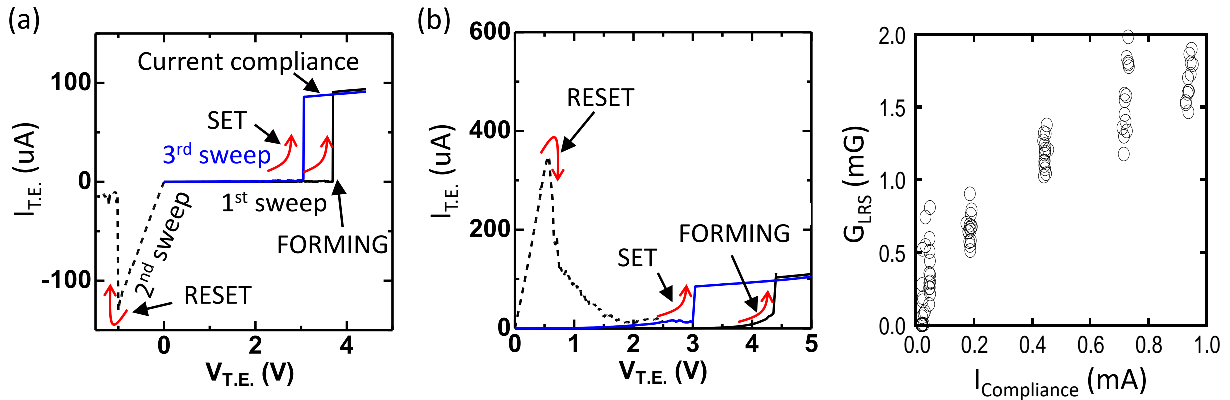

Figure 2-8 (a) Example of bipolar switching operation. (b) Example of unipolar switching operation. (c) Compliance current dependence of LRS conductance.

2-３ Measurement setup and Samples

In this section, the evaluation environments and the samples are described.

ⅰ Evaluation systems and measurement setup

Three type of measurement systems were used in this study.

Single cell level evaluations at and above the room temperature were done on a wafer by semi-automatic probing system (S300, CascadeMicrotech) with semiconductor parametric analyzer (4156C, Agilent). A heater installed in the wafer stage enabled the sample temperature to be varied from 300K–400K. Switching phenomena and basic electrical properties of the memory cells were investigated by this system.

Single cell level evaluations at low temperature were done on a diced chip which was mounted on cryogenic system. Cryogenic system (Oxford) consists of a low boil-off helium cryostat with a liquid nitrogen reservoir and a variable temperature insert (VTI). A heat exchange coil at the base of the VTI tail controls the temperature in the VTI. A heater installed on the heat exchanger enables the sample temperature to be varied from 2.0–300 K.

For the measurement at low temperatures, we used a special 1T-1R type device which has middle terminal on the node between the n-FET and the memory cell as shown in Figure 2-8(b). This configuration satisfies two necessary conditions: to control the current through the memory cell in the switching operation (Figure 2-8(c)), and to measure just the electrical properties of the memory cell free from that of transistor (Figure 2-8(d)). In this study, digital multimeters (34401A, Agilent)

and semiconductor parametric analyzer (4156C, Agilent) were used. It is noted that controllability of the current through the memory cell is poor in this special 1T-1R type device, because this device has large parasitic capacitance associated with the middle terminal. When we want to control the LRS resistance, normal 1T-1R device should be used (Figure 2-8(a)).

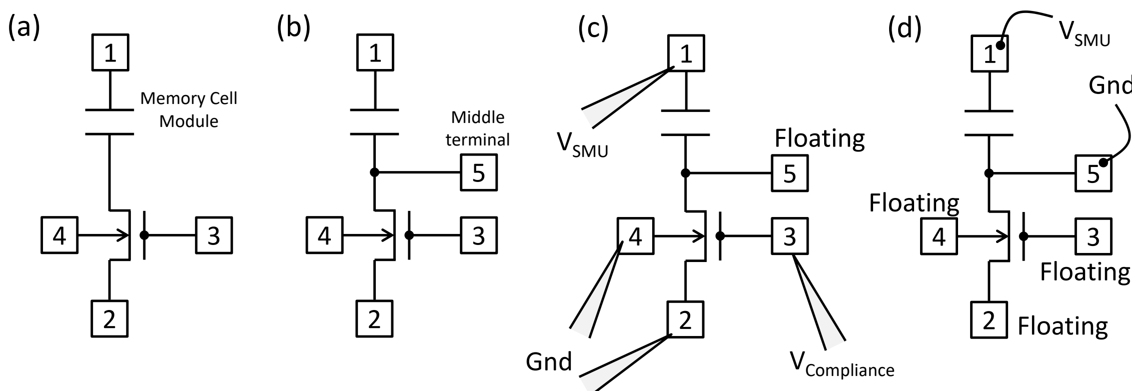

Figure 2-9 (a) Normal 1T-1R device. (b) Special 1T-1R device. Additional middle terminal is connected to the node between memory cell and transistor. (c) Bias condition for switching operation in special 1T-1R device on the "Cascade prober". Middle electrode is not biased. This configuration was used in preparation of states for detail memory cell evaluation at low temperatures. (d) Bias condition for detail memory cell evaluation at low temperatures. The samples are mounted on a cryogenic system with gold wire bonding. Middle terminal(Pad #5) is connected to GND.

Array level evaluation was done by using 1kbits-memory array on chip. This array has decoder for addressing to single 1T-1R cell. External voltage sources and a pulse-generators (Agilent81110C) were used for demonstration of high robust non-volatile memory [6]. Details are shown in Chapter 5.

ii Samples

We prepared two kinds of samples. In the first-group, TiO_2 layer were deposited by the reactive ion sputtering method which is conventional method Terai et al. used [1], while in the second-group,TiO_2 layer were fabricated with the post-plasma oxidation method [2, 7]. Details of the process conditions and list of samples with structural information for each group are given in table 2-2(a), (b) and 2-3(a), (b).

Table 2-2(a) Process conditions for first-group samples

Table 2-1	Bottom electrode		TiO_2	Ta_2O_5	Top electrode
Target	Pt	Ru	Ti	Ta_2O_5	Ru
Power	(dc)	0.5kW(dc)	0.2kW(dc)	2.0kW(rf)	0.05kW(dc)
Gas flow		Ar=40sccm	Ar/O2=46/4sccm	Ar/O2=40/5sccm	Ar=50sccm
Pressure		-	-	-	0.1Pa
Temperature		300C	300C	350C	RT
Deposition rate		0.81nm/sec	0.38nm/sec	0.154nm/sec	0.01nm/sec
Tool	1060	1060	1060	1060	C7100

Note: TiO_2 layer is formed by the reactive sputtering method.

Table 2-2(b) List of the first-group samples

Name	Wf-ID	Bottom electrode	Switching layer	Stable layer	Top electrode
A1	-	Pt	p-TiO_2 (3nm)	-	Ru
A2	-	Pt	-	a-Ta_2O_5 (10nm)	Ru
A3	-	Pt	p-TiO_2 (3nm)	a-Ta_2O_5 (10nm)	Ru
A4	-	Ru	p-TiO_2 (3nm)	a-Ta_2O_5 (10nm)	Ru
A5	-	Ru	p-TiO_2 (6nm)	a-Ta_2O_5 (10nm)	Ru
A6	-	Ru	p-TiO_2 (3nm)	a-Ta_2O_5 (14nm)	Ru

Note: Ta_2O_5 layer is amorphous with high stoichiometric composition. TiO_2 layer is polycrystalline (rutile) with high stoichiometric composition.

Table 2-3(a) Process conditions for second-group samples

	Bottom electrode	Ti	Ta_2O_5	Top electrode
Target	Ru	Ti	Ta_2O_5	Ru
Power	0.5kW(dc)	0.2kW(dc)	2.0kW(rf)	0.05kW(dc)
Gas flow	Ar=40sccm	Ar=50sccm	Ar/O2=40/5sccm	Ar=50sccm
Pressure	-	-	-	0.1Pa
Temperature	300C	300C	350C	RT
Deposition rate	0.81nm/sec	0.38nm/sec	0.154nm/sec	0.01nm/sec
Tool	1060	1060	1060	C7100

Note: TiO_2 layer is formed by applying post-plasma oxidation to thin Ti layer on bottom electrode.

Table 2-3(b) List of the second-group samples

Name	Wf-ID	Bottom electrode	Ti	Plasma Oxidation	Ta_2O_5	Top electrode
B1	ID24	Ru (5nm or 20nm)	5nm	5min@2kW, 250C	15nm	Ru (20nm)
B2	ID27	Ru (5nm or 20nm)	2nm	1min@2kW 250C	15nm	Ru (20nm)
B3	ID25	Ru (5nm or 20nm)	2nm	5min@2kW, 250C	15nm	Ru (20nm)
B4	ID21	Ru (5nm or 20nm)	2nm	10min@2kW 250C	15nm	Ru (20nm)

Note: Both of Ta_2O_5 layer and TiO_2 layer are amorphous with high stoichiometric composition. B3- and B4-samples have a RuO_2 layer in the interface between TiO_2 and ruthenium bottom electrode.

2-４ Reference

[1] M. Terai, S. Kotsuji, H. Hada, N. Iguchi, T. Ichihashi, and S. Fujieda, “Effect of ReRAM-Stack Asymmetry on Read Disturb Immunity”, *IRPS Tech. Dig.*, pp. 134-138 (2009).

[2] Y. Sakotsubo, M. Terai, M. Tada, Y. Yabe, and Y. Saito, “SEMICONDUCTOR DEVICE WITH VARIABLE RESISTANCE ELEMENT AND METHOD FOR MANUFACTURING THE SAME”, US 8,766,233 (2014).

[3] Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Kawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Iijima, T. Mikawa, T. Ninomiya, R. Miyanaga, Y. Kawashima, K. Tsuji, A. Himeno, T. Okada, R. Azuma, K. Shimakawa, H. Sugaya, and T. Takagi, R. Yasuhara, K. Horiba, H. Kumigashira, and M. Oshima, “Highly Reliable TaOx ReRAM and Direct Evidence of Redox Reaction Mechanism”, *IEDM Tech. Dig.*, pp. 293-296 (2008).

[4] S. Kim and Y.-K. Choi, “A Comprehensive Study of the Resistive Switching Mechanism in Al/TiOx/TiO2/Al-Structured RRAM”, *Electron Devices*, **56**, 3049-3054 (2009).

[5] G.-S. Park, X.-S. Li, D.-C. Kim, R.-J. Jung, M.-J. Lee, and S. Seo, “Observation of electric-field induced Ni filament channels in polycrystalline NiO_x film”, *Appl. Phys. Lett.*, **91**, 222103 (2007).

[6] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, and Y. Sugiyama, “Reduction in the reset current in a resistive random access memory consisting of NiOx brought about by reducing a parasitic capacitance”, *Appl. Phys. Lett.*, **93**, 033506 (2008).

[7] Y. Sakotsubo, M. Terai, S. Kotsuji, Y. Saito, M. Tada, Y. Yabe, and H Hada, "A New Approach for Improving Operating Margin of Unipolar ReRAM using Local Minimum of Reset Voltage", *2010 Symposium on VLSI (VLSI-8-2), Tech. Dig.*, pp. 87-88 (2010)

Chapter 3. Filamentary resistance change phenomenon in Ta_2O_5/TiO_2 stacked structure

The Ru/Ta_2O_5/TiO_2/Ru stacked structure was proposed as resistance change devices by M. Terai et al. in 2008 [1]. This device needs the FORMING operation at first [Fig. 3-1(a)]. The resistance is changed to the LRS from the initial insulating state by the FORMING operation, which is due to the formation of conductive filament in the Ta_2O_5/TiO_2 layers. by the FORMING operation. The conductive filament formed in the Ta_2O_5 layer is believed to be un-switchable stable filament because single Ta_2O_5 layer never shows the switching properties [1]. In the early papers [1], they reported that the RESET phenomenon was observed only at the voltage with polarity opposite to the SET voltage like a bipolar operation. Later, however, it became clear that unipolar operation in either polarity is also possible as long as sufficient current is supplied in RESET operation as shown in Figure 3-1(b).

Terai et al. speculated that the resistance change phenomenon is based on the redox reaction [1]. However, this speculation contradicts the fact that unipolar switching operation is possible in the Ta_2O_5/TiO_2 stacked structure. We expected that the resistance change phenomenon is based on the thermal reaction in filamentary conductive path in the TiO_2 layer.

In this chapter, we characterize the resistance change phenomena such as FORMING, RESET, and SET in the Ta_2O_5/TiO_2 stacked structure with three states including initial state, low resistance state (LRS), and high resistance state (HRS). At first, we investigate structural and temperature dependence of initial leakage current and FORMING voltage in pristine Ta_2O_5/TiO_2 stacked structure, and reveal the principle governing the FORMING phenomenon. After that, we investigate the correlation between LRS/HRS and RESET/SET phenomenon, then we give another thought to the nature of resistance change phenomenon in the Ta_2O_5/TiO_2 stacked structure.

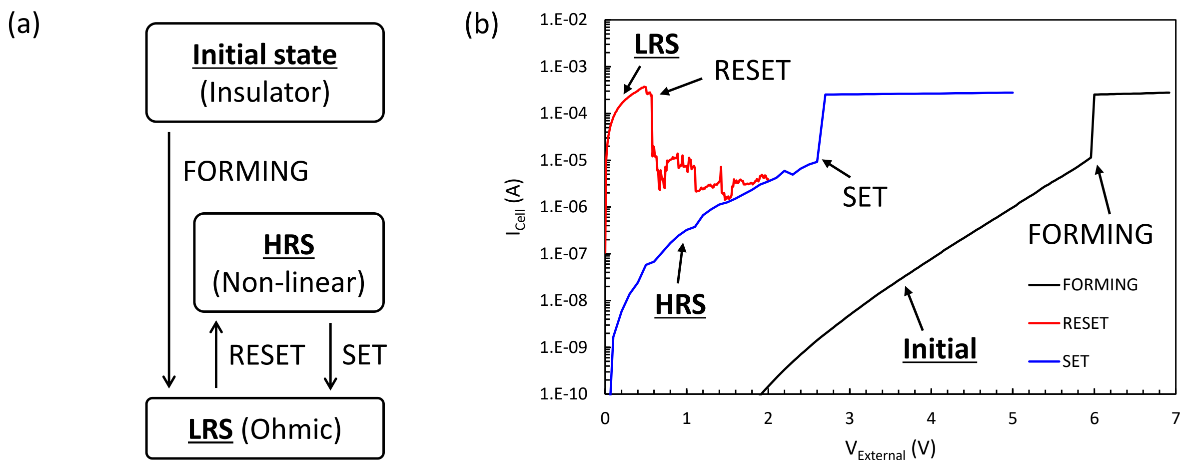

Figure 3-1 (a) Switching operation flow. (b) I-V characteristics including three states (Initial, LRS, and HRS) and three switching phenomena (FORMING, RESET, and SET). The data were plotted with semi-logarithm scale.

The samples used in this study were fabricated using the same equipment ant prototype line as Terai et al. [1]. Therefore, the film quality of Ta_2O_5, which is an important factor of this structure, is the same as that of Terai et al. All the electrical properties were obtained on the 1T-1R type devices. So, device parameters such as RESET voltage and LRS conductance include the influence of the series transistor and interconnect. The switching parameters intrinsic to the stack cell can be extracted by subtracting their contribution [Table 2-1].

3-１ I-V characteristics of pristine film and FORMING phenomenon

Figure 3-2(a) shows *I-V* characteristics of a pristine Ta_2O_5(10nm)/TiO_2(3nm)stacked structure. The *I-V* curves include two major features. One is exponential current increase with applied voltage in relatively low voltage region, and the other one is an abrupt current increase at applying relatively high voltage, that is, the electro-forming.

In general, an initial leakage current of the resistance change devices is proportional to the cell area. The leakage current in Metal/Ta_2O_5/Metal (MIM) capacitors has been studied extensively [11-18], and there have been examined several conduction models, which include the space-charge-limited conduction [19, 20], the *Fowler-Nordheim* (*F.-N.*) tunneling [21, 22], the *Poole-Frenkel* (*P.-F.*) emission [23] and so on. The exponential voltage dependence in Figure 3-2(a) indicates that the *P.-F.* emission is a plausible model for the conduction of the initial state [11, 13]. In this model, the conduction is limited by the excitation from the electron trap, the potential barrier of which is lowered in strong electric field.

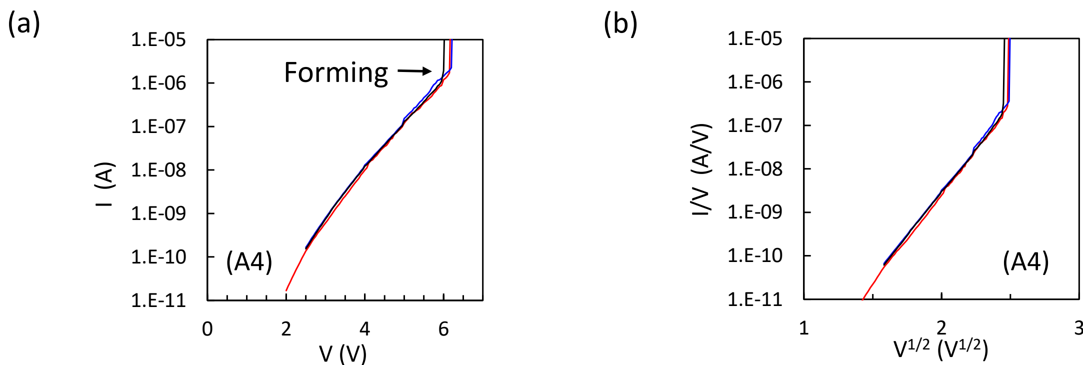

Figure 3-2 (a) I-V characteristic of pristine Ru/Ta_2O_5 (10nm)/TiO_2 (3nm)/Ru stacks. (b) P.-F. plot of the I-V characteristic, re-plotted from the data between 2 V and 6 V in (a).

The following formulas give the relationships between current density (J) and electrical field (E_i) in the *P.-F.* conduction for simple MIM system [23]:

$$J = \sigma_0 E exp\left(-\frac{\phi_t - \sqrt{qE_i/\pi\varepsilon_i}}{k_B T}\right), \qquad (3-1)$$

$$E_i = \frac{V_i}{d_i}, \qquad (3-2)$$

where σ_0 is a prefactor, ϕ_t is the activation energy, ε_i is the dielectric constant, q is the electrical charge, and k_B is the Boltzmann constant.

Figure 3-2(b) shows a *P.-F.* plot of the *I-V* characteristic replotted from the data between 2.0 and 6.0 V in the Fig. 3-2(a). The slope of the linear part of the plot is related to the dielectric constant of the insulator material in this model.

According to Equ. 3-1, the current shows thermal-activation dependence. To confirm it, we measured the *I-V* characteristics of sample A6 at 25, 85 and 150 degrees C. Figure 3-3(a) shows the results. The current increases with temperature, and is consistent with the theory as shown in Figure 3-3(b). The activation energy obtained from *Arrhenius* plot shown in Figure 3-3(c) where the value obtained by extrapolating the slope of the linear part of the *P.-F.* plot [Fig. 3-3(b)] are replotted versus inverse temperature is about 0.29 eV. This value corresponds to the energy level of impurities or defects induced trap states below the conduction band of Ta_2O_5 [16, 17].

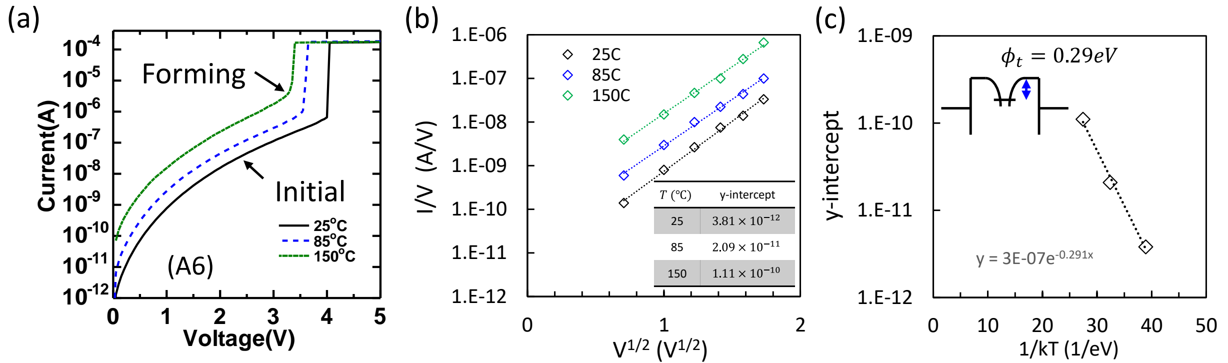

Figure 3-3 (a) Temperature dependence (25℃, 85℃, 150℃) of I-V characteristic of pristine Ru/Ta_2O_5 (14nm)/TiO_2 (3nm)/Ru stacks (A6). Cell size is 1μm x 1μm. (b) P.-F. plot of the I-V characteristic, re-plotted from the data between 0.5 and 3 V in the Fig. 3-2 (a). (c) Arrhenius plot of the y-intercept in the Fig. 3-2 (b). Activation energy is about 0.29eV from this plot.

Figure 3-4(a) shows *I-V* characteristics of pristine Ru/Ta_2O_5/TiO_2/Ru stacks with differences in the thickness, i.e., Ta_2O_5/TiO_2=10nm/3nm (A4), 10nm/6nm (A5) and 14nm/3nm (A6) as shown in table 2-2(b). Each sample includes about 10 devices. The devices are equipped with an MOS-FET to limit the current after FORMING. In the measurement, we set the gate voltage of the MOS-FET at 1.5 V to limit the current less than 0.3 mA. The bias voltage was changed from 0 V up to 6 V with an incremental step/dwell time of 0.05 V/10 ms. As the film thickness of the Ta_2O_5 increases by 4 nm, the leakage current decreases by two orders of magnitude, while the change of thickness of TiO_2 does not affect so much.

Figure 3-4(b) shows the normal probability plot of the FORMING voltage for three Ta_2O_5/TiO_2 samples with different stack structure. The FORMING voltage strongly depends on the Ta_2O_5 thickness in case of TiO_2 film thickness is 3 nm. TiO_2 thickness also affects to the voltage but the effect is small in case of thicker Ta_2O_5 film applied to the stack.

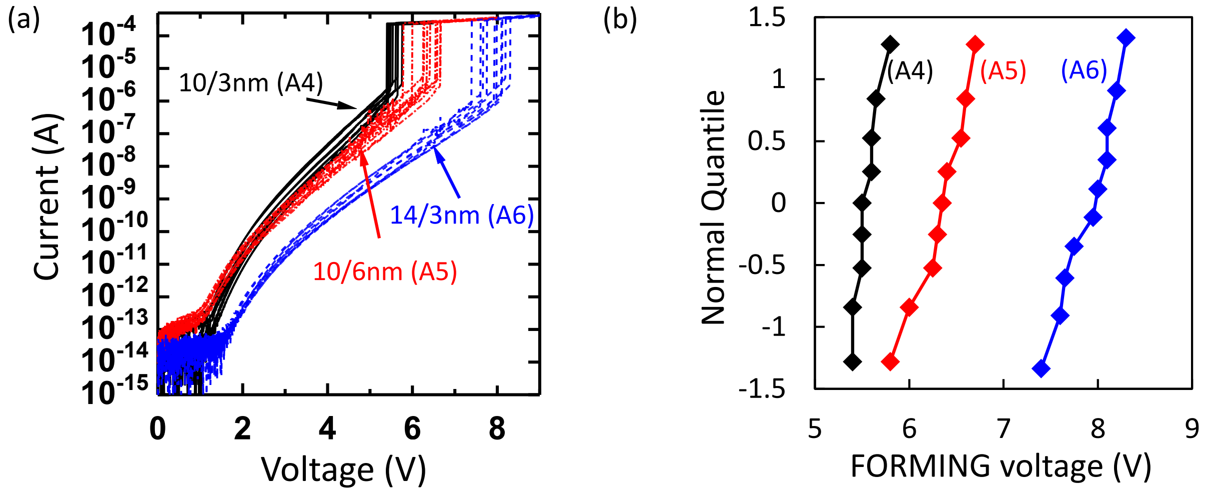

Figure 3-4 (a) I-V characteristics of pristine Ru/Ta_2O_5/TiO_2/Ru stacks with differences in the thickness. (b) Normal probability plot of FORMING voltage for each stacks.

In order to make quantitative analysis using Equ. 3-1, we have to know the electric field in each layer. The electrical field in the Ta_2O_5 and TiO_2 layers is a function of thickness *d* and electric permittivity *k* of both layers and the applied voltage *V,* and is given as

$$E_{Ta_2O_5(TiO_2)} = \frac{k_{TiO_2(Ta_2O_5)}}{k_{TiO_2(Ta_2O_5)} d_{Ta_2O_5(TiO_2)} + k_{Ta_2O_5(TiO_2)} d_{TiO_2(Ta_2O_5)}} V_{Bias}. \quad (3-3)$$

To ascertain the layer's thickness, we took cross-sectional TEM images of the sample A4 and A5. As shown in Figure 3-5, the actual film thickness was thinner than the design thickness, which is summarized in Table 3-1. Assuming that the electric fields where the FORMING occurs are the same in all samples, we can determine the ratio of electric permittivity of TiO_2 to that of Ta_2O_5 and the critical electric field. The calculated ratio is about 2. Hence, the electric permittivity of TiO_2 is estimated to be about 40, because that of Ta_2O_5 is about 20 in Fig. 4-2(b). The value of the electric permittivity of TiO_2 found in literature is 50~100 and 40 is not bad estimation. Electric fields in both layers at FORMING are 6.10 MV/cm in Ta_2O_5, and 3.05 MV/cm in TiO_2. In references 14 and 16, the breakdown field of Ta_2O_5 is reported to be 2~4.5MV/cm (26 nm-Ta_2O_5), which is not far from the present estimation.

Table 3-1 Electrical field in the TMO layers at FORMING

Sample name	Ta_2O_5 thickness (Design value)	TiO_2 thickness (Design value)	FORMING voltage	E-field in Ta_2O_5 at FORMING	E-field in TiO_2 at FORMING
A4	8.0 nm (10 nm)	2.1 nm (3 nm)	5.50 V		
A5	8.0 nm (10 nm)	4.7 nm (6 nm)	6.35 V	6.10 MV/cm	3.05 MV/cm
A6	12.0 nm (14 nm)	2.1 nm (3 nm)	7.95 V		

Note: Actual thickness of TMO layers was obtained by the cross-sectional TEM images in Figure 3-5. Median FORMING voltage represents the FORMING voltage of each samples. Specific permittivity of Ta_2O_5 is 20 come from capacitance meter. Specific permittivity of TiO_2 is 40 calculated from these values. Finally, we obtained electrical field in the TMO layers at FORMING as shown in this table.

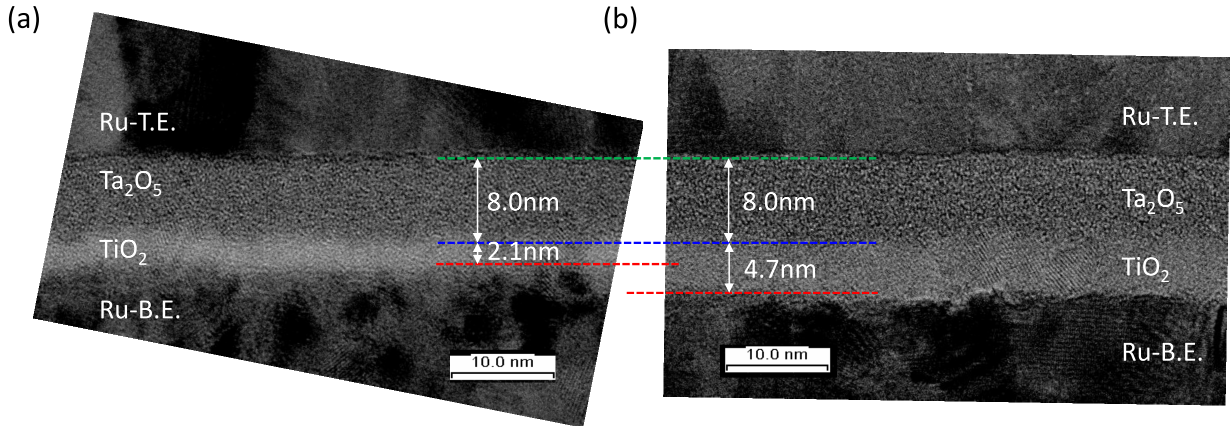

Figure 3-5 (a) Cross-sectional TEM images of the A4-sample. Actual film thickness is 8.0nm for Ta_2O_5 and 2.1nm for TiO_2, respectively. (b) Cross-sectional TEM images of the A5-sample. Actual film thickness is 8.0nm for Ta_2O_5 and 4.7nm for TiO_2, respectively.

Using these values, we analyzed the data in Fig. 3-1(a) using the *P.-F.* equation;

$$ln\left(\frac{J}{E}\right) = ln(\sigma_0) - \frac{\phi_t}{k_B T} + \frac{\sqrt{q}}{kT\sqrt{\pi\varepsilon_i}}\sqrt{E}, \qquad (3-4)$$

The results are shown in Figure 3-6(b), where the data between 0.1 nA and 1 μA in the Fig. 3-1(a) are plotted. We find the data of different structures almost coincide each other, and the slope is consistent with the theory. Thus, we conclude that the electrical conduction just before the FORMING is explained by the *P.-F.* emission [Fig. 3-6(a)].

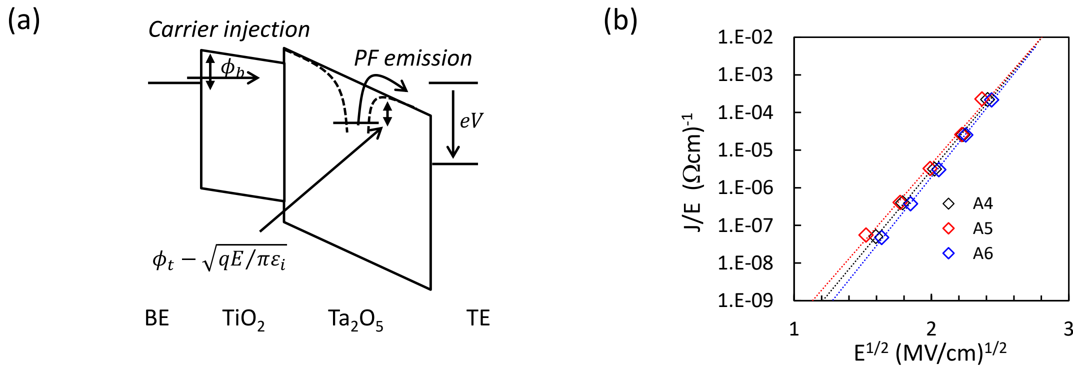

Figure 3-6 (a) Schematics for carrier (electron) injection and Poole-Frenkel emission in biased condition. (b) P.-F. plots of the I-V characteristic of Ru/Ta_2O_5/TiO_2/Ru stacks, re-plotted from Fig. 3-3 (a). The data were normalized by electrical field in Ta_2O_5 layer, respectively. Electrical field was calculated from the relation: $E_{Ta_2O_5} = \left(\varepsilon_{TiO_2}/\left(\varepsilon_{TiO_2}d_{Ta_2O_5} + \varepsilon_{Ta_2O_5}d_{TiO_2}\right)\right) \times V_{Applied}$.

Figure 3-7(a) shows *I-V* characteristics of the samples A3 and A4 which have the same stack but have different electrodes: Ru/Ta_2O_5(10nm)/TiO_2(3nm)/Pt for A3, and Ru/Ta_2O_5(10nm)/TiO_2(3nm)/Ru for A4 as shown in table 2-2(b). Each sample includes about 20 devices. In the measurement, we set the gate voltage of the MOS-FET at 1.5 V to limit the current less than 0.3 mA. The bias voltage was changed from 0 V up to 6 V with an incremental step/dwell time of 0.05 V/10 ms. As altering an electrode material from Ru to Pt, the leakage current increases by one order of magnitude. This should be caused by the work function difference in the electrode materials. When the voltage bias *V* bias is applied between the electrodes, the electric field in the TMO layer is given as

$$E_{Ta_2O_5(TiO_2)} = \frac{k_{TiO_2(Ta_2O_5)}}{k_{TiO_2(Ta_2O_5)}d_{Ta_2O_5(TiO_2)} + k_{Ta_2O_5(TiO_2)}d_{TiO_2(Ta_2O_5)}}(V_{bias} + \Delta\phi). \quad (3-5)$$

where $\Delta\phi$ is the difference in work function between the top and bottom electrodes. As shown in Figure 3-7(b), *I-V* characteristics of Pt-B.E. stack is in good agreement with that of Ru-B.E. stack when the data was re-plotted with $\Delta\phi = 1.0V$ on the *P.-F.* plot. This value is consistent with the difference in the work function (Ru: 4.7 eV, Pt: 5.7 eV) [13].

Figure 3-7(c) shows the normal probability plot of the FORMING voltage for two Ta_2O_5/TiO_2 samples with different B.E.-material. The voltage difference in the stacks is about 0.3 V, Pt-B.E. samples have a smaller FORMING voltage compared with Ru-B.E. samples, because the stack with Pt-B.E. has larger internal electrical field compared with the stack with Ru-B.E. This trend supports the electrical field-induced FORMING model [26].

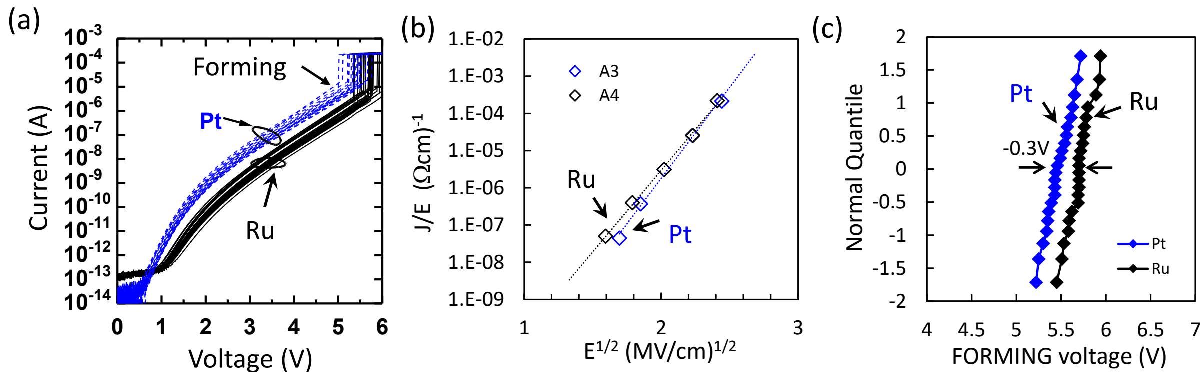

Figure 3-7 (a) I-V characteristics of pristine Ru/Ta_2O_5/TiO_2/BE stacks with the difference in BE materials (Ru or Pt). (b) P.-F. plots of the I-V characteristic, re-plotted from Fig. 3-6 (a). The data were normalized by effective electrical field in Ta_2O_5 layer, respectively. (c) Normal probability plot of FORMING voltage for each stacks.

To summarize this section, we identified the electric permittivity of TiO_2 layer from the physical thickness of each layers and stack structure dependence of FORMING voltage, and showed that the current through the pristine Ta_2O_5/TiO_2 stacks can be explained by the *P.-F.* emission from the trap states existed at 0.29eV below the conduction band of Ta_2O_5 as shown in Figure 3-6 (a). The leakage current just before the FORMING is also explained by the *P.-F.* emission, and the FORMING voltage just depends on the breakdown field in the Ta_2O_5 layer.

3- 2 Filamentary resistance change phenomenon in TiO_2 layer

Figure 3-8(a) shows the unipolar resistive switching behavior in Ta_2O_5/TiO_2 stacked cells. The sample is B1 in the Table 2-3(b) (Ru/Ta_2O_5(13nm)/Plasma-oxidized Ti(5nm)/Ru), and the data of 22 devices are shown in the figure. The figure depicts the results of two independent measurements simultaneously: LRS curves showing RESET resistance jump and HRS curves showing SET jump. In the former measurement, we changed the voltage from 0 V to 2 V with an incremental step/dwell time of 10 mV / 10 ms, applying 5.0 V to the gate of MOS-FET. In the latter measurement, we change the current from 0 V to 3 V with an incremental step/dwell time of 100 mV / 10 ms applying 1.5 V to the gate.

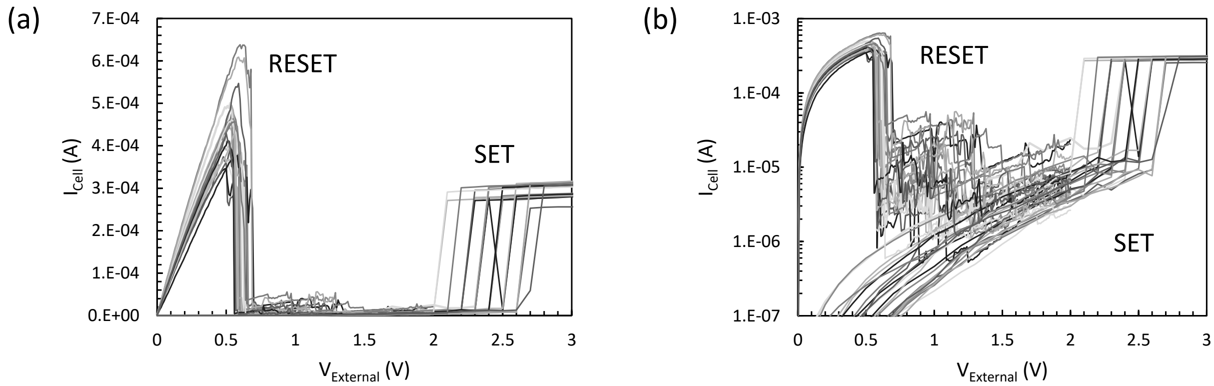

Figure 3-8 Unipolar resistive switching phenomenon in Ta_2O_5/TiO_2 stacked structure. The sample is B1 which is connected to T3 transistor (W=40μm), and data of 22 devices distributed on 6-inch wafer are shown. Gate voltages were set to 5.0V and 1.5V at RESET and SET operation, respectively. (a) Linear scale plot. (b) Logarithm scale plot. (Note: RESET operation was done by sweeping the voltage from 0.0V to 2.0V with 10mV-step. SET operation was done by sweeping the voltage from 0.0V to 3.0V with 100mV-step. Stress-time for each steps is about 10msec.)

In this sample, the RESET and SET occur at around 0.5 V and around 2.5 V, respectively. We notice that RESET current is little bit higher than the compliance current after SET, and SET voltage has larger variation than RESET voltage. The data were re-plotted on a semi-logarithm scale in Figure 3-9(b). We realize that there occur continuous small jumps in current even after the first RESET jump to the HRS occurs, and the resistance increases with increasing the applied voltage. If we increase the voltage further, the SET phenomenon should occur. In our Ru/Ta_2O_5/TiO_2/Ru stacked structure, the resistance of both LRS and HRS does not vary with the cell size down to 40nm [27]. This means that the resistance change phenomena in this structure is very local phenomena, i.e., filamentary switching phenomena.

i RESET phenomenon in Ta_2O_5/TiO_2 stacked memory cell

In this subsection, we will argue how the reset voltage changes when the resistance of LRS varies. We use group-B samples which include difference of oxidation degree in TiO_2 layer formation, and we use the 1T-1R type device with T3-transistor (W = 40 μm) for this study. The current after FORMING was limited 1 mA (V_{Gate} = 2.05 V), and various LRSs with different conductance were prepared by changing the gate voltage at SET operation (V_{Gate} = 2.05 V, 1.90 V, 1.65 V, 1.35 V, and

1.10 V). As V_{Gate} increases, the compliance current increases, and the LRS resistance becomes small. Here we used several (5 ~ 9) devices of B1, B2 and B3, and performed SET/RESET operations cyclically to obtain the distribution with the different V_{Gate}.

Figure 3-9(a) shows the *I-V* curves at RESET operation for two cases. The sample is B1. We find that higher resistive LRS can be reset by the lower RESET current (I_{RESET}). (I_{RESET} is the maximum current in the RESET operation.) Figure 3-9(b) is a distribution plot of I_{RESET} against the LRS conductance. The RESET current increases with G_{LRS}.

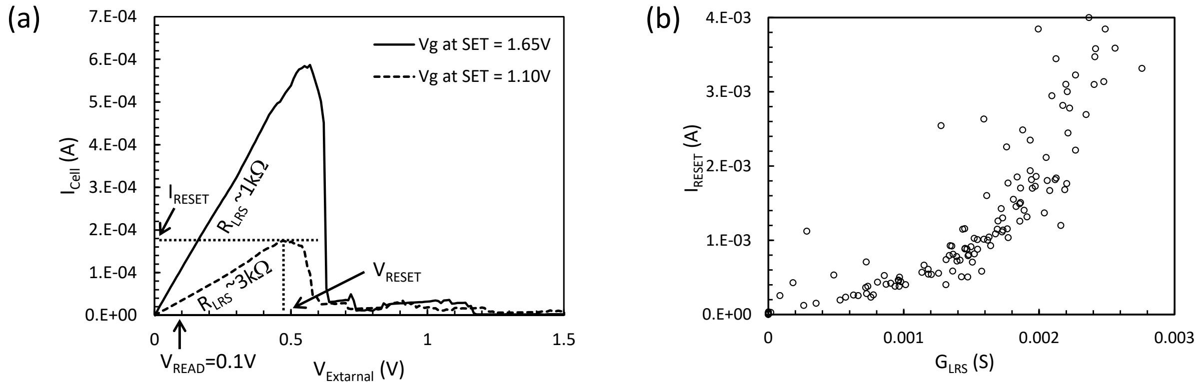

Figure 3-9 (a) Typical I-V curves at RESET operation with difference in gate voltage at SET. The sample is B1 which is connected to T3 transistor (W=40μm). RESET current (I_{RESET}) and RESET voltage (V_{RESET}) were defined by maximum current in the operation and its voltage, respectively. LRS resistance (R_{LRS}) was calculated by the cell current at 0.1V. (b) Distribution plot of I_{RESET} against the LRS conductance (G_{LRS}).

Figure 3-10(a) shows typical *I-V* curves at RESET operation of samples B1, B2, and B3. Their device structures are listed in Table 3-2(b), which we reshow above. We chose the data which have similar LRS resistance (R_{LRS}) to see the variation between samples clearly. We find that the B3 sample needs larger voltage to RESET than the B1 and B2 samples. Figure 3-10(b) is a distribution plot of the RESET voltage (V_{RESET}) vs G_{LRS}. V_{RESET} is defined as the applied voltage at the maximum current in the RESET operation, just like I_{RESET}. We confirm that V_{RESET} for B3 is considerably larger than B1 and B2. The RESET voltage increase as the LRS conductance increases above about 1 mS. In extremely low conductance region, rather large V_{RESET}'s result but they are hardly "low resistance" states.

Table 3-2: List of group-B samples (reshown of Table 2-3(b))

Name	Wf-ID	Bottom electrode	Ti	Plasma Oxidation	Ta_2O_5	Top electrode
B1	ID24	Ru (5nm or 20nm)	5nm	5min@2kW, 250C	15nm	Ru (20nm)
B2	ID27	Ru (5nm or 20nm)	2nm	1min@2kW 250C	15nm	Ru (20nm)
B3	ID25	Ru (5nm or 20nm)	2nm	5min@2kW, 250C	15nm	Ru (20nm)
B4	ID21	Ru (5nm or 20nm)	2nm	10min@2kW 250C	15nm	Ru (20nm)

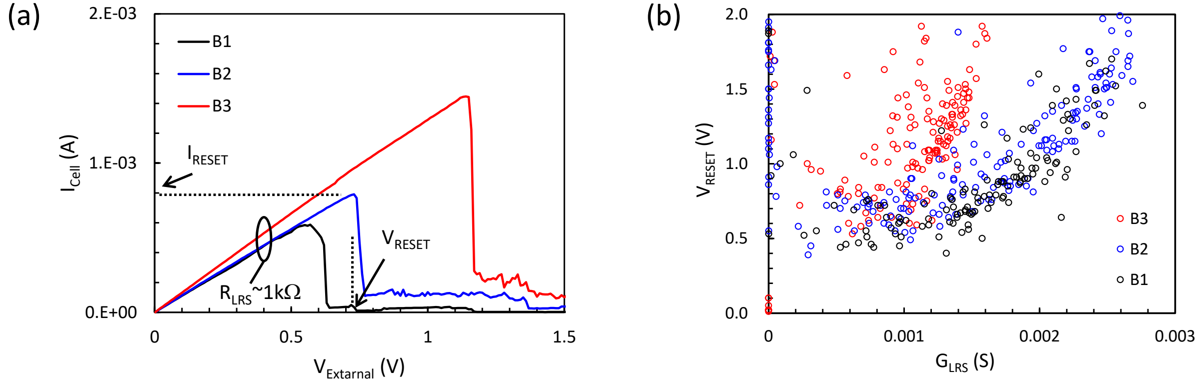

Figure 3-10 (a) Typical I-V curves at RESET operation with difference in sample. The data was compared with same LRS resistance (R_{LRS}) which was calculated from the cell current at 0.1V. T3 transistor (W=40μm) was connected to the sample. RESET current (I_{RESET}) and RESET voltage (V_{RESET}) were defined by maximum current in the operation and its voltage, respectively. (b) Distribution plot of V_{RESET} against the LRS conductance (G_{LRS}) with difference in sample.

The parameters V_{RESET} and G_{LRS} are useful practically for optimizing RESET operations as will be described later in the Chapter 5. However, these values are not inherent in the Ta_2O_5/TiO_2 stacked structure because the contributions of the series transistor and interconnect are included as shown in Figure 3-11. So, the component from the series resistive elements should be subtracted to obtain parameters proper to the Ta_2O_5/TiO_2 stacked structure.

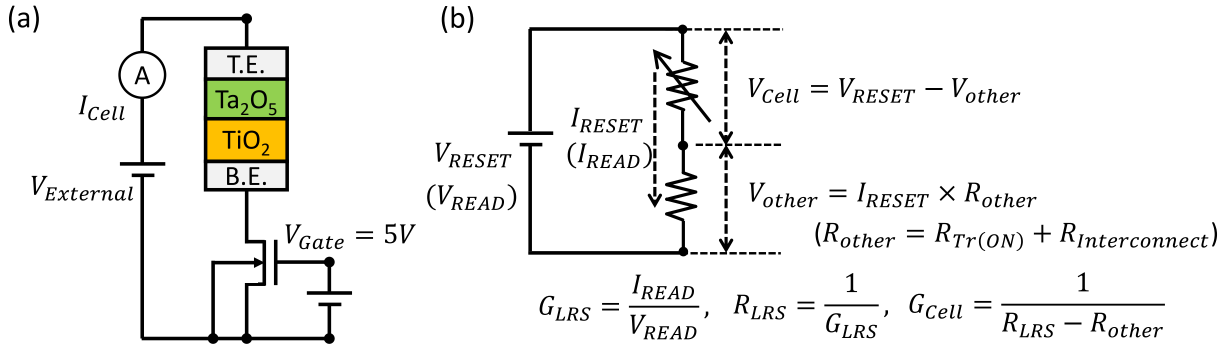

Figure 3-11 (a) Schematic of 1T-1R device with bias condition. T3 transistor (W=40μm) was used in this study. Gate voltage of series transistor (V_{Gate}) in RESET and READ operation is fixed to 5V. $V_{External}$ at READ was set to 0.1V. (b) Schematic of *IR* drop on series resistive elements including transistor and interconnect at RESET (V_{other}). The resistance (R_{other}) is about 128Ω when T3 is used as the transistor. V_{RESET} includes the *IR* drop not just RESET voltage of Ta_2O_5/TiO_2 stacked structure (V_{Cell}).

The transistor is set ON at the RESET and READ operations, and the saturation current is much larger than the I_{RESET} and the READ current (I_{READ}) (V_{Gate} = 5 V, V_{sd} = 5V, $I_{Saturation}$ ~ 10 mA). In this case, we can regard the series transistor as an ohmic resistor. As the ON resistance ($R_{Tr(ON)}$) of transistor used in this study was about 100 Ω and the resistance of interconnect to the Ta_2O_5/TiO_2 stacked

cell ($R_{Interconnect}$) was 28 Ω, the LRS-cell conductance (G_{Cell}) and the voltage dropped on the cell at RESET (V_{Cell}) is calculated simply by subtracting $R_{Tr(ON)}$ and $R_{Interconnect}$ as shown in Figure 3-11(b).

Figure 3-12(a) shows a distribution plot of the RESET cell voltage V_{Cell} against G_{Cell} for samples B1, B2 and B3. V_{Cell} at RESET increases with G_{Cell} for all types of devices with G_{Cell} larger than about 1 mS. We also show the distribution in the RESET current I_{RESET} vs. G_{Cell} plane in Figure 3-12(b). The I_{RESET} and G_{Cell} has a super-linear relation in all samples.

Filamentary switching device should have following two features in general. One is that the RESET voltage hardly depends on the compliance current at SET [28-30], and the other is that the RESET current is proportional to the compliance current at SET [28-30]. It is speculated that these features is caused from the thermal reaction [8, 9] at the critical region as shown in the inset of the Fig. 1-4(c). The RESET voltage and current in our Ta_2O_5/TiO_2 stacked structure does not agree with these features. It is a reason why M. Terai et al. speculated that the resistance change is caused by the redox reaction in the thin TiO_2 layer [1]. In what followings, we examine the experimental results by taking into account the device structure and argue the resistance change mechanism, again.

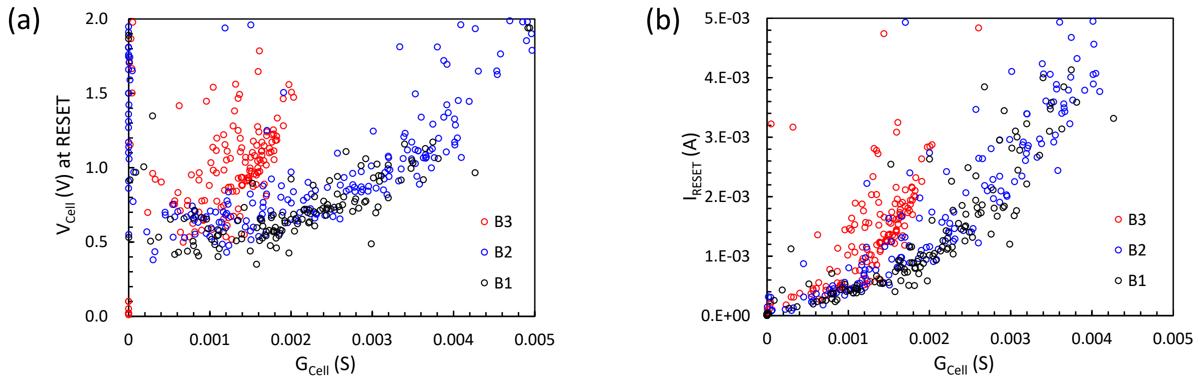

Figure 3-12 (a) Distribution plot of RESET voltage of Ta_2O_5/TiO_2 stacked structure (V_{Cell}) against the LRS conductance (G_{Cell}) with difference in sample. V_{Cell} at RESET increases with G_{Cell} in all samples. (b) Distribution plot of RESET current against the LRS conductance (G_{Cell}) with difference in sample. The relationship between I_{RESET} and G_{Cell} has a super linear property in all samples.

In Figure 3-13(a), we show a distribution plot of V_{Cell} vs. I_{RESET}. We find a very strong correlation in this plot; V_{Cell} linearly increases with I_{RESET} in large current region, but the linear relation has a finite intercept on V_{Cell} axis. The interception is about 0.4 ~ 0.5 V that is common among B1, B2 and B3. This seems to suggest that there is a definite critical voltage for SET event that is common among the three samples and at the same time there is a ohmic component that does not contribute SET and hardly fluctuates cycle-to-cycle in the cell. From the slope of the correlation, the resistances of the component is estimated 170 Ω for B1 and B2, and 340 Ω for B3.

As described in §2-1(i) and §2-3(ii), these three samples were fabricated by different TiO_2 forming process. Namely, in B1 process, Ti metal 5 nm thick was deposited and oxidized by oxygen plasma for 5 min., while Ti thickness and oxidation time were 2 nm and 1 min in B2, and 2 nm and 5 min in B3 process. Thus B3 sample was fabricated with the heavily oxidation condition to the thin Ti film on the Ru-B.E. As we wrote above, by HR-RBS measurement, we found the oxidation of Ti film

reaches 8nm depth after 5 min exposure to the oxygen plasma. It means, Ru-B.E. was also oxidized by the process, especially in B3 sample. So, the different resistance of B3 from B1 can be attributed to the resistance of interface between TiO_2 and Ru-B.E. [31]. On the other hand, little difference between B1 and B2 means the thickness of TiO_2 layer does not matter. However, we should not think it means the resistance in the TiO_2 layer is only a small part of the total resistance, because TiO_2 is regarded as an active layer for the resistance change phenomena. We should rather think the intercept voltage is the voltage of the TiO_2 part, whose resistance, i.e. (0.4 ~ 0.5) V / I_{RESET}, varies largely cycle to cycle. In this case, the remaining of the resistance that gives linear background in Fig. 3-13(a) is attributed to Ta_2O_5, which we expected to give stable filament that does not show resistance change [1]. Thus, we conclude that Figure 3-13(a) is consistent with our initial expectation.

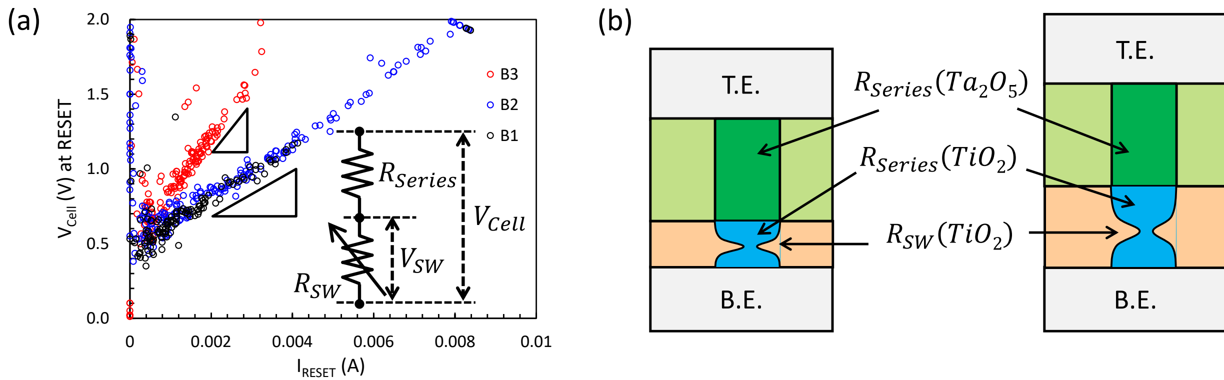

Figure 3-13 (a) Correlation between V_{Cell} and I_{RESET}. V_{Cell} is influenced by series resistance (R_{Series}) as shown in the inset. (b) Schematic pictures of resistive components in LRS. R_{Series} is composed of $R_{Series}(Ta_2O_5)$ and $R_{Series}(TiO_2)$. $R_{Series}(TiO_2)$ is negligibly small compared with R_{Cell}, and $R_{Series}(Ta_2O_5)$ depends on maximum current during cycling including FORMING. It is speculated that just $R_{SW}(TiO_2)$ is only changed by SET/RESET operations.

In this way, we can show the schematic pictures of resistive elements as Figure 3-13(b). The series resistance consists of $R_{Series}(Ta_2O_5)$ and $R_{Series}(TiO_2)$, and $R_{Series}(TiO_2)$ is negligibly small compared with R_{LRS}. So, R_{LRS} depends on just $R_{Series}(Ta_2O_5)$ and $R_{SW}(TiO_2)$. $R_{Series}(Ta_2O_5)$ has a large impact to the V_{RESET} and R_{Cell} although just the component $R_{SW}(TiO_2)$ only contributes the resistance change phenomena in SET/RESET cycling. When the R_{Cell} is smaller than $R_{Series}(Ta_2O_5)$, we cannot ignore the effects of IR-drop on the component of $R_{Series}(Ta_2O_5)$ for V_{RESET} and G_{Cell}.

Figure 3-14 shows the conductance dependence (G_{SW}) of switching voltage (V_{SW}) for the RESET. The voltage was calculated by subtracting the *IR*-drop of the series resistive element ($I_{RESET} \times R_{Series}$) from the cell voltage (V_{Cell}) at the RESET. The G_{SW} was calculated by $1/(R_{Cell} - R_{Series})$, which we used estimated value from Fig. 3-13(a), i.e., 170 Ω for B1 and B2, and 340 Ω for B3, as R_{SERIES}. We confirm that the V_{SW} is constant with increasing the conductance, and the voltage does not depend on the thickness of the TiO_2 layer, i.e., the RESET phenomenon depends on a critical voltage and that is very local phenomenon in the TiO_2 layer.

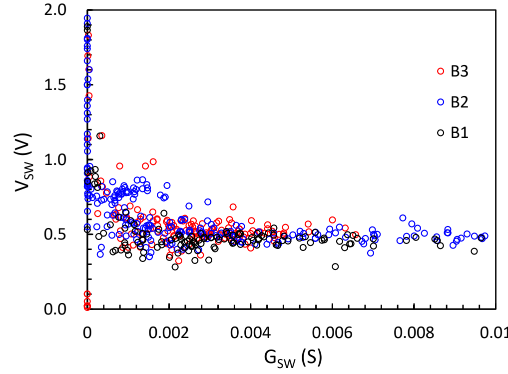

Figure 3-14 Distribution plot of essential switching voltage ($V_{SW} = V_{Cell} - I_{RESET} \times R_{Series}$) against the LRS conductance (G_{SW}) with difference in sample. The influence of series resistive element was excluded from both RESET voltage and LRS conductance.

RESET current of Ta_2O_5/TiO_2 stacked structure is also re-plotted as a function of G_{SW} in Figure 3-15(a). The relationship between I_{RESET} and G_{SW} has a linear property in all samples. Figure 3-15(b) shows the conductance dependence of switching power (P_{SW}) for the RESET. The power was calculated based on the Joule-heating at the active part ($P_{SW} = I_{RESET}^2/G_{SW}$) that does not include the heating in Ta_2O_5 and oxidized Ru. We find that the P_{SW} is proportional to the conductance, and the power does not depend on the thickness of the TiO_2 layer. This RESET power dependence on the conductance of critical region on the filament is consistent with that in the general filamentary switching devices [4, 32-38] as shown in the Fig. 3-15(b).

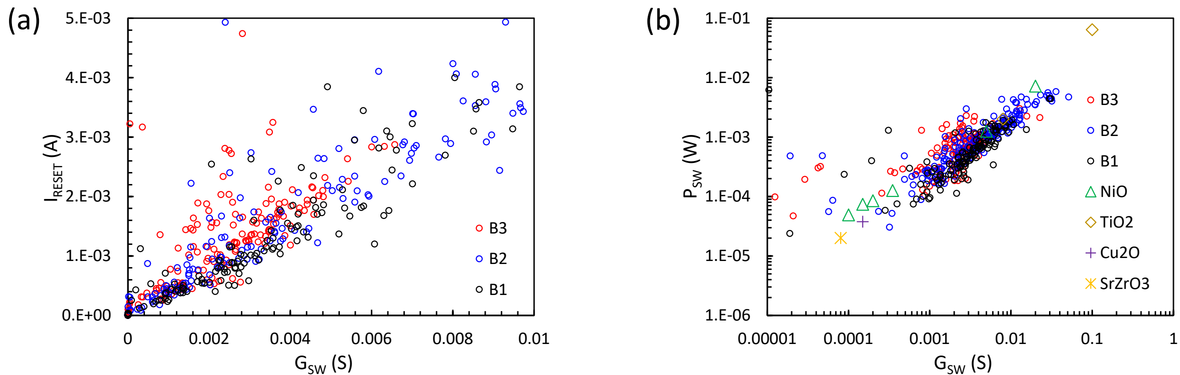

Figure 3-15 (a) Distribution plot of RESET current against the LRS conductance (G_{SW}) with difference in sample. The influence of series resistive element was excluded from LRS conductance. (b) Distribution plot of RESET power (P_{RESET}) against the LRS conductance (G_{SW}) with difference in sample with logarithm scale. The relationships between P_{RESET} and G_{Cell} has a linear property in all samples, and the relationship is almost same between the samples. This feature is consistent with the feather in other filamentary switching devices such as NiO[4, 32-34], TiO_2[35, 36], Cu_2O[37], and $SrZrO_3$[38].

Recently, studies of direct observation of the conductive filaments in single TiO_2 layer cell by analyzing crystal structure using a transmission electron microscope (TEM) have been reported [39-42]. According to D.H. Kwon et al., Magnéli phases (Ti_4O_7) was confirmed in the TiO_2 layer after

FORMING [39]. As Ti_4O_7 shows metallic conduction at room temperatures, Ti_4O_7 region bridging the electrodes is regarded as the conducive filament. Moreover, it was confirmed that the Magnéli phases is disappeared in the middle region between the electrodes after RESET operation [39].

So, we believe that the conductive filament formed in the TiO_2 layer of our Ta_2O_5/TiO_2 stacked structure is ruptured by the joule heating during the RESET operation.

ii SET phenomenon in Ta_2O_5/TiO_2 stacked memory cell

In this subsection, we show the correlation between HRS resistance and SET voltage, and explain the role of the compliance current in the SET operation. The samples we used were B1, B2, and B3, and the compliance current at FORMING was 1 mA (V_{Gate} = 2.05V, $I_{Saturation}$ ~ 1 mA). Various HRSs with different resistance were prepared by changing maximum voltage at RESET operation.

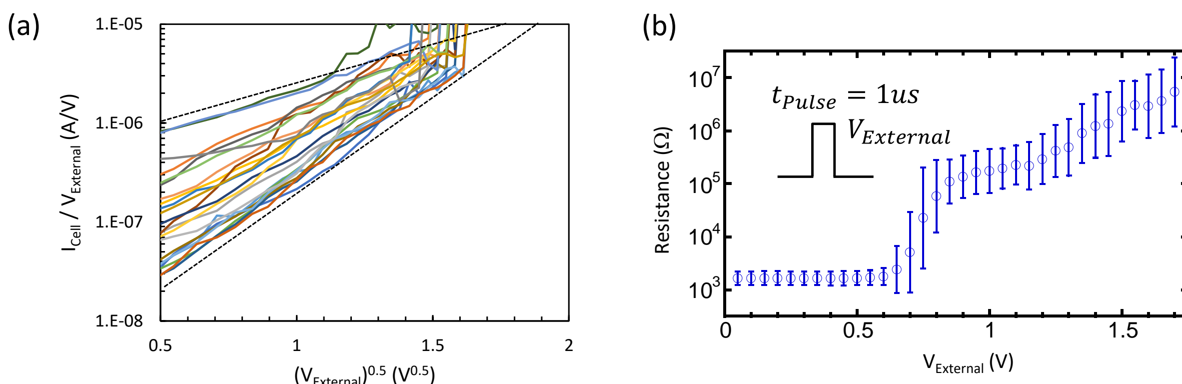

Figure 3-16 (a) P.-F. plots of the I-V curves at SET operation, re-plotted from Figure 3-8. The data were normalized by external voltage to Ta_2O_5/TiO_2 stacked structure. The sample is B1 connected to T3 transistor (W=40μm), and data of 22 devices distributed on 6-inch wafer are shown. External voltage was swept from 0.0V to 3.0V with 100mV/10ms. (Note: HRSs were prepared by same RESET condition. It was done by sweeping the voltage from 0.0V to 2.0V with 10mV/10ms.) (b) Resistance after applying incremented voltage pulse to LRSs. The pulse with 1us-width was incremented from 0.0V to 1.8V with 0.05V. Resistance was monitored every time after the pulse. The sample is B1 connected to T3 transistor (W=40μm), and data of 22 devices distributed on 6-inch wafer are shown. The bars in the figure show standard deviation for device-to-device variation. (Note: LRSs were prepared by same SET condition ($V_{External}$=3.0V, V_{Gate}=1.35V).)

In contrast to LRS, *I-V* curve of HRS is not ohmic, and voltage drop on the series resistive elements is very small because of the small current. Then, the external voltage almost drop on the switching region. Figure 3-16(a) shows *P.F.* plots of the *I-V* curves at SET operation, replotted from the Fig. 3-8. The data were normalized by external voltage instead of electric field because we do not know the width between the ruptured filaments. So, the slope of the linear part of the plot is related to the width. Thus, we realized at least that the conduction after RESET is caused by lowering barrier height to the conduction band by applying large electric field. However, we cannot distinguish the *P.F.* conduction from the Schottky conduction, because the slope depends on not only the width

but also other factors such as a dielectric constant and a local temperature. In Chapter 4, we investigate the conduction mechanism in details.

Figure 3-16(b) shows the HRS resistance (R_{HRS}) dependence on maximum voltage at RESET. The sample is B1 connected to T3 transistor (W = 40 mm), and data of 22 devices distributed on 6-inch wafer are shown. 1 μs-pulse was incremented from 0.0 V to 1.8 V with 0.05 mV. LRSs before the RESET operation were prepared by same SET condition ($V_{External}$ = 3.0 V, V_{Gate} = 1.35 V). R_{HRS} was monitored every time after the pulse. The bars in the figure show standard deviation for device-to-device variation. We find that resistance of all devices changes to HRS from LRS after applying the 0.8 V-pulse, and the resistance increases with increasing the voltage height. If we apply more high voltage to the HRS, the resistance additionally increase or suddenly decreases. The later behavior is the SET phenomenon.

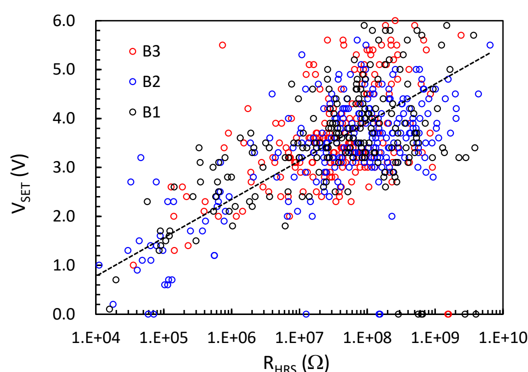

Figure 3-17 Correlation between HRS resistance (R_{HRS}) and SET voltage (V_{SET}). HRSs were prepared with difference in maximum voltage (V_{MAX}) at RESET operation with sweep mode (V_{MAX} = 1.0V, 1.5V, 2.0V, 2.5V, 3.0V with 10mV/10ms). SET operation was done by sweeping the voltage from 0.0V to 6.0V with 100mV-step. Stress-time for each steps is about 10msec.

Figure 3-17 is a distribution plot of the SET phenomena is sample B1, B2, and B3, and shows a correlation between HRS resistance (R_{HRS}) and SET voltage (V_{SET}). Here, the HRS resistance is defined at V = 0.1 V, i.e., R_{HRS} = 0.1 V / I(0.1 V). HRSs were prepared by DC sweep mode. In order to prepare various R_{HRS}, we intentionally changes the maximum voltage (V_{SET}) of the sweep, i.e. V_{MAX} = 1.0 V, 1.5 V, 2.0 V, 2.5 V, and 3.0 V. SET operation was done by sweeping the voltage from 0.0 V to 6.0 V with 100 mV / 10 ms-step. We find that higher resistive HRS needs larger V_{SET}. If we want to reduce the V_{SET}, R_{HRS} should be suppressed which is possible to just reduce the V_{MAX} at RESET operation.

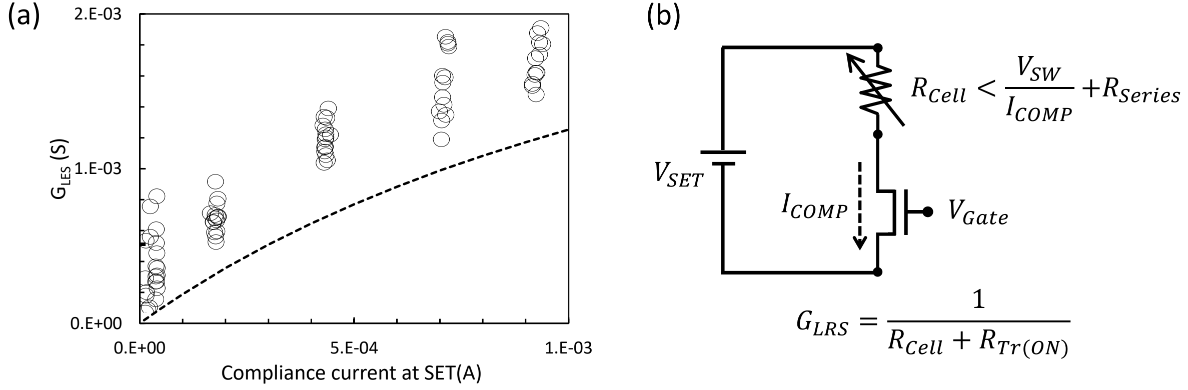

Figure 3-18 (a) I_{COMP} dependence of G_{LRS}. Dashed line is the expected minimum G_{LRS} from the I_{COMP}. (b) I_{COMP} effect for R_{Cell} after SET operation, and the G_{LRS} formula.

The resistance after SET, i.e. R_{LRS} varies device-to-device, but has some correlation to the compliance current I_{COMP} at SET. The correlation between G_{LRS} and I_{COMP} was shown in Figure 3-18(a). We realize that the G_{LRS} increases with increasing I_{COMP}. In unipolar resistance change devices, the voltage across the cell just after SET jump has to be smaller than the RESET voltage (V_{SW}). Otherwise, RESET takes place and the device becomes unstable. As shown in Figure 3-18(b), it gives the upper (lower) bound for R_{LRS} (G_{LRS}). The dashed line in the Fig. 3-18(a) depicts this limit. We find that the G_{LRS} surely satisfies the stability condition. The device-to-device variation of the G_{LRS} might come from the difference of stressing time with constant current after SET [34, 36].

3-３ Summary

In this chapter, we characterized the resistance change phenomena, i.e., FORMING, RESET, and SET, together with three states, i.e., initial state, low resistance state (LRS), and high resistance state (HRS) in the Ta_2O_5/TiO_2 stacked structure.

We showed that the electrical conduction in the pristine Ta_2O_5/TiO_2 stacks can be explained by the *Poole-Frenkel* emission model; Carriers are trapped in trap states and occasionally released into the conduction band. The energy of the trap is estimated 0.29eV below the conduction band of Ta_2O_5. The *P.-F.* emission-limited conduction holds valid just before the FORMING, and the FORMING voltage strongly depends on the electric field in the stack.

After FORIMNG, the electrical conduction changes fundamentally. The resistance diminishes many orders of magnitude and is ohmic in nature. This low-resistance state (LRS) is supported by a conductive filament in the TiO_2/Ta_2O_5 stack layer formed by the FORMING operation. The filamentary nature was confirmed by the area dependence of the resistance. Namely, the current in the pristine cell is proportional to the cell area, while the resistance of LRS is almost independent of cell area. The resistance varies depending on the compliance current at the FORMING operation.

We confirmed that the conduction filament in the TiO_2/Ta_2O_5 stack layer shows unipolar-type resistance change; we performed RESET in either polarity. We analyzed distribution of RESET voltage

and RESET current for various LRS of three types of samples, B1, B2 and B3, and found they are consistently understood by a filamentary conduction model where the switching takes place in TiO_2 layer while Ta_2O_5 gives a stable filament that does not change resistance. The resistance switching occurs at a definite critical voltage of about 0.5V irrespective of TiO_2 resistance. This voltage means the voltage applied to the TiO_2 layer, and the apparent RESET voltage changes depending on the R_{LRS}, because there are series resistances of Ta_2O_5, oxidized Ru and FET.

In addition, we analyzed the correlation between HRS and SET phenomenon. The SET voltage correlates weakly with HRS resistance as shown in Fig.3-17. We argued the stability of SET operation and showed that there is a lower bound of the conductance after SET that is a function of the compliance current at SET operation. Later one can be explained based on the RESET parameters such as intrinsic RESET voltage (V_{SW}) and series resistance, but the origin of the correlation between SET voltage and HRS resistance had not been explained. We discuss this origin after investigating the HRS in Chapter 4, again.

3-４ Reference

[1] M. Terai, S. Kotsuji, H. Hada, N. Iguchi, T. Ichihashi, and S. Fujieda, “Effect of ReRAM-Stack Asymmetry on Read Disturb Immunity”, *IRPS Tech. Dig.*, pp. 134-138 (2009).

[2] Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Kawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Iijima, T. Mikawa, T. Ninomiya, R. Miyanaga, Y. Kawashima, K. Tsuji, A. Himeno, T. Okada, R. Azuma, K. Shimakawa, H. Sugaya, and T. Takagi, R. Yasuhara, K. Horiba, H. Kumigashira, and M. Oshima, “Highly Reliable TaOx ReRAM and Direct Evidence of Redox Reaction Mechanism”, *IEDM Tech. Dig.*, pp. 293-296 (2008), and “Switching Mechanism of TaOx ReRAM”, *SSDM Tech. Dig.*, pp1202-1203 (2009).

[3] J. H. Hur, M.-J. Lee, C. B. Lee, Y.-B. Kim, and C.-J. Kim, “Modeling for bipolar resistive memory switching in transition-metal oxides”, *Phys. Rev. B*, **82**, 155321 (2010).

[4] D. C. Kim, S. Seo, et al., “Electrical observations of filamentary conductions for the resistive memory switching in NiO films”, *Appl. Phys. Lett.*, **88**, 202102 (2006).

[5] H. Shima, F. Takano, H. Akinaga, Y. Tamai, I. H. Inoue, H. Takagi, “Resistance switching in the metal deficient-type oxides: NiO and CoO”, *Appl. Phys. Lett.*, **91**, 012901 (2007).

[6] Y. Sato, K. Kinoshita, M. Aoki, and Y. Sugiyama, “Consideration of switching mechanism of binary metal oxide resistive junctions using a thermal reaction model”, *Appl. Phys. Lett.*, **90**, 033503 (2007)

[7] U. Russo, D. Jelmini, C. Cagli, A. L. Lacaita, S. Spigat, C. Wiemert, M. Peregot and M. Fanciullit, “Conductive-filament switching analysis and self-accelerated thermal dissolution model for reset in NiO-based RRAM”, *IEDM Tech. Dig.*, pp.775-778 (2007)

[8] C. Cagli, D. Ielmini, F. Nardi and A. L. Lacaita, “Modeling of Set/Reset Operations in NiO-Based Resistive-Switching Memory Devices”, *IEDM Tech. Dig.*, p.301 (2008).

[9] C. Cagli, F. Nardi, and D. Ielmini, “Modeling of Set/Reset Operations in NiO-Based Resistive-Switching

Memory Devices", *Electron Devices*, **56**, 1712-1720 (2009).

[10] C. Cagli, D. Ielmini, F. Nardi and A. L. Lacaita, "Evidence for threshold switching in the set process of NiO-based RRAM and physical modeling for set, reset, retention and disturb prediction", *IEDM Tech. Dig.*, pp.301-304 (2008).

[11] P. C. Joshi and M. W. Cole, "Influence of postdeposition annealing on the enhanced structure an electrical properties of amorphous and crystalline Ta_2O_5 thin films or dynamic random access memory applications", J. Appl. Phys. **80**, 871-880 (1999).

[12] S. Ezhilvalavan, T.-Y. Tseng, "Electrical properties of Ta_2O-thin filme deposited on Cu", *Thin Solid Films*, **360**, 268-273 (2000).

[13] R. M. Fleming, D. V. Lang, C. D. W. Jones, M. L. Steigerwald, D. W. Murphy, G. B. Alers, Y.-H. Wong, R. B. van Dover, J. R. Kwo, and A. M. Sergent, "Defect dominated charge transport in amorphous Ta_2O_5 thin films", *J. Appl. Phys.*, **88**, 850-862 (2000).

[14] M. Houssa, P. W. Mertens, M. M. Heyns, J. S. Jeon, A. Halliyal, B. Ogle, "Soft breakdown in very thin Ta_2O_5 gate dielectric layers", *Solid-State Electronics*, **44**, 521-525 (2000).

[15] Z. J. Luo, X. Guo, T. P. Ma, and T. Tamagawa, "Temperature dependence of gate current in thin Ta_2O_5 and TiO_2 fims", *Appl. Phys. Lett.*, **79**, 2803-2804 (2001).

[16] E. Atanassova and A. Paskaleva, "Breakdown fields and conduction mechanisms in thin Ta_2O_5 layers on Si for high density DRAMs", *Microelectronics Reliability*, **42**, 157–173 (2002).

[17] H.-J. Kim, J.-S. Song, I.-S. Kim, and S.-S. Kim, "Electrical characteristics of Ti-O/Ta_2O_5 thin film sputtered on Ta/Ti/Al_2O_3 substrate", *Thin Solid Films*, **446** 124 (2004).

[18] J.-W. Lee, M.-H. Han, W.-J. Maeng, H. Kim, and J.-M. Myoung, "Dependence of electrical properties on interfacial layer of Ta_2O_5 films", *Microelectronic Engineering*, **84**, 2865-2868 (2007).

[19] J. J. O'Dwyer, "Current-Voltage Characteristics of Dielectric Films", *J. Appl. Phys.*, **37**, 599-601 (1966).

[20] J. Antula, "Effect of Positive Ionic Space Charge on Electrical Capacitance and Schottky Current in Thin Al_2O_3 Films", *Thin Solid Films*, **4**, 281-289 (1969).

[23] J. G. Simmons, "Poole-Frenkel Effect and Schottky Effect in Metal-Insulator-Metal Systems", *Phys. Rev.*, **155**, 657-660 (1967).

[21] M. Lenzlinger and E. H. Snow, "Fowler-Nordheim Tunneling into Thermally Grown SiO_2", *J. Appl. Phys.*, **40**, 278-283 (1969).

[22] C. M. Osburn and E. J. Weitzman, "Electrical Conduction and Dielectric Breakdown in Silicon Dioxide Films on Silicon", *J. Electrochem. Soc.*, **119**, 603-609 (1972).

[23] J. G. Simmons, "Poole-Frenkel Effect and Schottky Effect in Metal-Insulator-Metal Systems", *Phys. Rev.*, **155**, 657-660 (1967).

[24] B. C. Lai and J. Y. Lee, "Leakage Current Mechanism of Metal-Ta2O5-Metal Capacitors for Memory Device Applications", *J. Electrochem. Soc.*, **146**, 266-269 (1999).

[25] K. Kukli, J. Aarik, A. Aidla, O. Kohan, T. Uustare, and V. Sammelselg, "Properties of tantalum oxide thin films grown by atomic layer deposition", *Thin Solid Films*, **260**, 135-142 (1995).

[26] T. W. Hickmott, "Voltage-dependent dielectric breakdown and voltage-controlled negative resistance in anodized Al-Al_2O_3-Au diodes", *J. Appl. Phys.*, **88**, 2805-2812 (2000).

[27] M. Terai, M. Saitoh, T. Nagumo, Y. Sakotsubo, Y. Yabe, K. Takeda, and T. Hase, "High Thermal Robust ReRAM with a New Method for Suppressing Read Disturb", *2011 Symposium on VLSI, Tech. Dig.*, pp. 50-51 (2011)

[28] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, and Y. Sugiyama, "Reduction in the reset current in a resistive random access memory consisting of NiOx brought about by reducing a parasitic capacitance", *Appl. Phys. Lett.*, **93**, 033506 (2008).

[29] W. Wang, S. Fujita, and S. S. Wong, "RESET Mechanism of TiOx Resistance-Change Memory Device", *Elec. Dev. Lett.*, **30**, 733-735 (2009).

[30] H. Shima, F. Takano, H. Muramatsu, H. Akinaga, Y. Tamai, I. H. Inque, and H. Takagi, "Voltage polarity dependent low-power and high-speed resistance switching in CoO resistance random access memory with Ta electrode", *Appl. Phys. Lett.*, **93**, 113504 (2008).

[31] Y. Sakotsubo, "NONVOLATILE SEMICONDUCTOR OTHER PUBLICATIONS MEMORY DEVICE AND MANUFACTURING METHOD THEREOF", US 8,598,564 (2013).

[32] S. Seo, M. J. Lee, D.H. Seo, S. K. Choi, D.-S. Suh, Y. S. Joung, I. K. Yoo, I.S. Byun, I. R. Hwang, S. H. Kim, and B. H. Park, "Conductivity switching characteristics and reset current in NiO films", *Appl. Phys. Lett.*, **86**, 093509 (2005).

[33] K. Tsunoda, K. Kinoshita, H. Noshiro, Y. Yamazaki, T. Jizuka, Y. Ito, A. Takahashi, A. Okano, Y. Sato, T. Fukano, M. Aoki, and Y. Sugiyama, "Low Power and High Speed Switching of Ti-doped NiO ReRAM under the Unipolar Voltage Source of less than 3 V", *IEDM Tech. Dig.*, pp. 767-770 (2007).

[34] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, and Y. Sugiyama, "Reduction in the reset current in a resistive random access memory consisting of NiOx brought about by reducing a parasitic capacitance", *Appl. Phys. Lett.*, **93**, 033506 (2008).

[35] K. M. Kim, B. J. Choi, Y. C. Shin, S. Choi, and C. S. Hwang, "Anode-interface localized filamentary mechanism in resistive switching of TiO_2 thin films", *Appl. Phys. Lett.*, **91**, 012907 (2007).

[36] B. J. Choi, S. Choi, K. M. Kim, Y. C. Shin, C. S. Hwang, S.-Y. Hwang, S.-S. Cho, S. Park, and S.-K. Hong, "Study on the resistive switching time of TiO_2 thin films", *Appl. Phys. Lett.*, **89**, 012906 (2006)

[37] T.-N. Fang, S. Kaza, S. Haddad, A. Chen, Y.-C. Wu, Z. Lan, S. Avanzino, D. Liao, C. Gopalan, S. Choi, S. Mahdavi, M. Buynoski, Y. Lin, C. Marrian, C. Bill, M. VanBuskirk and M. Taguchi, "Erase Mechanism for Copper Oxide Resistive Switching Memory Cells with Nickel Electrode", *IEDM Tech. Dig.*, pp. - (2006).

[38] A. Beck, J. G. Bednorz, C. Gerber, C. Rossel and D. Widmer, “Reproducible switching effect in thin oxide films for memory applications”, *Appl. Phys. Lett.*, **77**, 139–141 (2000).

[39] D.-H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X.-S. Li, G.-S. Park, B. Lee, S. Han, M. Kim, and C. S. Hwang, “Atomic structure of conducting nano-filaments in TiO_2 resistive switching memory”, *Nature Nanotechnology*, **5**, 148 (2010).

[40] J. P. Strachan, M. D. Pickett, J. J. Yang, S. Aloni, A. L. David Kilcoyne, G. Medeiros-Ribeiro, and R. Stanley Williams, “Direct identification of the conducting channels in a functioning memristive device”, *Advanced Materials*, **22**, 3573 (2010).

[41] K. Szot M. Rogala, W. Speier, Z. Klusek, A. Beshmehn, and R. Waser, “TiO_2-a prototypical memristive material”, *Nanotechnology*, **22**, 254001 (2011).

[42] F. Miao, J. P. Strachan, J. J. Yang, M. –X. Zhang, I. Goldfarb, A. C. Torrezan, P. Eschbach, R. D. Kelley, G. Medeiros-Ribeiro, and R. S. Williams, “Anatomy of a Nanoscale Conduction Channel Reveals the Mechanism of a High-Performance Memristor”, *Advanced Materials*, **23**, 5633 (2011).

Chapter 4. Electrical conduction in High resistance states of Ta_2O_5/TiO_2 stacked structure

Electrical properties of the conductive filament formed in the thin TMO layer by FORMING or SET process have been studied in reference 1-6. According to them, the current in the conductive filament is carried by diffusive electron moving in the delocalized defect states. On the other hand, electrical properties of the ruptured filament after the RESET have not been investigated, enough, although understand it is important to know the nature of the resistance change at the RESET.

Figure 4-1 shows the *I-V* curves of the LRS and the HRS in the Ru/Ta_2O_5(12.5nm)/TiO_2(3nm)/Ru structure. *I-V* curve of the LRS is linear up to the RESET voltage as shown in the Fig. 4-1(a). Namely, the conductive filament in the Ta_2O_5/TiO_2 stacked cell, i.e. both of the stable filament and the switching filament, has an ohmic property. In contrast, *I-V* curve of the HRS has strong non-linearity in the voltage above 0.1V as shown in the Fig. 4-1(b), though it is symmetric about the origin.

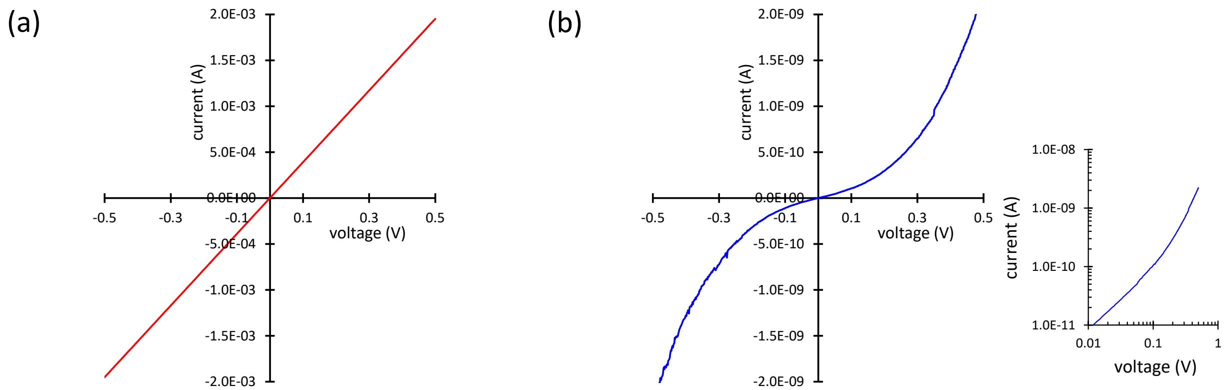

Figure 4-1 Typical I-V characteristics of LRS (a) and HRS (b) in Ru/Ta_2O_5/TiO_2/Ru stack (A4) at room temperature. Inset is re-plotted from (b) with log-log scale. Special 1T-1R type device which has middle terminal on the node between the n-FET and the memory cell as shown in the Fig 2-8 (b) was used. The external voltage was applied directly to the Ta_2O_5/TiO_2 stacked structure without passing through the MOS-FET.

In this chapter, we investigate the conduction mechanism of the HRS by analyzing the *I-V* characteristics at low temperatures. We also discuss the resistance variation after the RESET.

We used the type-A samples with special 1T-1R device configuration as shown in §2-3. The device has middle terminal on the node between the MOS-FET and the memory cell as shown in the Fig. 2-8(b). In the measurement at low temperatures, the external voltage was applied directly to the Ta_2O_5/TiO_2 stacked structure without passing through the MOS-FET by using the middle terminal.

4-1 Electrical properties of low resistance states

Prior to examine the HRS, we examine the electrical properties of the LRS before RESET at first. We prepared three LRS-devices with the difference in conductance. In FORMING and SET operations, the bias voltage was changed from 0.0 V up to 6.0 V with an incremental step/dwell time of 0.05 V/10 ms, and the compliance current was 0.3 mA. As described in the Section 3-2, the conductive filament formed in Ta_2O_5 layer is un-switchable stable filament and the resistance just depends on the compliance current at the FORMING operation. However controllability of the current through the memory cell was poor in the used 1T-1R type device, because it has large parasitic capacitance associated with the middle terminal.

Figure 4-2 shows the *I-V* characteristics of the LRSs in the Ru/Ta_2O_5(10nm)/TiO_2(3nm)/Ru stack (A4) at various temperature between the room temperature and the liquid helium temperature. In this measurements, the voltage was applied directly to the Ta_2O_5/TiO_2 stacked structure by using middle terminal in the device. The *I-V* curves have a linear property, and the conductance is about 80 μS (~12.5 kΩ) for LRS1, ~3 mS (~333 Ω) for LRS2, and ~4 mS (~250 Ω) for LRS3 at the room temperature.

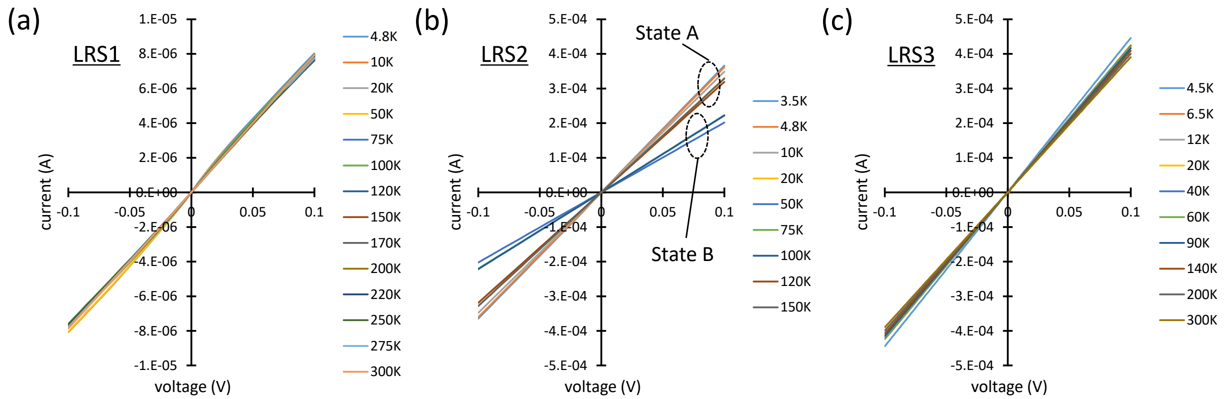

Figure 4-2 Temperature dependence (300K to 4.2K) of I-V characteristics of LRS1 (a), LRS2 (b), and LRS3 (c). LRS2 data contains two states, which is due to the state change during this measurement. (Memory cell: Ru/Ta_2O_5(10nm)/TiO_2(3nm)/Ru stack (A4), Cell size: 0.28um)

Figure 4-3 shows the temperature dependence of conductance of LRS samples. The conductance of LRS1 hardly depends on the temperature, while the conductance of LRS2 and LRS3 slightly increases with decreasing the temperature. The residual resistance ratio (RRR = R(300 K)/R(4 K)) of LRS1, LRS2 and LRS3 are 1.01, 1.11, and 1.14, respectively. According to the theory of weak localization and the electron-electron theory [5], the conductance of a one-dimensional disordered metal should decrease as $\Delta G \propto \tau_\varepsilon{}^{-0.5}$ or $\Delta G \propto T^{-0.5}$ at low temperatures. Here, τ_ε is the inelastic scattering time of electron. We do not find either tendency in the data down to 4 K. Thus, the LRS is disordered metallic states where the scattering by random potential exceeds the phonon scattering, but the randomness is not so high as to cause prominent weak localization.

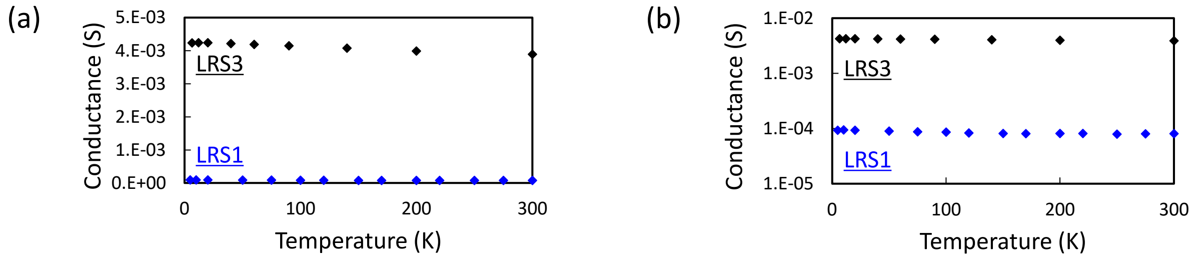

Figure 4-3 Temperature dependencies of conductance of LRS1 and LRS3 with linear scale (a) and with logarithm scale (b).

By the arguments, in §3-2, we conclude the conductive filament formed in Ta_2O_5 layer is stable and un-switchable, and its resistance (including the resistance of oxidized Ru) is about 170 Ω for B1 and B2 samples. Although the resistance varies depending on cell structure and FORMING condition, we can expect it does not differ much in the present devices because the structure is essentially the same. In Figure 4-4(a), we plot the conductance of LRS1 and LRS3 with dashed line on the Fig. 3-12(b). LRS3 needs about 5 mA for RESET, and the resistance includes two components, i.e., resistance of stable filament formed in Ta_2O_5 layer and resistance of switching filament formed in TiO_2 layer. On the other hand, LRS1 resistance is large than that of the stable filament formed in Ta_2O_5 layer. So, the electrical properties of LRS1 depends strongly on the switching filament.

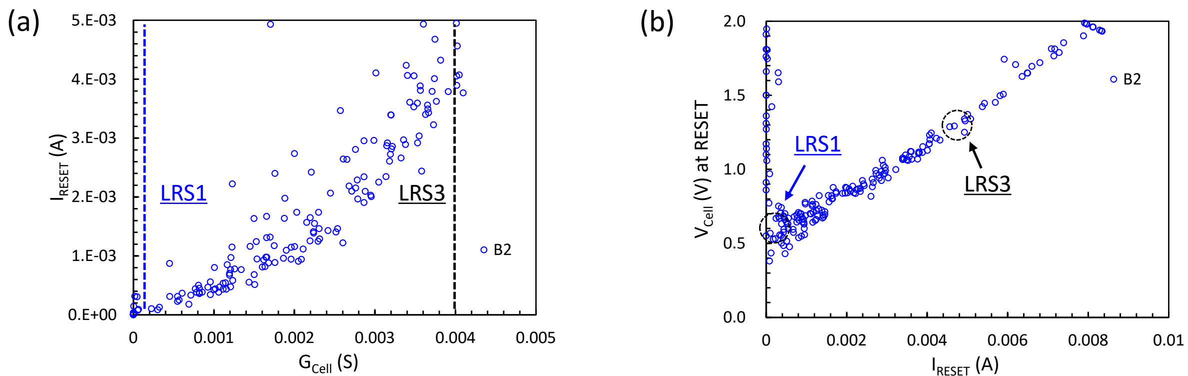

Figure 4-4 (a) Relationship between RESET current and LRS conductance in Ta_2O_5/TiO_2 stacked structure, re-plotted from Fig. 3-12 (b). Dashed lines are conductance of LRS1 and LRS3, respectively. (b) Relationship between RESET voltage (V_{Cell} at RESET) and current (I_{RESET}) in Ta_2O_5/TiO_2 stacked structure, re-plotted from Fig. 3-13. Dashed circles means operating parameters for LRS1 and LRS3, respectively. LRS3 resistance includes two component, the resistance of stable filament formed in Ta_2O_5 layer and the resistance of switching filament formed in TiO_2 layer. On the other hand, LRS1 resistance is large than that of the stable filament formed in Ta_2O_5 layer. So, the electrical properties of LRS1 depends strongly on the switching filament formed in TiO_2 layer.

In §3-2(i), we argued the electrical conductance of LRS stack layer and conclude that the stable filament is formed in Ta_2O_5 whose resistance is about 170 Ω for B1 and B2 samples. According to Landauer, the electrical conductance of a mesoscopic conductor is given as

$$G = G_0 \Sigma_\mathrm{i} T_i.$$

Here, T is the electron's transmission probability, i is the index of conduction channel, and $G_0 = 2e^2/h$ is the quantum conductance. If we express the number of the active conduction channel, and their average transmission probability as *N* and *T*, then $G = G_0 NT$. So, in the case of the stable filament in B1 and B2, the value of *NT* is evaluated to be 74. As the transmission coefficient is unity at most, the number of conductance channel have to be larger than 74. According to the first-principle calculation of oxygen-deficient Ta_2O_5 by Yang et al. [7], shallow defect states are induced near the bottom of conduction band, and can be expected to carry the leakage current in Ta_2O_5. The state is composed mainly of the Ta 5d and O 2p orbitals. If it is also the case in conductive filament and when we assume the degeneracy of the defect states is 1, a cross-section of the stable filament must have at least 74 such defect states. So, we can conclude the cross-section of the stable filament include at least 37 oxygen vacancy sites.

4-２ Electrical properties of high resistance states

i Temperature dependence of I-V characteristics

The RESET phenomenon in the Ta_2O_5/TiO_2 stacked cell occurs in the TiO_2 layer as shown in §3-2. It is believed that the resistance change to the HRS is caused by rupturing the conductive filament there. We prepared three HRS-devices with the difference in conductance, which was prepared differentially from LRS-devices. We set the gate voltage of the MOS-FET at 5.0 V to minimize the *IR*-drop on the MOS-FET at RESET operation. The bias voltage was changed from 0.0 V up to 2.0 V with an incremental step/dwell time of 0.01 V/10 ms. After the operation, HRS resistance was distributed between 1 MΩ and 1 GΩ [8].

Figure 4-5 shows the *I-V* characteristics of the HRSs in the Ru/Ta_2O_5(10nm)/TiO_2(3nm)/Ru stack (A4) at various temperature between the room temperature and the liquid helium temperature. In this measurement, the voltage was applied directly to the Ta_2O_5/TiO_2 stacked structure by using middle terminal in the device. The zero-bias conductance after RESET is ~1 μS (~1 MΩ) for HRS1, ~10 nS (~100 MΩ) for HRS2, and ~1 nS (~1 GΩ) for HRS3 at the room temperature. The *I-V* curves between -0.1 V and +0.1 V at the low temperatures have a non-linear property in contrast to the I-V curves at the room temperature which is almost linear. The conductance of HRSs is significantly decreased with decreasing the temperature in contrast to the LRSs as shown in Figure 4-6(a).

Arrhenius plots of the HRS conductance in Figure 4-6(a) is shown in Figure 4-6(b). The conductance decreases exponentially with increasing the inverse of the temperature around room temperature. This means that the conduction is based on thermally activated phenomenon, and the activation energy obtained by fitting the data between the room temperature and 150 K is about 30 meV for HRS1, 57 meV for HRS2, and 134 meV for HRS3. The conductance ceases to decrease below about 40 K. It means that dominant conduction mode in HRS changed from thermally activated conduction to the tunneling conduction at low temperatures.

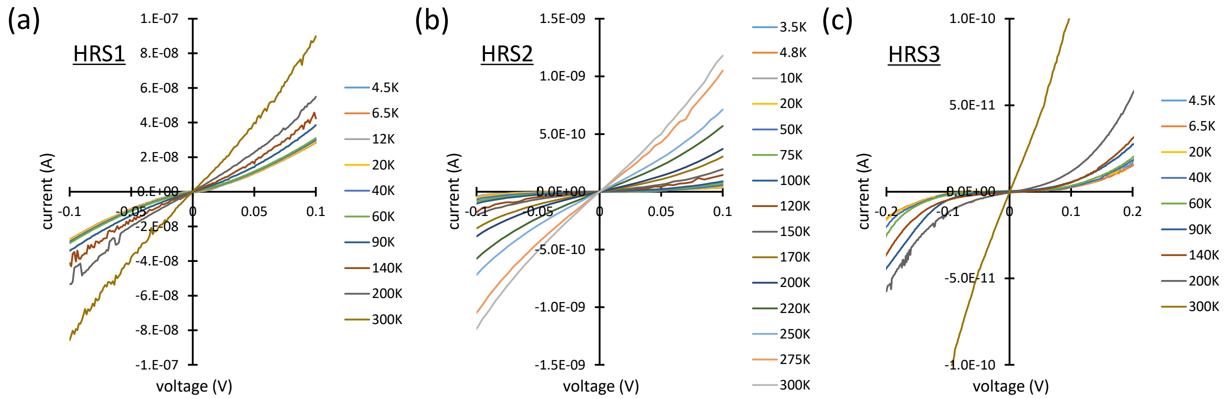

Figure 4-5 Temperature dependence (300K to 4.2K) of I-V characteristics of HRS1 (a), HRS2 (b), and HRS3 (c). (Memory cell: Ru/Ta_2O_5(10nm)/TiO_2(3nm)/Ru stack (A4), Cell size: 0.28um)

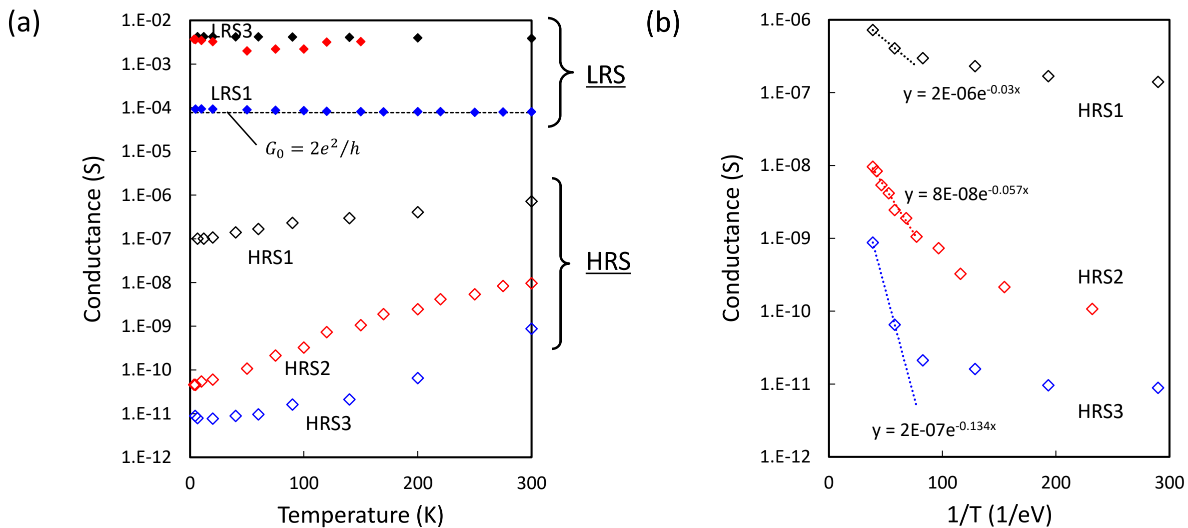

Figure 4-6 (a) Temperature dependencies of zero-bias conductance. Dashed line is the quantum conductance. (b) Arrhenius plot of the zero bias conductance of HRSs, re-plotted from (a). Activation energy in temperature above 150K is 30meV for the HRS1, 57meV for the HRS2, and 134meV for the HRS3. (Note: Zero-bias conductance was calculated from the slope of the I-V curve between -15mV and 15mV.)

ii Thermally activated conduction around the room temperature

In §3-2, we analyzed the *I-V* characteristics of HRS with *P.-F.* emission model, however, the model could not explain the various HRSs, consistently.

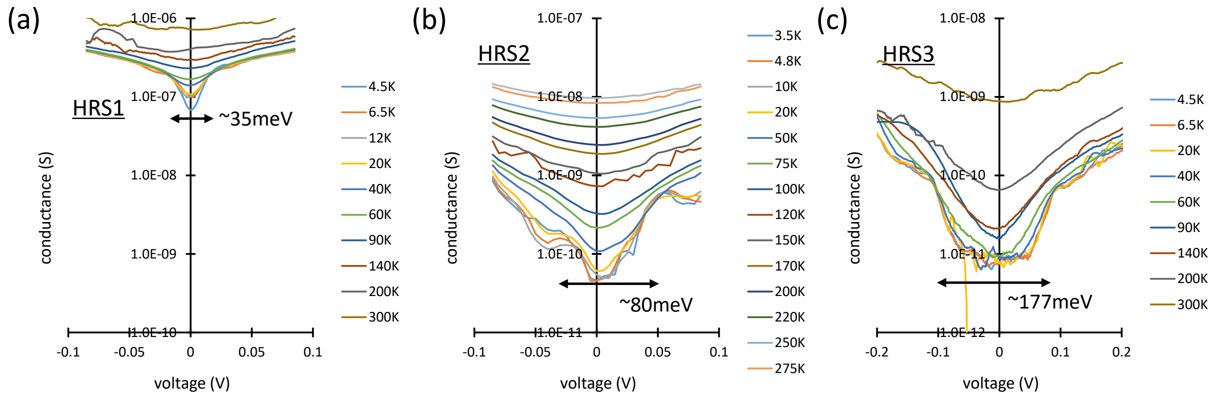

Figure 4-7 Temperature dependence of dI/dV-V characteristics in HRS1 (a), HRS2 (b), and HRS3 (c). The dI/dV near zero-bias depends strongly on temperature. The region (ΔE), which defined as inflection point of the dI/dV-V characteristics, is 35meV for HRS1, 80meV for HRS2, and 177meV for HRS3. (Memory cell: Ru/Ta_2O_5(10nm)/TiO_2(3nm)/Ru stack (A4), Cell size: 0.28um)

Figure 4-7 shows the temperature dependence of *dI/dV-V* characteristics in HRS1, HRS2, and HRS3. The *dI/dV* around zero-bias depends strongly on the temperature, and there seems to be a characteristic energy scale in the curves. For example, the width (ΔE) defined from the inflection points of the *dI/dV-V* characteristics, is 35 meV for HRS1, 80 meV for HRS2, and 177 meV for HRS3. We realized that this energy (ΔE) correlates with the activation energy calculated from the temperature dependence of the conductance as found in Figure 4.8.

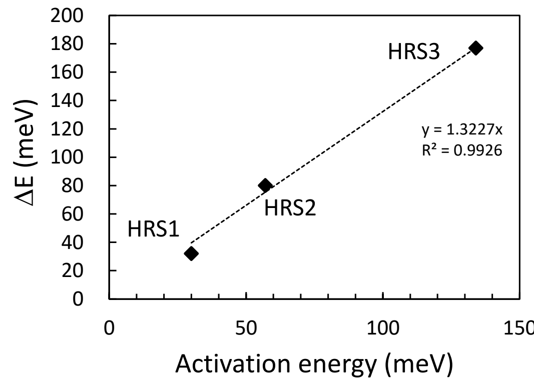

Figure 4-8 Correlation between the activation energy and the ΔE. Activation energy was calculated from the slope in the Arrhenius plot of the zero bias conductance (Fig. 4-2 (b)). ΔE was extracted from the Fig. 4-5.

In addition, at the lowest temperatures, fine structures become remarkable in the *dI/dV-V* characteristics of HRS2 and HRS3. As shown in Figure 4-9(b), the *dI/dV-V* curve below 90K have peaks at -0.23, -0.10, 0.08, and 0.30 V, which correspond kinks of the *I-V* characteristics [Figure 4-9(a)].

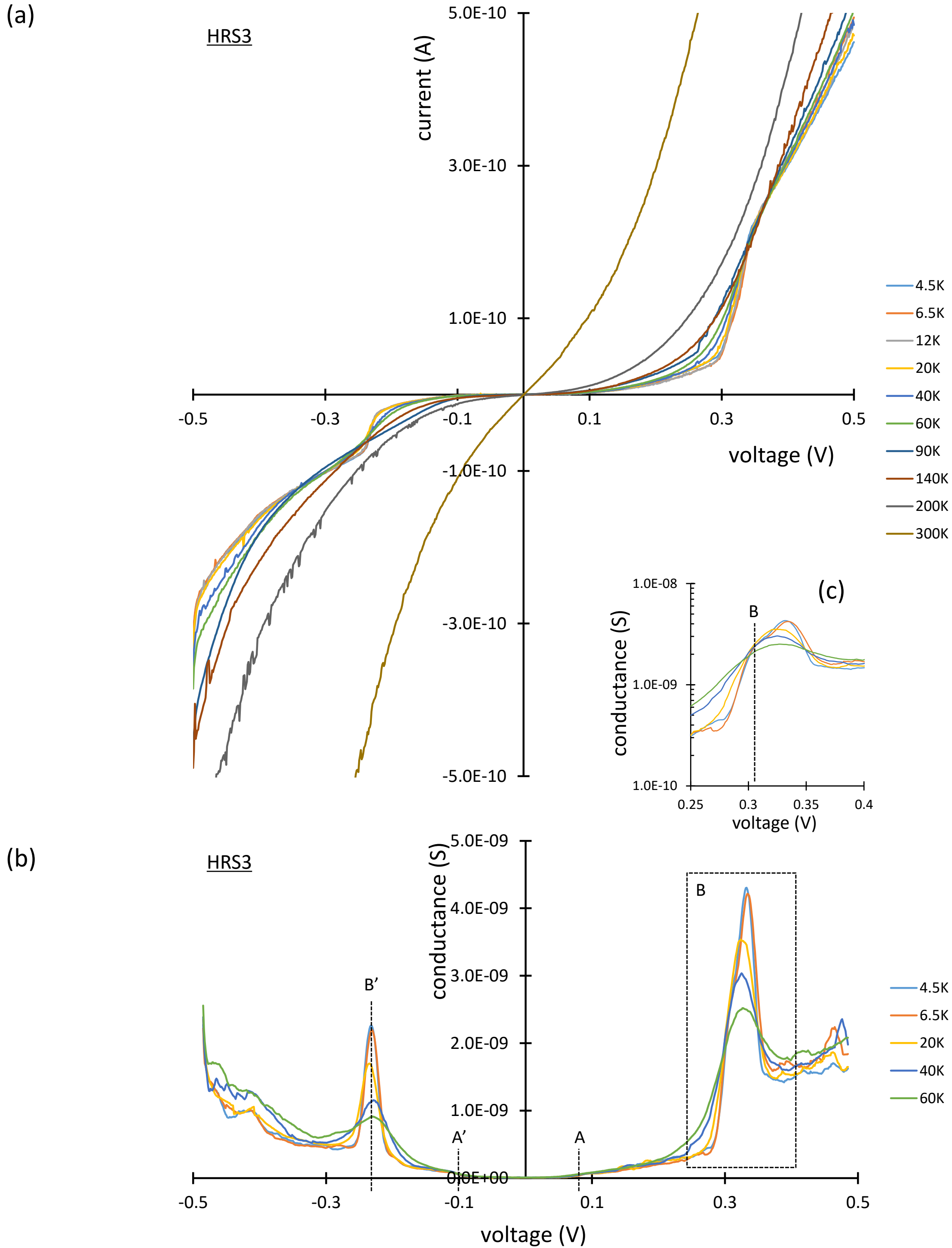

Figure 4-9 Temperature dependence (300K to 4.2K) of I-V characteristics between -0.5V and 0.5V (a) and dI/dV-V characteristics between -0.5V and 0.5V (b) in HRS3. Dashed lines indicate the kink structures. Magnified plot for B was re-plotted to (c) with semi-logarithm scales. In the double tunnel barrier model, the kink structures correspond to $(-e/2 - Q_0)/C_2$ for A', $(e/2 - Q_0)/C_2$ for A, $(-e/2 + Q_0)/C_1$ for B', and $(e/2 + Q_0)/C_1$ for B.

The fine structures in the I-V curves mean some other mechanism takes part in the tunnel conduction. Here, we point out that such kink structures can appear in single-electron tunneling transport via two (or more) tunnel barriers as shown in the Fig. 4-10(a) [9, 10]. Following Amman et al.'s model [11, 12], let a tunnel barrier be characterized by tunnel resistance (R_t) and capacitance (C). The single-electron tunneling phenomenon is observable under the conditions that i) the tunnel resistance is larger than the quantum resistance ($G_0^{-1} \sim 2.5 k\Omega$), and ii) the charging energy ($e^2/2C$) is larger than the thermal energy $k_B T$ [10, 11]. In this case, the resultant electron tunneling rate is

$$r_t(N,V) = \frac{1}{e^2 R_t} \frac{eV_t(N,V) - E_c}{1 + exp[(-eV_t(N,V) + E_c)/k_B T]}, \qquad (4-3)$$

where E_c is the charging energy, V_t is the voltage dropped on the tunnel barrier [12, 13].

For the sake of simplicity, we analyzed the data by the "double-tunnel-barrier model" with constant density of states and simple electrical field dependency of the tunneling probability. In the Fig. 4-10(a), $R_{1(2)}$ and $C_{1(2)}$ represent tunnel resistance and the capacitance of the top (bottom) side tunnel barrier [barrier I (II)], respectively. For sufficiently low temperatures, the current did not flow around zero bias, which leads to kink structures at -0.10 and 0.08 V. This phenomenon is the so-called "Coulomb blockage". In addition, the other two kink structures are the so-called "Coulomb staircase", which arises upon changing <N> in the region between tunnel barriers. We can calculate the $C_{1(2)}$ based on the *dI/dV* peak positions in the Fig. 4-9(b). In addition, we can calculate the $R_{1(2)}$ based on shape of the kink structure as shown in Figure 4-10(b). As shown in the Fig. 4-10(b), the simulated *I-V* curve in the case when the R_1/R_2 ratio is 10 does not agree with the experimental data, whereas the curve in the case when the ratio is more than 1000 agrees well with the data. A large (>1000) R_1/R_2 ratio means that the resistance of the top side tunnel barrier (barrier I) is the dominant factor in determining the resistance in the HRS. Finally, the kink structure of the simulated *I-V* curves closely matched the experimental results shown in Fig. 4-10(b) when C_1 = 0.291 aF, C_2 = 1.064 aF, $R_1 + R_2$ = 4 GΩ, and R_1/R_2 = 1000.

Table 4-1 Electrical properties of HRSs

Sample	Stack structure	G at RT (nS)	G at 4.2K (nS)	E_A above 150K (meV)	ΔE at 4.2K (meV)	$2E_C = e^2/(C_1+C_2)$ (meV)
HRS1	Ru/Ta_2O_5(10nm)/TiO_2(3nm)/Ru (A4)	723	101	30	35	-
HRS2		9.63	0.045	57	80	40
HRS3		0.876	0.0089	134	177	118

Note: I-V characteristic of HRS1 cannot be explained by the double-tunnel-barrier model.

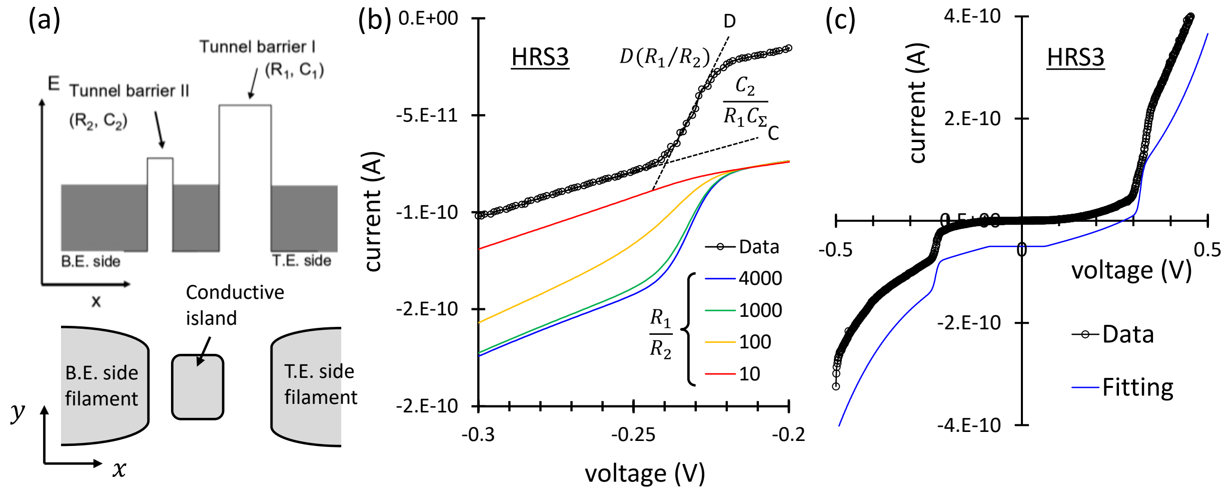

Figure 4-10 (a) Energy diagram of double-tunnel-barrier model. $R_{1(2)}$ and $C_{1(2)}$ represent tunnel resistance and the capacitance of the top (bottom) side tunnel barrier [barrier I (II)], respectively. (b) Simulated *I-V* curves when the R_1/R_2 ratios are 10, 100, 1000 and 4000. Slope of C is inversely proportional to the R_1, and slope of D is proportional to the R_1/R_2 in the double-tunnel-barrier model. The *I-V* curve when the ratio is 1000 agrees well with the experimental data. (c) Simulated I-V curve with $C_1 = 0.291aF$, $C_2 = 1.064aF$, $R_1 = 4G\Omega$, $R_1/R_2 = 1000$.

To summarize this section, we have analyzed the *I-V* characteristics of HRS at low temperatures. The conductance of HRS decreases in accord with the thermal-activation type dependence down to about 100 K, and levels off at the lowest temperatures. The *dI/dV-V* characteristics shows a dip at *V*=0, and the characteristic energy of the dip shows clear correlation with the activation energy. The *dI/dV-V* characteristics at the lowest temperatures show distinct peaks, and we showed the structures can be reproduced very well by the single-electron tunneling model, in which the current flows by way of a small island isolated from the leads by tunnel junctions. From these facts, we present a model for the HRS; By RESET operation, the conducting filament in the cell breaks, and the current is curried by tunneling there. Furthermore, in many cases, the fracture occurs at more than one points and the sequential electron tunneling via the isolated island takes place.

4-３ Physical model for high resistance state

In chapter 3 and chapter 4, we have argued the FORMING, SET and RESET phenomena and the electrical transport properties of pristine, high-resistance and low-resistance states of the Ta_2O_5/TiO_2 stacked cell. In this section, we will summarize the results and consider the physical model for each state and resistance change phenomena.

Concerning the resistance change phenomena in transition metal oxides (TMO), it is commonly accepted that filamentary conduction structure is generated by FORMING, and that the filament path is ruptured and regenerated by RESET and SET repeatedly. The filamentary nature of the conductance

path in our Ta_2O_5/TiO_2 stacked cell is confirmed by the fact that the LRS resistance is almost independent of cell area [13].

There are lots of papers on the microscopic entity of the conductive filament, mostly based on the first principle calculations, and they commonly ascribe it to oxygen vacancies. Rutile TiO_2 is a semiconductor and its conduction band is mainly of Ti 3d character while the valence band is of O 2p states. When one Introduce oxygen vacancies in TiO_2, the Fermi energy increases and it shows n-type conduction. If the deficiency of oxygen is large enough, the Fermi level can be expected to enter the conduction band, showing metallic conduction. In fact, the conductivity of oxygen-deficient Magneli phase, Ti_nO_{2n-1} ($3 < n < 10$), is as high as 25 – 2000 S/cm at room temperature [14]. It is also the case in Ta_2O_5, where the valence band are of O 2p character, while the conduction band is of Ta 5d character, and the Fermi energy increases as the oxygen vacancy is introduced. So, if sufficient amount of vacancies aggregate in these materials, it can form conductive path. Actually, Kwon et al. have identified Magneli phase Ti_4O_7 composition in the TEM image of the conductive filament of $Pt/TiO_2/Pt$ devices [15].

In our Ta_2O_5/TiO_2 stacked structure, filamentary conduction path is developed through both layers by FORMING. As we discussed in section 4-2, we can say any cross-section of the filament in Ta_2O_5 layer must have at least about 40 oxygen deficient sites. The filament is metallic in the sense that the resistance decrease at low temperatures, but the residual resistance ratio RRR is 1.14 at most, indicating that the random potential other than phonon is the predominant scattering mechanism. The resistance of LRS1, about 12.5 kΩ, is very close to the quantum resistance, suggesting that the filament in TiO_2 layer is very thin or highly disordered. Actually, RRR of this sample is 1.01, but the randomness is not so high as to cause prominent weak localization.

As mentioned in §3-2, resistance change occurs in the TiO_2 layer in the Ta_2O_5/TiO_2 stacked cell. Conventional picture of RESET is a rupture of the conductive filament. Microscopically, it should mean aggregated oxygen vacancies in the conductive filament disperse. Kope et al. made first-principle calculation of oxygen vacancies in TiO_2 [16]. Figure 4-11(b) shows the charge density of single oxygen vacancy state in TiO_2. The state is strongly localized in three nearest-neighboring Ti ions. The interatomic distance between the nearest Ti-Ti ions is 0.354nm (Figure 4-11(a)), and the energy of the defect state is about 0.4eV below the conduction band minimum.

In the previous section, we showed the *I-V* curve of HRS3 can be reproduced very well by the single electron tunneling model, and we gave a model for HRS, that is an isolated island on the current path playing a prominent role in the conduction. Now, it is possible to make rough estimation of the island size: The single-electron charging energy *E*c of the island evaluated from the fitting is $E_c = e^2/2(C_1 + C_2) = 118$ meV in case of HRS3. On the other hand, *E*c of a small conductor in TiO_2 medium whose relative dielectric constant is 40 (see §3-1) is 0.12eV when its diameter is 0.3 nm. Thus, the radius of island in the HRS3 is roughly estimated about 0.3 nm. Interestingly enough, it is close to the size of the isolated oxygen vacancy state mentioned above, and we may think the island is the single oxygen vacancy in the case of HR3.

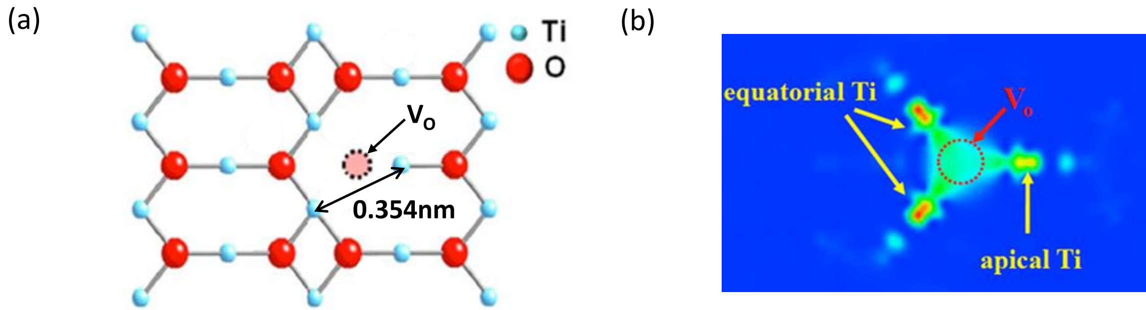

Figure 4-11 (a) Schematic picture of the (110) plane in rutile TiO_2 [16] (b) Band decomposed partial charge density distribution in TiO_2 (110) plane containing one isolated single oxygen vacancy [16]. The partial density of states for the nearest neighboring Ti ions.

In the actual resistance switching, oxygen ions have to get over the potential barrier to migrate. Although the potential barrier may be reduced by applied electric field, assistance of thermal energy should be essential for the switching. In the case of filamentary conduction, the temperature can rise easily by the current concentration. Balatti et al. calculate the local temperature using a simple model of thermal diffusion and Joule heating [17], and concluded that the local temperature of filament center rises to above 450 degree C at RESET [18]. Similarly, Borghetti et al. estimated the temperature of LRS filament of TiO_2. They measured the temperature coefficient of LRS resistance in advance, and using it as a resistance thermometer, they determined the temperature of the filament and the thermal resistance from the I-V curve during RESET. They concluded the local temperature of the LRS filament is as high as 550 K when RESET takes place. Very recently, Kwon et al. reported the local temperature of conductive filament in $Hf_{0.82}Al_{0.12}O_x$ can reach as high as 1600K at the onset of RESET [19].

During RESET operation, oxygen vacancies (oxygen ions) begin to migrate when the temperature rise due to Joule heating is large enough. As the thinning of conductive filament goes on, it may be accelerated by the current confinement. However, after the resistance jump to HRS by RESET occurs, the temperature decreases rapidly. As this process occurs in very short period of time and is inhomogeneous in nature, we think it rather natural that the dispersion of oxygen vacancy is imperfect and that fragments of filament can occasionally remain in the current path as shown in Figure 4-12(b).

Finally, we will briefly mention the mechanism of resistance change, which is a matter for active debate now. As we mentioned above, temperature is an important factor for the switching, but it should not enough. In the case of bipolar switching, redox reaction model is proposed. However it is apparently not applicable to the unipolar switching. Recently Kamiya et al. [20, 21] calculated the formation energy and energy band diagram of an oxygen vacancy (Vo-) chain, partial-Vo-chain and disrupt-Vo-chain in TiO_2, and derived Vo cohesive energy for the Vo-chain with respect to the isolated-Vo model. The defect energy levels Vo-chain model have large dispersion in the gap region, indication metallic conduction. This large dispersion leads to a large amount of electron energy gain when the electrons occupy the levels. As a result, the Vo-chain itself is stabilized when it captures electrons. On the other hand, if the electrons leave the chain, the chain becomes unstable and

disrupts to the isolated Vo's. Based on such consideration, they proposed a model for SET/RESET mechanism of TMO: the Vo cohesion-isolation transition upon carrier injection and removal is a strong driving force.

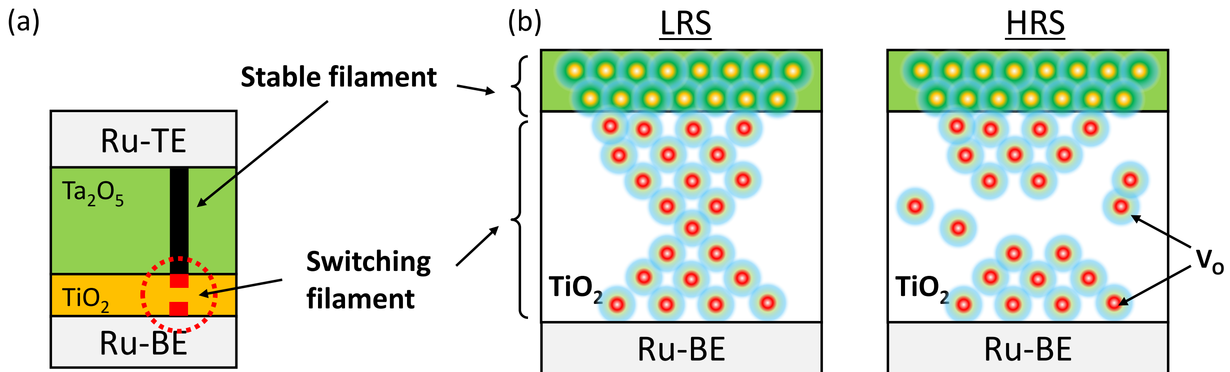

Figure 4-12 Schematics of conductive filament in the Ta_2O_5/TiO_2 stacked cell. (a) Resistance change phenomenon occur in the switching filament in the TiO_2 layer. (b) Magnified view for the switching filament in the TiO_2 layer. Isolated trap sites is remained on the current path after the RESET operation.

4-4 Summary

In this chapter, we examined *I-V* characteristics of HRS at the low temperature in details. We realized that the conductance of HRS decreases in accord with the thermal-activation type dependence down to about 100 K, and levels off at the lowest temperatures. The *dI/dV-V* characteristics shows a dip at *V*=0, and the characteristic energy of the dip shows clear correlation with the activation energy. The *dI/dV-V* characteristics at the lowest temperatures show distinct peaks, and we showed the structures can be reproduced very well by the single-electron tunneling model, in which the current flows by way of a small island isolated from the leads by tunnel junctions.

In accord with these facts, we constructed the physical model for HRS of the Ta_2O_5/TiO_2 stacked structure. The conductive filament formed in Ta_2O_5 layer is un-switchable stable filament and the resistance just depends on the compliance current at the FORMING operation. Resistance change phenomena occur in the switching filament in the TiO_2 layer. The HRS after RESET is insulating state where the traps remained in the gap across the ruptured filaments assists the tunneling through the gap. The probability of the trap-assisted tunneling is larger than that of the direct tunneling through the gap at the room temperature. At lower temperatures, the probability become smaller than that of the direct tunneling.

4-5 Reference

[1] J. F. Gibbons and W. E. Beadle, "Switching properties of thin NiO films", *Solid State Electronics Pergamon Press*, **7**, 785-797 (1964).

[2] F. Abgall, “Switching phenomena in titanium oxide thin films”, *Solid-State Elrctronics Pergamon Press*, **11**, 535-541 (1968).

[3] G. Dearnaley, A. M. Stoneham, and D. V. Morgan, “Electrical phenomena in amorphous oxide films”, *Rep. Prog. Phys.*, **33**, 1129–1191 (1970).

[4] A. L. Efros and B. L. Shklovskii, “Coulomb gap and low temperature conductivity of disordered systems”, *J. Phys. C*, **8**, L49 (1975).

[5] P.A. Lee, T.V. Ramakrishnan, “Disordered electronic systems”, *Rev. Mod. Phys.*, **57**, 287 (1985).

[6] X. Li, C. H. Tung and K. L. Pey, “The nature of dielectric breakdown”, Appl. Phys. Lett., Vol. 93, p. 072903, 2008

[7] Y. Yang, H.-H. Nahm, O. Sugino, and T. Ohno, “Electronic structures of oxygen-deficient Ta_2O_5”, *AIP Advances*, **3**, 042101 (2013).

[8] Y. Sakotsubo, M. Terai, S. Kotsuji, T. Sakamoto and H. Hada, "Physical Model for Reset State of Ta_2O_5/TiO_2-stacked Resistance Random Access Memory", *Jpn. J. Appl. Phys.*, **49**, 04DD19 (2010).

[9] T. A. Fulton and G. J. Dolan, “Observation of single-electron charging effects in small tunnel junctions”, *Phys. Rev. Lett.*, **59**, 109-112 (1987).

[10] C. W. J. Beenakker, “Theory of Coulomb-blockade oscillations in the conductance of a quantum dot”, *Phys. Rev. B*, **44**, 1646 (1991).

[11] M. Amman, R. Wilkins, E. Ben-Jacob, P. D. Maker, and R. C. Jaklevic, “Analytic solution for the current-voltage characteristic of two mesoscopic tunnel junctions coupled in series”, *Phys. Rev. B*, **43**, 1146 (1991).

[12] A. E. Hanna and M. Tinkham, “Variation of the Coulomb staircase in a two-junction system by fractional electron charge”, *Phys. Rev. B*, **44**, 5919 (1991).

[13, 27] M. Terai, M. Saitoh, T. Nagumo, Y. Sakotsubo, Y. Yabe, K. Takeda, and T. Hase, "High Thermal Robust ReRAM with a New Method for Suppressing Read Disturb", *2011 Symposium on VLSI, Tech. Dig.*, pp. 50-51 (2011)

[14] F.C. Walsh and R.G.A. Wills, “The continuing development of Magnéli phase titanium sub-oxides and Ebonex electrodes”, *Electrochimica Acta*, **55**, 6342-6351 (2010).

[15] D.-H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X.-S. Li, G.-S. Park, B. Lee, S. Han, M. Kim, and C. S. Hwang, “Atomic structure of conducting nano-filaments in TiO_2 resistive switching memory”, *Nature Nanotechnology*, **5**, 148 (2010).

[16] B. M.-Köpe, S.-G. Park, H.-D. Lee, Y. Nishi, “First principles calculations of oxygen vacancy-ordering effects in resistance change memory materials incorporating binary transition metal oxides”, *J. Mater. Sci.*, **47**, 7498–7514 (2012).

[17] D. Ielmini, “Modeling the Universal Set/Reset Characteristics of Bipolar RRAM by Field- and Temperature-Driven Filament Growth”, *IEEE Transactions on Electron Devices*, **58**, 4309-4317 (2011).

[18] S. Balatti et al., “Voltage-Controlled Cycling Endurance of HfOx-Based Resistive-Switching Memory”, *IEEE Transactions on Electron Devices*, **62**, 3365-3372 (2015).

[19] Kwon, Jonghan, et al. "Transient thermometry and high-resolution transmission electron microscopy analysis of filamentary resistive switches", *ACS Applied Materials & Interfaces*, 8.31, 20176-20184 (2016).

[20] K. Kamiya, M.Y. Yang, S.G. Park, B. Magyari-Köpe, Y. Nishi, M. Niwa, and K. Shiraishi, “ON-OFF switching mechanism of resistive–random–access–memories based on the formation and disruption of oxygen vacancy conducting channels”, *Appl. Phys. Lett.*, **100**, 073502 (2012).

[21] K. Kamiya, M.Y. Yang,.T.Nagata, S.G. Park, B.M. Kope, T. Chikyow, K. Yamada, M. Niwa, Y. Nishi, and K. Shiraishi, “Generalized mechanism of the resistance switching in binary-oxide-based resistive random-access memories”, *Phys. Rev. B*, **87**, 155201 (2013).

Chapter 5. Non-volatile memory performance of Ta_2O_5/TiO_2 stacked structure

In the preceding chapters we argued the transport characteristics of Ta_2O_5/TiO_2 stacked cell, including *I-V* curves of pristine state, LRS and HRS, and the resistance change phenomena at FORMING, SET and RESET. Originally, this stack cell was proposed as a suitable system for the resistance change memory application [1]. As mentioned in the Chapter 1, the practical memory cell must satisfy the following three requirements; highly READ/WRITE latencies, long cycle endurance, and long retention time. Among them, the most interesting function in the filamentary switching devices is the cycle endurance property, because the evidence of cycle endurance was very poor compared with that in the interface switching devices. It is considered that the risk of unnecessary additional or thicker filament formation at switching operations, which causes the RESET failure as described in the Chapter 1, is very high in the filamentary switching devices intrinsically. The idea of Terai et al. [1] was that the stable conducting filament In Ta_2O_5 layer prevent the formation of succeeding unnecessary filaments, while the resistance change takes place in spatially confined TiO_2 layer. In order to confirm this expectation, we examined the operation condition for SET and RESET, and demonstrated the memory function of Ta_2O_5/TiO_2 stack cell on 1 kbit memory cell arrays.

5- 1 Integrated Ta_2O_5/TiO_2 stacked memory cell to the 1 kbit array

I-V characteristics of as-deposited Ta_2O_5/TiO_2 stacked structure needs to satisfy some requirements in order for the FORMING operation to succeed. First of all, the leakage current at FORMING voltage must be smaller than the compliance current, if not, electrical breakdown voltage cannot applied to the cell. The compliance current is frequently set to 50 μA or more to realize ohmic LRS. On the other hand, the compliance current should be suppressed for achieving low power operation.

As clarified in §3-1, leakage current and FORMING voltage of as-deposited Ta_2O_5/TiO_2 stacked structure depend on the electrical field in the Ta_2O_5 layer. This means that the leakage current at FORMING does not depend on the thickness of each layer. Based on *P.-F.* emission model, the leakage current density is proportional to trap density in the Ta_2O_5 film which depends on deposition process conditions [2].

In general, the post deposition annealing in oxygen or ozone atmosphere is useful for reducing the trap density in oxides [3]. However, leakage current and cell-to-cell variation increase simultaneously with the reduction due to crystallization of Ta_2O_5. Therefore, our Ta_2O_5 was just deposited below a crystallization temperature in an oxygen atmosphere [4].

Figure 5-1(a) shows the cell area dependence of the leakage current at the FORMING voltage of Ta_2O_5/TiO_2 stacked structure. Our Ta_2O_5/TiO_2 stacked structure can be operated with below 1 μm^2 cell area.

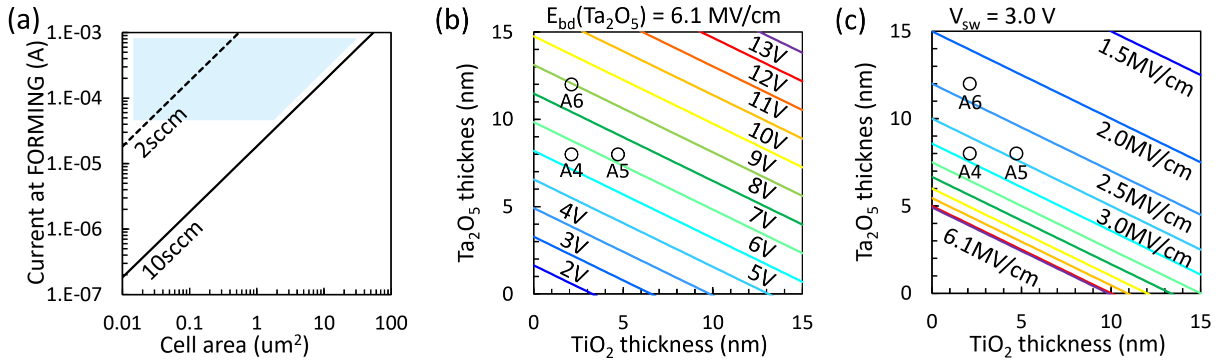

Figure 5-1 (a) Cell area dependence of leakage current at FORMING. Current density at FORMING voltage is about 1830 A/cm^2 in our Ta_2O_5 film (O_2-flow: 10 sccm), which value does not depend on the thickness. Blue color shows the configurable operating region. Dashed line shows the dependence in using leaky Ta_2O_5 film (O_2-flow: 2 scccm). (b) Contour plot of estimated FORMING voltage dependence on Ta_2O_5 and TiO_2 thickness in Ta_2O_5/TiO_2 stacked structure. $E_{bd}(Ta_2O_5)$ = 6.1 MV/cm was used in this estimation. If larger voltage than the FORMING voltage was applied during the SET/RESET operations, additional conductive filament is formed in the Ta_2O_5 layer. (c) Contour plot of in-Ta_2O_5 layer electrical field dependence on Ta_2O_5 and TiO_2 thickness in Ta_2O_5/TiO_2 stacked structure under 3.0 V.

Trap density in the Ta_2O_5 layer is increased with cumulative electrical stress during SET/RESET cycling operation [5-9]. If the trap density becomes percolation density which bridge the two electrodes across the oxide, it will adversely affect resistance change operation [10, 11]. As introduced in the Chapter 1, generation ratio of defects act as the trap increases exponentially with electrical field in the Ta_2O_5 layer. Therefore, reduction of electrical field in Ta_2O_5 layer is a key for improving the SET/RESET cycle endurance.

The electrical field in Ta_2O_5 layer depends on the switching voltage and the thickness of Ta_2O_5/TiO_2 stacked structure. Figure 5-1(b) shows the contour plot of estimated FORMING voltage dependence on Ta_2O_5 and TiO_2 thickness in the Ta_2O_5/TiO_2 stacked structure. 6.1 MV/cm as a breakdown electric field of Ta_2O_5 was used in this estimation. If larger voltage than the FORMING voltage was applied during the SET/RESET cycling operation, additional conductive filament is formed in the Ta_2O_5 layer, which causes the RESET failure as described in the Chapter 1.

Contour plot of in-Ta_2O_5 layer electrical field dependence on Ta_2O_5 and TiO_2 thickness of the stack in case of V_{sw} = 3 V was shown in Figure 5-1(c). The increase in thickness of the Ta_2O_5 compared with the TiO_2 layer effectively reduces the electrical field as a result from the difference in electric permittivity. The electrical field in the Sample A6 is 30% smaller than that in the Sample A4 as shown in the Figure 3-7(c).

Thicker Ta_2O_5 layer is effective to suppress the additional conductive filament during the SET/RESET cycling operation, however, the increase in the layer thickness is limited from the breakdown voltage of series transistor. In this study, the transistor was fabricated by using the standard CMOS process, and the maximum operating voltage is about 5.5 V. Then, acceptable Ta_2O_5 thickness is less than 9 nm in maximum.

Optimized Ta_2O_5/TiO_2 stacked cell was integrated between Cu interconnects on the 1 kbit array with bit-line-shared 1T-1R type memory cell. We can access randomly to the single memory cell by adapting voltage to the BL (Bit line) and WL (Word line) selectors with an appropriate procedure as shown in Figure 5-2(a). Figure 5-2(b) shows the cross-sectional TEM image of the integrated Ta_2O_5/TiO_2 stacked cells. The TiO_2 for switching layer was formed by the post-plasma oxidation method with the B2 condition. As we discussed in §2-1, the resistance caused by the Ruthenium oxidization is small in B2-samples.

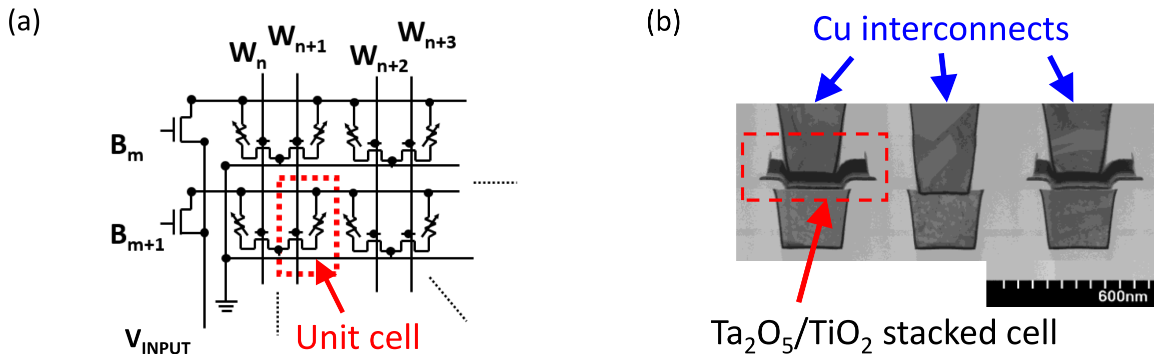

Figure 5-2 (a) Schematic circuit diagram of 1kbits 1T-1R device array. (b) Cross-sectional TEM image of the integrated Ta_2O_5/TiO_2 stacked cells.

5-２ Optimization of SET/RESET operation

To reserve sufficient margin between SET and RESET operations is the most important for improving the cycle endurance. In chapter 3, we found that the switching voltage V_{RESET} (V_{SET}) varies depending on the resistance just before the resistance change RESET (SET) occurs as indicated in Fig. 3-10(a) and Fig.3-17. On the other hand, the resistance R_{LRS} (R_{HRS}) after the resistance change varies depending on the condition of SET (RESET) operation, i.e. the compliance current and the maximum applied voltage as depicted in Fig. 3-18(a) and Fig. 3-16(b). (In Fig. 5-3, we reshow these graphs again.) These graphs mean that we have a chance to optimize cycle endurance by tuning various parameters in SET/RESET operations.

At first, we will consider the RESET voltage. To get a good margin, i.e., to make the V_{SET}/V_{RESET} ratio large, we should reduce V_{RESET} (I_{RESET}). Reducing I_{RESET} is important particularly in the Ta_2O_5/TiO_2 stacked cells, because there adds IR drop due to the series resistance of the stable filament in the Ta_2O_5, and the transistor, that is not negligibly small in the device as we have discussed in §3.2. Looking at Fig.3-10(b), we find V_{RESET} becomes minimum at around 0.5~0.6V when G_{LRS} = 0.5~1 mS. So we should make the conductance 0.5 ~ 1 mS after SET.

The conductance after SET, G_{LRS}, is mainly influenced by the compliance current at the SET operation. Fig. 3-18(a) (Fig. 5-3(d)) shows the relation, from which we know I_{COMP} should be about 200 μA to get G_{LRS} = 0.5 ~ 1 mS. In Chapter 3, we measure the *I-V* characteristics of devices using quasi-DC method,

i.e., by measuring the voltages while sweeping the bias voltage rather slowly. In actual memory operation, however, SET, RESET and READ are done within a short time using pulses. Figure 5-4(a) shows the G_{LRS} distribution of conductance after SET operation. Here, we plot two data, i.e., the results of the DC method and the pulse method. In the DC method, the voltage was increased from 0 up to 3.0 V with 100 mV incremental step and 10 ms dwell time, while single 1 us pulse with 3.0 V height was applied in the pulse method. In both cases, the compliance current was set to the same value, i.e., 300 μA. We find two data do not coincide, but the conductance after pulsed SET operation is smaller than that after DC-swept SET operation. It means the magnitude of the compliance current is not the only factor influencing the G_{LRS}, but the duration of the compliance current affects it, presumably. Anyway, results of pulse method obtained in Figure 5-4(a) satisfy the requirement of G_{LRS} = 0.5 ~ 1 mS. Thus, we determine the parameters of SET operation; single 1 μs pulse with 3.0 V height and the compliance current of 300 μA, in this case we expect V_{RESET} to be around 0.5 ~ 1.0 V. As shown in Figure 5-5, the distribution of RESET voltage for the LRS prepared by I_{COMP} = 300 μA is rather sharp comparing with I_{COMP} = 1 mA case.

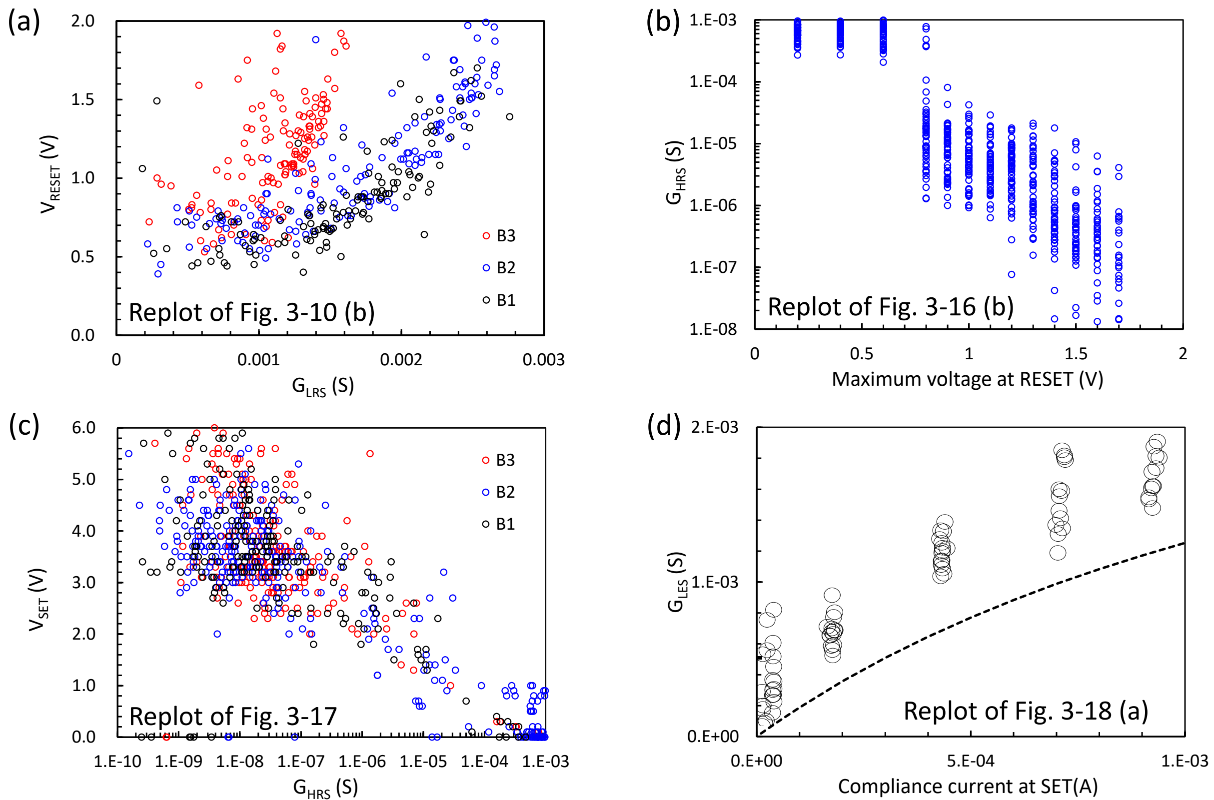

Figure 5-3 SET and RESET characteristics of Ta_2O_5/TiO_2 stacked cells (Replot after Chapter 3).

Now we will move to the SET voltage, V_{SET}. To get a good margin, larger V_{SET} seems desirable. But the situation is not so simple, because if the V_{SET} so large that it is comparable to the FORMING voltage ($V_{FORMING}$), the possibility of generation of additional filaments which brings about irreversible change in the characteristics becomes large. So, we should avoid such a high V_{SET} and tune V_{SET} at the moderate voltage. As seen in Fig. 3-17 (Fig. 5-3(c)), V_{SET} strongly depends on the resistance of the

HRS. When the R_{HRS} is as large as 100 MΩ, V_{SET} can be larger than 5.0 V, that is close to $V_{FORMING}$. In order to get moderate V_{SET}, e.g. 2.0 ~ 3.0 V, which is substantially smaller than $V_{FORMING}$ and at the same time enough larger than V_{RESET}, R_{HRS} should be 0.1 ~ 10 MΩ.

The resistance of HRS can be controlled by how large voltage is applied after RESET. Fig. 3-16(b) (Fig. 5-3(b)) depicts the resistance after applying 1 μs pulse with various height, V_{Ext}. In this case, the resistance does not change when V_{Ext} < 0.6 V. The resistance change occurs at V_{Ext} =0.65 ~ 0.75 V, that means V_{RESET} = 0.65 ~ 0.75 V. When the pulse height is 0.8 ~ 1.2 V, the resistance after pulse stays at around 100 kΩ, and at larger V_{Ext} region, R_{HRS} gradually increases. Figure 5-4(b) is the normal probability plot for the distribution of R_{HRS} after RESET operation by 1 μs pulse with various height. We understand that 1.0 V-height gives sharp R_{HRS} distribution. It is expected that the V_{SET} is less than 3.0 V even in 3σ, and this value is enough smaller than the $V_{FORMING}$.

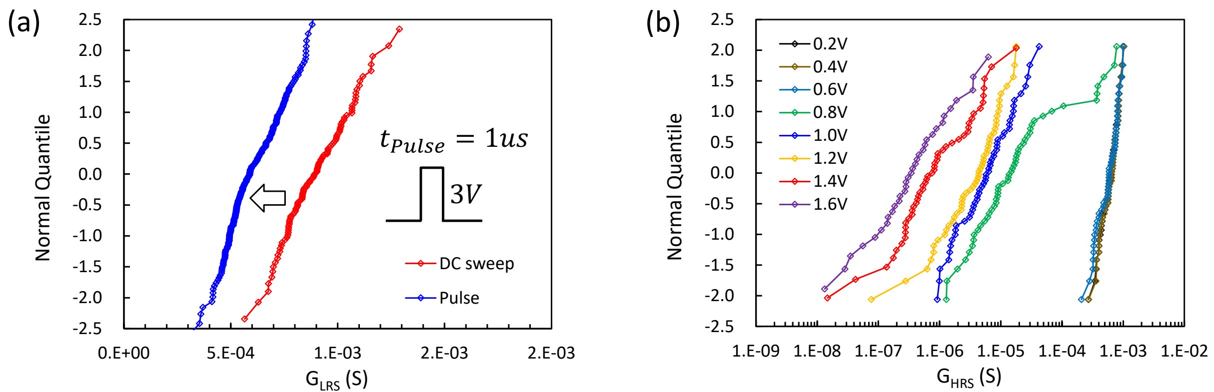

Figure 5-4 (a) Normal probability plots of LRS conductance from different SET operations. Red plots are the data come from the dc sweep method which was done by stepping the voltage from 0.0V to 3.0V with 100mV-step. Stress-time for each steps is about 10msec. Blue plots are the data come from the pulse method which was done by applying the single 1us-pulse with 3.0V-height. (b) Normal probability plots of cell conductance after RESET pulses. The plots are the data come from the pulse method which was done by applying the single 1us-pulse with different pulse height. 1.0V-height pulse achieves tight distribution around 100kΩ as shown with blue color.

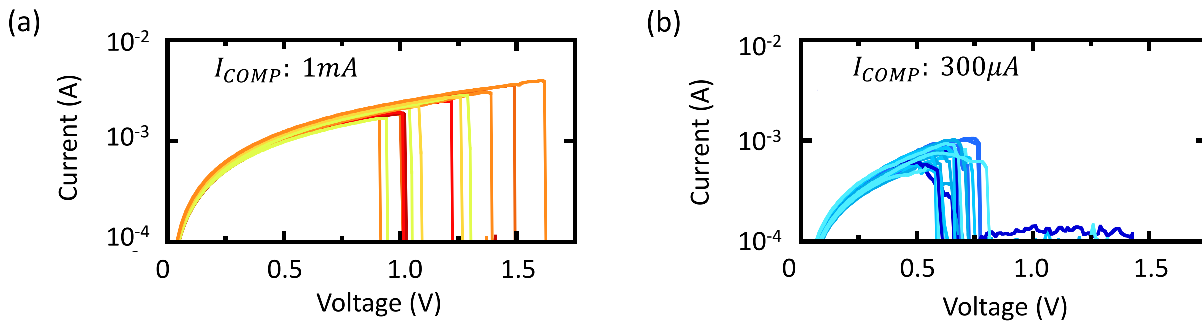

Figure 5-5 I-V curves at RESET operation with different I_{COMP} at SET operation: I_{COMP}=1mA (a), I_{COMP}=300uA (b). I_{COMP}=300uA condition has small variation in V_{RESET}.

5-３ Demonstration of highly robust non-volatile memory

From the consideration in previous section, we determine the optimum operation condition for our memory device, that is summarized in Table 5-1. Using them, we performed SET-RESET cycles on 1 kbit array.

Table 5-1 Optimum operation condition for our memory device.

Operation	Pulse height	Pulse width	Compliance current	Target specs
FORMING	5.5V	dc (~10ms)	300μA (Vg=1.5V)	G_{LRS} ~ 0.5mS
SET	3.0V	1μs	300μA (Vg=1.5V)	G_{LRS} ~ 0.5mS
RESET	1.0V	1μs	N/A (Vg=5.0V)	G_{HRS} < 10μS

Note: FORMING operation was not optimized in this study. FORMING operation was done by sweeping the voltage from 0.0V to 5.5V with 100mV-step. Stress-time for each steps is about 10msec.

Figure 5-6(a) shows schematic of test system for 1 kbit 1T-1R device array (see Fig. 5-2(a)). READ and WRITE were performed by using an external source measure unit (SMU), pulse generators (PG), and constant voltage sources. The system includes two modes, DC mode and Pulse mode. DC mode was used in READ and getting *I-V* curves. Pulse mode was used in SET and RESET cycling test. Switching between the DC mode and the Pulse mode was performed with an external controller.

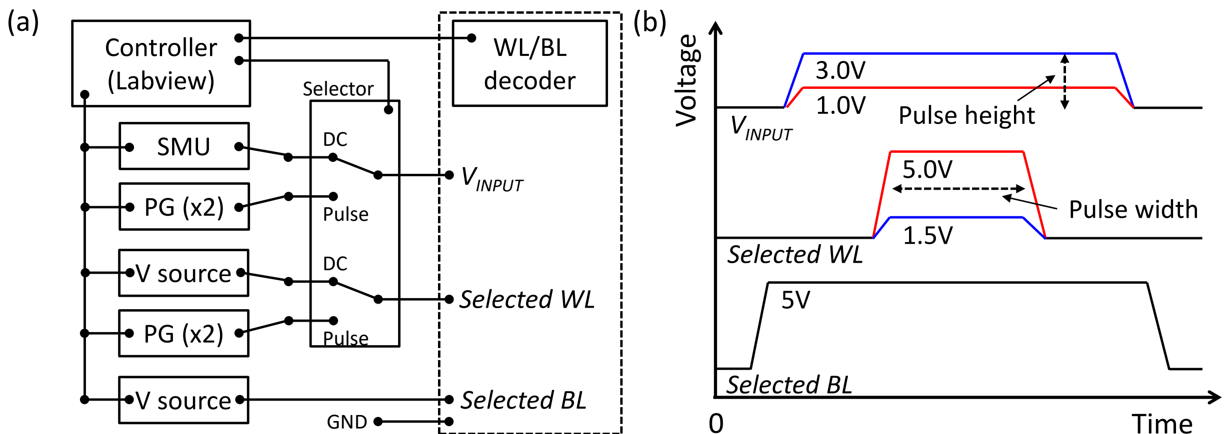

Figure 5-6 (a) Schematic test system for 1kbits 1T-1R device array. READ, SET and RESET were performed by using external source measure unit (SMU) and pulse generators (PG). The system includes two modes, DC mode and pulse mode. DC mode was used in READ and getting I-V curves. Pulse mode was used in SET and RESET cycling test. Switching between DC mode for and pulse mode was performed with an external controller (*Labview*). (b) Schematics of input waveform to input terminals. Two type waveforms were prepared for both SET and RESET operations. Blue line and red line show the waveform for SET and RESET, respectively. Waveform of input pulse to the 1T-1R device is defined by both V_{INPUT} and $V_{Selected\ WL}$. The V_{INPUT} and $V_{Selected\ WL}$ determines amplitude and width of the input pulse, respectively. $V_{Selected\ WL}$ at SET is set to small value for limiting the current during SET operation.

Figure 5-6(b) shows input waveform to the input terminals. Two type waveforms for SET and RESET operations were performed. Red line and blue line show the waveform for SET and RESET,

respectively. Waveform of input pulse to the 1T-1R device is defined by both V_{INPUT} and $V_{Selected\ WL}$. V_{INPUT} and $V_{Selected\ WL}$ determines amplitude and width of the input pulse, respectively. $V_{Selected\ WL}$ at SET is set to 1.5 V for limiting the current during SET operation.

Figure 5-7 shows cycle-to-cycle variation of the switching voltages with the optimized conditions, i.e. the compliance current at SET operation is 300 μA, and the operating voltage for RESET is 1.0 V. We confirmed (i) tight V_{RESET} distribution around 0.4 V ~ 0.7 V, (ii) enough voltage margin between the operating voltage for RESET (1.0 V) and distribution tail of V_{SET}, and (iii) enough voltage margin between operating voltage for SET (3.0 V) and the voltage for forming additional filament to the Ta_2O_5 layer (~5.5V).

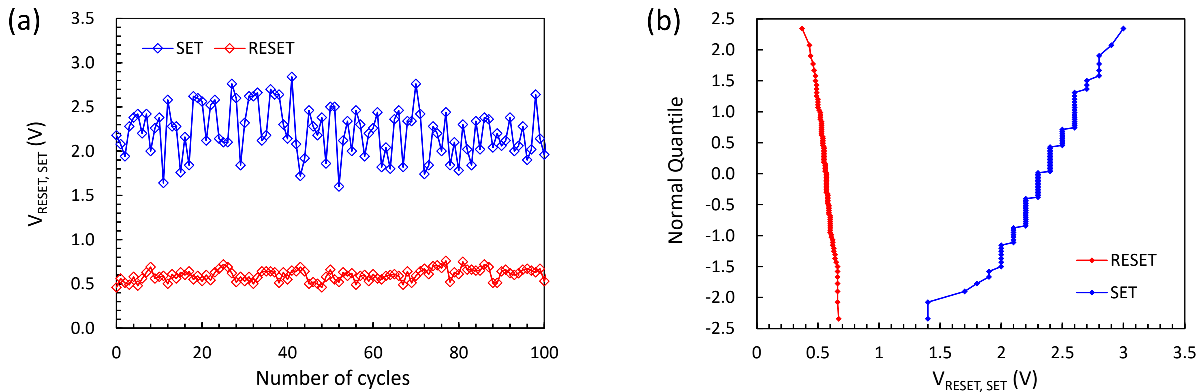

Figure 5-7 (a) V_{SET} and V_{RESET} dependence on cycle. (b) Normal probability plots of V_{SET} and V_{RESET} from optimized operating conditions. Gate voltages were set to 1.5V and 5.0V at SET and RESET operation, respectively. (Note: RESET operation was done by sweeping the voltage from 0.0V to 1.0V with 10mV-step. SET operation was done by sweeping the voltage from 0.0V to 3.0V with 100mV-step. Stress-time for each steps is about 10msec.)

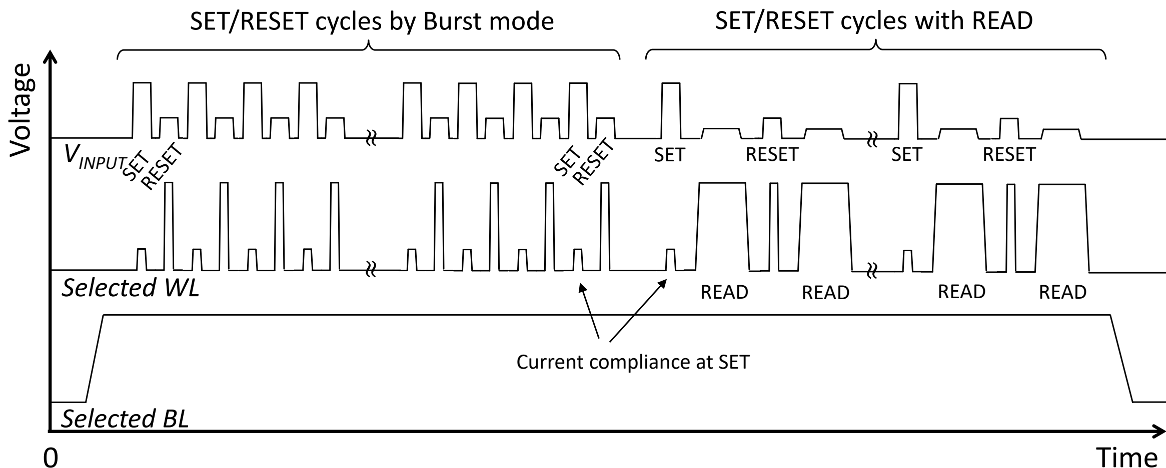

Figure 5-8 Schematics of cycle endurance test. SET/RESET cycling was done by using burst mode in the function of the pulse generator(81110C, Agilent). The cell current after WRITE was monitored by using SMU of the semiconductor parametric analyzer(4156C, Agilent), intermittently.

Based on the above switching evidence, we performed SET-RESET cycle endurance test on 1 kbit array by using optimized switching condition shown in the Table 5-1. Schematics of cycle endurance test was shown in Figure 5-8. SET-RESET cycling was done by using burst mode in the function of the pulse generator (81110C, Agilent). The cell current after SET and RESET was monitored by using SMU of the semiconductor parametric analyzer (4156C, Agilent), intermittently.

Figure 5-9(a) shows the result of cycle endurance test at room temperature. The cell current after SET and RESET was monitored by using SMU of the semiconductor parametric analyzer (4156C, Agilent) as shown in the Fig. 5-8. Bars in the plot means standard deviation of the cell-to-cell distribution on 1 kbit array. LRS/HRS conductance ratio keeps about 100 in median even after 100k cycles. We believe that additional filament was not formed in the Ta_2O_5 layer during the 100kcyces.

Figure 5-9(b) shows the thermal stability of the LRS and HRS. We prepared 500 states for each LRS and HRS on 1 kbit array, respectively. The cell current after bake at 100 degrees C was monitored by using the SMU, intermittently. The states hardly depends on the stress time. The conductive filament formed in the Ta_2O_5/TiO_2 stacked cell is enough stable under the 100 degrees C.

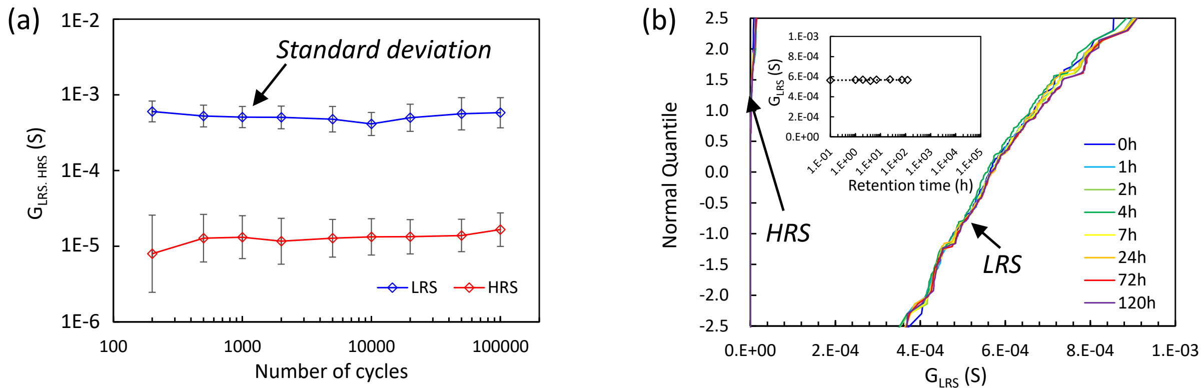

Figure 5-9 (a) SET/RESET cycling endurance at room temperature. The cell current after SET and RESET was monitored by using SMU of the semiconductor parametric analyzer(4156C, Agilent) as shown in the Fig. 5-8. Bars on the plot means standard deviation of the cell-to-cell distribution on 1 kbit array. LRS/HRS conductance ratio keeps about 100 even after 100k cycles in median. (b) Thermal stability of the LRS and HRS conductance. 500 states for LRS and HRS were prepared on 1 kbit array, respectively. The cell current after bake at 100 degrees C was monitored by using SMU of the semiconductor parametric analyzer(4156C, Agilent), intermittently. The states hardly depends on the stress time.

5-４ Summary

We have tested 1 kbit unipolar-type non-volatile memory using Ta_2O_5/TiO_2 stack. Optimized Ta_2O_5/TiO_2 stacked cell was integrated between Cu interconnects on the 1-kbit array with bit-line-shared 1T-1R type memory cell: 3 nm-TiO_2 for switching layer was formed by the post-plasma oxidation method with the B2 condition, and 8 nm-Ta_2O_5 for stable layer was formed on the TiO_2 layer by RF sputtering for Ta_2O_5 target.

We applied the optimized SET/RESET condition to the cycle endurance test; i.e., the compliance current at SET operation is 300 μA, and the operating voltage for RESET is 1.0 V. As a result, excellent

operation margin and more than 10^5 set/reset cycling times was successfully demonstrated using the integrated device. Moreover, the conductance in both LRS and HRS was thermally stable even at 100 degrees C. Device parameters accomplished in this study are summarized in Table 5-2. Filamentary resistance change-based memory function was firstly demonstrated on 1kbits array [12].

Table 5-2 Device parameters of this study compared to other published results.

Cell structure	Ru/NiO/WOx/W (Ref. 13)	$Ru/Ta_2O_5/TiO_2/Ru$ (This study [12])
Device structure	1T-1R (Single bit)	1kbits array with 1T-1R
RESET current	~1mA (Typical)	0.2~0.3mA
RESET voltage	~0.5V (Typical)	0.40V ~ 0.65V
SET voltage	~1.0V (Typical)	1.4V ~ 3.0V
Operating voltage margin	N/A	~0.75V
LRS/HRS ratio	~1000 (Typical)	~100
Cycle endurance	N/A	$>10^5$
Data retention	N/A	>120h at 100 degrees C

Note: Filamentary resistance change-based memory function was firstly demonstrated on 1kbits array [12].

5-５ Reference

[1] M. Terai, S. Kotsuji, H. Hada, N. Iguchi, T. Ichihashi, and S. Fujieda, “Effect of ReRAM-Stack Asymmetry on Read Disturb Immunity”, *IRPS Tech. Dig.*, pp. 134-138 (2009).

[2] R. M. Fleming, D. V. Lang, C. D. W. Jones, M. L. Steigerwald, D. W. Murphy, G. B. Alers, Y.-H. Wong, R. B. van Dover, J. R. Kwo, and A. M. Sergent, “Defect dominated charge transport in amorphous Ta_2O_5 thin films”, *J. Appl. Phys.*, **88**, 850-862 (2000).

[3] P. C. Joshi and M. W. Cole, “Influence of postdeposition annealing on the enhanced structure an electrical properties of amorphous and crystalline Ta_2O_5 thin films or dynamic random access memory applications”, J. Appl. Phys. **80**, 871-880 (1999).

[4] Y. Sakotsubo, M. Terai, M. Tada, Y. Yabe, and Y. Saito, “SEMICONDUCTOR DEVICE WITH VARIABLE RESISTANCE ELEMENT AND METHOD FOR MANUFACTURING THE SAME”, US 8,766,233 (2014).

[5] D. Ielmini and R. Waser, “Resistive switching from fundamentals of nanoionics redox processes to memristive device applications” *WILEY-VCH* (2016).

[6] M. A. Alam, “A Study of Soft and Hard Breakdown-Part I: Analysis of Statistical Percolation Conductance”, *Electron Devices*, **49**, 232-238 (2002).

[7] M. A. Alam, “A Study of Soft and Hard Breakdown-Part II: Principles of Area, Thickness, and Voltage Scaling”, *Electron Devices*, **49**, 239-246 (2002).

[8] J. Sune, “New physics-based analytic approach to the thin oxide breakdown statistics”, *Elec. Dev. Lett.*, **22**, 296-298 (2001).

[9] E. Wu and J. Sune, “Power-law voltage acceleration: a key element for ultra-thin gate oxide reliability”, *Microelectronics reliability*, **45**, 1809-1834 (2005).

[10] R. Degraeve, P.H. Roussel, L. Goux, D. Wouters, J. Kittl, L. Altimime, M. Jurczak, and G. Groeseneken, “Generic learning of TDDB applied to RRAM for improved understanding of conduction and switching mechanism through multiple filaments”, *IEDM Tech. Dig.*, pp. 633-636 (2010).

[11] M. A. Alam, “Statistically independent soft-breakdown redefine oxide reliability specifications”, *IEDM Tech. Dig.*, pp. 151-154 (2002).

[12] Y. Sakotsubo, M. Terai, S. Kotsuji, Y. Saito, M. Tada, Y. Yabe, and H Hada, "A New Approach for Improving Operating Margin of Unipolar ReRAM using Local Minimum of Reset Voltage", *2010 Symposium on VLSI (VLSI-8-2), Tech. Dig.*, pp. 87-88 (2010).

[13] H. S. Yoon, et al. Symp. On VLSI Technol., p. 26, (2009).

Chapter 6. Summary

We have investigated the resistance change phenomena in Ta_2O_5/TiO_2 stacked structure which is expected to work as a non-voluntary random access memory.

In chapter 3, we argued FORMING, SET and RESET phenomena in the Ta_2O_5/TiO_2 stacked cell. The LRS resistance is almost independent from the cell size, which means the resistance change of this system is filamentary-type. Unipolar SET/RESET switching was found to be possible in this device, and from the analysis of the switching parameters, especially that of the RESET voltage, we conclude the resistance change phenomenon in the Ta_2O_5/TiO_2 stacked cell is brought about by disruption and re-formation of the conductive filament in the TiO_2 layer, while the filament in Ta_2O_5 layer does not switch. We found two facts through the analysis. Firstly, we identified the resistance of the stable filament in the Ta_2O_5 layer from the switching parameters of the RESET. The resistance depends on not only the device structure such as the cell size and TMO thickness but also the method of the FORMING operation. Secondly, the disruption of the conductive filament in the TiO_2 layer is caused by the joule heating-induced thermal reaction.

In Chapter 4, we investigated the conduction mechanism of the HRS by analyzing the I-V characteristics at the low temperatures. The LRS shows the metallic conduction; the resistance slightly decreases at low temperatures. On the other hand, the resistance of HRS shows thermal-activation type increase down to about 100K, below which it ceases to increase. We found distinct structures in the differential conductance curve of HRS at the lowest temperature, and analyzed the data by two-barrier model. As a result, we realized that the conduction in the HRS is composed of not only the direct tunneling but also the trap-assisted tunneling. The thermally activated behavior in the zero-bias conductance could be well explained by this model.

In Chapter 5, unipolar type non-volatile memory with Ta_2O_5/plasma oxidized TiO_2 stack was demonstrated on 1 kbit array. At first, we considered the condition for good SET/RESET cycle endurance based on the data obtained in chapter 3, and obtained the optimum operating parameters such as the I_{COMP} at SET operation and the pulse height for RESET. Excellent operation margin and more than 10^5 set/reset cycling times was successfully demonstrated using the integrated device.