

1 **Sn-inserted Al-induced layer exchange for large-grained GeSn thin films**
2 **on insulator**

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10 Large-grained polycrystalline GeSn layers on glass are achieved through the layer exchange
11 between a-Ge and Sn-doped Al layers. The thicker Sn layers, inserted below Al layers,
12 provided the faster growth velocity, resulting in the smaller grain size of the GeSn layer.
13 Controlling the Sn thickness (10 nm) and the growth temperature (300 °C) allowed for
14 approximately 80% (111)-oriented GeSn layer with grains having an average size of 40 μm.
15 The lower growth temperature led to the higher Sn content in GeSn: 300 °C resulted in a Sn
16 content of 2%. These findings are meaningful to researches related to GeSn on insulators for
17 fabricating advanced electrical and optical devices on inexpensive substrates as well as on Si
18 platforms.

19

20 Keywords: Metal-induced crystallization; Al-induced layer exchange; Crystal orientation;
21 Solid phase crystallization; Polycrystalline films; Semiconducting germanium

22 **1. Introduction**

23 GeSn offers exciting possibilities as a next-generation material for advanced
24 electronic and photonic devices based on group-IV semiconductors [1,2]. Although the
25 solubility limit of Sn in Ge is as low as 1%, non-equilibrium low-temperature process using
26 molecular-beam epitaxy (MBE) [3-6], chemical-vapor deposition (CVD) [7,8], or ion
27 implantation [9] have allowed for Sn contents more than the solubility limit. These studies
28 have demonstrated the advantage of GeSn: the carrier mobility of GeSn exceeded that of Ge
29 [10,11]; the infrared detection capability, covering all the relevant telecommunications
30 wavelengths, is extended by Sn contents over 2% [12-14]; high substitutional Sn content (>
31 6%) in GeSn provides the direct transition in the near infrared region, allowing for lasing
32 [15,16].

33 The study of GeSn on insulators (GSOIs) has been accelerated for fabricating
34 monolithically integrated GeSn-based devices on three-dimensional Si large-scale
35 integrated circuits and on multi-functional displays with glass or plastic substrates [17-26].
36 The incorporation of 2% Sn into Ge passivated the vacancy defects or reduced the grain
37 boundary scattering, resulting in the higher carrier mobilities than Ge [18,19]. The
38 tin-induced crystallization (TIC) of amorphous Ge (a-Ge) has recently garnered attention
39 [23-26]. We controlled the Sn content in the resulting polycrystalline (poly-) GeSn by tuning
40 the TIC temperature and achieved high-Sn (25%) content poly-GeSn on glass at 70 °C [26].
41 The grain sizes of the poly-GeSn layers formed by TIC, however, were small (< 1 μm),
42 which would deteriorate the electrical properties of the GeSn layer.

43 For fabricating a large-grained (> 100 μm) poly-Ge on insulators, layer exchange
44 growth between metal and a-Ge layers has been widely investigated using Al [27-31] or Au

45 [32-33]. Besides, the layer exchange technique enables us to form (111)-oriented Ge [31-33],
46 which is preferable for Ge devices [34,35]. In the preset paper, we studied a way using
47 Sn-doped Al-induced crystallization (AIC) to form a large-grained, (111)-oriented
48 poly-GeSn thin film on an insulator. The Sn-doping facilitated the growth and resulted in a
49 2% Sn-content GeSn layer with 40 μm grains.

50

51 **2. Experimental details**

52 Figure 1 shows the process of sample preparation. The Sn (thickness: 0-20 nm) and
53 Al (thickness: 50 nm) layers were prepared in sequence on SiO_2 glass substrates. After the
54 depositions, the Al layers were exposed to air for 10 min to form native AlO_x membranes as
55 diffusion limiting layers, which significantly influence the growth properties of AIC. From
56 our previous study, the thickness of the AlO_x membrane is estimated to be approximately 2
57 nm [29]. After that, 60-nm-thick undoped a-Ge layers were prepared. All depositions were
58 carried out at room temperature using a radio-frequency magnetron sputtering method. The
59 samples were then annealed at 300-350 $^\circ\text{C}$ for 100 h in N_2 ambient. Here we expected the
60 following reactions: the Sn and Al layers were mixed each other during annealing because
61 the Sn-Al eutectic point is 231 $^\circ\text{C}$, and then the a-Ge layer is crystallized in GeSn via the
62 layer exchange, as schematically shown in Fig. 1.

63 After the completion of the layer exchange, the Ge islands and Al layer, remaining
64 in the top layer, are sequentially removed using 50% H_2O_2 solution for 30 min and 1.5% HF
65 solution for 1 min [31]. The resulting layers were characterized by using Nomarski optical
66 microscopy, a θ -2 θ X-ray diffraction (XRD) measurement (spot size: 10 mm), and electron
67 backscatter diffraction (EBSD) analysis.

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70 **3. Results and discussion**

71 Figure 2 shows Nomarski optical micrographs of the back surfaces of the 300 °C
72 annealed samples with and without a 10-nm-thick Sn layer. As representatively shown in Fig.
73 2, at 300 °C, the layer exchange of the samples with the thin Sn layers (0-5 nm) did not finish
74 within 100 h, while that of the samples with the thick Sn layers (10-20 nm) finished. These
75 results mean that the growth velocity increased with increasing the initial Sn thickness. This
76 behavior, i.e., the growth velocity enhancement of a-Ge using Sn as a catalyst, is consistent
77 with the previous reports [25,26]. This is because the temperature of the reaction between Sn
78 and a-Ge is quite low. On the other hand, at 350 °C, the samples with the thick Sn layers (>
79 10 nm) led to the crystallization of a-Ge without layer exchange, resulting in fine grains (< 1
80 μm) according to the EBSD measurement. This is likely owing to the diffusion of Sn into
81 the a-Ge layer, which crystallized the a-Ge layer before layer exchange started. Note that
82 the thickness of the resulting Ge(Sn) layer was the same as the total thickness of the initial
83 Al and Sn layers. The surface roughness of the Ge(Sn) was measured using atomic force
84 microscopy. The root mean square value was found to be 4.3 nm, which was almost the same
85 as that of the Al layer stacked on the Sn layer before annealing. These results suggest that the
86 mixed Al-Sn layer acted as a catalyst for layer exchange growth of a-Ge [30].

87 Figure 3 shows the EBSD images of the samples grown via layer exchange,
88 indicating that the crystal orientation of the resulting Ge(Sn) layers is significantly affected
89 by the Sn insertion as well as the growth temperature. Figures 3(a) and 3(c) show that the
90 samples without Sn layers are highly (111)-oriented, consistent with our prior studies using

91 50-nm-thick Al layers [29,30]. When the Sn layers are inserted, the resulting Ge(Sn) layers
92 have (100)-oriented regions. This phenomenon is pronounced for the samples with thicker
93 Sn layers and higher growth temperatures, as shown in Figs. 3(b), 3(e), and 3(f). Thus, the
94 AIC-Ge(Sn) layers are (111)- or (100)-oriented. This behavior is the same as AIC-Si, where
95 the interfacial energy of Si nuclei in Al becomes minimum in (111) or (100) planes
96 depending on the growth conditions [36]. By tuning the Sn thickness and growth
97 temperatures, (111)-oriented Ge layers can be obtained, as shown in Figs. 3(d) and 3(g).

98 The crystal orientation fraction and the average grain size of the resulting Ge(Sn)
99 layers were estimated from the EBSD images shown in Fig. 3. Figures 4(a)-4(c)
100 respectively indicate that the thicker Sn layer provides the lower (111) orientation fraction,
101 the higher (100) orientation, and the smaller grain size. This is a typical behavior when the
102 growth velocity in AIC is promoted [37,38]: the insertion of the Sn layer likely facilitated
103 the nucleation other than (111) orientation, and reduced the size of the resulting grains.
104 Thus, by lowering the growth temperature, i.e., lowering the growth velocity, the (111)
105 orientation and the grain size are improved. For all the samples grown via the layer
106 exchange, the grain sizes are no less than 20 μm , which is large enough for device
107 fabrications.

108 The Sn content in the resulting layers was evaluated by using a θ - 2θ XRD
109 measurement. Figure 5 (a) shows the XRD patterns of the samples annealed at 325 °C. The
110 peaks at around 27°, originated from the Ge(111) plane, are observed for all the samples. In
111 the measured 2θ range (20-60°), other peaks were not observed because the poly-GeSn
112 layers were thin and preferentially (111)-oriented. With increasing the thickness of the
113 inserted Sn layer, the peak intensity is further weakened. This behavior is attributed to the
114 lower (111) orientation fraction, as shown in Fig. 4(a). The detailed analysis clarified that

115 the peak positions of the samples with a Sn layer slightly shifted to smaller angles,
116 suggesting the formation of GeSn containing substitutional Sn atoms [26]. The Sn contents
117 were calculated from the peak positions assuming the validity of Vegard's law. The results
118 are shown in Fig. 5(b). When the Sn layer is thin, the Sn content in GeSn increases as the
119 Sn thickness increases. On the other hand, when the Sn layer is thick, the Sn content in
120 GeSn is constant regardless of the Sn thickness. The saturated Sn content is determined by
121 the annealing temperature: the lower temperature provides the higher Sn content. The
122 maximum Sn content of 2% was obtained at 300 °C. We evaluated the electrical properties
123 of the poly-GeSn, formed at 300 °C with a 10-nm-thick Sn layer, using Hall measurement.
124 The carrier mobility was 20 cm²/Vs and the hole concentration was 3.5×10^{20} cm⁻³. These
125 values are almost the same as those of the Al-doped Ge layer formed by conventional AIC.
126 Figure 5 (c) shows that the Sn content clearly increases with decreasing the annealing
127 temperatures and that the result of AIC-GeSn is consistent with that of TIC-GeSn [26] on
128 the perspective of the relationship between the Sn content and growth temperature. These
129 results suggest that the maximum Sn content in GeSn is limited by the growth temperature
130 when the GeSn is formed as a result of the reaction between Sn and a-Ge. This is because
131 that the saturated Sn concentration is likely determined by both the solubility limit of Sn in
132 Ge (approximately 1%) and the non-equilibrium fluctuation, depending on the process
133 temperature. Lowering the growth temperature in AIC using growth promotion techniques,
134 reported in Ref. 30, will yield a large-grained GeSn layer with a higher Sn content.

135

136 **4. Conclusions**

137 The Sn-doped AIC of a-Ge, initially inserting Sn layers below Al, was

138 investigated to obtain a large-grained GeSn layer on insulators. Thickening the Sn layer
139 facilitated the growth velocity of AIC, deteriorating the grain size and (111) orientation
140 fraction of the resulting GeSn layer. By tuning the thickness of the Sn layer (10 nm) and
141 the growth temperature (300 °C), a large-grained (~40 μm), (111)-oriented (~80%) GeSn
142 layer on glass was achieved. Those growth properties are the advantages over the previous
143 poly-GeSn layers formed by the solid-phase crystallization of a-GeSn. The Sn content in the
144 GeSn layer was 2%, which was determined by the growth temperature. These findings are
145 meaningful to the research on GSOIs for fabricating high-performance electrical and optical
146 devices on inexpensive substrates.

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248

249

250 **Figure Captions**

251

252 **Fig. 1.** Schematic of the sample preparation.

253

254 **Fig. 2.** Nomarski optical micrographs of the back surfaces of the 300 °C annealed samples
255 (a) without and (b) with a 10-nm-thick Sn layer.

256

257 **Fig. 3.** EBSD images of the Ge(Sn) layers in the normal direction, summarized as a matrix
258 of the initial Sn thickness (0, 5, 10, and 20 nm) and the annealing temperature (300, 325,
259 and 350 °C). The coloration indicates crystal orientation, as shown in the legend.

260

261 **Fig. 4.** Initial Sn thickness dependence of (a) (111) orientation fraction, (b) (100)
262 orientation fraction, and (c) average grain size in the AIC-GeSn layers annealed at 300 °C
263 (circles), 325 °C (squares), and 350 °C (triangles) for 100 h.

264

265 **Fig. 5.** (a) θ - 2θ XRD patterns of the AIC-GeSn layers with initial Sn thickness of 0-20 nm
266 after annealed at 325 °C for 100 h. (b) Initial Sn thickness dependence of Sn concentration
267 in AIC-GeSn after annealed at 300 °C (circles), 325 °C (squares), and 350 °C (triangles)
268 for 100 h, derived from the XRD peak position of Ge(111) using Vegard's law. (c)
269 Annealing temperature dependence of Sn concentration in AIC-GeSn (open circles) and
270 TIC-GeSn (open circles) from Ref. 26.

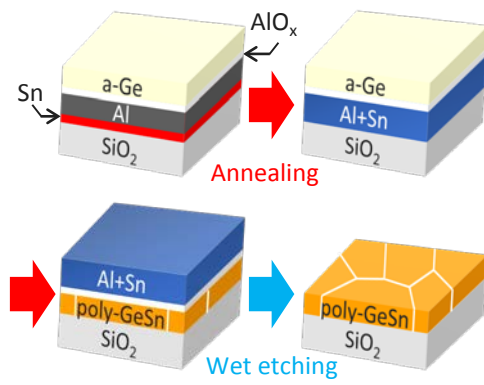


Figure 1

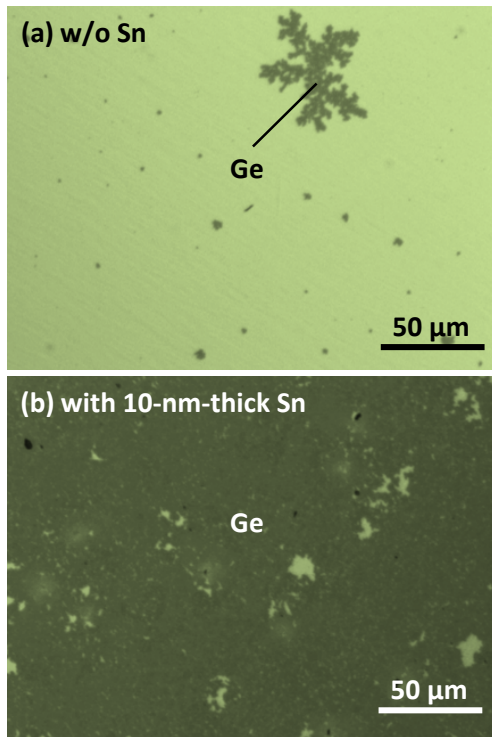


Figure 2

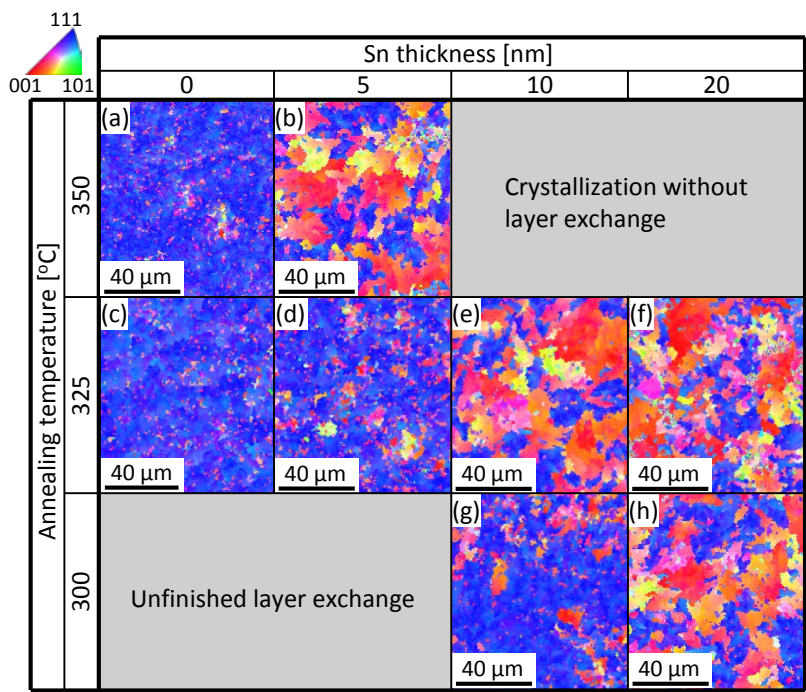


Figure 3

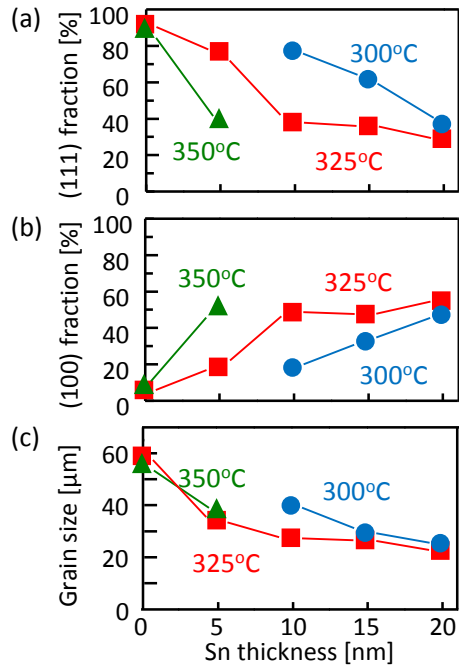


Figure 4

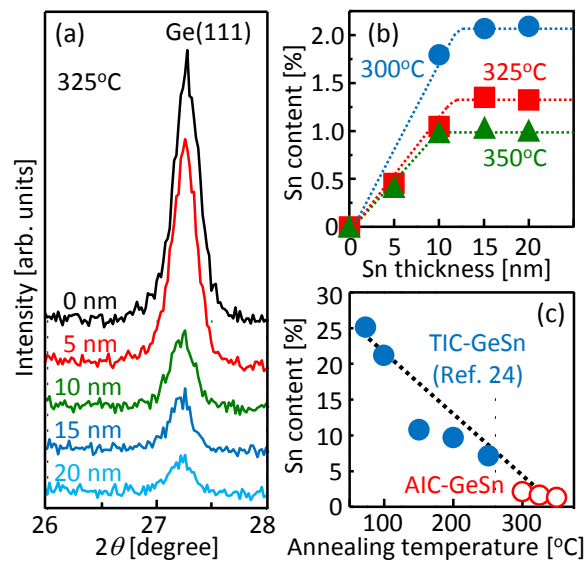


Figure 5