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Graphene was used as the topmost electrode for a metal-oxide-semiconductor planar-type electron emission device. With several various layers, graphene as a gate electrode on the thin oxide layer was directly deposited by gallium vapor-assisted chemical vapor deposition. The maximum efficiency of the electron emission, defined as the ratio of anode current to cathode current, showed no dependency on electrode thickness in the range from 1.8 nm to 7.0 nm, indicating that electron scattering on the inside of the graphene electrode is practically suppressed. In addition, a high emission current density of 1–100 mA/cm^2 was obtained while maintaining a relatively high electron emission efficiency of 0.1%–1.0%. The graphene-oxide-semiconductor planar-type electron emission device has great potential to achieve both high electron emission efficiency and high electron emission current density in practical applications. © *2016 AIP Publishing LLC*.
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Compared with a field emitter array with needle structures,[1] electron emission devices based on metal-oxide-semiconductor (MOS) structure[2] have many advantages such as low operation voltage, operation in low vacuum pressure, electron emission from a planar surface, and compatibility with conventional semiconductor processes. Several practical applications such as field emission displays[3] and high-sensitive image sensors[4] have been proposed. However, the very low emission efficiency of electrons from a MOS-type electron emission device, which is typically less than 1% resulting in low electron emission current density, have prevented their use in practical applications. The reduction of the work function of the gate electrode by adsorption of alkali metals onto the electrode surface[5,6] and the use of nanocrystal silicon to the oxide layer[7–9] has been proposed to improve electron emission efficiency. Other approaches have involved the reduction of electron scattering within the topmost metal electrode by decreasing the electrode thickness. The electron emission efficiency is predicted to reach 3%–10% if electron scattering on the inside of the topmost metal electrode is perfectly suppressed.[8,10–12] For conventional metal electrodes, however, making a high-conductive continuous electrode with a thickness of below 1–2 nm is difficult. Graphene is a single atomic-layered carbon sheet with high electrical conductivity.[13,14] In addition, the electron scattering cross section of carbon atoms is smaller than that of conventional topmost metal electrodes such as Au and Al. Therefore, the use of graphene as the topmost gate electrode for a MOS-type electron emission device will improve its electron emission efficiency. However, a planar-type electron emission device based on a graphene-oxide-semiconductor (GOS) structure has not been developed so far because of difficulties in the direct synthesis of the graphene layer onto the SiO_2 substrate. Graphene synthesized onto a Cu foil by chemical vapor deposition (CVD) has been widely used to achieve large-area graphene on an insulating substrate in many studies on using graphene in electronic devices.[15–17] However, transferring graphene on a Cu foil onto an insulating substrate requires using an acid solution and a resist polymer,[18,19] which causes unavoidable contamination at the interface between the insulating substrate and the graphene layer. Direct synthesis of graphene on a SiO_2 substrate would achieve a contamination-free interface and result in a realization of the GOS planar type electron emission devices. In our recent study, a large area graphene of up to 20-mm square was directly synthesized onto an insulating substrate, such as SiO_2, quartz, and sapphire, by gallium vapor-assisted CVD.[20] In this paper, the fabrication of GOS planar-type electron emission devices using gallium vapor-assisted CVD and their electron emission properties are reported.

Figure 1 shows a typical fabrication process for GOS planar-type electron emission devices. The highly doped n-type Si substrate with a thermal oxide thickness of approximately 300 nm is the starting substrate. The electron emission area of 10–100 μm square was fabricated using conventional photolithography and buffered-hydrofluoric-acid wet etching. The thin oxide layer was then grown by thermal oxidation at 900 °C for 10 min under an oxygen gas flow of 2 l/min after conventional RCA cleaning. A graphene electrode with a varying number of layers was synthesized on the entire surface of the prepared substrate by gallium vapor-assisted CVD under atmospheric pressure using a CH_4 carbon source gas of 1 sccm and Ar carrier gas of 100 sccm

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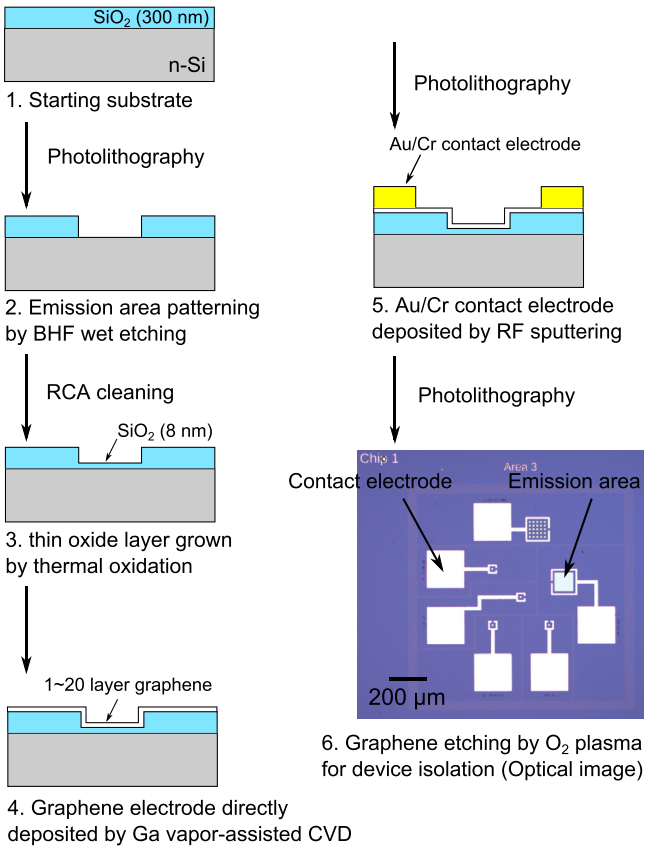

FIG. 1. Typical fabrication processes of GOS planar type electron emission devices.

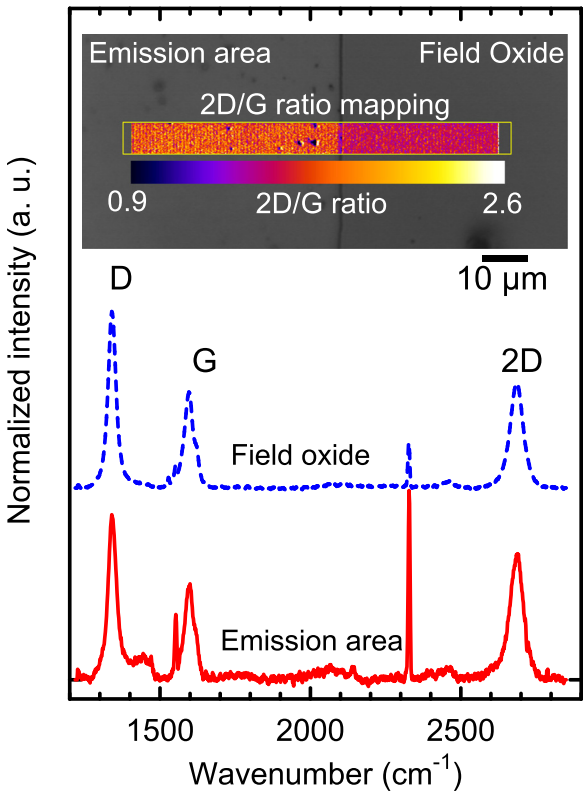

FIG. 2. Typical Raman spectra of the graphene electrode of a GOS planar type electron emission device. The inset is a superimposition of the optical image and the 2D/G ratio mapping of Raman spectra of the graphene electrode.

at 1050 °C for 7–30 min. Details of the synthesis of the graphene layers are described elsewhere.[20] The Au/Cr contact electrode was then fabricated using conventional photolithography, radio frequency sputtering, and the lift-off process. Finally, the graphene electrode was partially etched through photolithography and O_2 plasma for the device isolation.

The synthesized graphene was characterized using Raman spectroscopy with a laser beam of wavelength 532 nm. The cross-sectional structure of the GOS device fabricated by the conventional focused-ion-beam process was observed by transmission electron microscopy (TEM) operated at 200 kV. The thickness of the graphene electrode was measured using atomic force microscopy (AFM). The electron emission characteristics were measured in a vacuum chamber at base pressure of $\sim 10^{-6}$ Pa. An anode electrode, of either a phosphor screen or a metal plate, for applying a 1-kV voltage was placed 5–10 mm away from the gate electrode.

Figure 2 shows typical Raman spectra of the topmost graphene electrode of the GOS devices. The G and 2D peaks attributed to the crystal structure of graphene appear on both the emission area and the field oxide (i.e., the 300-nm-thick SiO_2 layer). The G peak position of graphene directly synthesized on SiO_2 layer was shifted to 1596 cm^{-1} from 1580 cm^{-1} for G peak position of the intrinsic graphene, which indicates that the synthesized graphene has internal compressive strain. The isotropic internal strain of the graphene electrode obtained from the G peak position shift is 0.28%.[21,22] Such a small strain hardly affects the electronic structure of graphene.[23] The inset gives the 2D/G ratio mapping of the Raman spectra of the graphene electrode superimposed on its optical image. The graphene electrode shows the homogeneous crystal quality over the whole surface of the device. A large D band attributed to defects in graphene also appears in the Raman spectra. This is because the small grains range in size from 50 nm to 200 nm, which was confirmed by the dark field TEM image taken from the single diffraction spot.[20]

Figures 3(a) and 3(b) show the scanning electron microscopy (SEM) image of the GOS device with an electron emission area of 100 μm square and the AFM image of graphene electrode on the emission area, respectively. The electron emission area of the GOS device in the SEM image showed very uniform contrast over the whole area. In addition, the electron emission area showed the small root-mean-square roughness of 0.65 nm in the AFM image. Figure 3(c) shows the cross-sectional TEM image of the GOS device fabricated with a graphene synthesis time of 30 min. The thickness of the SiO_2 layer in the electron emission area was approximately 8 nm, whereas that of the topmost graphene electrode was approximately 7 nm corresponding to 20 layers of graphene. The composition of SiO_2 layer was not changed by graphene growth processes, which was confirmed by electron energy loss spectroscopy using scanning TEM and time-of-flight secondary ion mass spectrometry (not shown in data here).

Figure 4(a) shows typical electron emission properties of the GOS planar-type electron emission device. The emission current was detected at a gate bias voltage of around 9 V and reached 7.3 mA/cm^2 at 20 V. The emission efficiency defined as the ratio of anode current to cathode current reached a

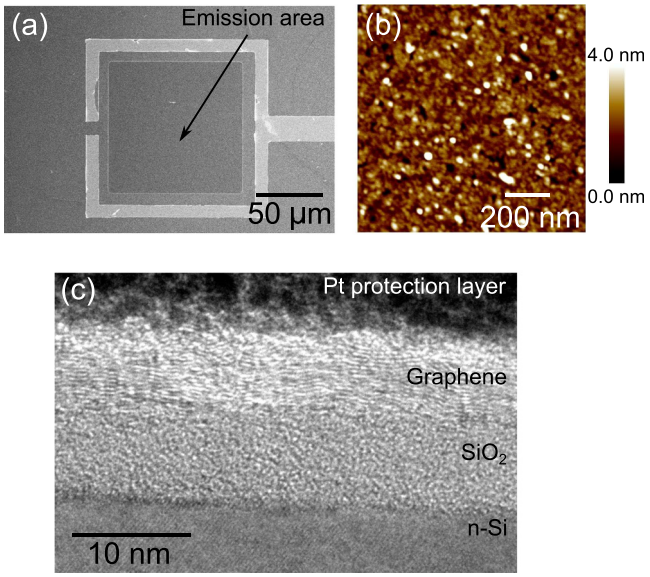

FIG. 3. SEM image of the GOS planar type electron emission device with an electron emission area of 100 μm square. (b) AFM image of the graphene electrode of electron emission area. (c) Cross-sectional TEM image of the GOS device.

maximum (approximately 0.36%) at 12 V and then gently decreased with gate voltage. In the previous report of the conventional MOS type devices,[10] their electron emission efficiency had less dependence on the gate bias voltage and became almost the constant value at high electric field in the case of the relatively thick oxide of 9.3 nm or thicker. This is because that the electrons have a thermal equilibrium energy distribution due to the large scattering of hot electrons within the conduction band of the oxide when the electrons travel a long distance within the conduction band of the oxide. The behavior of the gate bias dependence of the emission efficiency of the GOS devices is well consistent with that of the conventional MOS devices with relatively thick oxide layer since the oxide thickness of GOS devices is approximately 8 nm, which is close value to 9.3 nm. However, the electron emission efficiency of GOS devices (around 0.3%) was two orders of magnitude higher than that of the conventional MOS devices with relatively thick oxide layer (around 0.002%). In addition, most of the GOS planar-type electron emission devices were found to reach high electron emission current density of 1–100 mA/cm^2 maintaining a relatively higher emission efficiency of 0.1%–1.0%, as shown in Fig. 4(b). These results indicate that the GOS planar-type electron emission devices combine high emission efficiency and high emission current density, which is of great benefit in practical applications. Figure 4(c) shows the maximum electron emission efficiency as a function of the thickness of the graphene electrode. The maximum electron emission efficiency was found to be almost constant over the thickness range from 1.8 nm to 7 nm, which suggests that electron scattering inside the graphene electrode is negligible in these emission devices and the mean free path of hot electrons to the graphene electrode is longer than 7 nm. However, the maximum electron emission efficiency was still approximately 1%, which is probably because of the non-optimized thickness of the SiO_2 layer and the higher work function of the graphene electrode (e.g., 4.5–4.6 eV in the theoretical value[24,25]). In addition, the graphene synthesized by gallium vapor-assisted CVD showed p-type behavior,[20] which might lead to higher effective work function of the graphene electrode than that calculated from the theory. For the MOS-type electron emission devices, most of the electrons traveling through the oxide layer lose their energy through scattering. They cannot surmount the work function of the gate electrode if the work function of the gate electrode is high.[6] Therefore, chemical doping of the synthesized graphene to reduce its work function[26–28] is considered as one approach for the further improvement of electron emission efficiency of the GOS

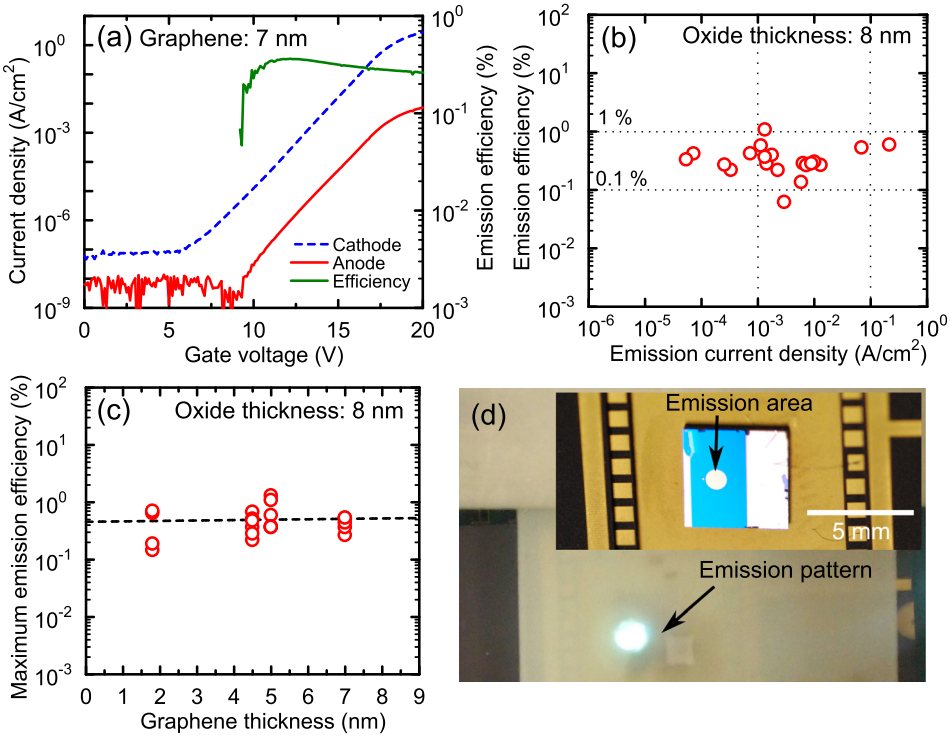

FIG. 4. Typical emission current density and electron emission efficiency of the GOS planar type electron emission device with a graphene electrode thickness of 7 nm as a function of gate voltage. (b) Electron emission efficiency of the GOS devices as a function of electron emission current density. The oxide thickness is 8 nm. (c) Maximum electron emission efficiency of the GOS devices as a function of graphene-electrode thickness. The oxide thickness is 8 nm. (d) Typical electron emission pattern on the phosphor screen for the GOS devices with an emission area of 1-mm diameter. The inset is an optical image of the GOS devices.

planar-type electron emission devices. Figure 4(d) shows the electron emission pattern of the GOS device on the phosphor screen and indicates that electrons are certainly emitted into vacuum from the whole emission area of the GOS device.

In summary, for a MOS-type electron emission device, a graphene electrode with various numbers of layers was fabricated by gallium vapor-assisted CVD. Electron emission from the fabricated GOS structures was demonstrated. The efficiency of electron emission was almost constant for graphene electrode thickness ranging from 1.8 nm to 7 nm, which indicates that the electron scattering over the graphene electrode is entirely suppressed. In addition, high emission current density of 1–100 mA/cm^2 was achieved, maintaining the relatively high electron emission efficiency of 0.1%–1.0%, which is two orders of magnitude higher than those of the conventional MOS devices. By combining high electron emission efficiency and high electron emission current density, the GOS structure has great practical potential in MOS-type electron emission devices.

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