AIP | Applied Physics Letters

Low-temperature (180°C) formation of large-grained Ge (111) thin film on insulator using accelerated metal-induced crystallization

K. Toko, R. Numata, N. Oya, N. Fukata, N. Usami, and T. Suemasu

Citation: Applied Physics Letters **104**, 022106 (2014); doi: 10.1063/1.4861890
View online: http://dx.doi.org/10.1063/1.4861890
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/104/2?ver=pdfcov
Published by the AIP Publishing

Low-temperature (180 °C) formation of large-grained Ge (111) thin film on insulator using accelerated metal-induced crystallization

K. Toko,[1,a)] R. Numata,[1] N. Oya,[1] N. Fukata,[2] N. Usami,[3] and T. Suemasu[1]
[1]*Institute of Applied Physics, University of Tsukuba, 1-1-1 Tennodai, Tsukuba, Ibaraki 305-8573, Japan*
[2]*National Institute for Materials Science, Namiki, Tsukuba 305-0044, Japan*
[3]*Materials, Physics and Energy Engineering, Nagoya University, Aichi 464-8603, Japan*

(Received 21 November 2013; accepted 27 December 2013; published online 14 January 2014)

The Al-induced crystallization (AIC) yields a large-grained (111)-oriented Ge thin film on an insulator at temperatures as low as 180 °C. We accelerated the AIC of an amorphous Ge layer (50-nm thickness) by initially doping Ge in Al and by facilitating Ge diffusion into Al. The electron backscatter diffraction measurement demonstrated the simultaneous achievement of large grains over 10 μm and a high (111) orientation fraction of 90% in the polycrystalline Ge layer formed at 180 °C. This result opens up the possibility for developing Ge-based electronic and optical devices fabricated on inexpensive flexible substrates. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4861890]

The low-temperature synthesis of polycrystalline Ge (poly-Ge) thin films on insulators has versatile applications, such as high-speed thin-film transistors, high-efficiency tandem solar cells, and three-dimensional on-chip optical interconnects.[1–3] A (111)-oriented large-grained poly-Ge layer is specifically desirable because it provides a high carrier mobility for metal-oxide-semiconductor transistors[4,5] and acts as an epitaxial template for III-V compound semiconductors, aligned nanowires, and spintronics materials.[6–8] Hence, fabricating such a poly-Ge layer on a plastic substrate develops novel flexible devices with advanced functions. Commonly-used inexpensive plastics (e.g., polymers) soften at temperatures as low as 200 °C, whereas the solid-phase crystallization (SPC) of amorphous Ge (a-Ge) requires temperatures higher than 400 °C.[9,10] Therefore, the Ge-based flexible devices desire the low-temperature growth technique of high-quality poly-Ge layers on insulators.

In line with this, metal-induced crystallization (MIC), utilizing catalytic metals for lowering the crystallization temperature of a-Ge, has been widely studied.[11] Some metals (e.g., Ni) locally formed single-crystal Ge layers at low temperatures (320–380 °C),[12–14] and others (e.g., Cu, Au, and Sn) significantly reduced the crystallization temperatures of a-Ge (160–250 °C).[15–17] Among them, the Al-induced crystallization (AIC) of a-Ge, originally developed for Si,[18–21] is gathering the most attentions.[22–25] Recently, the AIC enabled the preferentially (111)-oriented poly-Ge layers with relatively large grains through the layer exchange process between Ge and Al.[26–28] Moreover, we have significantly improved the (111) orientation fraction and the grain size of the AIC-Ge by forming a diffusion controlling interlayer (AlO_x) between Ge and Al.[29] However, it is still difficult to achieve the large-grained Ge (111) layers on insulators below the softening temperature of plastic substrates (~200 °C). This study investigates lowering the crystallization temperature in the AIC–Ge based on the layer-exchange growth mechanism. The accelerated AIC technique achieves a large-grained, (111)-oriented Ge on an insulator at temperatures as low as 180 °C.

In the experiment, we prepared four kinds of samples as summarized in Table I. Sample A, a standard AIC sample,[29] was prepared as follows. A 50-nm-thick Al layer was prepared on an amorphous SiO_2 substrate, and exposed to air for 5 min to form a native AlO_x interlayer as a diffusion control layer, followed by a 50-nm-thick a-Ge layer preparation. Sample B has the same stacked-layer structure as sample A expect that it additionally has a 1-nm-thick a-Ge insertion layer below the Al layer. Sample C has a native GeO_x interlayer in substitution for the AlO_x layer in sample A. Here, the GeO_x was prepared by the air-exposure (24 h) of a 1-nm-thick a-Ge layer prepared on the Al layer. Sample D has both of the Ge insertion layer and the GeO_x interlayer. The Al and Ge layers were prepared at room temperature using a radio-frequency magnetron sputtering method. Finally, the samples were annealed at 180–350 °C in N_2 for 0.1–100 h to induce the layer exchange growth. By removing the Al and interlayers using an HF solution (HF: 1.5%) for one minute, bared poly-Ge layers were obtained on the SiO_2 substrates. The sample preparation procedure is schematically shown in Fig. 1. The crystallization time, i.e., the time for completing layer exchange, in each sample was measured using a Nomarski optical microscopy and a micro-probe Raman scattering spectroscopy (excitation-laser spot-diameter: 1 μm, wavelength: 532 nm). The crystal orientation of the resulting poly-Ge layers was roughly evaluated by an x-ray diffraction (XRD) rocking curve measurement with a spot size of 5 mm. In addition, the detailed crystal orientation and the grain size were characterized using electron backscattered diffraction (EBSD) measurement.

Samples A, B, C, and D were annealed at 300, 275, 225, and 180 °C, respectively. The Nomarski optical microscopy suggested the completion of the layer exchange for each sample after annealing for 100 h. In addition, the Raman spectra in Fig. 2(a) show the large peaks at around 292 cm^{-1} for all samples after annealing. These results indicate the crystallization of the a-Ge layers, although the peaks shift to lower wavenumbers compared to the actual Ge optical phonon peak (~300 cm^{-1}).[7] These large wavenumber shifts are not completely understood, but are possibly due to the residual Al atoms (~0.5%) in the Ge layers. The insertion in

a)E-mail address: toko@bk.tsukuba.ac.jp

TABLE I. Samples prepared in this study.

Sample	Interlayer between Ge and Al	Ge insertion layer
A	AlO_x	None
B	AlO_x	1-nm thickness
C	GeO_x	None
D	GeO_x	1-nm thickness

Fig. 2(a) shows the full width at half maximum (FWHM) of the Raman peaks as a function of annealing temperature. The FWHM is independent on annealing temperature, whereas FWHM increases with decreasing annealing temperature for the conventional SPC of a-Ge.[9,10] This result suggests that the AIC process is completely different from the SPC process, i.e., the AIC proceeds through the Ge diffusion and segregation in the Al layer.[27–29]

Figure 2(b) shows the Arrhenius plots of crystallization time for samples A–D. Here, the crystallization time is defined as the time needed for the completion of the layer exchange. The resulting poly-Ge region covers more than 95% area of the substrate for all the samples. As seen in Fig. 2(b), the a-Ge insertion layer and the GeO_x interlayer work effectively for lowering crystallization temperature. In particular, sample D, combining the Ge insertion layer and the GeO_x interlayer, significantly reduces the crystallization temperature to as low as 180 °C. The mechanism of the crystallization temperature reduction is explained as follows. In the AIC process, Ge atoms diffuse from the top a-Ge layer to the Al layer through the interlayer. The Ge nucleation occurs when the Ge concentration in Al is supersaturated. After that, the lateral growth of the Ge crystals propagates due to the continuous supply of Ge atoms from the top a-Ge layer through the interlayer. Based on this mechanism, we consider that the a-Ge insertion layer works for initial Ge doping in the Al layer, which facilitates the Ge supersaturation (i.e., nucleation), while the GeO_x interlayer promotes the Ge diffusion (i.e., nucleation and lateral growth) compared to the conventional AlO_x interlayer.

The crystal orientation of the poly-Ge layers for samples A–D were characterized by the XRD rocking curve of the (111) Ge reflection and summarized in Fig. 3. All the

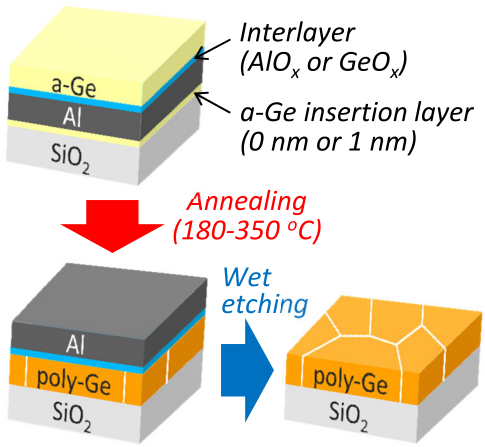

FIG. 1. Schematic image of the sample preparation procedure.

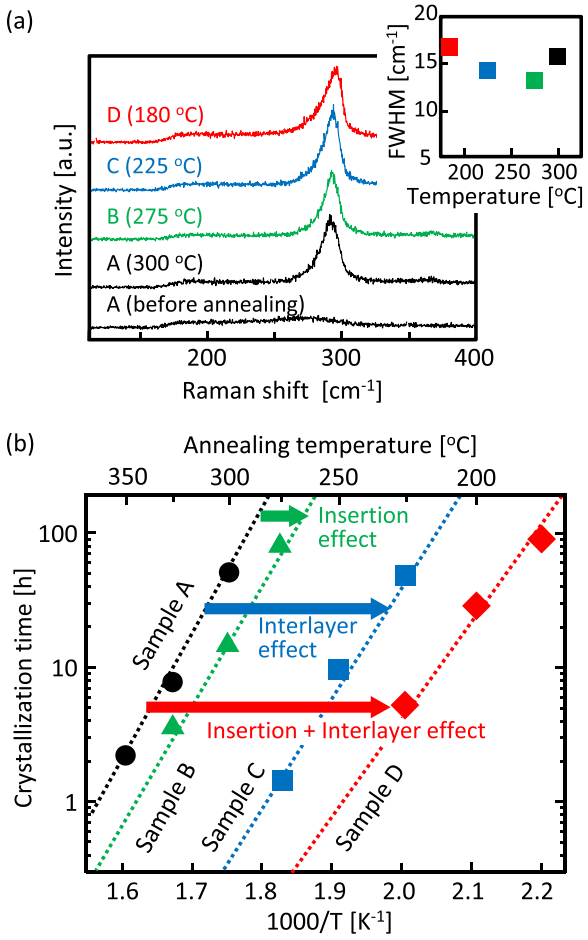

FIG. 2. (a) Raman scattering spectra for samples A-D, where the annealing temperatures are 300 °C for sample A, 275 °C for sample B, 225 °C for sample C, and 180 °C for sample D. The spectrum for sample A before annealing is shown for comparison. FWHM values for each sample are summarized in the insertion as a function of crystallization temperature. (b) Arrhenius plots of the crystallization time (i.e., the time for completing layer exchange) for samples A–D.

samples have a peak around 13.7° indicating preferential (111) orientation. The (111) orientation is explained from the view point of the interfacial energy minimization between the Ge layer and the SiO_2 substrate.[16,28,29] The

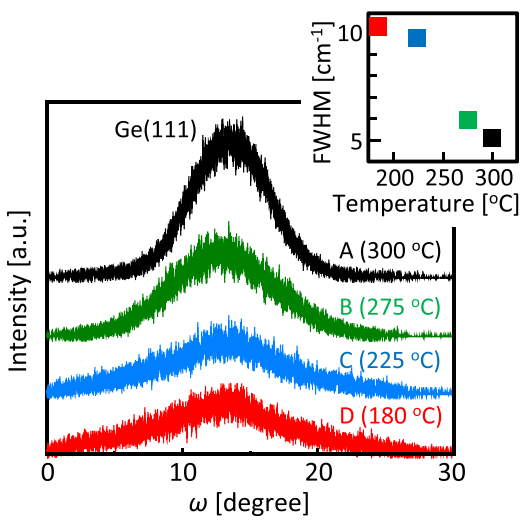

FIG. 3. XRD rocking curves (ω scans) of the (111) Ge reflection of samples A–D. FWHM values for each sample are summarized in the insertion as a function of crystallization temperature.

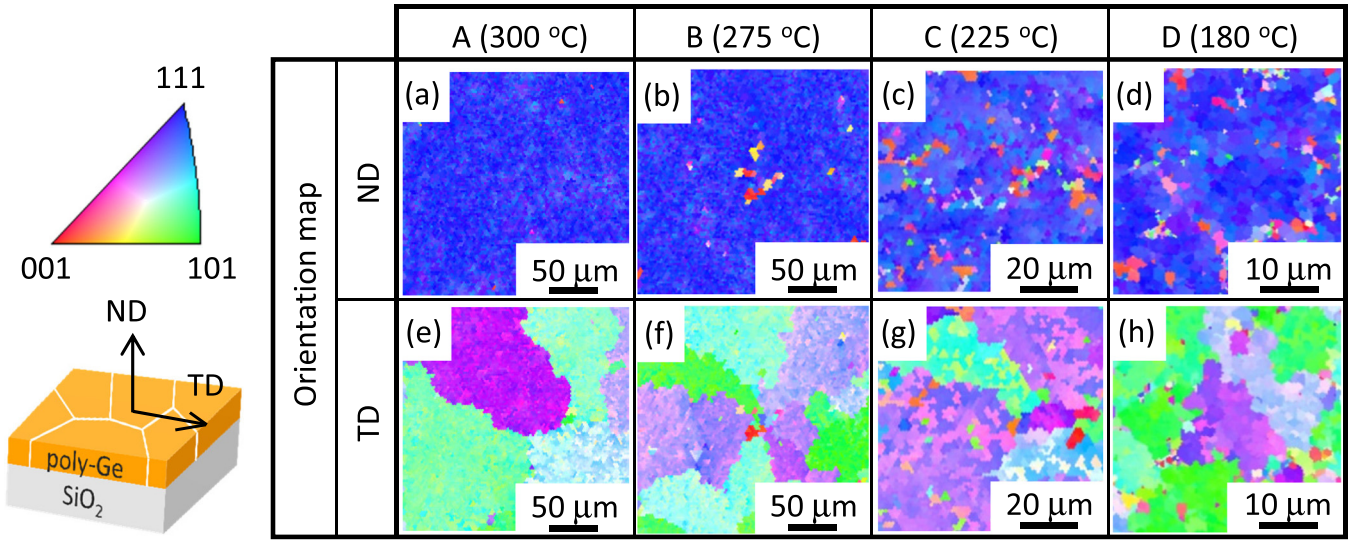

FIG. 4. EBSD images of the poly-Ge layers for samples A–D: (a)–(d) ND and (e)–(h) TD relative to the substrate, where the ND and TD maps correspond to the same region. The colors indicate the crystal orientation, according to the inserted color key.

FWHM values of the peaks are plotted in the inserted graph, which indicates that a lower annealing temperature provides a larger FWHM value, i.e., weaker (111) orientation. This behavior is likely because of the unstable thermal equilibrium condition during the accelerated low-temperature crystal growth.

The detailed crystal orientation and the grain size of the poly-Ge layers for samples A–D were characterized using the EBSD measurement. Figures 4(a)–4(d) exhibit the crystal orientation maps in the normal direction (ND). For all the samples, the Ge layers are highly (111) oriented. Figures 4(e)–4(h) exhibit the crystal orientation maps in the transverse direction (TD) and indicate that the grain size of the poly-Ge layer decreases with decreasing annealing temperature. This result suggests that the a-Ge insertion layer and the GeO_x interlayer increase the nucleation frequency while promoting the crystallization. Nevertheless, Fig. 4(h) indicates that sample D has large grains with approximately 10 μm even in a 180 °C process.

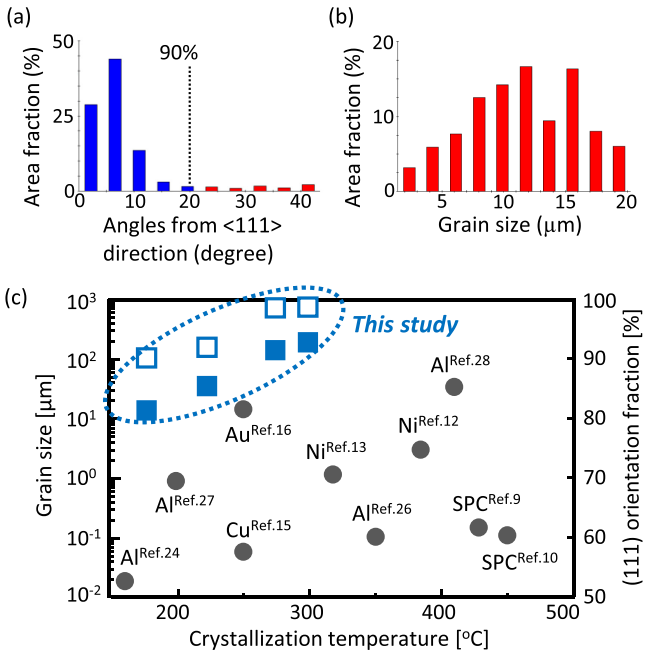

FIG. 5. Distribution histograms of (a) crystal orientation fraction and (b) grain size in the poly-Ge layer for sample D annealed at 180 °C. (c) (111) orientation fraction (open squares) and grain size (closed squares) of the poly-Ge layers for samples A–D as a function of crystallization temperature. The closed circles denote the grain sizes of the poly-Ge layers formed by conventional SPC or MIC techniques, which were measured by SEM, TEM, or EBSD analyses. Their catalyst metals and the reference numbers are mentioned with each symbol.

The (111) orientation fraction and the average grain size of the poly-Ge layers were calculated using EBSD analyses. Figures 5(a) and 5(b) show the typical results for sample D annealed at 180 °C. Figure 5(a) indicates that the poly-Ge layer principally consists of planes with tilt that is within 20° of the exact (111) plane. This result agrees with the XRD rocking curve in Fig. 3. The total (111) orientation fraction was defined as the integrated values of the area fractions from 0° to 20°, and was calculated to be 90%. On the other hand, from the grain size histogram in Fig. 5(b), the average grain size is calculated to be 12 μm. In the same manner, the (111) orientation fraction and the average grain size for samples A–C were calculated, and are summarized in Fig. 5(c) as a function of crystallization temperature. The (111) orientation fractions are more than 90% for all samples in this study. We note that the AIC is a unique crystallization technique providing such a highly oriented Ge layer on an amorphous substrate. On the other hand, the grain size for the samples in this study decreases with decreasing crystallization temperature; nevertheless, their grain sizes are larger than those obtained from the conventional SPC or MIC techniques, as shown in Fig. 5(c). It is worth noting that the grain size is as large as 12 μm for the sample crystallized at 180 °C in this study. Therefore, the accelerated AIC simultaneously enables the large-grained, orientation-controlled, and low-temperature formation of the poly-Ge thin film on an insulator.

In summary, the low-temperature AIC of a-Ge was investigated to achieve large-grained (111)-oriented Ge layers on low-heat-resistant substrates. We proposed two

growth promotion techniques: (i) initial Ge doping in Al by inserting an a-Ge layer below the Al layer and (ii) diffusion enhancement by substituting GeO_x for AlO_x as the interlayer. By combining these techniques, we reduced the crystallization temperature to as low as 180 °C. The EBSD analyses proved a large grain size (12 μm) and a high (111) orientation fraction (90%) in the resulting Ge layer on a SiO_2 substrate. This low-temperature growth technique of the large-grained (111)-oriented Ge layers on insulators opens up a possibility for developing Ge-based novel flexible devices.

This work was partially supported by the Casio Science Promotion Foundation and the Murata Science Foundation.

[1]T. Sadoh, H. Kamizuru, A. Kenjo, and M. Miyao, Appl. Phys. Lett. **89**, 192114 (2006).
[2]R. R. King, D. C. Law, K. M. Edmondson, C. M. Fetzer, G. S. Kinsey, H. Yoon, R. A. Sherif, and N. H. Karam, Appl. Phys. Lett. **90**, 183516 (2007).
[3]J. Michel, J. Liu, and L. C. Kimerling, Nature Photon. **4**, 527 (2010).
[4]T. Sasada, Y. Nakakita, M. Takenaka, and S. Takagi, J. Appl. Phys. **106**, 073716 (2009).
[5]T. Nishimura, C. H. Lee, T. Tabata, S. K. Wang, K. Nagashio, K. Kita, and A. Toriumi, Appl. Phys. Express **4**, 064201 (2011).
[6]E. P. A. M. Bakkers, J. A. van Dam, S. De Franceschi, L. P. Kouwenhoven, M. Kaiser, M. Verheijen, H. Wondergem, and P. van der Sluis, Nature Mater. **3**, 769 (2004).
[7]N. Fukata, K. Sato, M. Mitome, Y. Bando, T. Sekiguchi, M. Kirkham, J.-I. Hong, Z. L. Wang, and R. L. Snyder, ACS Nano **4**, 3807 (2010).
[8]K. Hamaya, H. Itoh, O. Nakatsuka, K. Ueda, K. Yamamoto, M. Itakura, T. Taniyama, T. Ono, and M. Miyao, Phys. Rev. Lett. **102**, 137204 (2009).
[9]K. Toko, I. Nakao, T. Sadoh, T. Noguchi, and M. Miyao, Solid-State Electron. **53**, 1159 (2009).
[10]C. Y. Tsao, J. W. Weber, P. Campbell, P. I. Widenborg, D. Song, and M. A. Green, Appl. Surf. Sci. **255**, 7028 (2009).
[11]Z. Wang, L. P. H. Jeurgens, J. Y. Wang, and E. J. Mittemeijer, Adv. Eng. Mater. **11**, 131 (2009).
[12]J. H. Park, P. Kapur, K. C. Saraswat, and H. Peng, Appl. Phys. Lett. **91**, 143107 (2007).
[13]K. Toko, H. Kanno, A. Kenjo, T. Sadoh, T. Asano, and M. Miyao, Appl. Phys. Lett. **91**, 042111 (2007).
[14]M. Uenuma, B. Zhenga, T. Imazawa, M. Horita, T. Nishidaa, Y. Ishikawa, H. Watanabe, I. Yamashita, and Y. Uraokaa, Appl. Surf. Sci. **258**, 3410 (2012).
[15]T. Sadoh, M. Kurosawa, T. Hagihara, K. Toko, and M. Miyao, Electrochem. Solid-State Lett. **14**, H274 (2011).
[16]J.-H. Park, T. Suzuki, M. Kurosawa, M. Miyao, and T. Sadoh, Appl. Phys. Lett. **103**, 082102 (2013).
[17]M. Kurosawa, N. Taoka, M. Sakashita, O. Nakatsuka, M. Miyao, and S. Zaima, Appl. Phys. Lett. **103**, 101904 (2013).
[18]O. Nast, T. Puzzer, L. M. Koschier, A. B. Sproul, and S. R. Wenham, Appl. Phys. Lett. **73**, 3214 (1998).
[19]A. Sarikov, J. Schneider, J. Berghold, M. Muske, I. Sieber, S. Gall, and W. Fuhs, J. Appl. Phys. **107**, 114318 (2010).
[20]B. I. Birajdar, T. Antesberger, B. Butz, M. Stutzmann, and E. Spiecker, Scr. Mater. **66**, 550 (2012).
[21]M. Kurosawa, N. Kawabata, T. Sadoh, and M. Miyao, Appl. Phys. Lett. **95**, 132103 (2009).
[22]F. Katsuki, K. Hanafusa, M. Yonemura, T. Koyama, and M. Doi, J. Appl. Phys. **89**, 4643 (2001).
[23]R. Zanatta and I. Chambouleyron, J. Appl. Phys. **97**, 094914 (2005).
[24]Z. M. Wang, J. Y. Wang, L. P. H. Jeurgens, F. Phillip, and E. Mittemeijer, Acta Mater. **56**, 5047 (2008).
[25]W. Zhang, F. Ma, T. Zhang, and K. Xu, Thin Solid Films **520**, 708 (2011).
[26]S. Peng, D. Hu, and D. He, Appl. Surf. Sci. **258**, 6003 (2012).
[27]S. Hu, A. F. Marshall, and P. C. McIntyre, Appl. Phys. Lett. **97**, 082104 (2010).
[28]M. Kurosawa, N. Kawabata, T. Sadoh, and M. Miyao, ECS J. Solid State Sci. Technol. **1**, P144 (2012).
[29]K. Toko, M. Kurosawa, N. Saitoh, N. Yoshizawa, N. Usami, M. Miyao, and T. Suemasu, Appl. Phys. Lett. **101**, 072106 (2012).