Surface Potential-Based Polycrystalline-Silicon Thin-Film Transistors Compact Model by Non-Equilirium Approach

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We propose a surface potential-based polycrystalline-silicon thin-film transistors (poly-Si TFTs) compact model taking a non-equilibrium state into account. A drain current model considers grain boundary (GB) trap-related physical phenomena: composite mobility of GB and intragrain, GB bias-induced mobility modulation, transient behavior due to carrier capture and emission at GBs, pinch-off voltage lowering, and GB trap-assisted leakage current. Besides, photo-induced current behavior is also considered by introducing quasi-Fermi potential. A capacitance model is derived from physically partitioned terminal charges and coupled to the drain current behavior. This compact model allows us to accurately simulate static characteristics of various types of poly-Si TFTs including temperature and luminance dependence. Furthermore, this model succeeded to simulate frequency dependence of circuit performance derived from the trap-related transient behavior, which was verified by evaluating delay time in a 21-stage inverter chain. The good agreements with the measurements of both static and dynamic characteristics confirm the validity of the compact model.

Index Terms– Thin Film Transistors, Semiconductor device modeling, Circuit simulation, SPICE

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1. Introduction

Polycrystalline-silicon thin-film transistors (Poly-Si TFTs) have been increasingly used for the pixel and driver circuits in flat-panel displays application such as smart phones, tablet PCs, and LCD/OLED TVs. High mobility and stability of poly-Si TFTs are preferable to reduce pixel circuits area for high resolution displays and to realize a “system-on-glass” which provides various functional circuits on the periphery of a display. Electrical property of poly-Si TFTs is influenced by poly-Si grain size (L_g) and grain boundary (GB) trap charge [1], [2]. Accordingly, poly-Si TFTs show various output characteristics depending on the fabrication process. Therefore, accurate compact model for circuit simulation is a key issue to design display circuits employing poly-Si TFTs. Thus far, several poly-Si TFTs compact models have been proposed for circuit simulations [3]–[5]. These are threshold voltage (V_{th})-based piecewise models in which model equations are provided for the individual operational regions of poly-Si TFTs. Connecting the individual equations requires artificial parameters, which sometimes causes a simulation error. Besides, the terminal capacitances in their models are not generated from the partitioned terminal charges but composed analytically. This is one of the reasons for breaking the charge conservation law in circuit simulation [6]. To improve the above drawbacks in the previous models, a surface potential-based poly-Si TFTs (defined hereinafter as SPT) model was proposed [7]. This model well reproduces various static output characteristics of poly-Si TFTs. However, it in insufficient to describe GB trap-related physical phenomena: GB bias-induced mobility modulation (GBMM) [8], transient current due to carrier capture and emission at GBs or time domain mobility modulation (TDMM) [9], pinch-off voltage lowering (PVL) [10]. In addition, it is

impossible to describe photo-induced current [11] peculiar to display circuits. Therefore, more physical and widely applicable poly-Si TFTs compact model has been required. The purpose of this work is to propose a new generation of SPT model to satisfy the above requirements.

2. Modeling Framework

A. Assumptions

A poly-Si film is divided by grains and the GBs run through the film perpendicular to the surface. Free carriers in poly-Si are trapped at the GBs giving rise to the GB barrier potential. In a TFT structure, distribution of electrostatic potential becomes two-dimensional and complicated. Then, we introduce several assumptions to make a new SPT compact model simple.

(A-1) A GB trap state density model is symmetric between acceptor- and donor-types.

(A-2) Intragrain (IG) surface potential is calculated with spatially averaged GB trap charge density.

(A-3) GB potential at poly-Si surface is calculated based on the IG surface potential.

(A-4) Electric field is set to be zero at the back surface.

(A-5) GB trap charge is unchanged along the channel.

(A-6) Photo-injected carrier density is constant.

(A-7) Quasi-Fermi potential of hole ϕ_{fp} is evaluated in the flat-band condition.

The (A-2) overestimates the GB trap charge and the (A-3) underestimates the channel free charge in subthreshold region. However, this is reasonable in on-region. We give priority to on-region in a compact model. The (A-5) was confirmed by device

simulation [10] to work approximately at the least in the linear region. The (A-7) is allowable because hole density does not affect the on current. In addition, the flat-band state is a unique point for us to evaluate the ϕ_{fp}. The (A-1), (A-4), and (A-6) are trivial.

B. GB Trap Model

We define an acceptor- and a donor-type trap state density per unit GB area as

$$N_t^A(\phi) = N_{\mathrm{te}} \exp[\gamma(\phi_c - \phi)] + N_{\mathrm{to}} \qquad (1)$$

and $$N_t^D(\phi) = N_{\mathrm{te}} \exp[\gamma(\phi - \phi_v)] + N_{\mathrm{to}} \ , \qquad (2)$$

where ϕ_c and ϕ_v refer to the conduction- and valence-band potentials, N_{te}, N_{to}, and γ are the model parameters. When we consider GB trap charge as neutral in the flat-band condition ($\phi = 0$), effective trap density per unit GB area $N_t(\phi)$ is described as

$$\begin{aligned} N_t(\phi) &= [p_t(\phi) - p_t(0)] - [n_t(\phi) - n_t(0)] \\ &= q\int_{\phi_f}^{-\phi+\phi_f} N_t^D(\phi')d\phi' - q\int_{-\phi+\phi_f}^{\phi_f} N_t^A(\phi')d\phi' \ , \end{aligned} \qquad (3)$$

where p_t and n_t refer to the hole and electron trap density, respectively (Fig. 1). Then, average GB trap charge density per unit volume $q_t(\phi)$ is given [12] by

$$q_t(\phi) = \frac{2q}{L_g} \cdot N_t(\phi) \ . \qquad (4)$$

C. Photo-induced effect

Illumination causes Fermi-level split and flat-band voltage (V_{fb}) shift. In *n*-channel (*n*-ch) TFTs, electron Fermi potential stays almost the same at the V_{fb} because electron can commute between the n^+ region and the channel region giving rise to an

increase in the $V_{\rm fb}$ as illustrated in Fig. 2. Considering carrier balance, the $V_{\rm fb}$ shift ϕ_o and the $\phi_{\rm fp}$ are given by

$$\phi_o = \frac{1}{\beta}\ln\left[1+\exp(\beta\phi_f)\cdot\left(\frac{n_{\rm ph}}{n_i}\right)\right], \qquad (5)$$

and $$\phi_{\rm fp} = \phi_o + \frac{1}{\beta}\ln\left[2\sinh\beta\phi_f + \exp[\beta(\phi_o-\phi_f)]\right]. \qquad (6)$$

Here, $n_{\rm ph}$ refers to the photo-injected carrier density and β stands for q/kT.

D. Surface and GB Potentials

Figure 3 defines physical quantities discussed in this section. Based on (4) and (6), Poisson equation for surface potential is written as

$$\frac{d^2\phi(x)}{dx^2} = \frac{2qn_i}{\varepsilon_s}\left[\frac{1}{2}\left\{\exp[\beta(\phi(x)-\phi_f)]-\exp[\beta(\phi_{\rm fp}-\phi(x))]\right\}+\sinh\beta\phi_f\right]-\frac{1}{\varepsilon_s}q_t(\phi(x)) \ . \quad (7)$$

By integrating (7) from ϕ_b to ϕ_s, surface charge Q_s is obtained as

$$Q_s(\phi_s,\phi_b)^2 = \frac{4q\varepsilon_s n_i}{\beta}\left\{\frac{1}{2}\left(\exp[\beta(\phi_s-\phi_f)]+\exp[\beta(\phi_{\rm fp}-\phi_s)]\right)\right.$$
$$\left.-\frac{1}{2}\left(\exp[\beta(\phi_b-\phi_f)]+\exp[\beta(\phi_{\rm fp}-\phi_b)]\right)+\beta(\phi_s-\phi_b)\sinh\beta\phi_f\right\}-2\varepsilon_s\int_{\phi_b}^{\phi_s}q_t(\phi)d\phi \ . \quad (8)$$

On the other hand, back surface potential ϕ_b is related to ϕ_s by

$$\phi_s = \phi_b - \frac{\rho_b}{2\varepsilon_s}\cdot t_{\rm Si}{}^2 \ , \qquad (9)$$

where, ρ_b and t_{Si} refer to the charge density at back surface and poly-Si film thickness.

Then, $$C_{\rm ox}(V_{\rm geff}-\phi_s) = Q_s(\phi_s,\phi_b) \qquad (10)$$

determines ϕ_s. The $V_{\rm geff}$ is defined by $V_{\rm gs}-V_{\rm fb}$.

GB potential is formed by the deviation of charge density in the vicinity of the GB from that in the IG. Then, Poisson equation for the GB potential is written as

$$\frac{d^2\varphi(y)}{dy^2} = \frac{qn_i}{\varepsilon_s}\left[\exp[\beta(\varphi(y)-\phi'_f)]-\exp[\beta(\phi'_{\mathrm{fp}}-\varphi(y))]+\exp(\beta\phi'_{\mathrm{fp}})-\exp(-\beta\phi'_f)\right] \qquad (11)$$

with notation of $\phi'_f \equiv \phi_f - \phi_s$, and $\phi'_{\mathrm{fp}} \equiv \phi_{\mathrm{fp}} - \phi_s$. By integrating (11) from 0 to ϕ_t, GB trap charge Q_t is obtained as

$$Q_t(\phi_t)^2 = \frac{8q\varepsilon_s n_i}{\beta}\Big(\{\exp[\beta(\phi_t-\phi'_f)]+\exp[\beta(\phi'_{\mathrm{fp}}-\phi_t)]\} + \beta\phi_t[\exp(\beta\phi'_{\mathrm{fp}})-\exp(-\beta\phi'_f)]-[\exp(-\beta\phi'_f)+\exp(\beta\phi'_{\mathrm{fp}})]\Big) . \qquad (12)$$

Then, $Q_t(\phi_t) = qN_t(\phi_s+\phi_t)$ (13)

determines ϕ_t.

E. Drain Current

Drain current equation in on-region follows the surface potential-based modeling scheme [13], [14]. Then, the drain current is expressed as

$$I_{\mathrm{on}} = -\frac{W}{L}\mu_u\left\{\int_{\phi_{s0}}^{\phi_{sL}} Q_n(\phi)d\phi - \frac{1}{\beta}[Q_n(L)-Q_n(0)]\right\} , \qquad (14)$$

where Q_n refers to the free charge density per unit surface area and subscript '0' and '*L*' denote source and drain edges, respectively. The Q_n is obtained by subtracting depleted body charge Q_b from the surface charge Q_s given by (8). The Q_b is defined as

$$Q_b(\phi_s,\phi_b)^2 = \frac{4q\varepsilon_s n_i}{\beta}\left\{\frac{1}{2}\left(\exp[\beta(\phi_{\mathrm{fp}}-\phi_s)]-\exp[\beta(\phi_{\mathrm{fp}}-\phi_b)]\right)+\beta(\phi_s-\phi_b)\sinh\beta\phi_f\right\} - 2\varepsilon_s\int_{\phi_b}^{\phi_s} q_t(\phi)d\phi . \qquad (15)$$

Then, total drain current is given by

$$I_{\mathrm{ds}} = (I_{\mathrm{on}} + I_{\mathrm{off}})\cdot f_{\mathrm{hc}} , \qquad (16)$$

where $I_{\rm off}$ is the off-current discussed later, $f_{\rm hc}$ is the hot carrier factor [15].

F. Terminal Charges and Capacitances

According to the surface potential-based modeling scheme, gate charge Q_g is expressed as

$$Q_g = \frac{W^2 \mu_u}{I_{\rm ds}} \left\{ \int_{\phi_{s0}}^{\phi_{sL}} Q_n(\phi)^2 d\phi - \frac{1}{2\beta} [Q_n(L)^2 - Q_n(0)^2] \right\} . \qquad (17)$$

In general, terminal charge is the charge responding the terminal voltage. Therefore, when we define source charge Q_s, the Q_s does not respond to the drain voltage, that is,

$$Q_s(V_{\rm gs}, V_{\rm ds}) = Q_s(V_{\rm gs}, V_{\rm ds} = 0) = -\frac{1}{2} Q_g(V_{\rm gs}, V_{\rm ds} = 0) . \qquad (18)$$

The Q_s is physically partitioned, and consequently, drain charge is given by

$$Q_d(V_{\rm gs}, V_{\rm ds}) = -Q_g(V_{\rm gs}, V_{\rm ds}) - Q_s(V_{\rm gs}, V_{\rm ds}) . \qquad (19)$$

On the other hand, Q_g is invariant under a simultaneous voltage shift with arbitrary value at the individual terminals. This principle leads to

$$\frac{\partial Q_g}{\partial V_g} + \frac{\partial Q_g}{\partial V_d} + \frac{\partial Q_g}{\partial V_s} = 0 . \qquad (20)$$

This gives a relationship between the gate-to-source and gate-to-drain capacitances $C_{\rm gs}$ and $C_{\rm gd}$, that is,

$$C_{\rm gs} = \frac{\partial Q_g}{\partial V_g} - C_{\rm gd} . \qquad (21)$$

Based on (17) and (21), $C_{\rm gs}$ and $C_{\rm gd}$ are obtained.

3. GB trap-induced physical phenomena

A. Composite Mobility

Poly-Si film is considered as a series resistance composed of IGs and GBs. IG mobility decreases with the vertical gate electric field. Since various factors affect the carrier transport, the IG mobility is semi-empirically modeled [16] as

$$\mu_{\mathrm{ig}} = \frac{\mu_{\mathrm{igo}}}{\left[1+\left(\frac{E_{s.\mathrm{eff}}}{E_o}\right)\right]^{g_n}} , \qquad (22)$$

where $Es_{.\mathrm{eff}}$ refers to the effective gate electric field and μ_{igo}, g_n, E_o are the model parameters. GB carrier transport is controlled by thermionic emission at GBs. The GB mobility is modeled [1], [2] as

$$\mu_{\mathrm{gb}} = \mu_{\mathrm{gbo}} L_g \exp(\beta\phi_t) , \qquad (23)$$

where μ_{gbo} is the model parameter. Based on (22) and (23), unified composite mobility μ_u is given by

$$\mu_u = (\mu_{\mathrm{ig}}{}^{-1} + \mu_{\mathrm{gb}}{}^{-1})^{-1} . \qquad (24)$$

When L_g is small or gate electric field is weak, low GB mobility dominates the total mobility as illustrated in Fig. 4.

B. GBMM effect

Output characteristics of poly-Si TFTs deviate from the scaling law of long channel MOSFETs. Figure 5 shows the output characteristics of TFTs with L_g = 86 nm and effective channel length L_{eff} = 3.4, 5.2, and 16.8 μm at V_{gs} = 10.5 V which are normalized at V_{ds} = 0.2 V. Pinch-off voltages of the TFTs are almost the same. However, drain current anomalously increases with V_{ds} as the L_{eff} decreases. This is

caused by the conductance or mobility modulation of poly-Si film. Linear current-voltage (*I-V*) characteristic of IG is expressed as

$$j_{\mathrm{ig}} = qn_{\mathrm{ig}} \cdot \mu_{\mathrm{ig}} \frac{V_{\mathrm{ig}}}{L_g} \equiv g_{\mathrm{ig}} \cdot V_{\mathrm{ig}} \tag{25}$$

and nonlinear *I-V* characteristic of GB is expressed as

$$\begin{aligned} j_{\mathrm{gb}} &= 2qn_{\mathrm{ig}} \cdot v_{\mathrm{th}} \exp(\beta\phi_t) \sinh\left[\frac{\beta(V_{\mathrm{gb}} - V_\delta)}{2}\right] \\ &\equiv g_{\mathrm{gb}} \frac{2}{\beta} \sinh\left[\frac{\beta(V_{\mathrm{gb}} - V_\delta)}{2}\right] \end{aligned}, \tag{26}$$

where n_{ig}, v_{th}, and V_δ refer to the IG carrier density, thermal velocity, and the parameter of the voltage drop at GBs. The g_{ig} and g_{gb} are the IG and GB conductance. While V_{ds} is small, V_{gb} increases with V_{ds} and low GB conductance dominates the drain current and keeps on increasing. Beyond the balancing point between the IG and GB conductance, V_{gb} saturates and the IG conductance controls the drain current instead and the anomalous current increase ceases as illustrated in the inset of Fig. 5. This behavior is described by the following equation which is obtained by equating (25) with (26).

$$\frac{\beta}{2} \cdot \frac{g_{\mathrm{ig}}}{g_{\mathrm{gb}}} \cdot \frac{L_g}{L_{\mathrm{eff}}} \cdot \left[V_{\mathrm{ds}} - \left(\frac{L_{\mathrm{eff}}}{L_g} + 1\right) \cdot V_{\mathrm{gb}}\right] = \sinh\left[\frac{\beta(V_{\mathrm{gb}} - V_\delta)}{2}\right]. \tag{27}$$

This equation indicates that $g_{\mathrm{ig}}/g_{\mathrm{gb}}$ and L_g/L_{eff} are the parameters to influence the V_{gb}. In other words, this is a scaling equation for the GBMM effect.

C. TDMM effect

TDMM effect is a transient phenomenon derived from carrier capture and emission at GBs, which is observed when switching on and off a poly-Si TFT. Poly-Si

film contains average trap density on the order of 10^{18} cm^{-3} [17], which corresponds to life time of 1 ns by rough estimation. Accordingly, when switching on, remaining holes in the IGs rapidly recombine with electrons and the IGs reach almost stationary state in 1 ns or so. Then, electron capture follows at the GBs accompanying the increase in the GB barrier height (Fig. 6). This increase in the barrier height causes the GB mobility modulation. The above statement was verified by 2-D device simulation [18]. The device parameters are: $L = 6.0$ μm, $L_g = 300$ nm, $T_{si} = 50$ nm, and gate oxide film thickness $T_{ox} = 145$ nm. The GB trap density model is given as follows.

$$N_t(E) = N_{ta} \exp[(E - E_c)/W] \ . \qquad (28)$$

The trap parameters are: $N_{ta} = 5.0\times10^{21}$ $cm^{-3}eV^{-1}$, $W = 0.025$ eV. The capture cross section of electron and hole are $\sigma_n = 1.0\times10^{-15}$ and $\sigma_p = 1.0\times10^{-13}$ cm^2, respectively. The gate voltage V_{gs} was switched on from 0.0 to 3.3 V in 20 ns. Figure 7 shows the transient behavior of the surface and back-surface potential, while Fig. 8 shows that of the GB barrier height and drain current. In Fig. 7, the back-surface potential fluctuates in the rising time and reaches almost stationary state in 30 ns, right after the bias rise. In Fig. 8, the drain current begins decreasing simultaneously with the increase in the barrier height at 20 ns. Switching-off transient behavior is similarly verified. As a result, we have only to consider carrier capture and emission at GBs to model TDMM effect.

In the case of mono-energetic trap state, rate equation for electron capture is described [19], [20] by

$$\left.\frac{dn_t}{dt}\right|_{cap.} = c_n \cdot n \cdot (N_t - n_t) , \qquad (29)$$

where c_n stands for $\sigma_n v_{th}$, and life time τ is given by $(c_n \cdot n)^{-1}$. By using time step Δt, (29) can be rewritten as

$$n_t(t+\Delta t) - n_t(t) = [N_t - n_t(t)] \cdot [1 - \exp(-c_n n \Delta t)] \ . \qquad (30)$$

We expand (30) to continuously distributed trap states at channel surface (Fig. 9) with assumption of simple superposition. Then, we obtain the time variation of trap charge density as

$$\begin{aligned} \Delta\langle Q_t \rangle &= -\frac{2q^2}{L_g} \int [N_t(\varphi, x) - n_t(\varphi, x, t)] \cdot \{1 - \exp[-c_n n_i \Delta t \exp(\beta\phi(x))]\} d\varphi dx \\ &= -\frac{2q^2}{L_g} \int_{-\phi}^{0} d\varphi \int_{\phi_b}^{\phi_s} \frac{d\phi}{E(\phi)} [N_t(\varphi, \phi) - n_t(\varphi, \phi, t)] \cdot \{1 - \exp[-c_n n_i \Delta t \exp(\beta\phi)]\} \end{aligned} \ . \qquad (31)$$

Here, the second factor in the integrand substantially behaves as $\Delta t / \tau \approx 1$ with ϕ larger than a critical value ϕ_c. In addition, we can focus on the surface region because the trap state density is exponentially high near the conduction-band edge and potential increases near the surface. Then, (31) is simplified as

$$\Delta\langle Q_t \rangle \approx -\frac{4q^2}{L_g} \frac{(\phi_s - \phi_c)}{E_s} \frac{\Delta t}{\tau} \int_{-\phi_s}^{0} [N_t(\varphi) - n_t(\varphi, t)] d\varphi \ . \qquad (32)$$

The E_s refers to the surface electric field. This integral means the subtraction of the transient trap density from the stationary trap density. Then, (32) is rewritten as

$$\Delta\langle Q_t \rangle = \frac{4(\phi_s - \phi_s^t)}{L_g \cdot E_s} \frac{\Delta t}{\tau} [Q_t(\phi_s) - Q_t(\phi_s^t)] \ , \qquad (33)$$

where ϕ^t_s refers to the transient surface potential or trap filling level in the GB trap and ϕ_c in (32) was replaced by ϕ^t_s. On the other hand, the trap term in (8) can be rewritten by using (4) as follows.

$$\begin{aligned} \frac{4}{L_g} \int_{\phi_b}^{\phi_s} Q_t(\phi) d\phi &= 2 \int_{\phi_b}^{\phi_s} q_t(\phi) d\phi = 2 \int_{\phi_b}^{\phi_s} q_t(\phi) d\phi \\ &= 2 \int_{T_{Si}}^{0} q_t(x) \frac{d\phi}{dx} dx \cong 2E_{\text{eff}} \int_{0}^{T_{Si}} q_t(x) dx = E_s \cdot \langle Q_t \rangle \end{aligned} \ . \qquad (34)$$

Here, $\langle Q_t \rangle$ refers to the GB trap charge density per surface area. In transient state, only ϕ^t_s varies, and consequently, (34) becomes

$$\frac{4}{L_g} Q_t(\phi_s^t) \cdot \Delta\phi_s^t = E_s \cdot \Delta\langle Q_t \rangle \ . \qquad (35)$$

Finally, we obtain the relationship between the time variation of $\phi^t{}_s$ and that of $\langle Q_t \rangle$ in the case of switching-on as

$$\Delta\phi_s^t = (\phi_s - \phi_s^t) \cdot \left[\frac{Q_t(\phi_s) - Q_t(\phi_s^t)}{Q_t(\phi_s^t)} \right] \cdot \frac{\Delta t}{\tau} \ . \qquad (36)$$

When switching-off, the relationship is similarly obtained as

$$\Delta\phi_s^t = -(\phi_s^t - \phi_s) \cdot \left[\frac{Q_t(\phi_s^t) - Q_t(\phi_s)}{Q_t(\phi_s^t)} \right] \cdot \frac{\Delta t}{\tau} \ . \qquad (37)$$

These relationships describe the trap-related transient behavior.

D. PVL effect

GB traps are terminated through hydrogenation process such as diffusion from silicon nitride (SiN_x) film deposited by the plasma-enhanced chemical vapor deposition (PE CVD) method. When the hydrogenation efficiency is low, huge amount of traps remain at the GBs, and then, PVL phenomenon appears. Gate voltage dependence of the observed pinch-off voltage becomes smaller than that of the ideal pinch-off voltage $V_{\rm gs} - V_{\rm th}$ keeping linear relationship between them as shown in Fig. 10. There are two possible mechanisms for the PVL phenomenon. One is GB current saturation. When the GB trap density is high, most of the bias is applied to GBs. Since GB current is proportional to the difference in the carrier density across the GBs, the current does not increase further as long as the source-side barrier height remains the same as shown in Fig. 11. The other is “early depletion” at the drain edge. When the IG conductance at the drain edge decreases to become comparable with the GB conductance, current also saturates even when the IG region is not depleted. This is

because current saturation is caused by the increase in the voltage drop near the drain edge. In any case, pinch-off appears earlier than in the ideal case. Considering the complicated physics in the PVL phenomenon, we adopt a semi-empirical model for the PVL by employing the relationship in Fig. 10 expressed as

$$V_{\text{p.observed}} = \alpha_{\text{pvl}} \cdot V_{\text{p.ideal}} \ . \qquad (38)$$

E. Off Current

In the off-state of poly-Si TFTs, drain current consists of three components: generation, gate-induced drain leakage (GIDL) [21], and diffusion current. Since poly-Si film contains huge number of traps, many carriers are generated via the traps in the depletion region of the drain junction. The generation current model is described by

$$I_{\text{gen}} = I_{\text{geno}} W \cdot N_t(0) \sqrt{V_{\text{ds}}} \exp(-\beta \phi_{\text{gen}}) \ , \qquad (39)$$

where I_{geno} is the model parameter, $N_t(0)$ and ϕ_{gen} refer to the trap density at the mid gap and activation potential for the generation. The GIDL is enhanced through tunneling via traps in poly-Si TFTs [22]. Then, the GIDL current becomes temperature dependent because the trap-assisted process is thermally activated. The trap-assisted GIDL current model is described by

$$I_{\text{gidl}} = W \cdot A_{\text{gidl}} \exp(-\beta \phi_{\text{gidl}})(V_{\text{dg}} - V_i) \exp\left(\frac{-B_{\text{gidl}}}{V_{\text{dg}} - V_i}\right) \cdot \left[1 - \exp\left(-\frac{\beta V_{\text{ds}}}{\text{C}_{\text{gidl}}}\right)\right] , \qquad (40)$$

where A_{gidl}, B_{gidl}, C_{gidl} are the model parameters and ϕ_{gidl} is the activation potential. The diffusion current becomes dominant when poly-Si TFTs are illuminated. Since electron is minority carrier in $V_{\text{gs}} < V_{\text{fb}}$, photo-generated electron diffuses to the drain region of *n*-ch TFTs. The diffusion current model is described by

$$I_{\mathrm{di}} = I_{\mathrm{dio}}(W \cdot t_{\mathrm{Si}})N \cdot \left[1 - \exp\left(-\frac{\beta V_{\mathrm{ds}}}{\alpha_{di}}\right)\right], \qquad (41)$$

where I_{dio}, α_{di} are the model parameters and N is the average carrier density per surface area.

4. Comparison with Measurements

A. Sample Preparation

Poly-Si TFTs with bottom-gate structure were fabricated on glass substrates. At first, the gate electrodes of molybdenum were defined. Then, silicon oxide (SiO_2) gate-insulator and amorphous silicon (a-Si) films were deposited successively by the PE CVD method, followed by the excimer laser annealing (ELA) crystallization process. Thickness of the gate-insulator was an alternative of 65 or 145 nm and that of a-Si was 40 nm. Poly-Si grain size was controlled by changing the ELA condition. Poly-Si islands were defined after the ion implantation for n^+ and LDD regions with dosage of 7.5×10^{19} and 1.8×10^{17} cm^{-3}, respectively. A composite inter-layer of SiO_2 and SiN_x films were deposited successively by the PE CVD method. Before the metallization, hydrogenation of poly-Si film was performed by 2-hour annealing at 400˚C in N_2 atmosphere, capped with the inter-layer SiN_x film.

B. Static Characteristics

Here, we verify the validity of the static characteristics of the model. All the evaluated samples are *n*-ch device without LDD structure and have drawn channel

length (L) of 20 μm in common. Figures 12 and 13 show output characteristics of type-1 and -2 poly-Si TFTs with same dimension of T_{ox} = 65 nm, L_g = 86 nm, and respective channel length L = 18 and 6 μm. In Fig. 12, drain current is well reproduced by the model. In Fig. 13, drain current keeps on increasing beyond the pinch-off point and current value is higher than that estimated in Fig. 12 by a simple scaling raw at any V_{ds}. The GBMM effect is well reproduced by the SPT model. Figure 14 shows output characteristics of a type-3 TFT with T_{ox} = 145 nm, L_g = 260 nm, and L = 18 μm. This sample has no inter-layer SiN_x film, then, the poly-Si film is not hydrogenated. Closed circles in the output characteristics show the ideal pinch-off voltage evaluated by the V_{th} value. The ideal pinch-off voltages seem higher for the output characteristics. The PVL effect is also well reproduced here. Model parameters for output characteristics of type-1 to -3 are listed in Table-I. Figure 15 shows transfer characteristics of a TFT with T_{ox} = 65 nm, L_g = 120 nm, and L = 8 μm at four different temperatures. Drain current increases with temperature as a whole. In the off-region, the plateau and the V_{gs} dependent portions respectively correspond to the generation and trap-assisted GIDL currents. Activation energy of the trap-assisted GIDL is smaller than that of the generation. Figure 16 shows transfer characteristics of a TFT with T_{ox} = 145 nm, L_g = 300 nm, and L = 18 μm with five illumination levels including a dark state. Drain current in off- and sbthreshold-regions increases with the luminance, while on-current remains almost the same. This is a big difference from the temperature dependence in Fig. 15. Finally, Fig. 17 shows V_{ds} dependence of the terminal capacitance C_{gs} and C_{gd} of the TFT in Fig. 12. As shown in Figs. 12-17, the SPT model can simulate static characteristics of poly-Si TFTs with good accuracy.

C. Dynamic Characteristics

Dynamic characteristics significantly influence the transient analysis of circuit simulations. Most essential issue in poly-Si TFTs is the TDMM effect. Figure 18 shows measured and simulated transient currents by single switching-on of an *n*-ch TFT with LDD structure and T_{ox} = 145 nm, L_g = 300 nm, and L = 9 μm. The drain current decays from high initial current value in millisecond time range. Such current decay can cause frequency dependence of circuit performance. Figure 19 shows simulated transient currents by sequential switching at 100 Hz and 1 kHz. Higher peak and larger decay current is observed in the case of 100 Hz driving. This frequency dependence is derived from the transient behavior of the GB traps. Figure 20 shows simulated transient potential ϕ^t_s corresponding to the current in Fig. 19. In 100 Hz driving, ϕ^t_s decreases sufficiently in the off-time and rapidly increases at switching on. This causes higher peak and larger decay current. In 1 kHz driving, on the other hand, ϕ^t_s cannot decrease much in the off-time, and consequently, ϕ^t_s stays within high value range. This causes lower peak and smaller decay current.

Following the previous discussion, a 21-stage inverter chain was prepared to verify the model performance by evaluating the frequency dependence of the delay time. The device parameters are T_{ox} = 145 nm, L_g = 300 nm, and L = 9 μm for both *n*- and *p*-ch TFTs of the inverter. *N*-ch TFTs have channel width W = 20 μm, overlap capacitance $C_{gso} = C_{gdo}$ = 3.13 fF, and LDD structures on both source and drain sides with resistance R-LDD = 3.8 kΩ. *P*-ch TFTs have W = 30 μm and $C_{gso} = C_{gdo}$ = 4.35 fF. Input voltage (V_{in}) of the inverter chain was set to be same as the high DC voltage (V_{dd}). Figure 21 shows measured and simulated frequency dependence of the delay time. The measured delay time increases with the frequency as a whole. We find that

this frequency dependence is well reproduced only by incorporating the TDMM effect. Without the TDMM effect, frequency dependence does not appear.

6. Conclusions

A new generation of SPT model has been developed considering the effect of carrier capture and emission, photo-induced carrier injection, and PVL phenomenon on the carrier transport. This model has realized simulation of GB trap-related frequency dependence of circuit performance and that of photo-induced current behavior. This model is the most suitable to simulate poly-Si TFTs circuits in display device with good accuracy.

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[List of figure captions]

Fig. 1. A diagram for the symmetric GB trap state density model. Effective acceptor-type trap density is defined by $n_t(-\phi+\phi_f) - n_t(\phi_f)$.

Fig. 2. A band diagram at MOS surface. (a) Dark (equilibrium) state. E_f coincides with E_{fm}. (b) Illuminated state. Electron Fermi level E_{fn} coincides with E_{fm}. Surface band bends upward due to the split in E_f.

Fig. 3. A band diagram of a poly-Si TFT channel region. Carrier trapping at GBs causes barrier potential. GB potential is measured from the base surface potential. Neumann boundary condition is applied at the back surface.

Fig. 4. V_{gs} dependence of composite mobility μ_u composed of IG and GB mobility.

Fig. 5. Drain current normalized at $V_{ds} = 0.2$ V. Current increases anomalously with V_{ds} as L_{eff} decreases despite almost the same pinch-off voltage. In this bias region, GB conductance is dominant. Beyond the critical point, IG conductance becomes dominant instead (inset).

Fig. 6. Origin of the TDMM effect in switching on. (a) Electron capture process at GBs. (b) Electron capture and increase in GB barrier height.

Fig. 7. Device simulation result of switch-on time evolution of the IG back-surface potential and potential difference between the both surfaces.

Fig. 8. Device simulation result of switch-on transient drain current and the GB barrier height at the surface.

Fig. 9. Definition of continuously distributed trap states in the channel surface.

Fig. 10. Relationship between observed pinch-off voltage and ideal one. For convenience, we evaluated the observed pinch-off by gds-minimizing point V_{min}. Thickness of SiN_x film controls hydrogenation efficiency in poly-Si.

Fig. 11. Device simulation result in the case of high GB trap density. Most of the bias is applied to the GB.

Fig. 12. Output characteristics of a poly-Si TFT with T_{ox} = 65 nm, L_g = 86 nm, and L = 18 μm.

Fig. 13. Output characteristics of a poly-Si TFT with T_{ox} = 65 nm, L_g = 86 nm, and L = 6 μm.

Fig. 14. Output characteristics of a poly-Si TFT with T_{ox} = 145 nm, L_g = 260 nm, and L = 18 μm. Poly-Si film is not hydrogenated. Closed circle refers to the ideal pinch-off voltage.

Fig. 15. Transfer characteristics of a poly-Si TFT with T_{ox} = 65 nm, L_g = 120 nm, and L = 8 μm at four different temperatures.

Fig. 16. Transfer characteristics of a poly-Si TFT with T_{ox} = 145 nm, L_g = 300 nm, and L = 18 μm with five illumination levels. Photo-1 to -4 correspond to the n_{ph}s of 1.40×10^{13}, 4.30×10^{13}, 1.10×10^{14}, and 1.42×10^{14} cm^{-3}.

Fig. 17. V_{ds} dependence of terminal capacitance C_{gs} and C_{gd} of a poly-Si TFT with T_{ox} = 65 nm, L_g = 86 nm, and L = 18 μm.

Fig. 18. Measured and simulated transient current by single switching of an *n*-ch TFT with LDD structure with V_{ds} = 0.2 V.

Fig. 19. Simulated transient current by sequential switching of an *n*-ch TFT with LDD structure (V_{ds} = 0.1 V). (a) 100 Hz switching case. (b) 1 kHz switching case.

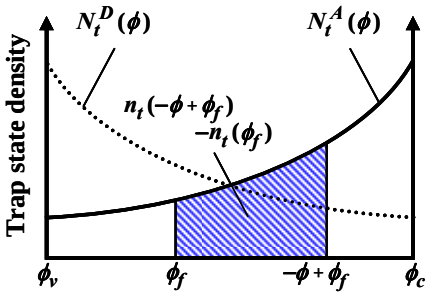
Fig. 20. Simulated transient potential ϕ_s^t by sequential switching of an *n*-ch TFT with LDD structure (V_{ds} = 0.1 V). (a) 100 Hz switching case. (b) 1 kHz switching case.

Fig. 21. Measured and simulated frequency dependence of delay time in a 21-stage inverter chain. Open circle refers to the measured data.

[Table captions and tables]

Table I. Model parameters for output characteristics of poly-Si TFTs in Figs. 12-14.

Parameter	Type-1	Type-2	Type-3
N_{te} ($cm^{-2}\,eV^{-1}$)	1.20×10^{13}	1.32×10^{13}	3.72×10^{13}
N_{to} ($cm^{-2}\,eV^{-1}$)	-4.00×10^{11}	-4.00×10^{11}	1.60×10^{12}
γ (eV^{-1})	3.57	3.70	2.15
V_{fb} (V)	−3.0	−3.2	−11.7
μ_{igo} ($cm^2\,V^{-1}s^{-1}$)	1.10×10^{3}	1.20×10^{3}	1.00×10^{3}
g_n (1)	0.56	0.40	0.10
E_o ($V\,cm^{-1}$)	1.7×10^{4}	1.1×10^{4}	1.0×10^{4}
μ_{gbo} ($cm\,V^{-1}s^{-1}$)	1.18×10^{7}	1.06×10^{7}	1.10×10^{8}
α_{gbmm} (1)	0.09	0.14	0.01
α_{pvl} (1)	1.00	1.00	0.443



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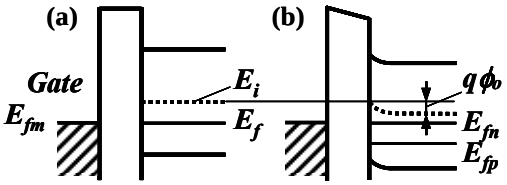

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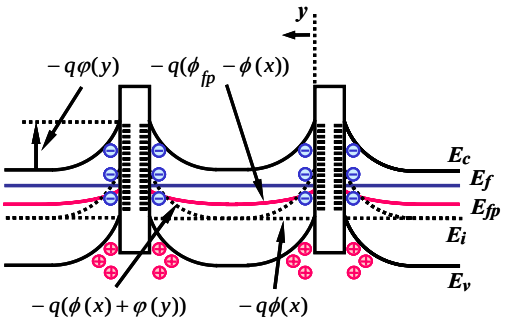

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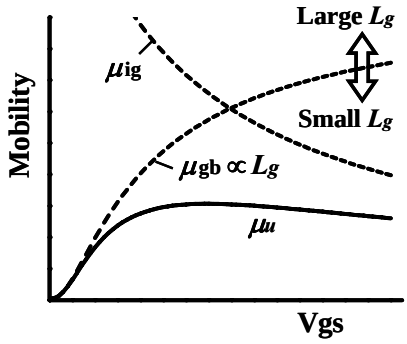

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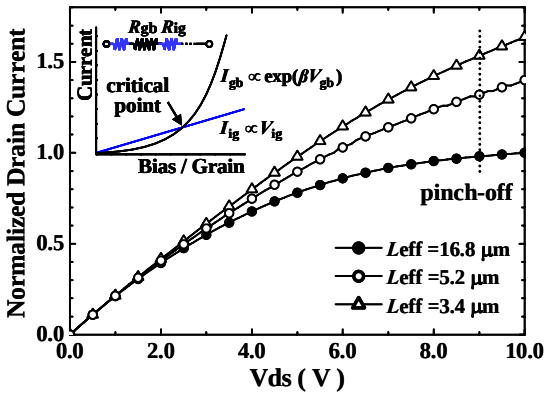

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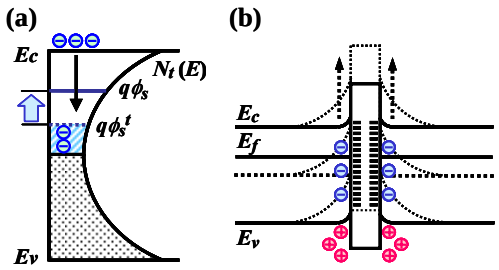

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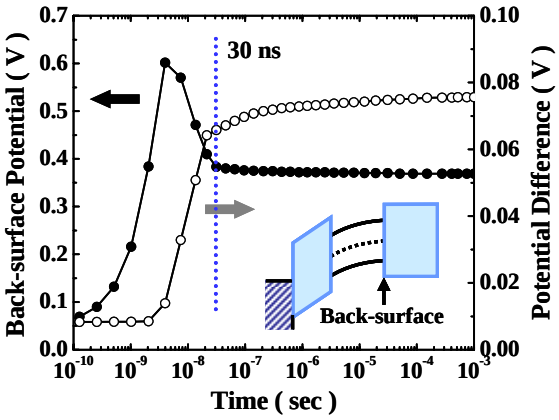

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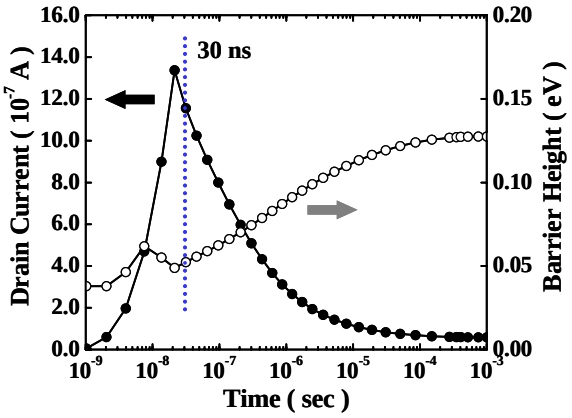

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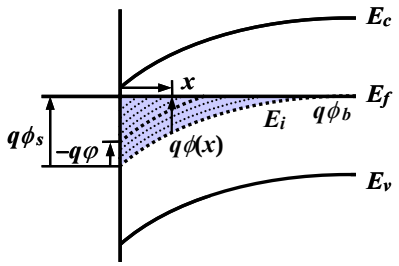

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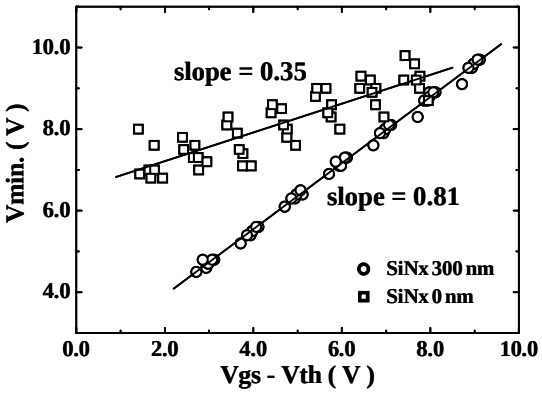

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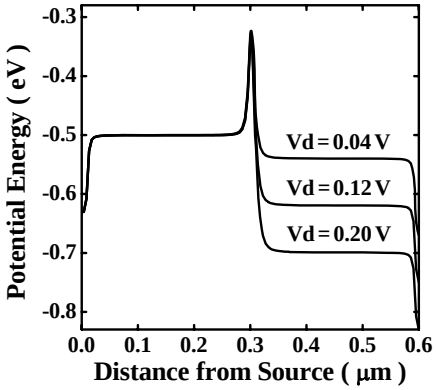

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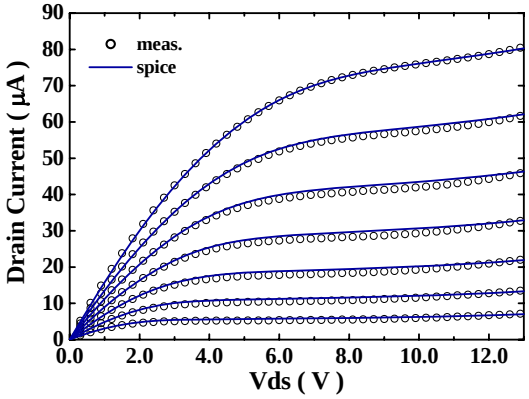

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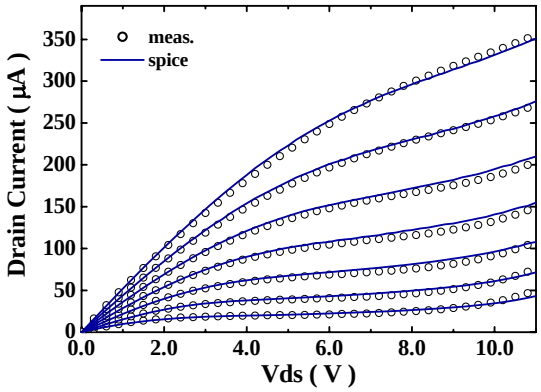

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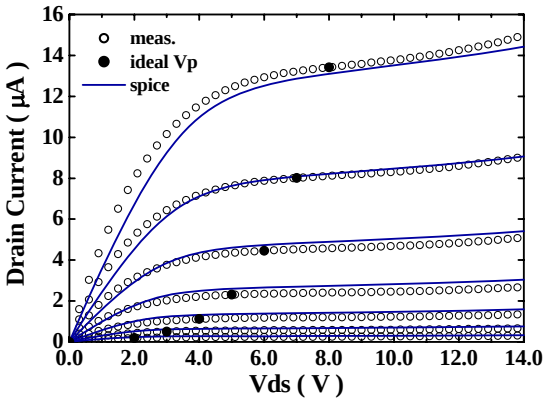

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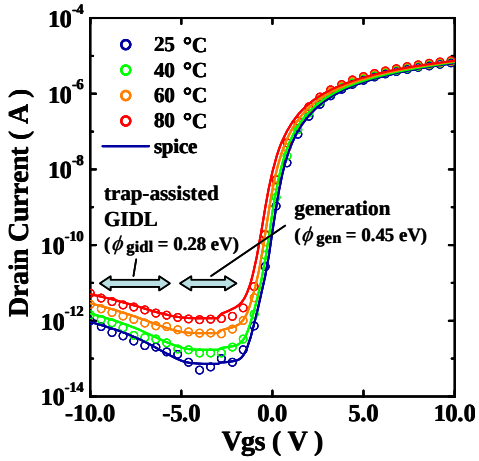

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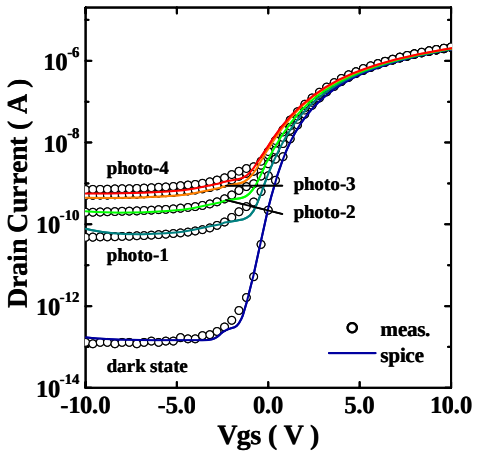

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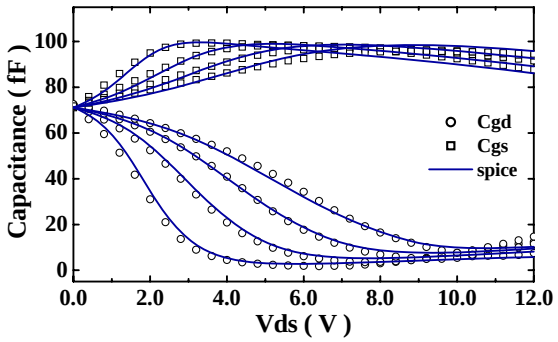

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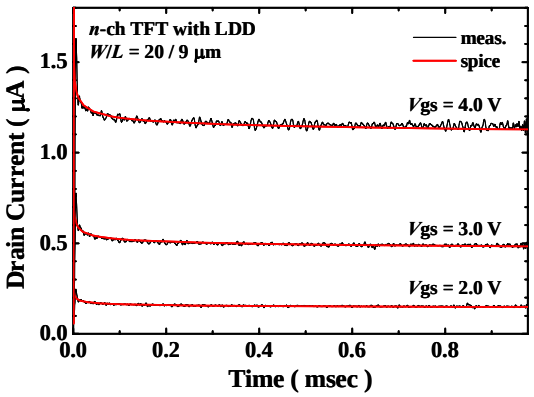

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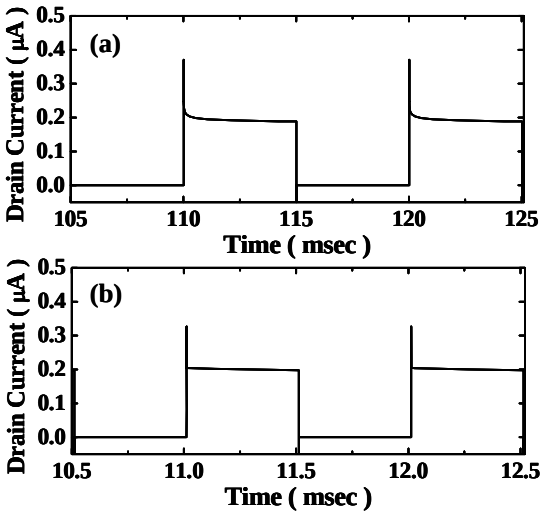

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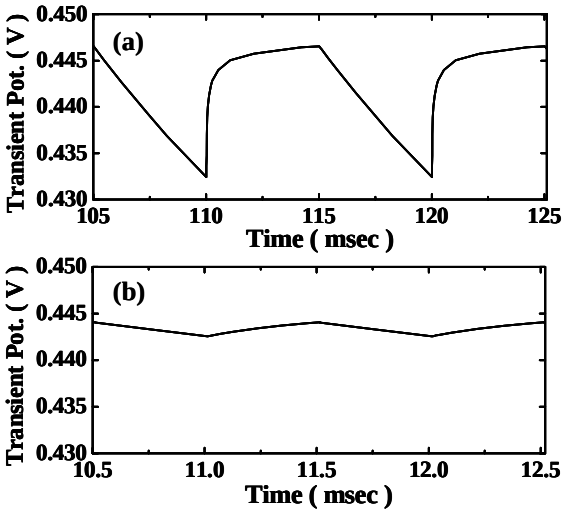

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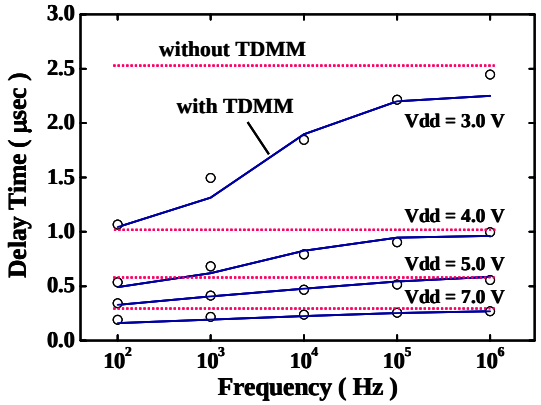

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