PAPER

An Improvement of Banyan Networks and 2-Dilated Banyan Networks Based on Bypasses Positioning

Komain PIBULYAROJANA[†], Shigetomo KIMURA^{††}, and Yoshihiko EBIHARA^{††}, Regular Members

SUMMARY Banyan networks and their improved switches such as 2-dilated banyan networks are usually constructed by a self-routing mechanism, and provide a high multiplexing transmission capacity to ATM networks. Due to cell blocking in the switching elements in these banyan networks, however, cell loss is occurred and then the throughput of each network is decreased. To improve this problem, we have introduced bypasses to the original and the 2-dilated banyan networks. This paper focuses on the position of the bypasses in these banyan networks and proposes the one-bypass-connection methods in order to minimize cell transfer delay caused by the bypasses. We also analyze output rate of each network and show that the bypass method gives network designers flexible selections for network performance and transfer delay.

 ${\it key\ words:}\ {\it bypass,\ banyan\ network,\ 2-dilated\ banyan\ network,\ cell\ blocking,\ ATM}$

1. Introduction

Asynchronous Transfer Mode (ATM) is developing for a basic technique to construct B-ISDN. ATM realizes transmitting many data streams simultaneously by slicing them to short fixed length labeled units called cells. These cells are exchanged to deliver their correct destination by an ATM switch, which is easy to be constructed by hardware and expected to faster processing.

For the ATM switch [1], there are several construction methods can be considered. The self-routing switch such as the banyan network [2], [3] is the one of their famous methods. For example, 2-dilated banyan networks [4] which are introduced from the banyan network by replacing each link between switching elements by two independent links. Due to cell blocking in the switching elements in these banyan networks, however, cell loss is occurred and then the throughput of each network is decreased. To improve this problem, we have introduced bypasses to the original and the 2-dilated banyan networks [5]. Since the bypasses may forward a blocked cell to the upper neighbored switching element, it is caused to decrease the cell loss rate, but increase cell transfer delay in the networks. From this result, this paper focuses on the position of the bypasses

Manuscript received August 9, 1999.

in these banyan networks, and proposes the networks with one-bypass-connection in order to minimize cell transfer delay caused by the bypasses.

There are other improved networks based on the banyan network, such as the rerouting banyan networks [6] and the folded banyan switching networks with bypass links [7]. The former has buffers to reroute blocked cells and provides the required cell loss rate by increasing columns of switching elements. The latter has distribution part and buffered routing part, which are connected by bypass links and turn back links. Each cell is tagged and entered the former part. If a cell satisfies some condition called the bypass check in each switching element, it is passed to the latter part though the bypass link, and destined to the output port. Otherwise the ordinary banyan process is repeatedly occurred until the bypass check is satisfied or operated at the turn back link. Thus, the purpose of the bypass link is different from the one of this paper.

Although these networks have buffers and provide higher output rate, our paper subjects to the unbuffered ATM switches based on the banyan network. The unbuffered switches have the advantages than the buffered switches in the following points. 1) The hardware size of the former is quite smaller than the one of latter. 2) The switching time (delay) is much shorter, since there is no waiting time in buffer. However, the former tends to be lower output rate than the latter. Our approach of bypass methods improves the output rate of the former.

We introduce the original and the 2-dilated banyan network in the next section, and insert bypasses into these banyan networks in Sect. 3. The performance analyses of these banyan networks with and without bypasses are also examined at each section, respectively. In Sect. 4, we propose the networks with one-bypass-connection to decrease cell transfer delay, and compare their performance to the ones of the other networks. Finally, we describe the conclusion and discuss the ability to expand another improved banyan networks by the bypass method in Sect. 5.

2. Banyan Networks and 2-Dilated Banyan Networks

This section briefly introduces banyan networks and 2-

Manuscript revised January 6, 2000.

[†]The author is with the Doctoral Programs in Engineering, University of Tsukuba, Tsukuba-shi, 305-8573 Japan.

^{††}The authors are with the Institute of Information Sciences and Electronics, University of Tsukuba, Tsukuba-shi, 305-8573 Japan.

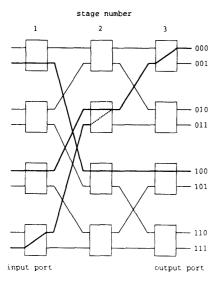


Fig. 1 8×8 banyan network with three stages.

dilated banyan networks, which are proposed for self-routing networks [8] of an ATM switch.

2.1 Banyan Networks

A regular $N \times N$ banyan network is constructed of the columns, called stages, of 2×2 switching elements which are set to either a straight through connection or a crossed connection. The switching elements are connected each other with links as shown in Fig. 1. The input cells to the network are labeled each destination output port number. An N input network has $\log_2 N$ stages (N is assumed to be a power of 2), and each stage has $\frac{N}{2}$ switching elements.

The routing algorithm of the banyan network is in below. In the *n*-th stage, a switching element examines the *n*-th bit of destination output port number in the cell header and selects an output port of the switching elements. If the bit is 0, the upper output port is selected, and otherwise the lower one is selected. Since only one cell can be forwarded on the single output link, cell loss occurs when two cells are arriving at a switching element and are destined for the same output port.

In Fig. 1, three cells enter at the input port 1, 4 and 7. Their destination output port numbers are 4, 0 and 1, respectively. From the routing algorithm, the cell from 1 arrives to 4 without blocking. However two cells from 4 and 7 are debated for the same link at the second stage which we call blocking. In this figure, the former one is forwarded, but the latter is deleted. In the next section, the latter cell will be also forwarded through bypass and received to its destination.

Let p_m be the input rate and p_{m+1} be the output rate of the m-th stage $(0 \le m \le \log_2 N - 1)$ of an $N \times N$ banyan network. By the above routing algorithm, they satisfy the following recurrence relation [9]:

$$p_{m+1} = 1 - \left(1 - \frac{p_m}{2}\right)^2,\tag{1}$$

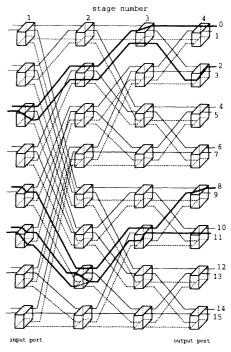


Fig. 2 16×16 2-dilated banyan network with four stages.

with boundary condition $p_0 = p$, where p is the probability of cell arrival at each input port.

2.2 2-Dilated Banyan Networks

The basic idea of the 2-dilated banvan network is to expand the internal link bandwidth in order to reduce cell-loss probability and then increase switch throughput. The 2-dilated banyan network is constructed of the original banyan network by replacing each link between switching elements by two independent links. Therefore, the routing algorithm of the network is shown as follows. A switching element receiving a cell examines the n-th bit destination output port number in the cell header and selects an output port of the switching elements as the original banyan network. But even when two cells select the same output port, both cells can be forwarded. If three or more cells select the same output port, then two cells are selected randomly and forwarded, and the others are blocked. For example, in the seventh switching element at the second stage in Fig. 2, three cells select the upper output port (at behind side of the element in this figure) and one of them is blocked. In the next section, we will recover such blocked cells by setting bypasses to increase network throughput.

The $N \times N$ 2-dilated banyan network is sequentially constructed from the 2×4 re-arrangeable input switches at the first stage of the network, the 2-dilated switches at the medium second to (n-1)-th stages where $n = \log_2 N$, and the 4×2 re-arrangeable output switches at the last stage. At the first stage, let us assume $p_0 = p$, where p is the probability of cell arrival

at the input port. We calculate the output rate at each stage as follows [10], [11]:

$$p_1 = \frac{1}{2}p,\tag{2}$$

$$p_{d+1} = p_d - \frac{1}{4}p_d^3 + \frac{1}{16}p_d^4 \quad (1 \le d \le n - 2), \tag{3}$$

$$p_n = 2p_{n-1} - \frac{3}{2}p_{n-1}^2 + \frac{1}{2}p_{n-1}^3 - \frac{1}{16}p_{n-1}^4.$$
 (4)

3. The Original and the 2-Dilated Banyan Networks with Bypasses

The purpose of a bypass is to forward a blocked cell to the upper switching element of the same stage to decrease the internal blocking in the network. But we cannot connect all switching element in the same stages of the network with bypasses because a wrong bypass may forward cells to the incorrect destinations. In the case of using bypasses in all stages of the $N \times N$ network, let $n = \log_2 N$, which is the number of stages. Then at d-th stage $(1 \le d \le n-1)$, from $((m-1)2^{n-d}+1)$ th to m^{2n-d} -th switching elements are connected by by passes sequentially, where $m=1, ..., 2^{d-1}$. Note that there is no bypass at n-th stage because a cell may be forwarded to the incorrect output destination. The 8×8 banyan network with bypasses is shown in Fig. 3. At this figure, the two blocked cells in the first and second stages are forwarded to the correct destination, respectively, by using the bypasses. We also notice that we do not adopt to connect a bypass between $((m-1)2^{n-d}+1)$ -th and $m2^{n-d}$ -th switching elements and make a bypass loop. This loop may decrease cell loss rate of its network, however, cell transfer delay of the network expands about twice and each switching element is more complicated to prevent any cells rounding on the loop.

In the case of 2-dilated banyan network, we insert the bypasses during the same stage of switching elements as the banyan network. But no blocking occurs in the first stage of 2-dilated banyan network, then the bypasses is not needed in this stage. The 16×16 2-dilated banyan network with bypasses is shown in Fig. 4, where the blocked cell in the 2nd stage is forwarded by the bypass.

3.1 Assumptions of Throughput Analysis

We respectively analyze the throughputs of the banyan network and the 2-dilated banyan network with bypasses. Their throughputs are considered on the switching elements at each stages under the following conditions:

1. Each network has not any sort of cell buffers.

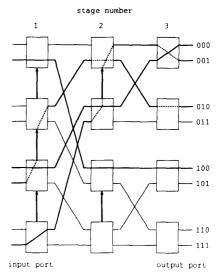


Fig. 3 8×8 banyan network with bypasses.

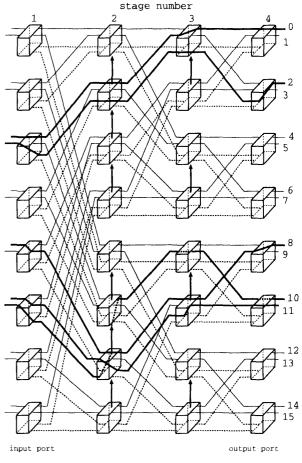


Fig. 4 16×16 2-dilated banyan network with bypasses.

- 2. Every processor in transmitting to these networks generates random and independent cells.
- 3. Cells arriving at an input of each network are uniformly distributed all over the outputs of the network.
- 4. The probability of output rate in a switching element becomes the probability of input rate into the connected switching element by a link or a bypass.

- 5. Cells may have link debate or be forwarded through a link or a bypass independently in the previous ones.
- The blocked cells are neglected. Then, the cells issued at the next time cycle are independent in the previous ones.
- 7. A link and a bypass between two switch elements can carry only one cell in each time cycle.

In the original and the 2-dilated banyan networks, we can suppose that every input rate of the same stage is equal. But such an assumption is not satisfied in the case of networks with bypasses. Thus, the output rates are rather complicated than the ones in the previous section.

For two switching elements connected by a bypass each other, the lower one must process cells before the upper one begins, because of the bypass direction. However, sequence control of cells is not concerned in ATM. Therefore, we also assume that all cells in the same stage is forwarded to the next stage after cells at the top switching element have been processed. In the next section, we will discuss about cell transfer delay according to this assumption.

3.2 Input Rate and Output Rate of the Banyan Network with Bypasses

There are four kinds of switching elements in banyan network with bypasses, illustrated in Fig. 5. Type 1 and 3 switching elements have bypass input and bypass output, respectively. They are placed at the bottom and the top of switching elements connected by bypasses in the same stage. Type 2 has both bypass input and output. It may be connect between Type 1 and 3 to construct the switching elements sequence. Type 4 is the original banyan switching element in the previous section.

We calculate the output rates of these switching elements at different input rates, and use the results of each switching element as the input rates to calculate the output rates of the next switching elements.

Assume a and b as the input rate of the switching elements, q as the bypass input rate from the lower switching element, p as the output rate and r as the output rate of the blocked cell forwarded to the bypass. First, we examine p and r of Type 2 (see detail in Appendix A.1). Then p and r are satisfied:

$$p = \frac{1}{2}a + \frac{1}{2}b - \frac{1}{4}ab + \frac{1}{2}q - \frac{1}{4}aq - \frac{1}{4}bq + \frac{1}{8}abq,$$
(5)

$$r = \frac{1}{2}ab + \frac{1}{2}aq + \frac{1}{2}bq - \frac{1}{2}abq.$$
 (6)

Type 1 and 4 have no input bypass link (parameter q). At Type 2, if no cell comes from the input bypass

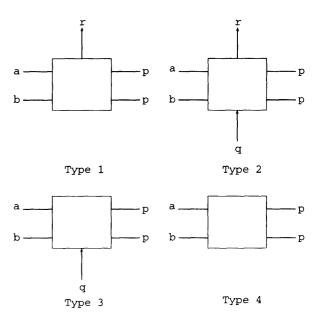


Fig. 5 Banyan switching elements.

link, i.e., the probability q is 0, then p of Type 1 and 4 equals to (5), and r of Type 1 equals to (6). p of Type 3 is the same result of (5) with no conditions.

From the construction of the banyan network with bypasses, all output rate in the final stage are equal. For throughput analysis, it is enough to obtain only one output rate of the network.

3.3 Input Rate and Output Rate of the 2-Dilated Banyan Network with Bypasses

As the banyan network, we solve the output rates of the 2-dilated banyan network for six kinds of switching elements in Fig. 6 and Fig. 7 at difference input rates. The results of output rates in each stage will be used as input rates to the next stage. In the 2-dilated banyan network, 2×4 re-arrangeable input switch Type 6 at the first stage has no bypass as we mentioned. Then, its output rate p at the first stage is the same as (2). From the second stage, four switching elements, called Type 1 to 4, which correspond to the ones of the banyan with bypasses respectively, are constructed. Note that Type 4 which is presented in Fig. 7 will be used at the next section. At the last stage of the network, the 4×2 rearrangeable output switching element Type 5 are used, whose the input rates are not equal.

As in the previous subsection, we examine two output rates of Type 2. Assume a, b, c and d as the input rate of a switching element, q as the bypass input rate from the lower switching element, p as the output rate and r as the output rate of the blocked cell forwarded to the bypass. Then p and r are calculated as in below (see detail in Appendix A.2). The output rates of Type 1, 3 and 4 are obtained as well as the banyan network with bypasses.

$$p = \frac{1}{4}a + \frac{1}{4}b + \frac{1}{4}c + \frac{1}{4}d - \frac{1}{16}abc - \frac{1}{16}abd - \frac{1}{16}acd$$

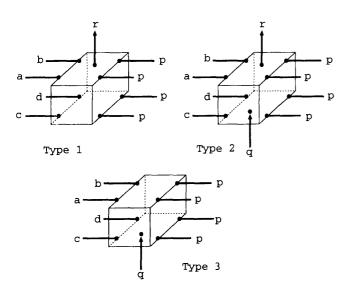


Fig. 6 2-dilated banyan switching elements Type 1, 2 and 3.

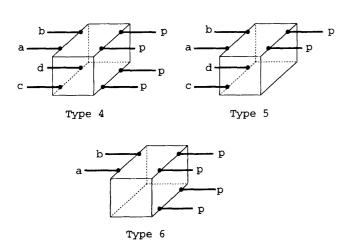


Fig. 7 2-dilated banyan switching elements Type 4, 5 and 6.

$$-\frac{1}{16}bcd + \frac{1}{16}abcd + \frac{1}{4}q - \frac{1}{16}abq - \frac{1}{16}acq$$

$$-\frac{1}{16}adq - \frac{1}{16}bcq - \frac{1}{16}cdq - \frac{1}{16}bdq + \frac{1}{16}abdq$$

$$+\frac{1}{16}acdq + \frac{1}{16}bcdq + \frac{1}{16}abcq - \frac{3}{64}abcdq, \qquad (7)$$

$$r = \frac{1}{4}abc + \frac{1}{4}acd + \frac{1}{4}abd + \frac{1}{4}bcd - \frac{3}{8}abcd - \frac{3}{8}abcq$$

$$-\frac{3}{8}acdq - \frac{3}{8}abdq - \frac{3}{8}bcdq + \frac{3}{8}abcdq + \frac{1}{4}abq$$

$$+\frac{1}{4}acq + \frac{1}{4}adq + \frac{1}{4}bcq + \frac{1}{4}bdq + \frac{1}{4}cdq. \qquad (8)$$

For Type 5, the output rate p is calculated as follows (refer Appendix A.2 for more detail):

$$p = \frac{1}{2}a + \frac{1}{2}b + \frac{1}{2}c + \frac{1}{2}d - \frac{1}{4}ab - \frac{1}{4}ac$$

$$-\frac{1}{4}ad - \frac{1}{4}bc - \frac{1}{4}cd + \frac{1}{8}abc + \frac{1}{8}abd$$

$$+\frac{1}{8}acd + \frac{1}{8}bcd - \frac{1}{16}abcd. \tag{9}$$

Note that (9) is equal to (4) when a = b = c = d.

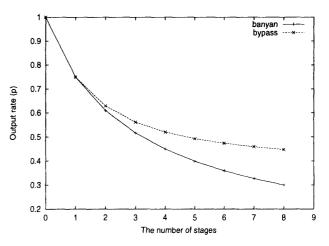


Fig. 8 The output rates of banyan networks with and without bypasses at input rate = 1.0.

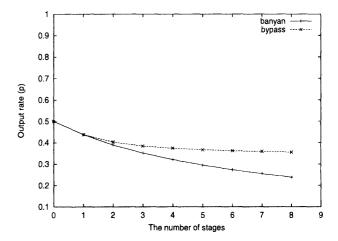


Fig. 9 The output rates of banyan networks with and without bypasses at input rate = 0.5.

From the construction of the switch, all output rates at the final stage are also equal.

3.4 Comparison of Output Rates of the Networks with and without Bypasses

From the equations presented at the previous subsection, the results of output rates for the $2^1 \times 2^1$ to $2^8 \times 2^8$ banyan networks with and without bypasses, whose arrival rate (input rate) are 1.0 and 0.5, are indicated in Fig. 8 and Fig. 9. The results for the 2-dilated banyan networks with and without bypasses are also indicated in Fig. 10 and Fig. 11. In these figures, x axis shows the number of stages and y axis denotes the output rates of each network.

In Fig. 8 and Fig. 9,

- "banyan" shows the output rate of the original banyan networks and,
- "bypass" shows the output rate of the banyan networks with bypasses.

From Fig. 8, we can find banyan networks with

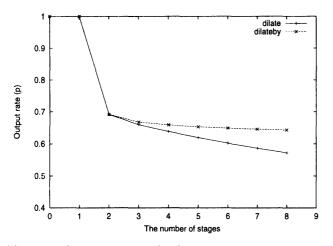


Fig. 10 The output rates of 2-dilated banyan networks with and without bypasses at input rate = 1.0.

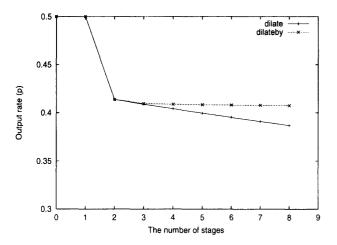


Fig. 11 The output rates of 2-dilated banyan networks with and without bypasses at input rate = 0.5.

bypasses have approximately 3 to 49 percent higher output rates than original banyan networks. For example at the 7 stages case in Fig. 8, its throughput becomes from 0.359 to 0.473, which is about 31.8 percent improvement. The maximum ATM transfer speed defined by ATM Forum is 622 Mbps. Since a cell has a header (5 bytes) and a payload (48bytes), the total length 424 bits. Thus, this transfer speed is equal to 1.46 Mcells/s. Therefore, the 31.8 percent performance improvement corresponds to 0.166 Mcells/s. This means about 42.8 MPEG1 (1.5 Mbps) or 16.0 MPEG2 (NTSC, 4 Mbps) channels is more available than the original banyan network.

When the network load is not so heavy, i.e., its input rate is 0.5, Fig. 9 shows that the output rates with usage of the bypasses are increased from 3 to 49 percent to the original ones. This fact concludes that the bypasses for the banyan networks are also much effective even if their network loads are low.

In Fig. 10 and Fig. 11,

• "dilate" shows the output rate of the 2-dilated banyan networks and,

• "dilateby" shows the output rate of the 2-dilated banyan networks with bypasses.

The 2-dilated banyan network is needed to be constructed at least 2×4 re-arrangeable input switches and 4×2 re-arrangeable output switches. Therefore, its switch size must be greater than $2^2 \times 2^2$. Indeed, when the number of stages in Fig. 10 is 1, the output rate is meaningless, since its result is observed from a 2×4 re-arrangeable input switch.

From 2 to 8 stages cases, in Fig. 10, 2-dilated banyan networks with bypasses have approximately 1 to 12.5 percent higher than the ones without bypasses. For example, the throughput at the 7 stages case is improved from 0.5862 to 0.6461, which corresponds that more 22.4 MPEG1 (1.5 Mbps) or 8.4 MPEG2 (NTSC, 4 Mbps) channels is useful than the ordinary 2-dilate one.

In Fig. 11, the output rates increase 0.1 to 5.3 percent, which are less improved than the previous cases. This means the bypass much effects to the throughput of the 2-dilated banyan network at the high input rate.

4. Original and 2-Dilated Banyan Networks with One-Bypass-Connection

In the previous section, we improve the throughput of the banyan network and the 2-dilate banyan network by inserting the bypasses during the switching elements in the same stage of the networks. As we mentioned, however, a switching element with a bypass from its lower switching element must stay its switching process until the lower switching element decides whether it forwards a cell to the bypass or not.

For example, the top switching element of the first stage in Fig. 3 can process its input cells, after fourth to second switching elements in the same stage have done. Therefore, its cell transfer delay may be four times greater than the one of the original banyan network, and the total switching times of banyan network and 2-dilated banyan network are increased. In order to minimize the increment of cell transfer delay, we construct networks with no Type 2 switching element and limit the maximum length of switching elements sequence connected by bypasses to at most two. Then, its cell transfer delay may be estimated twice as long as the original one.

4.1 Networks with One-Bypass-Connection

There are various designs to place bypasses for the networks with one-bypass-connection. When the highest output rate is required, every (2m-1)-th and 2m-th switching elements in all stages except the final one need to be connected by bypasses so as to maximize the number of bypasses in the $N \times N$ network, where $m=1, \ldots, \frac{N}{2}$. As in the previous section, bypasses in the

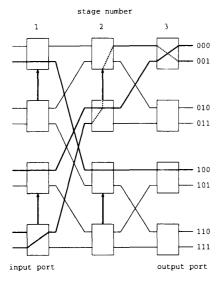


Fig. 12 8×8 banyan network with one-bypass-connection.

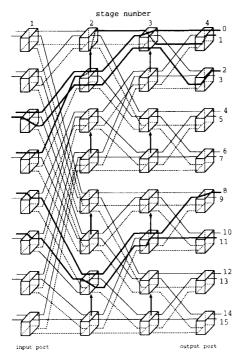


Fig. 13 16×16 2-dilated banyan network with one-bypass-connection.

first stage of 2-dilated banyan network are also omitted. The maximized network is called network with one-bypass-connection. Figure 12 and Fig. 13 illustrate the 8×8 banyan network with one-bypass-connection and the 16×16 2-dilated banyan network with one-bypass-connection, respectively.

4.2 The Throughputs of the Networks with One-Bypass-Connection

From the results in the previous section, we can also calculate the output rates of any design of networks with one-bypass-connection. Figure 14 and Fig. 15 show the output rates of three kinds of banyan network and 2-

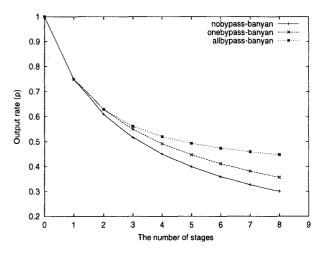


Fig. 14 The output rates of banyan networks with one-bypass-connection, all-bypasses-connection and no bypass at input rate = 1.0.

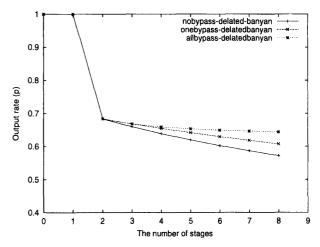


Fig. 15 The output rates of 2-dilated banyan networks with one-bypass-connection, all-bypasses-connection and no bypasses at input rate = 1.0.

dilated banyan networks, respectively, where their input rates are 1.0. In these figures, "nobypass" means the output rate of the original network. "onebypass" is the one of the network with one-bypass-connection in the previous subsection. "allbypass" is the one of the original or the 2-dilated banyan network with bypasses in the previous section, which we call the banyan or the 2-dilated banyan networks with all-bypasses-connection in the rest of the paper.

In Fig. 14, from 3 to 8 stages cases, banyan networks with one-bypass-connection have approximately 6.36 to 18.67 percent higher output rates than the original ones but 2.18 to 25.59 percent lower output rates than the banyan networks with all-bypasses-connection.

In Fig. 15, from 4 to 8 stages cases, 2-dilated banyan networks with one-bypass-connection have approximately 2.52 to 6.22 percent higher output rate than the original 2-dilated banyan network but 0.65 to 5.95 percent lower output rates than the 2-dilated banyan networks with all-bypasses-connection.

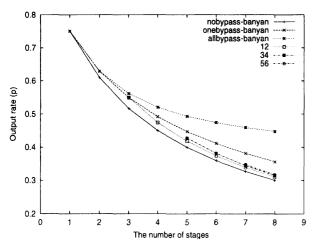


Fig. 16 The output rates of banyan networks with one-bypass-connection at two neighbored stages and the whole stages, all-bypasses-connection and no bypass at input rate = 1.0.

As the number of stages are increased, the network with all-bypasses-connection has larger output rate but greater cell transfer delay than the one with one-bypass-connection. For example, the former may have 64 times delay than the latter at the 8 stages case.

4.3 One-Bypass-Connection at Two Neighbored Stages of Networks

In the previous section, we construct one-bypass-connection at the whole stages we can. This subsection compares the effectiveness of this connecting at each stage for output rate. For this purpose, we construct banyan networks with one-bypass-connection, whose bypasses are inserted to only first and second stages or, third and fourth stages, fifth and sixth stages, respectively. At each inserted stage, every (2m-1)-th and 2m-th switching elements are connected by a bypass, where $m=1,\ldots,\frac{N}{2}$ for the $N\times N$ network.

For the 2-dilated banyan network, first stage is not needed to insert bypasses. Thus, we construct the new 2-dilated banyan network with one-bypass-connection as the same manner except that bypasses insertion begins from second stage, i.e., inserting second and third stages, and so on. Figure 16 and Fig. 17 show output rates of the banyan network and the 2-dilated banyan network with one-bypass-connection at two neighbored stages and the whole stages, all-bypasses-connection and no bypass at input rate = 1.0. In these figures, "12" etc. indicate the stage numbers inserted one-bypass-connection. The other plot marks are same as in Fig. 14 and Fig. 15.

We focus our discussion to the difference of the output rates in one-bypass-connection at two neighbored stages. From Fig. 16, we find that the bypasses inserted at two neighbored stages near the output ports gives higher output rates than the one near the input ports. Though the maximum difference of their output

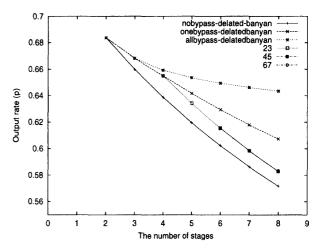


Fig. 17 The output rates of 2-dilated banyan networks with one-bypass-connection at two neighbored stages and the whole stages, all-bypasses-connection and no bypass at input rate = 1.0.

rates is less than 1 percent, the bypasses insertion stage influences to the performance improvement of banyan network.

Figure 17 also shows the same results as in Fig. 16. However, this figure indicates the output rates in one-bypass-connection at two neighbored stages almost equal each other. Since the occurrence of cell blocking in the 2-dilated banyan network is much smaller than the one of the banyan network, the bypasses insertion position has less influence to the output rate than the one of the original banyan networks.

5. Conclusions

We have proposed the original and 2-dilated networks with one-bypass-connection to decrease cell transfer delay and analyzed the output rates of each networks. We also have discussed to the influence of the bypasses insertion position to the output rates and found that the bypasses near output ports gives better performance. From this results, our proposal gives network system designers flexible choice of the position of bypasses in the networks with one-bypass-connection for the network performance and its delay.

The bypass methods can be applied to the networks using the banyan networks or 2-dilated banyan networks as their basic structure. In such networks, the tandem banyan network [12], [13] and the hybrid dilated banyan network [10], [11] are included.

The $N \times N$ tandem banyan network structure consists of K banyan networks connected in series, where each banyan network has N input ports and N output ports. Each output ports of a banyan network is connected to both the input of the subsequent banyan network and the output port concentrator of the tandem banyan network. When a cell is blocked at any stage in the n-th banyan network, the cell is transfered to a wrong output and forwarded to the connected in-

put port of the (n + 1)-th banyan network if n < K, or eliminated otherwise. If bypasses is inserted at this stage, the cell may arrive at correct output port of the n-th banyan network. From this fact, the performance of the tandem banyan network is expected to improve.

The $N \times N$ hybrid dilated banyan network is constructed from the 2-dilated banyan networks at first n stages and the original banyan networks at the rest N-n stages. We can insert bypasses at any stages expect first and final stages and expect a good the performance of the network. Note that the n-th stage is constructed by 4×2 re-arrangeable output switches, where no bypass is inserted in this paper. From [11], we confirmed to improve the performance by inserting bypasses at this stage.

Although the practical requirement order (such as 10^{-8} to 10^{-10}) of the cell loss rate is not archived by our bypass methods, the introduction of buffers to our method should be archived the required cell loss rate. For example, when the bypass methods are also applied to the rerouting network explained in Sect. 1, it may give the required cell loss rate by a fewer extra stages than the original network.

References

- R.Y. Awdeh and H.T. Mouftah, "Survey of ATM switch architectures," Computer Networks and ISDN Systems, vol.27, pp.1567–1613, 1995.
- [2] J.H. Patel, "Performance of processor-memory interconnections for multiprocessors," IEEE Trans. Comput., vol.C-30, pp.771-780, 1981.
- [3] M. Kumar and J.R. Jump, "Performance of unbuffered shuffle-exchange networks," IEEE Trans. Comput., vol.C-35, pp.573–577, 1986.
- [4] T.H. Szymanski and V.C. Hamacher, "On the universality of multipath multistage interconnection networks," J. Parallel and Distributed Computing, vol.7, pp.541–569, 1989.
- [5] K. Pibulyarojana, S. Kimura, and Y. Ebihara, "The banyan network and the 2-dilated banyan network with bypasses," ICOIN-13, pp.1C-3.1-3.6, 1999.
- [6] S. Urushidani, "Rerouting network: A high-performance self-routing switch for B-ISDN," IEEE J. Sel. Areas Commn., vol.9, no.8, pp.1194–1204, 1991.
- [7] S. Okamoto, "Modular expandable multi-stage ATM cross-connect system architecture for ATM broadband networks," IEICE Trans. Commun., vol.E75-B, no.3, pp.207–216, March 1992.
- [8] H.S. Kim and A. Leon-Garcia, "A self routing multistage switching network for broadband ISDN," IEEE J. Sel. Areas Commun., vol.8, no.3, pp.459–466, 1990.
- [9] C.P. Kruskal and M. Snir, "The performance of multistage interconnection networks for multiprocessors," IEEE Trans. Comput., vol.C-32, no.12, pp.1091-1098, 1983.
- [10] K. Pibulyarojana, S. Kimura, and Y. Ebihara, "A study on a hybrid dilated banyan network," IEICE Trans. Commun., vol.E80-B, no.1, pp.116-126, Jan. 1997.
- [11] K. Pibulyarojana, S. Kimura, and Y. Ebihara, "Hybrid dilated banyan network with bypasses at the stage of 4 × 2 re-arrangeable output switch," IEICE Trans. Commun., vol.E80-B, no.12, pp.1816-1818, Dec. 1997.
- [12] F.A. Tobagi, T. Kwok, and F.M. Chiussi, "Architecture, performance, and implementation of the tandem banyan

- fast packet switch," IEEE J. Sel. Areas Comm., vol.9, no.8, pp.1173-1193, 1991.
- [13] T.T. Lee and S.C. Liew, "Broadband packet switches based on dilated interconnection networks," IEEE Trans. Commun., vol.42, pp. 732–744, 1994.

Appendix: Analysis of Input Rate and Output Rate of Switching Elements

This section precisely induces the output rate of each switching element in the original, 2-dilated and hybrid dilated banyan networks. Through this section, the input rate of each input port is described by a and b for any banyan switching elements, or a, b, c and d for any 2-dilated banyan switching elements. The output rate of all output ports is p. When a switching element has input and/or output bypass links, its input and/or output rate is q and/or r.

Appendix.1 Input Rate and Output Rate of Banyan Switching Elements

In this subsection, the output rates of banyan switching elements are obtained. First, the banyan switching element Type 2 in Fig. 5 is considered. Then, the following two cases exist.

Case 1: No cell arrives at the input bypass link.

• When no cell arrives at any input port, the probability of this case is (1-q)(1-a)(1-b). No cell is sent to the output ports and the output bypass link. Then, the output rates of this case are: output port:

$$(1-q)(1-a)(1-b) \times 0 = 0,$$

output bypass link:

$$(1-q)(1-a)(1-b) \times 0 = 0.$$

• When there is an arriving cell at one of the two input ports, the probability of this case is (1-q)(a(1-b)+b(1-a)). No cell is blocked and the output probability of each output port is $\frac{1}{2}$. Then, the output rates of this case are: output port:

$$(1-q)(a(1-b)+b(1-a)) \times \frac{1}{2}$$

output bypass link:

$$(1-q)(a(1-b) + b(1-a)) \times 0 = 0.$$

• When there are arriving cells at both of the input ports, the probability of this case is $(1-q) \times a \times b$. The probability of cell blocking is $\frac{1}{2}$ and the output probability of each output port is $\frac{3}{4}$. Then, the output rates of this case are: output port:

PIBULYAROJANA et al.: IMPROVEMENT OF BANYAN NETWORKS BASED ON BYPASSES POSITIONING

$$(1-q) \times a \times b \times \frac{3}{4},$$

output bypass link:

$$(1-q) \times a \times b \times \frac{1}{2}.$$

Case 2: A cell arrives at the input bypass link.

• When no cell arrives at both of input ports, the probability of this case is $q \times (1-a)(1-b)$. No cell are blocked and the probability of each output port is $\frac{1}{2}$. Then, the output rates of this case are: output port:

$$q \times (1-a)(1-b) \times \frac{1}{2},$$

output bypass link:

$$q \times (1-a)(1-b) \times 0 = 0.$$

• When there is an arriving cell at one of the input ports, the probability of this case is q(a(1-b)+b(1-a)). The probability of cell blocking is $\frac{1}{2}$ and the output probability of each output port is $\frac{3}{4}$. Then, the output rates of this case are: output port:

$$q(a(1-b) + b(1-a)) \times \frac{3}{4}$$

output bypass link:

$$q(a(1-b) + b(1-a)) \times \frac{1}{2}$$

• When there are arriving cells at both of the input ports, the probability of this case is $q \times a \times b$. More than one cell must be blocked and the output probability of each output port is $\frac{7}{8}$. Then, the output rates of this case are: output port:

$$q \times a \times b \times \frac{7}{8}$$

output bypass link:

$$q \times a \times b \times 1$$
.

From the above results, the total output rate p of each output port is:

$$p = \frac{1}{2}a + \frac{1}{2}b - \frac{1}{4}ab + \frac{1}{2}q$$

$$-\frac{1}{4}aq - \frac{1}{4}bq + \frac{1}{8}abq,$$
(A·1)

and the total output rate r of the bypass link is:

$$r = \frac{1}{2}ab + \frac{1}{2}aq + \frac{1}{2}bq - \frac{1}{2}abq.$$
 (A·2)

For the banyan switching element Type 1 is shown in Fig. 5, there is no cell from the bypass input link.

Thus, the output rates are inferred from $(A \cdot 1)$ and $(A \cdot 2)$ whose q = 0, as follows:

$$p = \frac{1}{2}a + \frac{1}{2}b - \frac{1}{4}ab. \tag{A.3}$$

$$r = \frac{1}{2}ab,\tag{A-4}$$

For the banyan switching element Type 3 is shown in Fig. 5, p is same as $(A \cdot 1)$, but there is no bypass output link. The output rate p is described in the following again.

$$p = \frac{1}{2}a + \frac{1}{2}b - \frac{1}{4}ab + \frac{1}{2}q$$
$$-\frac{1}{4}aq - \frac{1}{4}bq + \frac{1}{8}abq. \tag{A.5}$$

For the banyan switching element Type 4 is shown in Fig. 5, p is equal to (A·3), but there is no bypass output link. The output rate p is described in the following again.

$$p = \frac{1}{2}a + \frac{1}{2}b - \frac{1}{4}ab. \tag{A-6}$$

For the original banyan network, all input rates of each input port is same, i.e., a=b. Then the output rate p is:

$$p = 1 - \left(1 - \frac{a}{2}\right)^2. \tag{A.7}$$

Appendix.2 Input Rate and Output Rate of 2-Dilated Banyan Switching Elements

This subsection infers the output rates of 2-dilated banyan switching elements. As in the previous subsection, the following 2-dilated banyan switching element Type 2 is considered. From Fig. 6, the following cases exist.

Case 1: No cell arrives at the input bypass link.

• When no cell arrive at any input ports, the probability of this case is (1-a)(1-b)(1-c)(1-d)(1-q). No cell is sent to the output ports and the output bypass link. Then, the output rates of this case are:

output port:

$$(1-a)(1-b)(1-c)(1-d)(1-q) \times 0 = 0,$$

output bypass link:

$$(1-a)(1-b)(1-c)(1-d)(1-q)\times 0=0.$$

• When there is an arriving cell at one of four input ports, the probability of this case is $[a(1-b)(1-c)(1-d)\times(1-q)]+[b(1-a)(1-c)(1-d)\times(1-q)]+[c(1-a)(1-b)(1-d)\times(1-q)]+[d(1-a)(1-b)(1-c)\times(1-q)]$. No cell is blocked and the

output probability of each output port is $\frac{1}{4}$. Then, the output rates of this case are: output port:

$$a(1-b)(1-c)(1-d) \times (1-q) \times \frac{1}{4}$$

$$+b(1-a)(1-c)(1-d) \times (1-q) \times \frac{1}{4}$$

$$+c(1-a)(1-b)(1-d) \times (1-q) \times \frac{1}{4}$$

$$+d(1-a)(1-b)(1-c) \times (1-q) \times \frac{1}{4},$$

output bypass link:

$$[a(1-b)(1-c)(1-d) \times (1-q)] \times 0$$

$$+ [b(1-a)(1-c)(1-d) \times (1-q)] \times 0$$

$$+ [c(1-a)(1-b)(1-d) \times (1-q)] \times 0$$

$$+ [d(1-a)(1-b)(1-c) \times (1-q)] \times 0 = 0.$$

• When there are arriving cells at two of the four input ports, the probability of this case is $[ab(1-c)(1-d)\times(1-q)]+[ac(1-b)(1-d)\times(1-q)]+[ad(1-b)(1-c)\times(1-q)]+[bc(1-a)(1-d)\times(1-q)]+[bd(1-a)(1-c)\times(1-q)]+[cd(1-b)(1-a)\times(1-q)]$. No cell is blocked and the output probability of each output port is $\frac{1}{2}$. Then, the output rates of this case are: output port:

$$\begin{split} ab(1-c)(1-d) \times (1-q) \times \frac{1}{2} \\ &+ ac(1-b)(1-d) \times (1-q) \times \frac{1}{2} \\ &+ ad(1-b)(1-c) \times (1-q) \times \frac{1}{2} \\ &+ bc(1-a)(1-d) \times (1-q) \times \frac{1}{2} \\ &+ bd(1-a)(1-c) \times (1-q) \times \frac{1}{2} \\ &+ cd(1-b)(1-a) \times (1-q) \times \frac{1}{2}, \end{split}$$

output bypass link:

$$ab(1-c)(1-d) \times (1-q) \times 0$$

$$+ ac(1-b)(1-d) \times (1-q) \times 0$$

$$+ ad(1-b)(1-c) \times (1-q) \times 0$$

$$+ bc(1-a)(1-d) \times (1-q) \times 0$$

$$+ bd(1-a)(1-c) \times (1-q) \times 0$$

$$+ cd(1-b)(1-a) \times (1-q) \times 0 = 0.$$

• When there are arriving cells at three of the four input ports, the probability of this case is $[abc(1-d)+acd(1-b)+abd(1-c)+bcd(1-a)]\times (1-q)$. The probability of cell blocking is $\frac{1}{4}$ and the output probability of each output port is $\frac{44}{64}$. Then, the output rates of this case are:

output port:

$$[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times (1-q) \times \frac{44}{64},$$

output bypass link:

$$[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times (1-q) \times \frac{1}{4}.$$

• When there are arriving cells at all of the four input ports, the probability of this case is $abcd \times (1-q)$. The probability of cell blocking is $\frac{10}{16}$ and the output probability of each output port is $\frac{208}{256}$. Then, the output rates of this case are: output port:

$$abcd \times (1-q) \times \frac{208}{256}$$

output bypass link:

$$abcd \times (1-q) \times \frac{10}{16}$$
.

Case 2: A cell arrives at the input bypass link.

• When no cell arrives at any input ports, the probability of this case is $(1-a)(1-b)(1-c)(1-d) \times q$. No cell is blocked and the output probability of each output port is $\frac{1}{4}$. Then, the output rates of this case are: output port:

$$(1-a)(1-b)(1-c)(1-d) \times q \times \frac{1}{4}$$

output bypass link:

$$(1-a)(1-b)(1-c)(1-d) \times q \times 0 = 0.$$

• When there is an arriving cell at one of four input ports, the probability of this case is $[a(1-b)(1-c)(1-d)\times q]+[b(1-a)(1-c)(1-d)\times q]+[c(1-a)(1-b)(1-c)\times q]$. No cell is blocked and the output probability of each output port is $\frac{1}{2}$. Then, the output rates of this case are:

output port:

$$[a(1-b)(1-c)(1-d) \times q] \times \frac{1}{2}$$

$$+ [b(1-a)(1-c)(1-d) \times q] \times \frac{1}{2}$$

$$+ [c(1-a)(1-b)(1-d) \times q] \times \frac{1}{2}$$

$$+ [d(1-a)(1-b)(1-c) \times q] \times \frac{1}{2}$$

output bypass link:

$$[a(1-b)(1-c)(1-d) \times q] \times 0$$

$$+ [b(1-a)(1-c)(1-d) \times q] \times 0$$

+ [c(1-a)(1-b)(1-d) \times q] \times 0
+ [d(1-a)(1-b)(1-c) \times q] \times 0 = 0.

• When there are arriving cells at two of the four input ports, the probability of this case is $[ab(1-c)(1-d)\times q]+[ac(1-b)(1-d)\times q]+[ad(1-b)(1-c)\times q]+[bc(1-a)(1-d)\times q]+[bd(1-a)(1-c)\times q]+[cd(1-b)(1-a)\times q]$. The probability of cell blocking is $\frac{1}{4}$ and the output probability of each output port is $\frac{44}{64}$. Then, the output rates of this case are:

output port:

$$ab(1-c)(1-d) \times q \times \frac{44}{64}$$

$$+ ac(1-b)(1-d) \times q \times \frac{44}{64}$$

$$+ ad(1-b)(1-c) \times q \times \frac{44}{64}$$

$$+ bc(1-a)(1-d) \times q \times \frac{44}{64}$$

$$+ bd(1-a)(1-c) \times q \times \frac{44}{64}$$

$$+ cd(1-b)(1-a) \times q \times \frac{44}{64},$$

output bypass link:

$$ab(1-c)(1-d) \times q \times \frac{1}{4}$$

$$+ ac(1-b)(1-d) \times q \times \frac{1}{4}$$

$$+ ad(1-b)(1-c) \times q \times \frac{1}{4}$$

$$+ bc(1-a)(1-d) \times q \times \frac{1}{4}$$

$$+ bd(1-a)(1-c) \times q \times \frac{1}{4}$$

$$+ cd(1-b)(1-a) \times q \times \frac{1}{4}$$

• When there are arriving cells at three of the four input ports, the probability of this case is $[abc(1-d)+acd(1-b)+abd(1-c)+bcd(1-a)] \times q$. The probability of cell blocking is $\frac{10}{16}$ and the output probability of each output port is $\frac{208}{256}$. Then, the output rates of this case are: output port:

$$[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times q \times \frac{208}{256},$$

output bypass link:

$$[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times q \times \frac{10}{16}.$$

• When there are arriving cells at all of the four input ports, the probability of this case is $abcd \times q$. More than one cell must be blocked and the output probability of each output port is $\frac{912}{1024}$. Then, the output rates of this case are: output port:

$$abcd \times q \times \frac{912}{1024}$$

output bypass link:

$$abcd \times q \times 1$$
.

From the above results, the total output rate p of each output port is:

$$p = \frac{1}{4}a + \frac{1}{4}b + \frac{1}{4}c + \frac{1}{4}d - \frac{1}{16}abc - \frac{1}{16}abd$$

$$-\frac{1}{16}acd - \frac{1}{16}bcd + \frac{1}{16}abcd + \frac{1}{4}q$$

$$-\frac{1}{16}abq - \frac{1}{16}acq - \frac{1}{16}adq - \frac{1}{16}bcq$$

$$-\frac{1}{16}cdq - \frac{1}{16}bdq + \frac{1}{16}abdq + \frac{1}{16}acdq$$

$$+\frac{1}{16}bcdq + \frac{1}{16}abcq - \frac{3}{64}abcdq, \qquad (A \cdot 8)$$

and the total output rate r of the bypass link is:

$$r = \frac{1}{4}abc + \frac{1}{4}acd + \frac{1}{4}abd + \frac{1}{4}bcd$$

$$-\frac{3}{8}abcd - \frac{3}{8}abcq - \frac{3}{8}acdq - \frac{3}{8}abdq$$

$$-\frac{3}{8}bcdq + \frac{3}{8}abcdq + \frac{1}{4}abq + \frac{1}{4}acq$$

$$+\frac{1}{4}adq + \frac{1}{4}bcq + \frac{1}{4}bdq + \frac{1}{4}cdq. \tag{A.9}$$

For the 2-dilated banyan switching element Type 1 in Fig. 6, there is no cell from the bypass input link. Thus, the output rates are inferred from $(A \cdot 8)$ and $(A \cdot 9)$ whose q = 0, as follows:

$$p = \frac{1}{4}a + \frac{1}{4}b + \frac{1}{4}c + \frac{1}{4}d - \frac{1}{16}abc - \frac{1}{16}abd$$
$$-\frac{1}{16}acd - \frac{1}{16}bcd + \frac{1}{16}abcd, \tag{A.10}$$

$$r = \frac{1}{4}abc + \frac{1}{4}acd + \frac{1}{4}abd + \frac{1}{4}bcd - \frac{3}{8}abcd.$$
 (A·11)

For the 2-dilated banyan switching element Type 3 in Fig. 6, p is same as $(A \cdot 8)$, but there is no bypass output link. The output rate p is described in the following.

$$p = \frac{1}{4}a + \frac{1}{4}b + \frac{1}{4}c + \frac{1}{4}d - \frac{1}{16}abc - \frac{1}{16}abd$$
$$-\frac{1}{16}acd - \frac{1}{16}bcd + \frac{1}{16}abcd + \frac{1}{4}q$$
$$-\frac{1}{16}abq - \frac{1}{16}acq - \frac{1}{16}adq - \frac{1}{16}bcq$$

$$-\frac{1}{16}cdq - \frac{1}{16}bdq + \frac{1}{16}abdq + \frac{1}{16}acdq + \frac{1}{16}bcdq + \frac{1}{16}abcq - \frac{3}{64}abcdq.$$
 (A·12)

For the 2-dilated banyan switching element Type 4 in Fig. 7, p is equal to $(A \cdot 10)$, but there is no bypass output link. The output rate p is described in the following again.

$$p = \frac{1}{4}a + \frac{1}{4}b + \frac{1}{4}c + \frac{1}{4}d - \frac{1}{16}abc - \frac{1}{16}abd - \frac{1}{16}acd - \frac{1}{16}bcd + \frac{1}{16}abcd.$$
 (A·13)

For the original 2-dilted banyan network, all input rates of each input port is same, i.e., a=b=c=d. Then, the output rate p is:

$$p = a - \frac{1}{4}a^3 + \frac{1}{16}a^4. \tag{A.14}$$

For the 2-dilated banyan switching element Type 5 in Fig. 7, the following cases exist.

• When no cell arrives at any input ports, the probability of this case is (1-a)(1-b)(1-c)(1-d). No cell is sent to the output ports. Then, the output rate of this case is:

$$(1-a)(1-b)(1-c)(1-d) \times 0 = 0.$$

• When there is an arriving cell at one of the four input ports, the probability of this case is [a(1-b)(1-c)(1-d)+b(1-a)(1-c)(1-d)+c(1-a)(1-b)(1-d)+d(1-a)(1-b)(1-c)]. No cell is blocked and the output probability of each output ports is $\frac{1}{2}$. Then, the output rate of this case is: output port:

$$a(1-b)(1-c)(1-d) \times \frac{1}{2}$$

$$+b(1-a)(1-c)(1-d) \times \frac{1}{2}$$

$$+c(1-a)(1-b)(1-d) \times \frac{1}{2}$$

$$+d(1-a)(1-b)(1-c) \times \frac{1}{2}.$$

• When there are arriving cells at two of the four input ports, the probability of this case is [ab(1-c)(1-d)+ac(1-b)(1-d)+ad(1-b)(1-c)+bc(1-a)(1-d)+bd(1-a)(1-c)+cd(1-b)(1-a)]. The output probability of each output ports is $\frac{3}{4}$. Then, the output rate of this case is:

$$ab(1-c)(1-d) \times \frac{3}{4} + ac(1-b)(1-d) \times \frac{3}{4}$$
$$+ ad(1-b)(1-c) \times \frac{3}{4} + bc(1-a)(1-d) \times \frac{3}{4}$$
$$+ bd(1-a)(1-c) \times \frac{3}{4} + cd(1-b)(1-a) \times \frac{3}{4}.$$

• When there are arriving cells at three of the four input ports, the probability of this case is abc(1-d)+acd(1-b)+abd(1-c)+bcd(1-a). The output probability of each output ports is $\frac{7}{8}$. Then, the output rate of this case is:

$$[abc(1-d) + acd(1-b) + abd(1-c) + bcd(1-a)] \times \frac{7}{8}.$$

When there are arriving cells at all of the four input ports, the probability of this case is abcd. The output probability of each output ports is ¹⁵/₁₆. The output rate of this case is:

$$abcd \times \frac{15}{16}$$

From the above results, the total output rate p of each output port is:

$$p = \frac{1}{2}a + \frac{1}{2}b + \frac{1}{2}c + \frac{1}{2}d - \frac{1}{4}ab - \frac{1}{4}ac$$

$$-\frac{1}{4}ad - \frac{1}{4}bc - \frac{1}{4}cd + \frac{1}{8}abc + \frac{1}{8}abd$$

$$+\frac{1}{8}acd + \frac{1}{8}bcd - \frac{1}{16}abcd. \tag{A.15}$$



Komain Pibulyarojana was born in Bangkok, Thailand, on October 8, 1971. He received the B.E. degree in information engineering in 1995 and the M.E. and Ph.D. degrees in engineering from the University of Tsukuba, Japan, in 1997 and 2000, respectively. He joined the National Electronics and Computer Technology Center, Thailand, in 2000. His research interests are in the high speed network architecture and ATM switching

networks. He is a number of IPSJ.



Shigetomo Kimura was born in 1967. He received the D. Info. degree in information science from Tohoku University, in 1995. He is currently a Lecturer of Institute of Information Sciences and Electronics, the University of Tsukuba, since 1995. His primary research interests are in the areas of algebraic formulation of concurrent processes and program synthesis by inductive inference. He is a member of IPSJ and JSSS.



Yoshihiko Ebihara was born in Ibaraki, Japan, on April 11, 1947. He received the B.E., M.E. and D.E. degrees in electrical communication engineering all from Tohoku University, in 1970, 1972 and 1978, respectively. From 1973 to 1975 he was on a staff of ALOHA system project in the University of Hawaii satellite communication network and also Hawaii node installation of ARPA computer network. In 1975 he was appointed

a research assistant in the Institute of Electrical Communication, Tohoku University. He was appointed a lecturer and an Associate Professor at the Institute of Information Sciences and Electronics, the University of Tsukuba, in 1976 and 1985 respectively. He is currently a Professor of the Institute of Information Sciences and Electronics, the University of Tsukuba since 1993. His primary research interests include computer network, performance measurement, distributed data base management and digital communication system. He is a member of ISPJ.