Electrical characteristics of asymmetrical silicon nanowire field-effect transistors

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This letter reports the electrical characteristics of nonuniform silicon nanowire *n*FETs with asymmetric source and drain widths. For electrostatic properties, reduced drain-induced barrier lowering (DIBL) is achieved in a device in which the source is wider than the drain. For carrier transport properties, higher values of surface-roughness-limited mobility (μ_{SR}) are obtained in the sample with the wider drain size. Our electrostatic model shows that the concentration of lines of electric force is relaxed near the wider source edge, which results in smaller DIBL. The asymmetric μ_{SR} is attributed to the channel surface morphology with (110)- and (100)-faceted surfaces. © *2011 American Institute of Physics*. [doi:10.1063/1.3665261]

The silicon nanowire (SiNW) metal–oxide–semiconductor field-effect transistor (MOSFET) is a promising candidate for further scaling because of its superior immunity to short channel effects.[1–7] The future may see the use of three-dimensional (3D) MOSFETs, such as vertically stacked SiNW FETs,[8–12] for high device densities. An asymmetric channel structure is expected for the vertically stacked SiNW FETs because of the fabrication processes. For a feasibility study, asymmetric SiNW *n*FETs with inhomogeneous wire widths were fabricated and electrically characterized. In particular, the electrostatic controllability and carrier transport properties of the asymmetric SiNW *n*FETs are reported and compared here, focusing on the different measurement conditions for the control and source/drain-flipped (S/D-flipped) configurations.

The asymmetric SiNW *n*FETs were fabricated on a (100)-oriented silicon-on-insulator (SOI) wafer with an SOI layer thickness of 28 nm and a buried oxide (BOX) layer thickness of 50 nm. After the formation of a ⟨110⟩-directed asymmetric fin structure that had an inhomogeneous wire width with embedded source and drain regions, using ArF lithography and dry-etching processes, the fin structure was oxidized in a dry oxygen ambient for 1 h at 1000 °C to form a SiNW channel. Detailed fabrication processes have been reported elsewhere.[13,14] A plan-view secondary-electron micrograph of an asymmetric SiNW *n*FET after gate patterning is shown in Fig. 1. The wire width at the drain edge of the asymmetric SiNW *n*FET was smaller than that at the source edge in the control configuration for measurements. Typical transfer characteristics of the asymmetric SiNW *n*FET were obtained with both the control and the S/D-flipped configurations. The effective gate length (L_{eff}) was extracted using the shift-and-ratio method.[15]

The electrostatic characteristics of the asymmetric SiNW *n*FET were investigated. The drain-induced barrier lowering (DIBL) measured in the control and S/D-flipped configurations is shown in Fig. 2. DIBL characterized in the control configuration (i.e., wider source edge) was lower than the DIBL characterized in the S/D-flipped configuration (i.e., narrower source edge). DIBL is caused by deep penetration of the electric field from the drain electrode into the

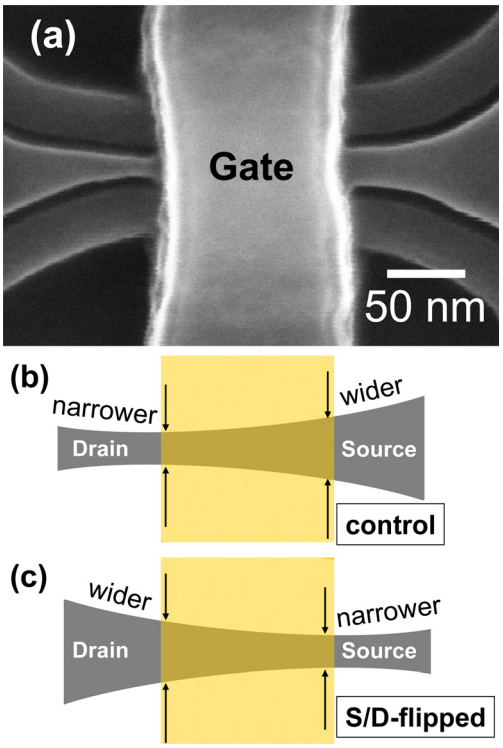

FIG. 1. (Color online) (a) A plan-view secondary-electron microscope image of an asymmetric silicon nanowire FET, and a schematic illustration of the asymmetric SiNW *n*FET with (b) control and (c) source/drain-flipped configurations.

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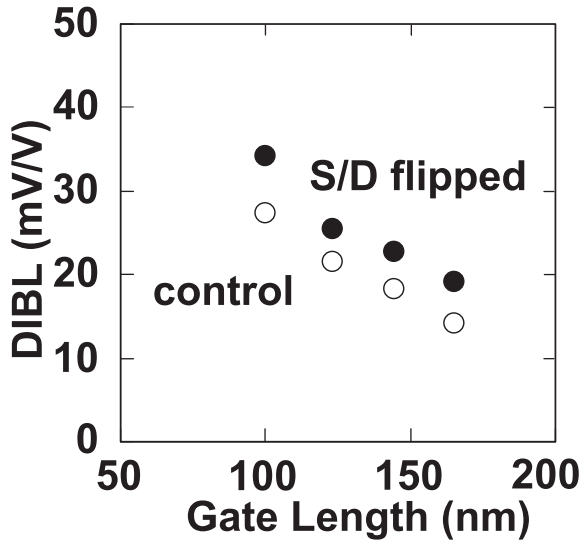

FIG. 2. Drain-induced barrier lowering of asymmetric silicon nanowire *n*FETs characterized with control and source/drain-flipped configurations.

SiNW channel region, which results in lowering of the potential barrier.[16] In the asymmetric SiNW *n*FET, as the wire width decreased, the electrical flux lines became more concentrated. As a result, a higher transverse electric field was applied to the narrower source edge of the S/D-flipped measurement configuration compared with that applied to the wider source edge of the control measurement configuration. The wider wire width at the source edge leads to a reduction in magnitude of the electric field at the top of the potential barrier near the source edge of the latter configuration. These experimental results are consistent with those of another work[17] and suggest that the asymmetric structure affects the electrical potential in the channel of the asymmetric SiNW *n*FET.

The carrier transport properties of asymmetric SiNW *n*FETs were also investigated. Transfer characteristics and transconductance (g_m) at a drain voltage of 50 mV were characterized at temperatures from 40 to 290 K. Effective carrier mobility (μ_{eff}) was also evaluated using the *Y*-function method.[18,19] At 290 K, the transfer characteristics and g_m measured for the control configuration were almost the same as those measured for the S/D-flipped configuration. However, at 40 K, I_{ds} in the transfer characteristics and g_m measured for the S/D-flipped configuration were larger than the measured values for the control configuration, as shown in Fig. 3(a). μ_{eff} at $V_{eff} = V_g - V_{th} = 1.0$ V was characterized as shown in Fig. 3(b) at various measurement temperatures. As the measurement temperature decreased, the effects of phonon scattering decreased, and surface-roughness-scattering limited mobility (μ_{SR}) can be obtained[20] at 40 K, with μ_{SR} of 120 cm^2/Vs in the control configuration and 125 cm^2/Vs in the S/D-flipped configuration. This result indicates that μ_{SR} for the asymmetric SiNW *n*FET depends on the direction of carrier flow.

One concern is the difference between the parasitic resistance near the source electrode (R_S) and the parasitic resistance near the drain electrode (R_D) of the asymmetric SiNW FET. In the literature, R_S particularly affects g_m.[21] In our previous experiments (data not shown here), as the symmetrical wire width decreased, R_{SD} ($=R_S+R_D$) increased. Therefore, R_S in the S/D flipped configuration should be greater than R_S in the control configuration. However, g_m was greater in the flipped configuration, which suggests that R_S and R_D were ineffective in our experiments.

One possible reason for the asymmetric μ_{SR} might be the channel surface morphology of the asymmetric SiNW *n*FET, because of the asymmetric structure. After formation of the fin structure, which had a surface tilted from the (110)-oriented side surfaces, the fin structure was oxidized in dry oxygen ambient for 1 h at 1000 °C. We considered that the oxidation rate dependence on the surface orientation[22] becomes dominant, which leads to the formation of the facet at the SiNW channel surface. We propose a schematic model of the side surface that is composed of (110)- and (100)-faceted surfaces of the asymmetric SiNW *n*FET to explain the dependence of μ_{SR} on the measurement conditions. The surface roughness (SR) experienced by carriers in the control configuration should differ from the SR in the S/D-flipped configuration.

In the literature, the SR of the interface between the silicon substrate and the thermally grown silicon dioxide was physically characterized using high-resolution transmission electron microscope images, and the SR was described using the exponential decay of an autocovariance function.[23] However, a tilted surface has periodic SR.[23] Based on the results of Ref. 23, the channel surface of the asymmetric SiNW *n*FET might have periodic SR that is composed of (110)- and (100)-faceted surfaces.

For further investigation of the surface morphology of the nonuniform SiNW channel and comparison with our model, measurement of the SiNW surfaces with a scanning probe microscope, such as the scanning tunneling microscope,[24] would be helpful.

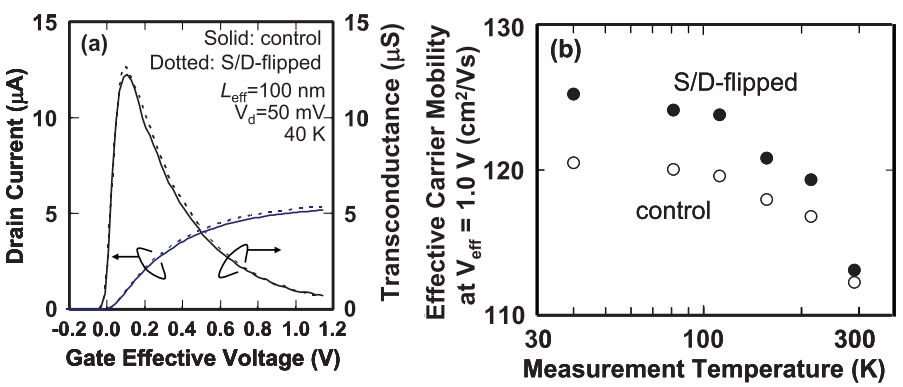

FIG. 3. (Color online) (a) Transfer characteristics and transconductance of the asymmetric silicon nanowire *n*FET measured at 40 K with control and source/drain-flipped configurations and a drain voltage of 50 mV. (b) Effective carrier mobility at the effective gate voltage of 1.0 V with the control and source/drain-flipped configurations obtained using the *Y*-function method on the different measurement temperatures.

In summary, the electrical characteristics of asymmetric SiNW *n*FETs were reported. The electrical characteristics were measured using the control and S/D-flipped measurement configurations. For the electrostatic properties, reduced DIBL was achieved with a wider source edge width. For the carrier transport properties, μ_{SR} depended on the measurement configuration, which indicates that SRS depends on the direction of current flow. These phenomena for both the asymmetric electrostatic controllability and the μ_{SR} are attributed to the asymmetric channel structure. For the electrostatic properties, our model shows that the concentration of the lines of electric force was relaxed near the wider source edge, which resulted in reduced DIBL. For the carrier transport properties, the asymmetric μ_{SR} is attributed to the channel surface, which is composed of (110)- and (100)-faceted surfaces.

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