Study of a DSP-Based Data-Acquisition System for the BELLE Silicon Vertex Detector

March, 1999

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Abstract

At the High Energy Accelerator Research Organization (KEK), Japan, the B-factory project is proceeding with the aim of measuring *CP*-violation effects in the B meson system. For this purpose, we are constructing the BELLE detector with which we will measure vertex points of B meson decays and try to measure *CP*-violation effects. The silicon vertex detector is one of the most important of its sub-detectors for detecting the vertex points. In the silicon vertex detector, there are about 82,000 readout strips. The data-acquisition system must cope with readout of this large number of strips at a 500 Hz trigger rate. We have developed a distributed data-acquisition system with high-speed digital signal processors for readout of the silicon vertex detector. In the system test, we could have fast enough VME transfer rate with SHARC DSP VME clusters. We could also have sufficiently fast transfer rate in the SHARC link. The silicon detectors showed a required level of performance. According to the pulse height distributions, Landau peaks were observed around 20,000 electrons in this measurement. We measured S/N ratios around 20 for most of the silicon detector ladders. The position resolution of the silicon detector ladders was estimated to be 24.7 μm. In this thesis, its concept and performance are explained in detail.

Acknowledgments

The work described in this thesis depends on the efforts of many people, especially the members of the BELLE collaboration, all of whom must receive my thanks. I am most indebted to my supervisors, Prof. Y. Asano and Prof. S. Mori, for their continuous encouragement and support. I would like to thank Prof. C. Fukunaga, Tokyo Metropolitan University, for his kind advice and encouragement and continuous support in the construction work of the DAQ system for BELLE SVD. I express my gratitude to my collaborators in the construction work of the DAQ system for BELLE SVD, especially to Dr. Y. Igarashi, KEK, Dr. J. S. Lange, CERN, and Dr. S. Okuno, Kanagawa University.

I would like to thank Dr. E. Banas, Dr. P. Jalocha, Dr. P. Kapusta and Dr. Z. Natkaniec, Krakow Institute of Nuclear Physics, for their kind advice and continuous support with regard to Halny FADC modules. I would also like to thank Dr. A. Bozek, KEK for his kind advice and continuous support in the Monte-Carlo simulation study by GSIM, and Dr. M. Tanaka and Dr. T. Tsuboyama, KEK for their valuable advice and continuous support in my study at KEK.

I would like to thank Prof. J. Haba, KEK, Dr. M. Hazumi, Osaka University, Dr. R. Itoh, KEK, Dr. M. Nakao, KEK, Dr. S. Suzuki, KEK, Dr. H. Tajima, University of Tokyo, Prof. F. Takasaki, KEK, Dr. Y. Yamada, KEK, and Prof. M. Yamauchi, KEK for their continuous and kind advice and support in the construction of BELLE SVD. I would also like to thank Mr. T. Higuchi, University of Tokyo, Mr. T. Kawasaki, Osaka University, Mr. T. Nakadaira, University of Tokyo, Mr. J. Ryuko, Osaka University, Mr. K. Shimada, Niigata University, Mr. K. Sumisawa, Osaka University, Mr. S. Takahashi, Niigata University, Mr. T. Tomura, University of Tokyo, and Mr. M. Yokoyama, University of Tokyo for their supports in the construction of BELLE SVD.

I express my gratitude to my fellow students at University of Tsukuba, especially Mr. S. Yoshida for his support and effort in the construction work for BELLE SVD.

I would like to thank the late Mr. H. Matsuo, Kyoto University for his useful advice and kind support.

Finally, I would like to thank my family for their continuous support and encouragement. Without their help, I could not have completed my thesis.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

At the High Energy Accelerator Research Organization (KEK), Japan, preparations for the B-factory project are under way. One of the objects of this project is to measure *CP*-violation effects in the B meson decay system with an e^+e^- asymmetric collider.

We will measure the effects of *CP*-violation by detecting vertex points of B meson decays. For this purpose, the BELLE detector is being constructed. In the BELLE detector, many different sub-detectors will be used. One of the most important sub-detectors to detect the vertex point is a silicon vertex detector (SVD) which measures track points with a few μm position resolution.

The SVD system consists of more than 80,000 readout strips. We are required to readout signals at a 500 Hz trigger rate. The data-acquisition (DAQ) system for the detector must cope with this requirement. To realize this requirement, we have constructed a DAQ system based on digital signal processors (DSP). One of the most important features is that our DAQ system is based on a distributed readout system with the help of DSPs.

These DSPs used are called SHARC (**S**uper **H**arvard **AR**chitecture **C**omputer) which were supplied from Analog Devices, USA. A SHARC DSP has six high speed link ports (SHARC link) and a common bus interface. In our DAQ system, we used six VME 6U-size DSP boards supplied from WIESE GmbH, Germany. This DSP board can mount up to six SHARC DSPs. Each DSP can communicate via a common bus on the board or SHARC link.

Through the present research and development work of constructing the DAQ system for BELLE SVD, we have made a DSP-based distributed DAQ system for SVD. Because the system is based on a distributed scheme, each

program on SHARC DSP is basically the same. Each program can run independently except when they are controlled by a host computer in the same VME crate.

In the whole DAQ system of the BELLE detector (global run mode), the SVD DAQ system must be controlled by the central DAQ system (CDAQ). For this purpose, we have made CDAQ interface routines which run on Sparc CPU-7V. In addition, with the help of links of SHARC DSP, we have constructed the DAQ system without sending data to CDAQ. In this system, the Sparc CPU-7V used as a run control master module stores data on a local disk from each detector as local data. This system was prepared for checking tasks with SVD only when other sub-detectors are not engaged (local run mode). The system was also used for checking functionalities of each detector. The system has performed good stability through many checking tasks. Since the DAQ program was made of many sub-programs, we must type many commands in executing. To avoid inconvenience for routine workers, we have made a GUI based run control system.

In Chapter 2, I will explain about the B-physics for *CP*-violation study and the motivation of the KEK B-factory project. In Chapter 3, details of the BELLE detector together with the silicon vertex detector and its DAQ system will be described. In Chapter 4, background effects in BELLE SVD are discussed. In Chapter 5, a system test of the silicon vertex detector will be described and test results will be discussed. In Chapter 6, the summary of this thesis is described.

Chapter 2

KEK B-Factory and BELLE Detector

2.1 *CP*-violation in the B meson system

In 1964, an effect of *CP*-violation in K^0 decay was discovered by Christenson, Cronin, Fitch and Turlay [1]. In any other particle systems, effects of *CP*-violation have not been observed. The B meson is one of the candidates to reveal *CP*-violation effects.

Table 2.1: Quarks and leptons in the Standard Model.

quarks	u	c	t
	d	s	b
leptons	e	μ	τ
	ν_e	ν_μ	ν_τ

Table 2.1 shows quarks and leptons in the Standard Model for electroweak interactions. The elements of the Cabibbo-Kobayashi-Maskawa matrix (CKM) [2], V_{KM}, shown below, describe the mixing between the quark generations.

$$V_{KM} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix}$$

where the furthest off-diagonal elements V_{ub} and V_{td} are complex numbers. In the Wolfenstein parameterization [3], the CKM matrix is written as follows:

$$V_{KM} = \begin{pmatrix} 1-\lambda^2/2 & \lambda & A\lambda^3(\rho - i\eta) \\ -\lambda & 1-\lambda^2/2 & A\lambda^2 \\ A\lambda^3(1-\rho-i\eta) & -A\lambda^2 & 1 \end{pmatrix}$$

where there are four parameters, λ, A, ρ and η, that have to be obtained from experiments. Of the four, λ and A are relatively well determined and the relative values of ρ and η specify the CKM *CP*-violating phase.

The unitarity relation of the CKM matrix implies that $\sum_i V_{ij}^* V_{ik} = \delta_{jk}$ which gives the following relation involving V_{ub} and V_{td}:

$$V_{ud}V_{ub}^* + V_{cd}V_{cb}^* + V_{td}V_{tb}^* = 0.$$

This equation implies that the three terms form a closed triangle in the complex plane as shown in Fig. 2.1. The three internal angles of this so-

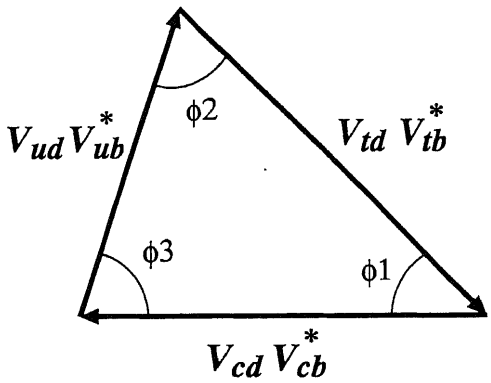


Figure 2.1: Unitarity triangle of the Cabibbo-Kobayashi-Maskawa matrix.

called *unitarity triangle* are defined as follows:

$$\phi_1 \equiv arg\left(-\frac{V_{cd}V_{cb}^*}{V_{td}V_{tb}^*}\right),$$
$$\phi_2 \equiv arg\left(-\frac{V_{ud}V_{ub}^*}{V_{td}V_{tb}^*}\right),$$
$$\phi_3 \equiv arg\left(-\frac{V_{cd}V_{cb}^*}{V_{ud}V_{ub}^*}\right).$$

If *CP*-violation exists, none of the angles are zero. In *CP*-violation measurements, we have several measurement methods in the B decay mode [4].

A typical decay mode of $\Upsilon(4S)$ in the KEKB asymmetric collider is shown in Fig. 2.2. Decays of neutral B mesons originating from the $\Upsilon(4S)$ into a

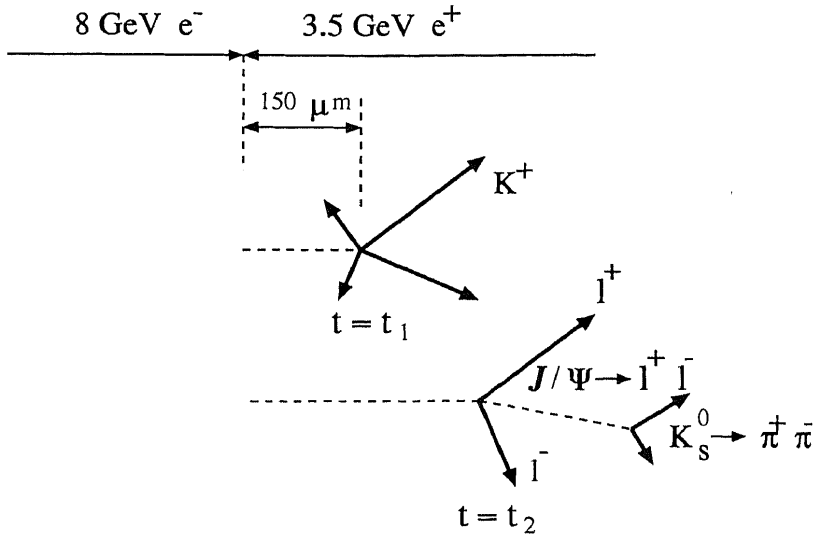


Figure 2.2: Typical decay mode of $\Upsilon(4S)$ in the KEKB, asymmetric electron-positron collider, where t_1 and t_2 are proper times of $B^0(\overline{B^0})$ and $\overline{B^0}(B^0)$ decays, respectively. l^+ and l^- are lepton with positive and negative charge, respectively

CP eigenstate f produce *CP*-violating asymmetries A_f given by [4]:

$$A_f = \frac{R(B^0 \to f) - R(\overline{B^0} \to f)}{R(B^0 \to f) + R(\overline{B^0} \to f)} = \sin 2\phi_{CP} \cdot \sin(\Delta m \cdot \Delta t), \qquad (2.1)$$

where Δm denotes the mass difference between the two B^0 mass eigenstates and $\Delta t = t_2 - t_1$. Here, t_1 and t_2 are the proper times for the B^0 and $\overline{B^0}$ decays, respectively. The determination of Δt is required for the observation of a *CP* asymmetry in experiments at $\Upsilon(4S)$. The angle ϕ_{CP} is the phase difference between the $B^0 - \overline{B^0}$ mixing amplitude and the $B^0 \to f$ decay amplitude and is directly related to the internal angles of the unitarity triangle.

Among the several methods, ϕ_1 measurement using $B^0(\overline{B^0}) \to J/\psi K_s$ decay mode is one of the cleanest methods. In the next section, the method is discussed.

2.2 ϕ_1 measurement in $B^0 \to J/\psi K_s$ decay mode

In this section, a measurement method of ϕ_1 is discussed.

One of the cases in which *CP*-violations will be measured is a decay mode of $B^0(\overline{B^0})$ to some *CP*-eigenstate. This phenomenon is realized as an interference of amplitudes between $B^0 \to f_{cp}$ and $B^0 \to \overline{B^0} \to f_{cp}$. In this section, the case of $B^0 \to J/\psi K_s$ as shown in Fig. 2.2 is described.

Let's think about the case in which B^0 ($\overline{B^0}$) will decay into J/ψ and K_s. *CP* eigenstates of J/ψ and K_S are -1 and +1, respectively. Figure 2.3 shows the quark diagrams responsible for the decay $B \to J/\psi K_S$ via the $\overline{b} \to \overline{c}(c\overline{s})$ quark-level process. The decay $B^0 \to J/\psi K_S \to l^+l^-\pi^+\pi^-$ is the most promising mode for the ϕ_1 measurement since the branching ratio for this decay mode has been measured and the signal is very clean with no appreciable background.

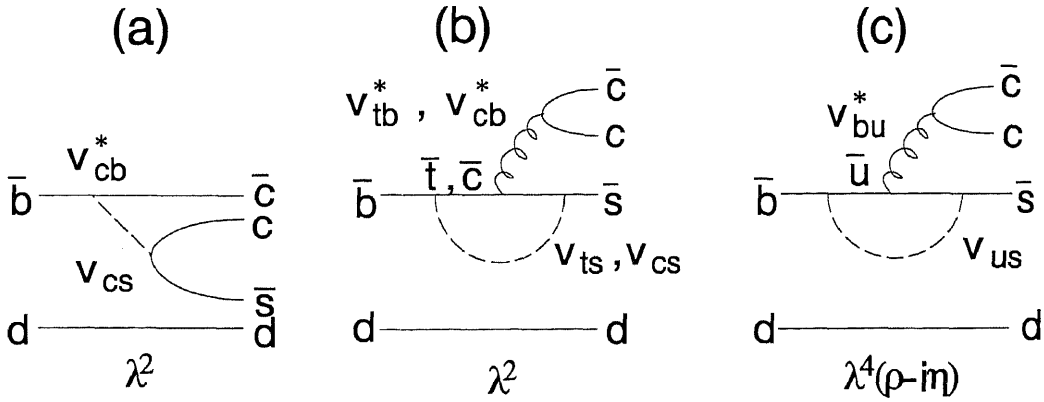


Figure 2.3: Quark diagrams responsible for $B^0_d \to J/\psi K_S$.

The probabilities that B^0 and $\overline{B^0}$ at time t decay into $J/\psi K_s$ are described as follows [5]:

$$R(B^0 \to J/\psi K_s) \sim exp(-\Gamma t)(1 + \sin\Phi \sin(x_d \Gamma t))$$

$$R(\overline{B^0} \to J/\psi\, K_s) \sim exp(-\Gamma\, t)(1 - \sin\Phi \sin(x_d \Gamma\, t))$$

where Γ, $\sin\Phi$ and x_d are the decay width of the B meson, the parameter of CP-violation and the mixing parameter in the $B^0\,\overline{B^0}$ system, respectively.

If we assume a pair creation of B^0 and $\overline{B^0}$ from the $\Upsilon(4S)$, the probability that $B^0(\overline{B^0})$ decays into $J/\psi\, K_s$ is described as follows:

$$R(B^0\overline{B^0} \to B^0 J/\psi\, K_s) \sim exp(-\Gamma(t_2 + t_1))(1 + \sin\Phi \sin(x_d \Gamma\, \Delta t))$$
$$R(B^0\overline{B^0} \to \overline{B^0} J/\psi\, K_s) \sim exp(-\Gamma(t_2 + t_1))(1 - \sin\Phi \sin(x_d \Gamma\, \Delta t))$$
$$\Delta t = t_2 - t_1$$

where t_1 and t_2 are the times of B^0 and another B^0 decay into $B^0 \to J/\psi\, K_s$.

In an asymmetric collider, Δt $(= t_2 - t_1)$ is measured, but t_1 and t_2 are not measured independently.

The previous equations are converted to the following equations, respectively:

$$R(B^0\overline{B^0} \to B^0 J/\psi\, K_s) \sim exp(-\Gamma|\Delta t|)(1 + \sin\Phi \sin(x_d \Gamma\, \Delta t)) \quad (2.2)$$
$$R(B^0\overline{B^0} \to \overline{B^0} J/\psi\, K_s) \sim exp(-\Gamma|\Delta t|)(1 - \sin\Phi \sin(x_d \Gamma\, \Delta t)) \quad (2.3)$$

From these equations, we can see that we need to measure the vertex points of B^0 and $\overline{B^0}$ decays. If we can measure these vertex points, we can measure the difference of vertex points, Δz, described below:

$$\Delta z = z_2 - z_1 = c\,\Delta t\,\beta\gamma \quad (2.4)$$
$$\beta\gamma = (E_{large} - E_{small})/M(\Upsilon(4S)) \quad (2.5)$$

where z_1 and z_2 are the vertex positions in the z-direction (direction of the beam) of B mesons, c is the speed of light, E_{large} and E_{small} are respectively the higher and lower beam energies, and $M(\Upsilon(4S))$ is the mass of the $\Upsilon(4S)$.

As described in Eq. 2.1, the CP-violating asymmetry A_f is defined by decay rates of neutral B mesons originating from the $\Upsilon(4S)$ into a CP eigenstate f. Using Eqs. 2.2 and 2.3, A_f is expressed as follows:

$$A_f = \frac{(1 - \sin\Phi \sin x_d\Gamma\Delta t) - (1 + \sin\Phi \sin x_d\Gamma\Delta t)}{(1 - \sin\Phi \sin x_d\Gamma\Delta t) + (1 + \sin\Phi \sin x_d\Gamma\Delta t)} = -\sin\Phi \sin x_d\Gamma\Delta t$$

Using Eqs. 2.4 and 2.5, we can estimate Δt by measuring Δz. In addition, we must distinguish B^0 from $\overline{B^0}$ to measure $\sin\Phi$.

For CP-violation studies, the following requirements must be satisfied:

- generation of a large number of B mesons (because the branching ratio of a desired decay mode is small),
- precise measurement of vertex points of B mesons, and
- distinction between B and $\overline{B}$ for the measurement of $\sin\Phi$.

Comparing A_f with Eq. 2.1, we have the relations:

$$\sin\Phi = -\sin 2\phi_{CP},$$

and

$$\Delta m = x_d\Gamma.$$

Thus,

$$A_f = \sin 2\phi_{CP} \sin \Delta m \Delta t.$$

In the decay mode, $B(\overline{B}) \to J/\psi\, K_S$, $\phi_{CP} \equiv \phi_1$ [6][1], one of the angles of the CKM unitarity triangle shown in Fig. 2.1. Therefore, ϕ_1 can be determined from measurements of the difference of vertex points, Δz, and the identification of B and $\overline{B}$.

Figure 2.4 [4] shows the proper time distribution for $B^0 \to J/\psi\, K_S$ decays for the case of $\sin 2\phi_1 = +0.6$ as a function of the time difference in units of B lifetime, τ. In this figure, parameters t and t' correspond to t_2 and t_1 in this section, respectively. The solid and dotted lines are the decay rates of the $\overline{B^0}$ (tagged by the other B decaying to B^0) and the B^0, respectively. A negative value of $\Delta t/\tau$ corresponds to the case where the tagging decay occurs after the $J/\psi\, K_S$ decay. The difference between the positive and negative time scale reflects the CP asymmetry. This can be seen either in the solid and dotted curves separately, or in the sum after the time scale of the dotted curve is reversed. The curves in the figure are drawn assuming perfect vertex-position resolution. When the finite time resolution is included, the difference between the positive and negative time scale is diluted.

Figure 2.5 [4] shows the integrated luminosity required for observing a given CP asymmetry in the $J/\psi\, K_S$ mode for different Δt resolutions in several values of $\sin 2\phi_1$. The corresponding Δz resolution is also indicated. The penalty for a resolution of $\Delta t/\tau = 0.5$ (as compared to perfect vertex resolution) is a 30 % increase in required luminosity. If $\Delta t/\tau$ degrades further

[1] In ref. [6], the angle is described by β, not ϕ_1. The ϕ_1 and β indicate the same angle in the CKM unitarity triangle.

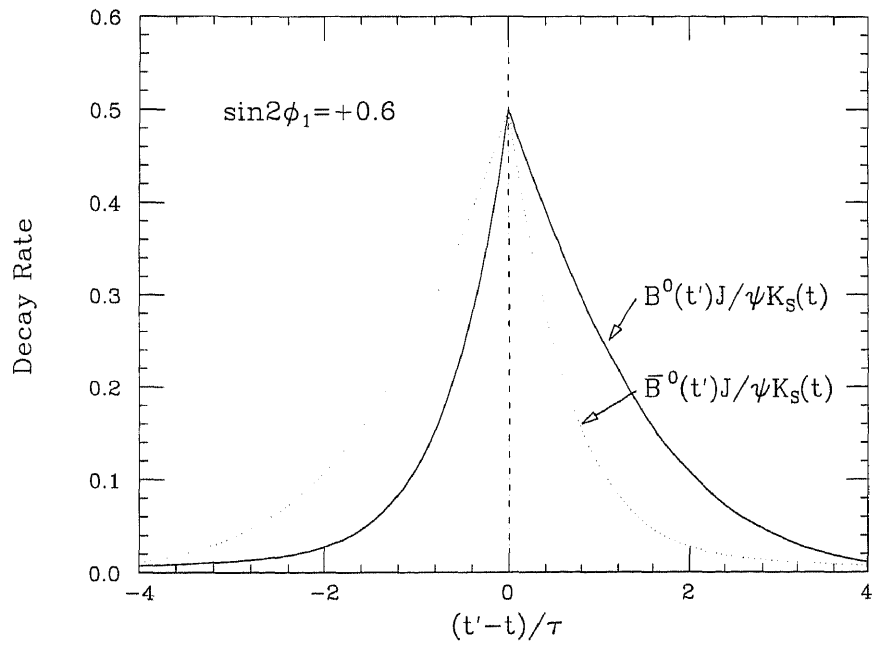


Figure 2.4: Calculated proper time distribution of $J/\psi K_S$ decay for a *CP* asymmetry corresponding to $\sin 2\phi_1 = +0.6$.

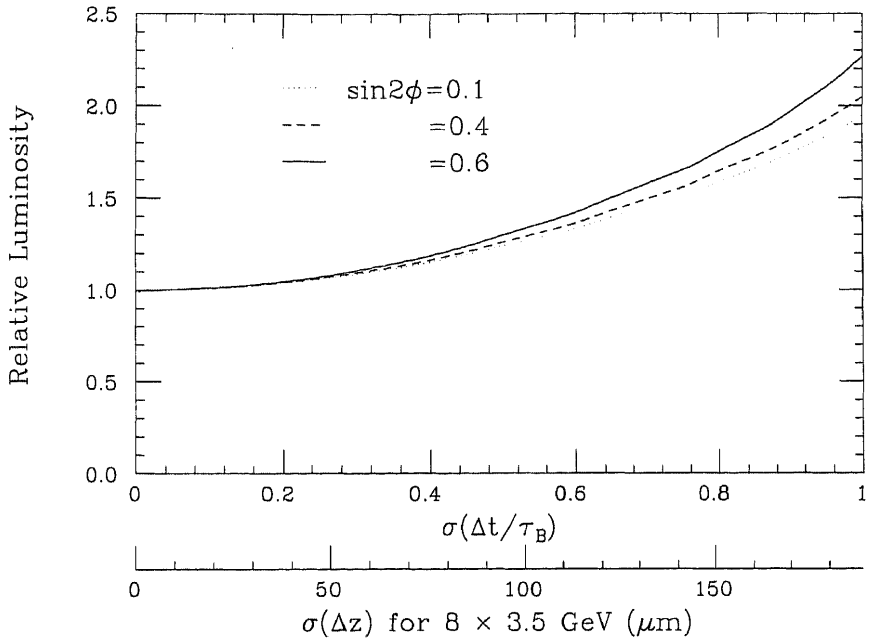


Figure 2.5: Required integrated luminosity as a function of the Δz resolution for three different values of $\sin 2\phi_1$.

from 0.5 to 1.0, another 70 % increase in luminosity is required. With silicon strip detectors, we expect to be able to achieve $\Delta t/\tau \leq 0.5$, corresponding to about a 95 μm position resolution in the beam direction. With the possible exception of silicon pixel detectors, alternative devices have worse resolution, leaving silicon strip detectors as the best practical choice. In addition to providing measurements essential for establishing a *CP* asymmetry, precise vertex information will be useful for eliminating continuum events and reducing combinatorial backgrounds. These considerations place a premium on achieving the best possible vertex position resolution.

2.3 KEK B-factory

At KEK, Japan, we are constructing an accelerator and a detector for *CP*-violation studies by B meson decays [7, 4]. The accelerator is an electron-positron asymmetric collider with a circumference of about 3 km. A schematic view of the accelerator is shown in Fig. 2.6. Typical machine parameters of the KEKB accelerator are listed in Table 2.2 [7]. In this table, LER and HER means the low energy ring (e^+ beam ring) and the high energy ring (e^- beam ring), respectively. The energy range of the B-factory is designed at the Υ(4S) state. The Υ(4S) state is a resonant state which is produced with b and $\bar{b}$ quarks. The mass is slightly larger than the sum of the masses of B_d and $\overline{B_d}$. The reasons why we select the energy of the Υ(4S) state are as follows:

- At the Υ(4S) state, the generation rate of B meson pairs is higher than any other resonant states.
- We can get a clean decay because the energy of the Υ(4S) is close to the threshold energy of a B meson pair.

Since the life time of the B meson is very short ($\sim$ 1 ps), a flight path of the B meson is much smaller than the resolution of existing instruments in any symmetric collider case. For this reason, at the B-factory, an asymmetric collider is selected with 8 GeV electron and 3.5 GeV positron beams. Then, generated B mesons travel about 200 μm, so we can measure vertex points by existing instruments.

For this purpose, a silicon detector is an excellent instrument. At the B-factory, we selected a double-sided three-layer detector system. Our goal

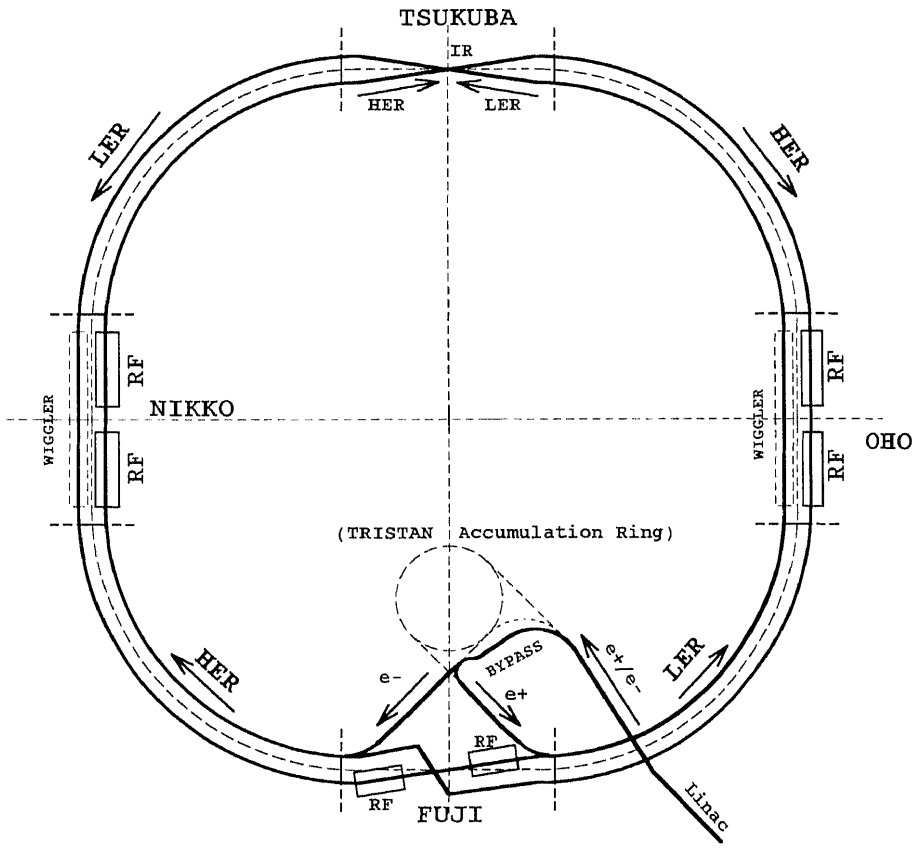


Figure 2.6: Schematic view of the KEKB accelerator.

Table 2.2: Typical machine parameters of the KEKB accelerator.

		LER	HER	
Beam energy	E	3.5	8.0	GeV
Luminosity	$\mathcal{L}$	1.0×10^{34}		$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Luminosity reduction factor	$R_{\mathcal{L}}$	0.845		
Half crossing angle	θ_x	11		mrad
Tune shifts	ξ_x/ξ_y	0.039/0.052		
Tune shift reduction	R_{ξ_x}/R_{ξ_y}	0.737/0.885		
Beta functions	β_x^*/β_y^*	0.33/0.01		m
Beam current	I	2.6	1.1	A
Bunch spacing	s_b	0.59		m
Particles/bunch	N	3.3×10^{10}	1.4×10^{10}	
Number of bunches/ring	N_B	5000		
Emittance	ϵ_x/ϵ_y	$1.8 \times 10^{-8}/3.6 \times 10^{-10}$		m
Bunch length	σ_z	4		mm
Momentum spread	σ_δ	7.1×10^{-4}	6.7×10^{-4}	
Synchrotron tune	ν_s	$0.01 \sim 0.02$		
Momentum compaction factor	α_p	$1 \times 10^{-4} \sim 2 \times 10^{-4}$		
Betatron tunes	ν_x/ν_y	45.52/46.08	47.52/43.08	
Circumference	C	3016.26		m
Damping time	τ_E	44.9	22.5	ms

with this system is to achieve a spatial resolution better than 100 μm in the z direction.

To collect as many events as possible in a short time, the luminosity of the accelerator is one of the important key-points for the B-factory. Since the luminosity of about $10^{34}\text{cm}^{-2}\text{s}^{-1}$ is required, a positron beam of 2.6 A and an electron beam of 1.1 A must be provided in collider mode in the experiment. The number of bunches must be substantially larger for this requirement than that in the original TRISTAN arrangement.

The design for the interaction region (IR) is shown in Fig. 2.7. The beam

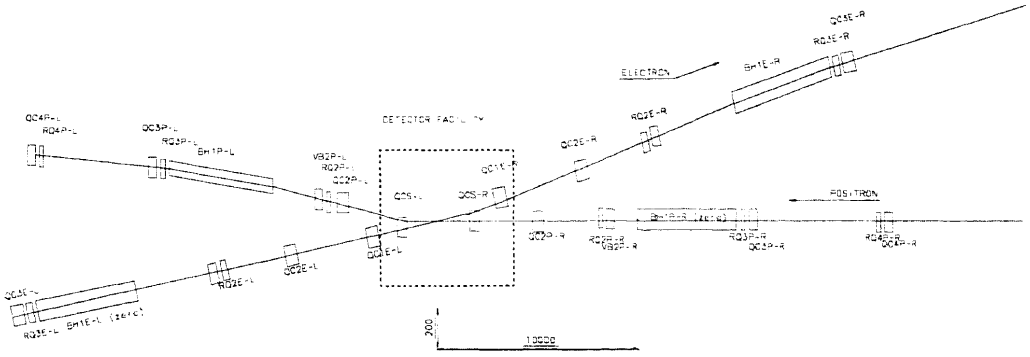


Figure 2.7: Layout of the interaction region for the large-angle crossing scheme.

crossing angle of ± 11 mrad allows us to to fill all RF buckets with the beam and still avoid parasitic collisions, thus permitting higher luminosity. Another important merit of the large crossing-angle scheme is that it eliminates the need for the separation-bend magnets discussed in ref. [8], significantly reducing beam-related backgrounds in the detector.

The risk associated with the choice of a non-zero crossing angle is the possibility of luminosity loss caused by the excitation of synchro-beta resonances. However, the results of simulations of the beam-beam interaction done by the KEKB accelerator group indicate that, although some new resonances are excited by a ± 11 mrad crossing angle, there are still regions of the tune diagram suitable for operation. The details of these simulations are described in ref. [7].

The low energy beam line is aligned with the axis of the detector solenoid since the lower-momentum beam particles would suffer more bending in the

solenoid field if they were off-axis. This results in a 22 mrad angle between the high energy beam line and the solenoid axis.

2.4 BELLE detector

Figure 2.8 shows a side view of the BELLE detector. A silicon vertex detector (SVD) is located around a beam pipe. Around SVD, a central drift chamber (CDC) is placed to detect tracks of charged particles. Around CDC, aerogel Čerenkov counters (ACC) are located. Time-of-flight (TOF) counters are located between ACC and a superconducting solenoid magnet to identify charged particles, typically π and K. The solenoid magnet provides a 1.5 T magnetic field in the axial direction. In the most outer region inside the solenoid magnet, there are electro-magnetic calorimeters (ECL) to measure energies of photons and electrons. Extreme forward calorimeters (EFC) will be attached to the front faces of the cryostats of the QCS magnets of the KEKB accelerator, surrounding the beam pipe, and in both the forward and backward directions. Thus, SVD, CDC, ACC, ECL, TOF and EFC are operated in the magnetic field. Outside of the magnet, muon chambers (KLM) are placed for detection of μ particles. The expected performance of the BELLE detector is summarized in Table 2.3.

SVD is comprised of three layers of double sided 300 μm thick silicon detectors (DSSD). SVD can measure $r-\phi$ and z positions. Readout strip pitches in the p-side $(r-\phi)$ and n-side (z) are 50 μm and 84 μm, respectively.

CDC measures tracks and deposit energies, dE/dx, of penetrating charged particles. CDC has 52 cylindrical layers organized in 13 super-layers, each containing between three and five layers which are either axial or small-angle stereo.

ACC is comprised of silica aerogel radiators. To detect emitted lights, fine-mesh photomultipliers (FM-PMT) are used, because of the magnetic field in the superconducting solenoid magnet. ACC is used to distinguish $\pi^{\pm}$ from $K^{\pm}$ in the momentum range from 1.2 GeV/c to 4.0 GeV/c.

TOF is time-of-flight counters which comprise scintillators and FM-PMTs. TOF is used to distinguish $\pi^{\pm}$ from $K^{\pm}$ by measuring the flight times of charged particles in the momentum range up to 1.2 GeV/c with 100 psec time resolution.

ECL is CsI calorimeters which comprise CsI(Tl) crystals with a silicon PIN photodiode readout system. The CsI detector is used to measure energies

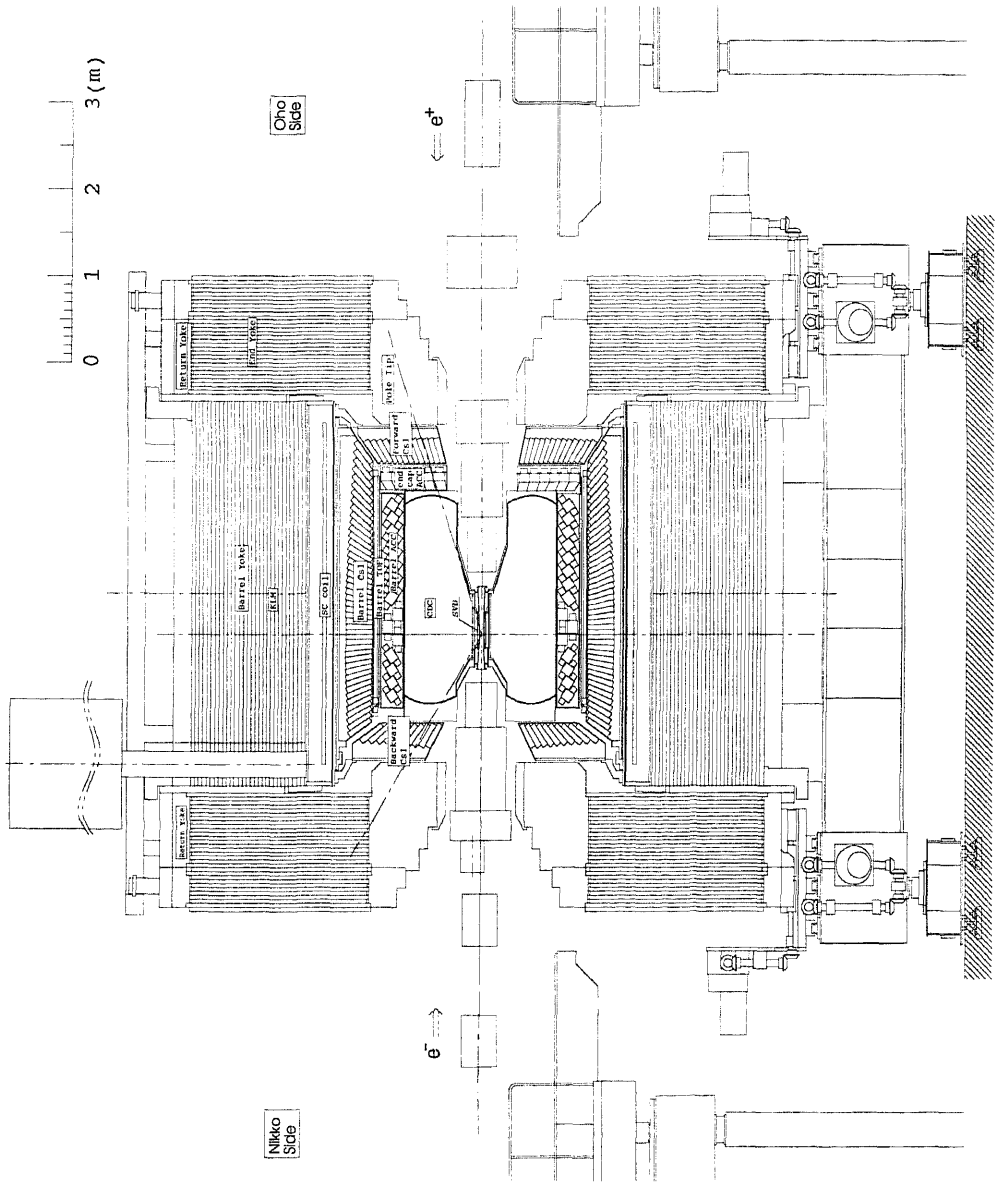


Figure 2.8: Side view of the BELLE detector.

Table 2.3: Performance parameters of the BELLE detector.

Detector	Type	Configuration	Readout	Performance
Beam pipe	Beryllium double-wall	Cylindrical, r = 2.3 cm 0.5 mm Be/2 mm He/ 0.5 mm Be		Helium gas cooled
SVD	Double sided silicon strip detector	300 μm thick 3 layers (double-sided) layer 1: r = 30.0 mm layer 2: r = 45.5 mm layer 3: r = 60.5 mm	ϕ: 41 K z: 41 K	$\sigma_{\Delta z} \sim 100$ μm
CDC	Small cell drift chamber	Anode: 52 layers Cathode: 3 layers $r = 8.5 \sim 90$ cm $-77 \leq z \leq 160$ cm	Anode: 8.4 K Cathode 1.5 K	$\sigma_{r\phi} = 130$ μm $\sigma_z = 200 \sim 1400$ μm $\sigma_{p_t}/p_t = 0.3\ \% \sqrt{p_t^2 + 1}$ $\sigma_{dE/dx} = 6$ %
ACC	$n \simeq 1.01$ Silica Aerogel	$\sim 12 \times 12 \times 12$ cm^3 blocks 960 barrel/268 endcap FM-PMT readout	2188	$N_{pe} \geq 6$ K/π separation: $1.2 \leq p \leq 3.5$ GeV/c
TOF	Scintillator	128 ϕ segmentation r = 120 cm, 3 m-long	128 × 2	$\sigma_t = 100$ ps K/π separation: up to 1.2 GeV/c
ECL	CsI	Towered structure $\sim 5.5 \times 5.5 \times 30$ cm^3 crystals		$\sigma_E/E =$ 0.67 %/$\sqrt{E} \oplus$ 1.8 % $\sigma_{pos} = 0.5$ cm/$\sqrt{E}$ E in GeV
		Barrel: $r = 125 \sim 162$ cm	6624	
		Endcap: $z = -102$ and +196 cm	forward: 1216 backward: 1040	
Magnet	Super conducting	inner radial = 170 cm		B = 1.5 T
KLM	Resistive plate chamber	14 layers (5 cm Fe + 4 cm gap) two RPCs in each gap θ and ϕ strips	θ: 16 K ϕ: 16 K	$\Delta\phi = \Delta\theta = 30$ mr for K_L $\sigma_t = 1$ ns 1 % hadron fakes
EFC	Bismuth germanate crystals (BGO) $n \simeq 2.15$	5 segments in θ 32 segments in ϕ	forward: 160 backward: 160	$\sigma_E/E =$ (0.3 ∼ 1) %/$\sqrt{E}$ [9]

of γ rays and electrons.

For K_L and μ detection, the KLM detector is used. KLM consists of an octagonal barrel section and two endcaps that are composed of a sandwich of fourteen 5 cm iron absorbor plates and fifteen (fourteen) 4 cm instrumented gaps in the barrel (in each endcap) region.

The EFC detector is comprised of radiation-hard bismuth germanate crystals (BGO). EFC is used as a calorimeter which covers the uncoverd small-angle region by CsI.

Chapter 3

Silicon Vertex Detector System

3.1 Silicon vertex detector

We constructed a silicon vertex detector for BELLE SVD. The silicon detector is required to have a vertex resolution about 100 μm to detect vertex points of B meson decays. The detector is a double-sided silicon detector (DSSD) fabricated by Hamamatsu Photonics (HPK), originally designed for the DELPHI micro vertex detector [11]. A typical layout of a DSSD is shown in Fig. 3.1. In this figure, there are readout Al lines with the double metal layer (DML) technique in the n-side readout. DML is used in the case when the direction of readout strips does not match with the connection of preamplifier chips. Specifications of detectors for BELLE SVD are shown in Table 3.1. Table 3.2 shows measured parameters of a DSSD.

A cross-sectional view of the silicon vertex detector (SVD) is shown in Fig. 3.2. SVD comprises three layers of DSSD ladders. There are eight, ten and fourteen ladders in the inner, middle and outer layers, respectively. A schematic view of these silicon detector ladders is shown in Fig. 3.3. In this figure, hybrid boards with five VA1 preamplifier chips are attached to both ends of the silicon detector ladders. As shown in this figure, the length of each ladder in these three layers is different. All ladders use the same size silicon detectors whose parameters are listed in Table 3.2. Ladders consist of two, three and four detectors and two double-sided hybrid boards with five VA1 chips on each side. Details of the VA1 chip is described in the next section.

Electrical connection between silicon detectors is made by a wire-bonding

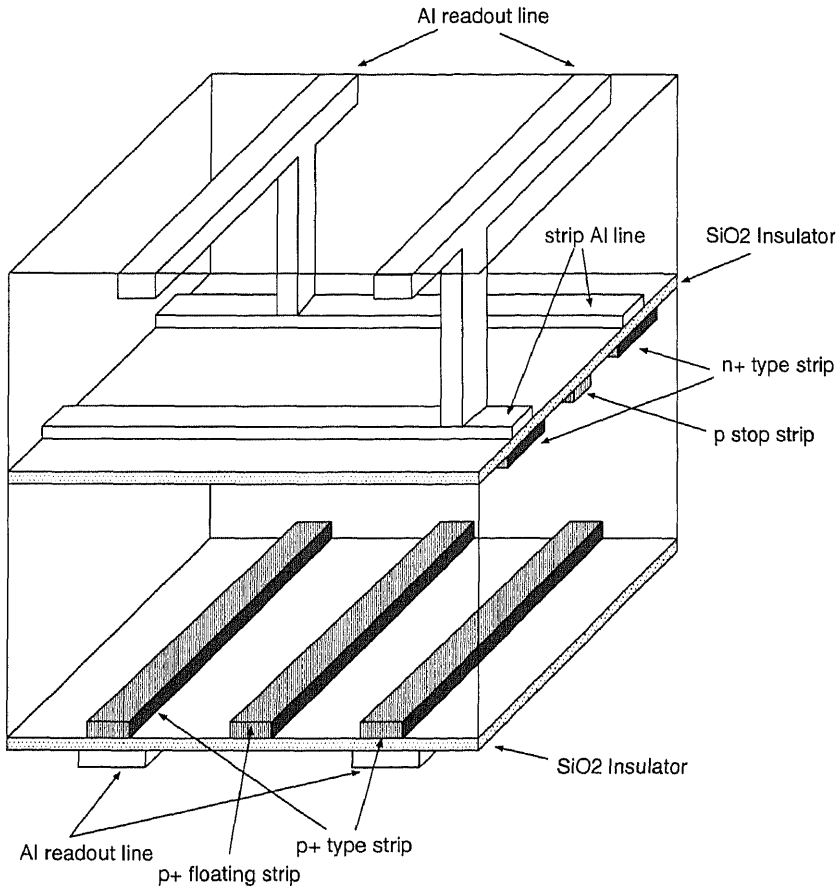


Figure 3.1: Typical layout of a DSSD with a double metal layer.

Table 3.1: Specifications of a silicon detector for BELLE SVD.

Parameter	p-side	n-side
Chip size	57.5 mm × 33.5 mm	
Active area	54.5 mm × 32.025 mm	53.76 mm × 32.04 mm
Thickness	300 ± 15 μm	
Readout (Bias) method	AC (Poly-Si)	
Strip pitch	25 μm	42 μm
Number of strips	1281	1280
Number of readout strips	641	640
Strip width	8 μm	
Readout electrode width	8 μm	14 μm
DML (double metal layer) insulator material, thickness	N/A	SiO_2, 5 μm
DML trace pitch, width	N/A	48 μm, 8 μm
Full depletion voltage (V_{fd})	80 V Maximum	
Breakdown voltage	100 V Minimum	
Leakage current at V_{fd}	2 μA Maximum	
Bias resistance	25 MΩ Minimum	
Coupling capacitance at 10 kHz	55 pF	40 pF
Breakdown voltage of coupling capacitor	50 V Minimum	
Load capacitance at 1 MHz	8 pF	20 pF
Number of NG channels	19 Maximum	
Passivation	SiO_2	

Table 3.2: HPK S6936 parameters assumed in the performance estimation.

Capacitance	calculated by D. Husson's model [12] in agreement with measurement [13]
Leak current	2.1 nA/readout channel [14]
Bias resistance	20 MΩ/strip on p-side, 35 MΩ/strip on n-side [15]
p-stop noise on n-side	600 e^-/readout channel [14]
Damage constant	5 nA/cm^2/krad [16]
Fraction of good channels	0.95^n; n = 1 or 2: number of daisy-chains

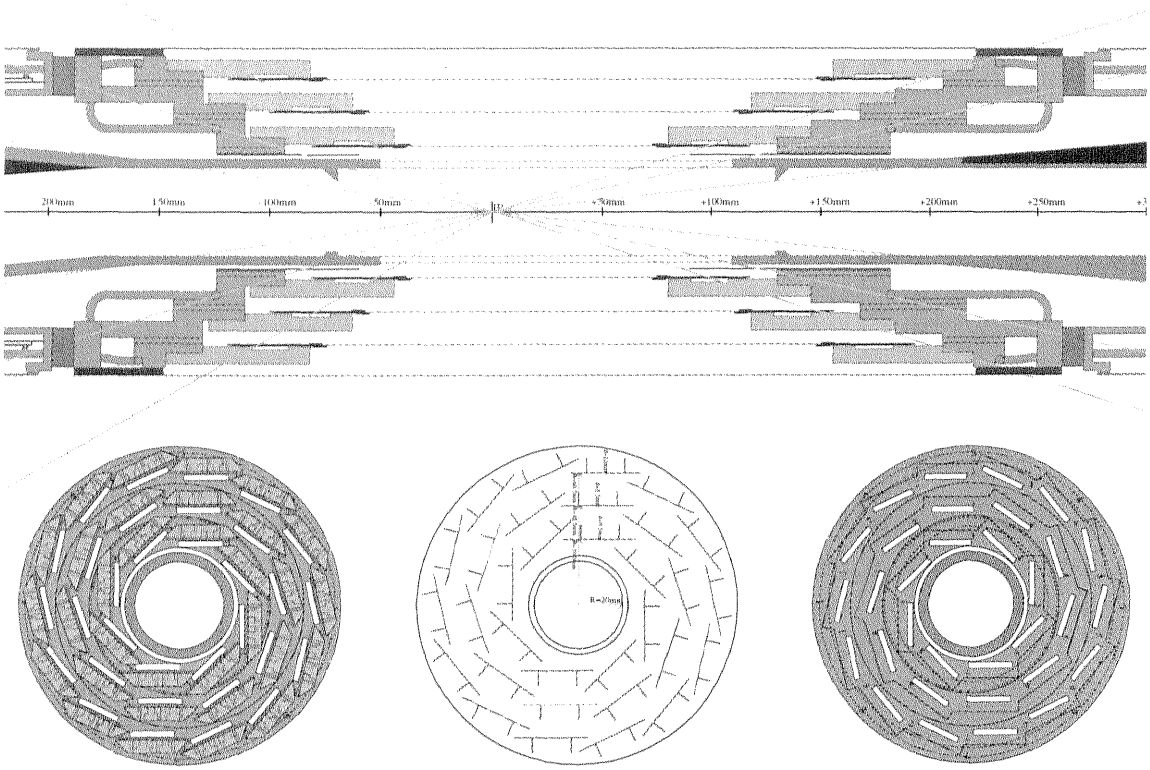


Figure 3.2: Cross-sectional view of the silicon vertex detector.

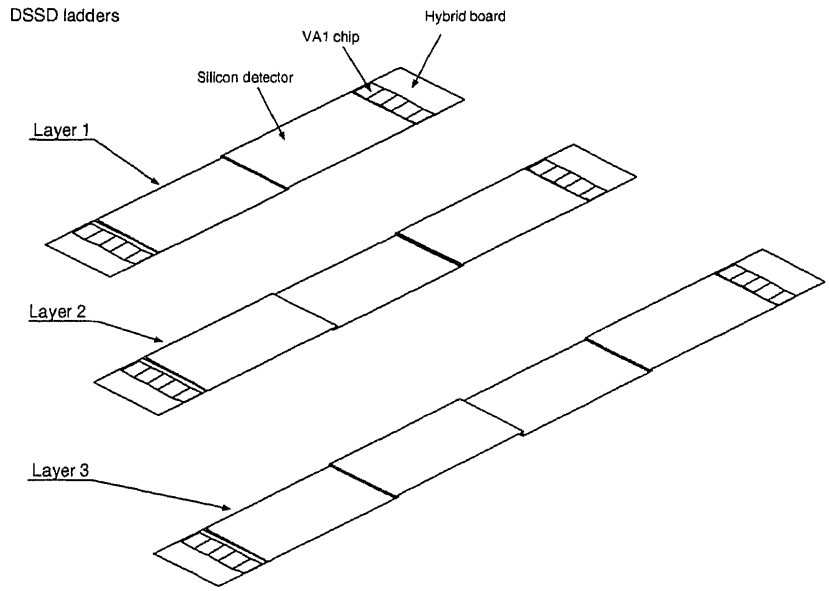


Figure 3.3: Schematic view of silicon detector ladders of layer 1 (inner), layer 2 (middle) and layer 3 (outer layer).

method. This method was also used in the electrical connection between VA1 chips on a hybrid board and a silicon detector. A ladder consists of either just a single detector or two detectors with an overlap joint. In order to minimize noises of the double-detector module, different sides of the two detectors are connected, i.e. p-strips on one detector are wire-bonded to n-strips on the other detector as shown in Fig. 3.4. This is possible because the detectors incorporate integrated coupling capacitors. This is called a p-n flipped half-ladder.

The detector capacitance, expected noise (ENC: electron noise charge) and signal-to-noise ratio (S/N) for a normal incidence of MIP are summarized in Table 3.3 [10]. The several parameters of the silicon detector system are summarized in Table 3.4. Electrical connection between hybrid boards which are connected to the both ends is isolated at the center or near the center of a ladder to avoid ground loop. In the inner layer case, the electrical connection is isolated among two silicon detectors. A ladder in the middle layer consists of one silicon detector and one p-n flipped half-ladder. The electrical connection is isolated among the detector and the ladder. A ladder

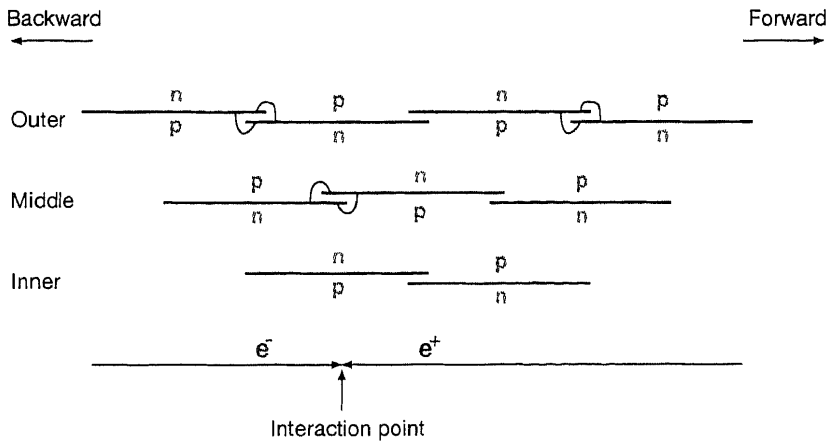


Figure 3.4: Assignment of the silicon detector ladders.

Table 3.3: Detector capacitance (C), expected noise (ENC: electron noise charge) and signal-to-noise ratio (S/N) for the radiation dose of 0 krad.

Half-ladder	Side	C (pF)	ENC (e^-)	S/N
Detector × 1	p	7	510	32
	n	22	750	22
Detector × 2	p-n	29	890	18

Table 3.4: Parameters of the silicon detector system.

Layer	Inner	Middle	Outer
Number of silicon detector ladders	8	10	14
Number of detector units in one ladder	2 DSSDs = 2 × DSSD half ladder	3 DSSDs = 1 × p-n flipped half ladder + 1 × DSSD	4 DSSDs = 2 × p-n flipped

in the outer layer comprises two p-n flipped half-ladders. The electrical connection is isolated among those ladders.

The dependence of S/N on radiation dose is shown in Table 3.5 [10].

Table 3.5: Expected signal-to-noise ratio after irradiation. The radiation dose values shown are for the inner layer. The radiation doses in the middle and outer layers are assumed to scale as r^{-1}.

Half-ladder	Side	0 krad	50 krad	100 krad	150 krad
inner (1 DSSD)	p	32	23	19	15
	n	22	18	15	13
middle (forward) (1 DSSD)	p	32	25	21	18
	n	22	19	17	15
middle (backward) (2 DSSDs)	p-n	18	16	13	12
outer (2 DSSDs)	p-n	18	16	14	13

3.2 Frontend electronics

For amplifying and sending signals from the DSSDs, front-end VLSI chips on hybrid boards are connected to the DSSDs by a wire bonding method. We need good front-end electronics for low noise signal handling. To meet this requirement, we selected VA1 chips for amplifying signals from the silicon vertex detectors. The VA1 chip was developed at CERN and is commercially available from IDEAS, Oslo, Norway. VA1 chips mounted on hybrid boards are connected at the both ends of the DSSDs. The schematic diagram of a VA1 chip is shown in Fig. 3.5. The VA1 chip is produced with 1.2 μm CMOS technology. This chip has excellent noise characteristics, and has 128 low power (1.2 mW/channel) charge sensitive preamplifiers followed by CR-RC shapers, sample & hold circuitry, output multiplexing and output buffer. The output channels are daisy chained, and read out at 5 MHz. In BELLE SVD, we operate VA1 chips with a peaking time of 2.5 μs according to the trigger latency. With this peaking time, noise performance will be expected

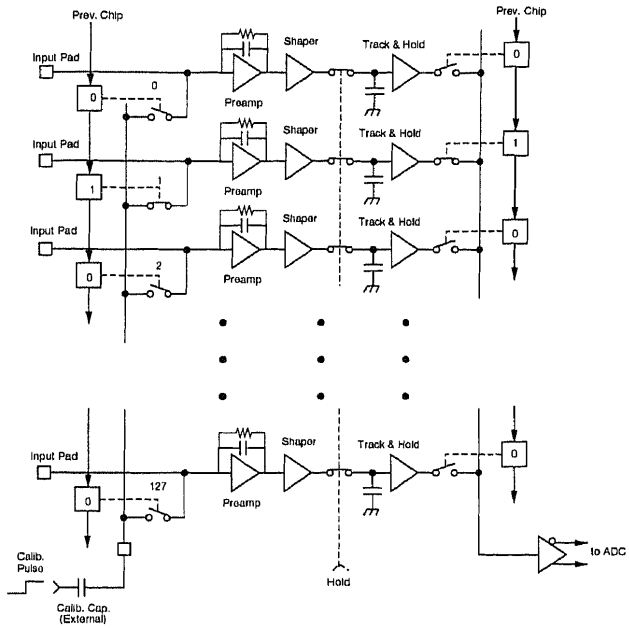


Figure 3.5: Schematic diagram of a VA1 chip.

to be about $165 + 6.1 \times C$ electrons equivalent noise charge (ENC), where C is the capacitance at the input in pF, giving less than 400 electrons for 35 pF, the average strip capacitance expected.

Figure 3.6 shows the operation sequence of the VA1 chips. The shaping time of the VA1 chips is adjusted to 2.5 μs, which matches the level-1 trigger latency time of the BELLE trigger. Before receiving a trigger signal, HOLD is low and the storage capacitors tied to the output of each shaper amplifier follow signals as shown in Fig. 3.5 and 3.6. To avoid crosstalk between the sensitive analog frontend and the digital control signals, no clock signals are sent to the system during this time. Upon receipt of a level-1 trigger, HOLD goes to high and the shaper outputs are stored in analog form pending readout. The stored voltage ($\propto$ deposited charge) in each channel is sequentially routed to an on-chip analog buffer via a built-in analog multiplexer. This analog signal is transmitted from the hybrid through the repeater cards to an FADC (flash analog-to-digital converter) module in an electronics hut. A VA1 chip ignores all readout clocks until assertion of its SHIFT-IN line. Once all channels in a chip have been scanned, it asserts its SHIFT-OUT

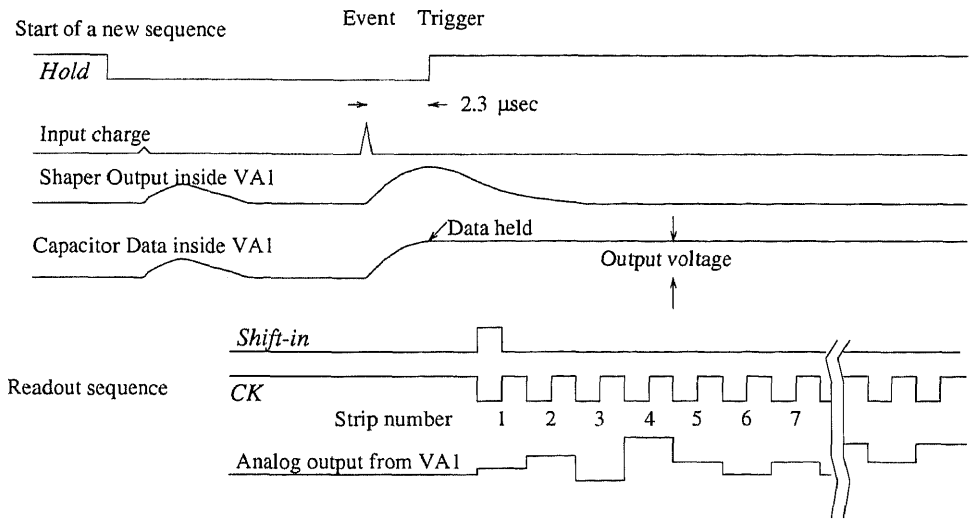


Figure 3.6: The operation sequence of the VA1 chip.

line. By connecting SHIFT-OUT of one chip to the SHIFT-IN of the next, an arbitrary number of chips can be daisy-chained together.

In BELLE the five VA1 chips of each side of the single-sided hybrids are daisy chained. Figure 3.7 shows a schematic of a hybrid card with five VA1 chips. Readout of each chain will be initiated by asserting SHIFT-IN for the first chip in the chain. Monitoring of the SHIFT-OUT line of the last chip in the chain will provide a check on system operation. Once all strips are read out, the front-end system becomes ready to start a new sequence.

3.3 Repeater system for BELLE SVD

A repeater system (CORE) [10] is designed for buffering analog signals from VA1 chips on hybrids, which are connected at the both ends of silicon detectors, and the system will receive (transfer) digital signals from (to) the upper level system (frontend electronics), typically to control the VA1 chips on the hybrids. The system also supplies electric power to the frontend electronics.

This system comprises analog buffer cards (ABC), a frontend control boards (REBO), a monitoring board (RAMBO), a mother board (MAMBO) and a cooling and shielding case (DOCK). Block diagrams of the REBO,

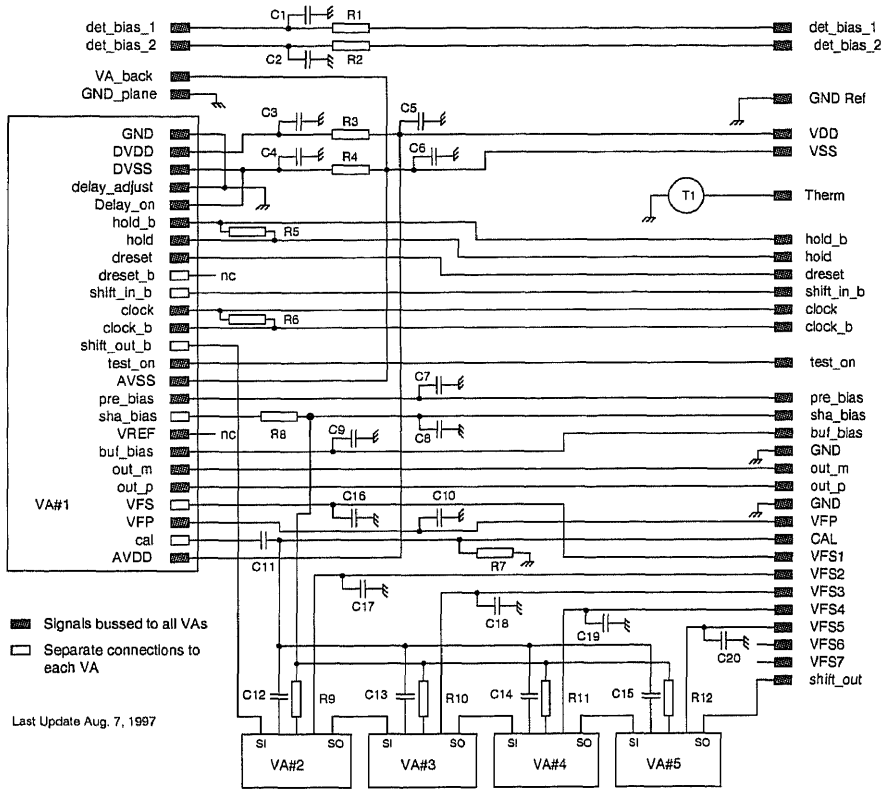


Figure 3.7: Schematic of a hybrid with five VA1 chips, where *SI* and *SO* at the bottom of this figure denote SHIFT-IN and SHIFT-OUT, respectively.

RAMBO and MAMBO are shown in Figs. 3.8, 3.9 and 3.10, respectively.

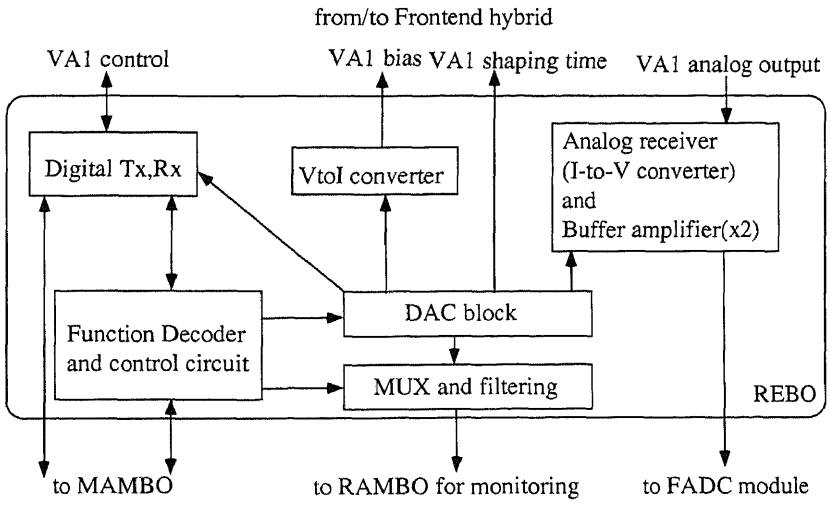


Figure 3.8: Block diagram of a REBO.

Four REBOs and one MAMBO are installed in the DOCK in order to satisfy the cooling requirement, immunity from EMI and the cable clearance. A schematic diagram of the DOCK is shown in Fig. 3.11. Two cooling pipes are mounted on the both sides of the DOCK. The size of the DOCK is 12 cm in height, 20 cm in width and 40 cm in length to settle all components in between QCS magnet and ACC/EFC. The DOCK is made of aluminum. A side view of the DOCK in the BELLE complex is shown in Fig. 3.12. There are four DOCKs in the forward and backward directions as shown in Figs. 3.13 (a) and (b), respectively. In order to isolate heat transfer between a DOCK and a CDC, a thick PCB is located among them. Figure 3.14 shows a schematic diagram of the CORE system. ABCs are put on a support cylinder about 20 cm away from the hybrid cards of the detectors. The DOCKs, in which there are a MAMBO, four REBOs and a RAMBO, are placed about 2 m away from the ABCs. Cables from the DOCKs are connected to the FADC modules in the electronics hut about 30 m away from the DOCKs.

Analog signals from VA1 chips are received and transferred to MAMBOs via ABCs. The analog signals on MAMBO are sent to REBO. Four shielded twisted pair cables are connected from one FADC module to one REBO to transfer analog signals with low noises. After analog signals on REBO are amplified and filtered, these signals are sent to FADCs as differential

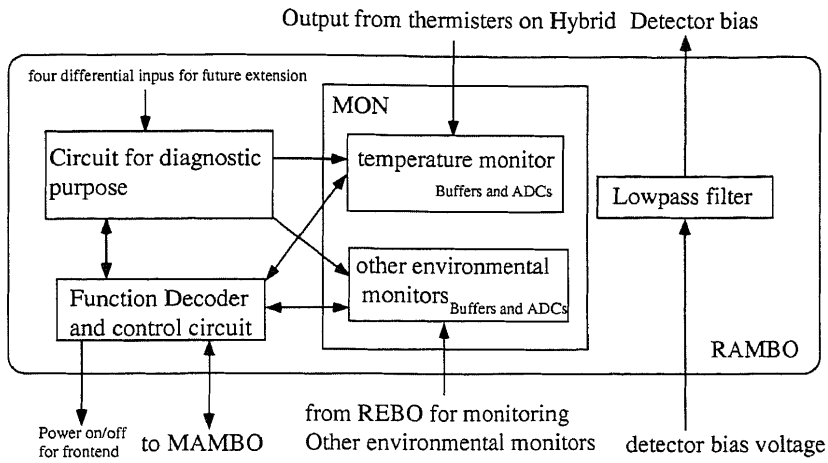


Figure 3.9: Block diagram of a RAMBO.

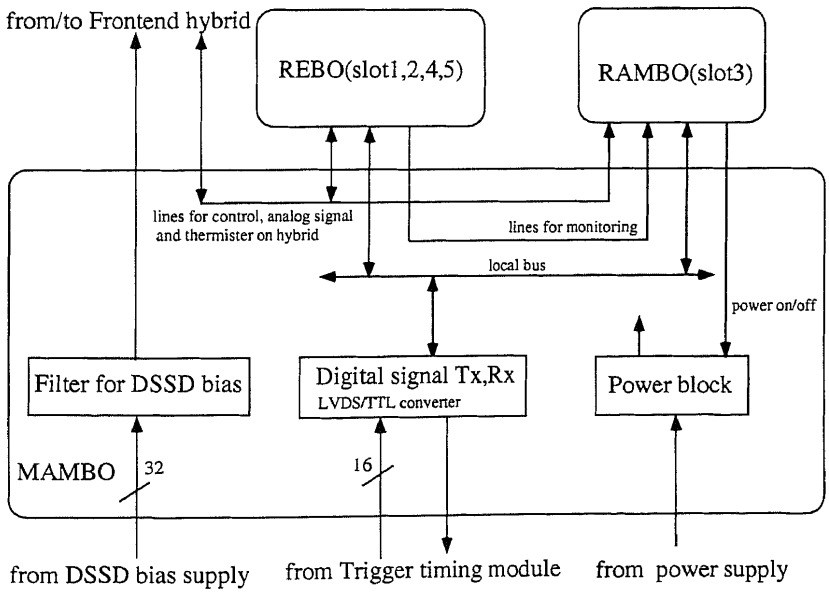


Figure 3.10: Block diagram of a MAMBO.

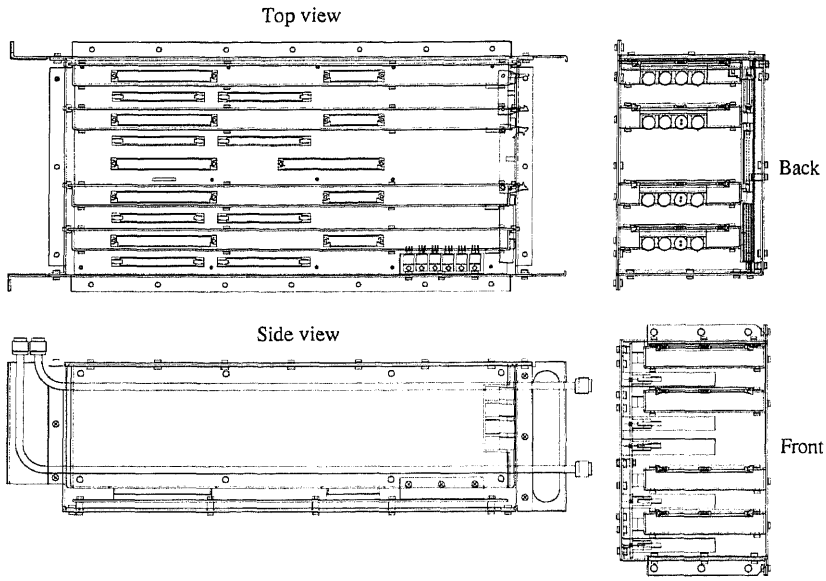


Figure 3.11: Schematic diagram of DOCK.

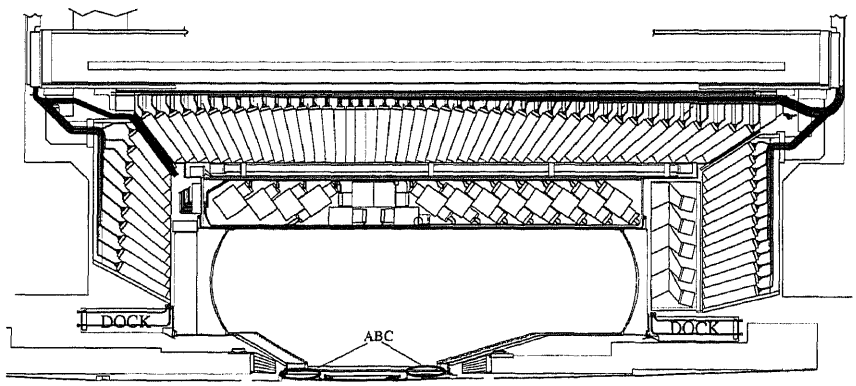


Figure 3.12: Side view of DOCK in the BELLE complex.

(a) Forward direction (b) Backward direction

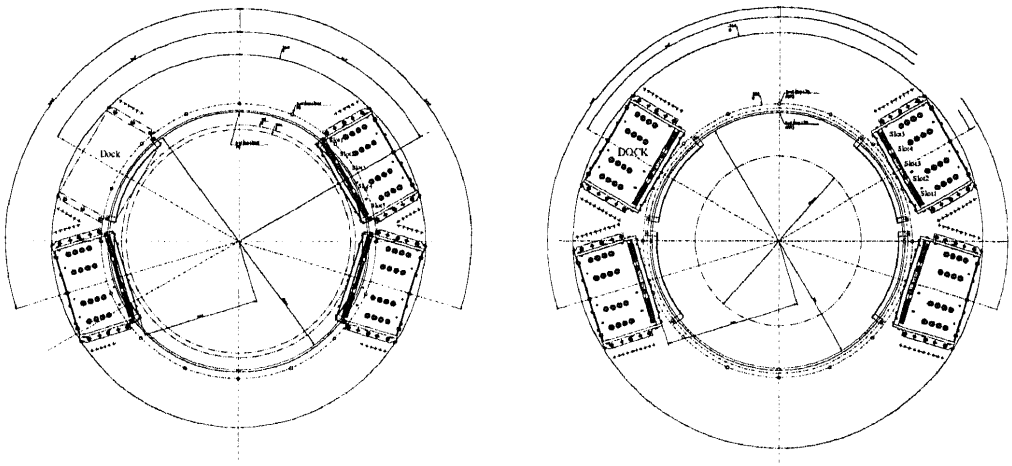


Figure 3.13: Cross sectional view of DOCK in the BELLE complex (a) from the forward direction and (b) from the backward direction.

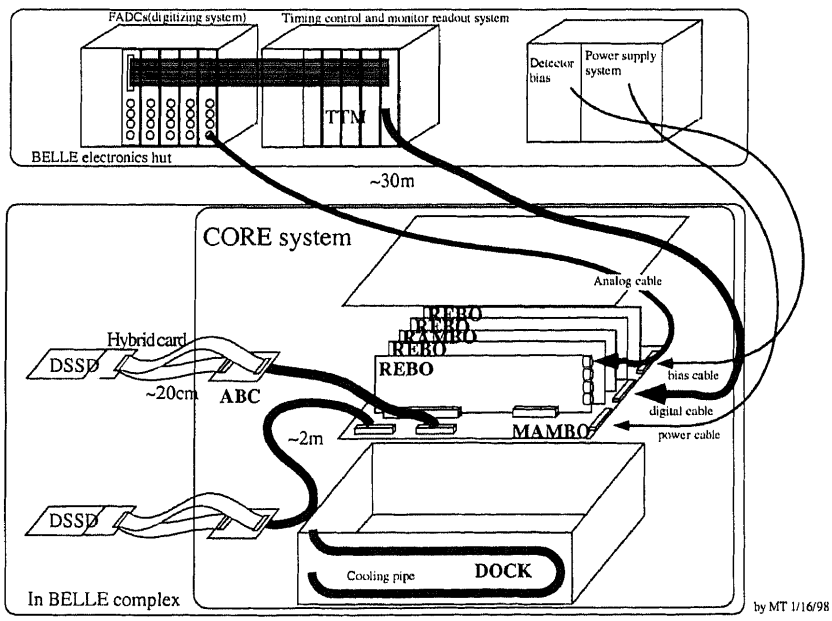


Figure 3.14: Schematic diagram of a CORE system.

analog signals. Digital control and timing signals are transferred from a trigger timing and monitor readout system (TTM) to MAMBO via a digital cable, and distributed to all the boards on MAMBO. TTM can also read monitored data in MAMBO. Cables from power supplies in the electronics hut are connected to the MAMBOs. Detector bias signals are fed into the DSSDs via ABCs.

For power supplies for detector biasing, the CAEN SY403 high voltage system is selected. Digital and analog biases are supplied from series regulators on repeater cards. To supply whole digital and analog biases, two 5 V $\times$ 100 A power units, which are fabricated by NISTAC Co. Ltd., Japan, are used in the electronics hut. It is known that the tolerance of the front-end system and DSSD against radiation doses can be improved if power is not applied during the period of high-radiation environment. Therefore the power supply units should be controlled by a slow-control system[1].

3.4 Backend electronics

The BELLE DAQ system employs a simple architecture wherein the front-end electronics is temporarily inhibited upon receipt of a level-1 trigger. Thus a busy signal is asserted and remains until all front-end subsystems have transferred their data to secondary buffers. To keep the dead-time minimum, all front-end subsystems are required to release their busy signal within 200 μs from the level-1 trigger time, at which point they must be ready to accept and process another level-1 trigger.

The time required for the analog multiplexer scan of VA1 outputs sets the ultimate limit to the readout rate. If the maximum scan rate of the VA1 output is 5 MHz, no more than 1000 channels ($\sim$ eight VA1 chips) can be read by a single DAQ channel. Therefore it is necessary to ensure that there is no additional dead-time incurred in the process of data transfer and/or pedestal subtraction and zero suppression. We achieved this by using pipelined logic and by inserting a derandomizing FIFO buffer memory between the ADCs and the downstream portions of DAQ. For this purpose, we have developed an analog pipelined flash ADC (FADC) module which has DSPs and FPGAs.

[1]The terminology, *slow-control* is used to distinguish from *fast-control*. The fast-control denotes the DAQ system.

3.4.1 Timing distributor module

The BELLE DAQ system is a large-scale distributed system. The readout system of each sub-detector is almost independent, except for the fast trigger system which is centrally controlled. Data are fed into the event builder. Figure 3.15 shows a schematic diagram of the BELLE trigger and DAQ

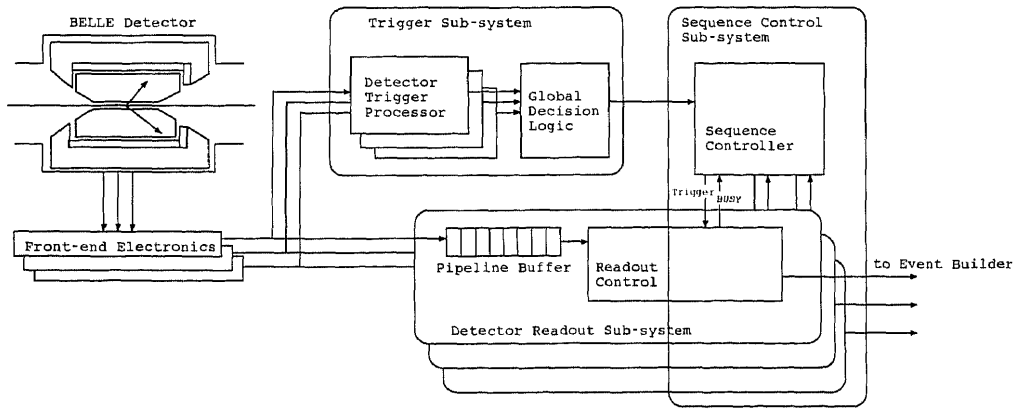


Figure 3.15: Schematic diagram of the trigger and DAQ system of the BELLE detector.

system. For each interesting event which happens at the interaction point, detector signals are processed through the detector trigger system in order to be fed into the global decision logic (GDL) system within 1.85 μs. The level-1 trigger decision is made 2.2 μs after the event occurs. Finally the trigger signal is distributed back to the readout electronics of the detector sub-systems within 2.5 μs.

A timing distributor module (TDM) [17], which was fabricated by the central DAQ group, is used to receive the trigger signal in each detector readout sub-system. This module has two operation modes; one is the *online* mode and the other the *stand-alone* mode. In the online mode, the TDM receives the trigger signal from the central DAQ system. On the other hand, the local clock signal from TDM is used in the stand-alone mode.

3.4.2 Timing trigger module

For timing control of the frontend electronics and Halny FADC control, we used timing trigger modules (TTM). The TTM modules were designed and fabricated by Princeton group. The TTM modules distribute timing signals to FADCs and frontend electronics according to the CDAQ control and clock signals. Signals going to or coming from the VA1 chips are routed through the repeater system, which provides fan-in/fan-out, level translation, and additional buffering. This board can be used in the master or slave mode in asserting the timing signals. A setup of TTM boards in the SVD DAQ system is shown in Fig. 3.16. The system consists of nine modules: one master and eight slave modules. Two types of TTM are implemented using the same hardware, but are configured with a different firmware (Xilinx FPGA design code). The master TTM receives timing control signals from a timing distributor module (TDM), supplied from CDAQ, and asserts signals to slave TTMs. While each slave module handles the interaction with one repeater dock via a point-to-point low-voltage differential signaling (LVDS) link[2]. The TTMs are also used to send signals to each FADC module in FADC crates. RS 485 (differential TTL) is used for communication between the TTMs and the FADCs. Each slave TTM serves timing control signals to frontend electronics and eight FADCs which are assigned.

3.4.3 FADC module

The FADC module must be able to scan analog outputs of the VA1 chips in 200 μs or less (thus dead time less than 10 % at a trigger rate of 500 Hz). In addition, the system must also perform zero suppression so as to reduce the data flow in the downstream portions of DAQ in analog-to-digital conversion. To achieve these requirements, we have selected to use a Motorola DSP56302 digital signal processor (DSP) chip. Digital first-in/first-out (FIFO) memories are incorporated in the readout chain to derandomize events, allowing the most efficient use of DSP. The FADC module called *Halny* was designed and fabricated by Krakow and Princeton groups. A block diagram of the Halny FADC is shown in Fig. 3.17. The Halny FADC module has a capability of sparse data scan. Details of the sparse data scan is described in Appendix D. In this mode, each DSP on this module calculates pedestal and

[2]The LVDS standard employs differential signal swing of $\pm$350 mV, resulting in reduced power consumption and reduced electromagnetic interference relative to standard TTL.

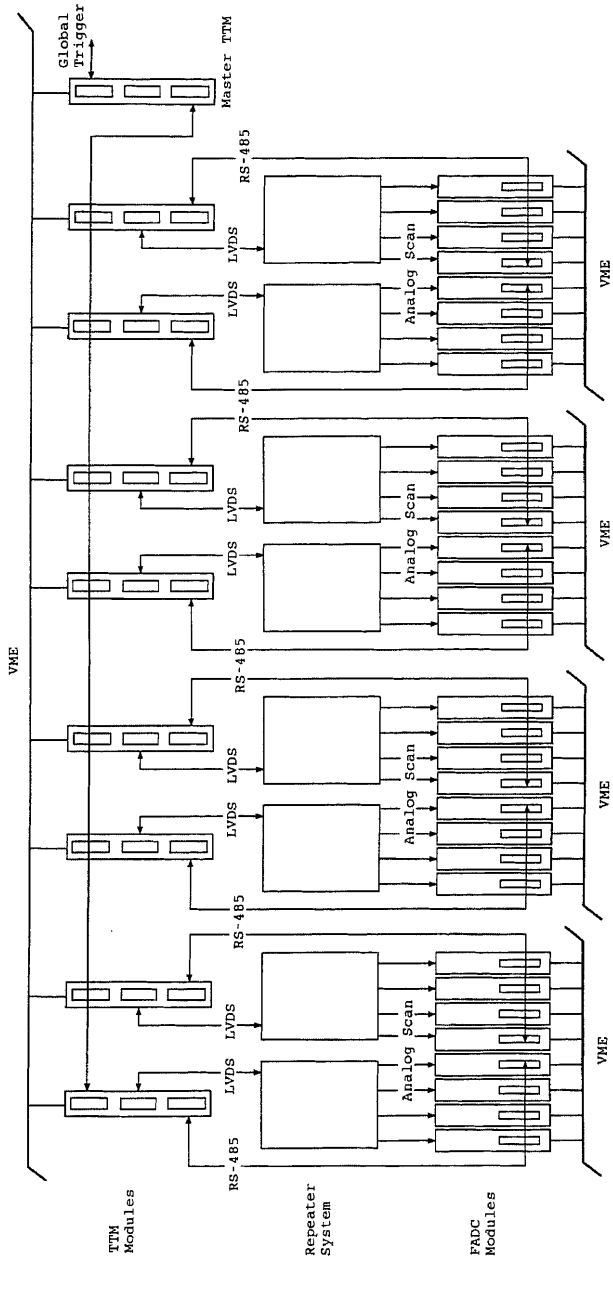


Figure 3.16: Setup of TTM boards in the SVD DAQ system.

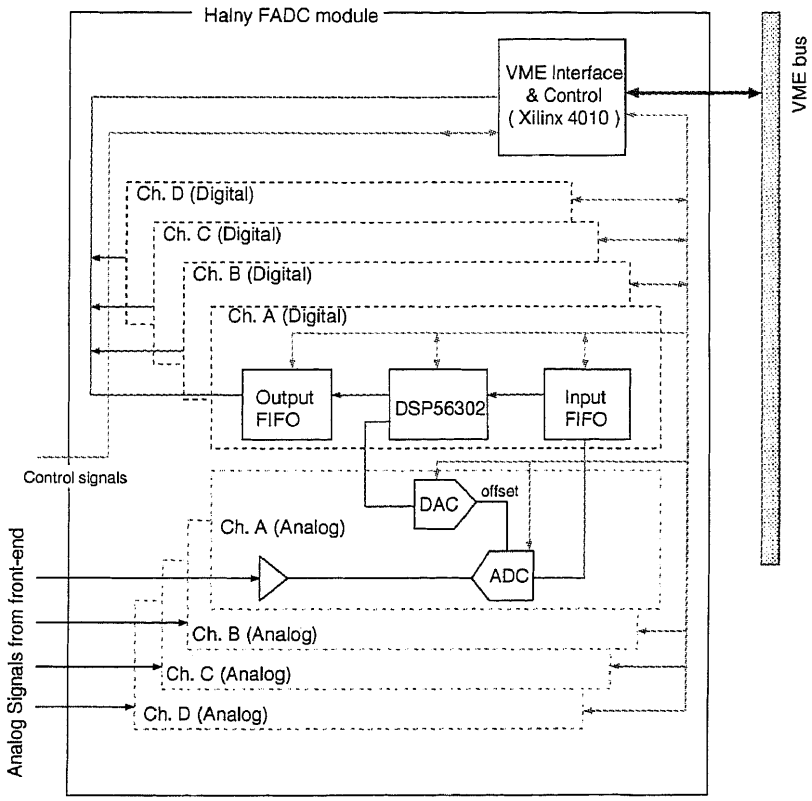


Figure 3.17: Block diagram of a Halny FADC module.

noise levels of each channel. According to these data and a threshold value, each DSP defines whether the channel is hit or not from a digitized signal value.

3.4.4 SHARC VME cluster board

In the DAQ system for BELLE SVD, we selected a SHARC DSP VME cluster board (WS2126) as a core of data acquisition task. The WS2126 reads data from Halny FADC modules and send the data to Sparc CPU VME board (CPU-7V) via VME bus. The CPU-7V is used as a part of central event builder interface (CEBTX), which sends data to the central DAQ system.

The WS2126 and SHARC DSP were delivered from WIESE Signalverarbeitung GmbH, Germany and Analog Devices, USA, respectively. WS2126 has capabilities of a high speed data transfer on the VME bus, a point-to-point flexible link connection for data transfer and a communication between DSPs. For this link connection, SHARC IO piggy pack (WS9002), which was fabricated by WIESE Signalverarbeitung GmbH, supports flexible link connection on the front panel of WS2126. A similar type of modules has been already used in HERA-B [21, 22] and performed a high speed data transfer. The SHARC DSP itself also has been used in several experiments [23, 24, 25]. A block diagram of a WS2126 mounting a WS9002 is shown in Fig. 3.18. WS2126 is a VME 6U-size board. This board can mount up to six SHARC DSPs (ADSP-21060 or ADSP-21062) and six WS9002s. A functional diagram of WS2126 is shown in Fig. 3.19. This module has a capability of acting the VME slave and the master mode. First, this module is set to an A24/D16 VME slave mode after power is on a VME crate. After that, this module is set to a VME master mode by a downloaded program which runs on a SHARC DSP. In the VME slave mode, data on the on-chip RAM of the SHARC DSPs and on the external memory are accessible from the VME bus via the FIFO memory. In the VME master mode, each DSP can have access to the VME bus via a customized logic chip for VME P2 access (ALTERA MAX 9000) on this board.

A SHARC DSP supports JTAG test connector [18]. WS2126 also supports the JTAG test connector facility [19]. Using this JTAG connector, we can debug a DSP program, download a specific logic firmware to the ALTERA MAX 9000 and so on.

SHARC DSP has six link ports (SHARC link). These links are used for transferring data between WS2126s in different VME crates. This link

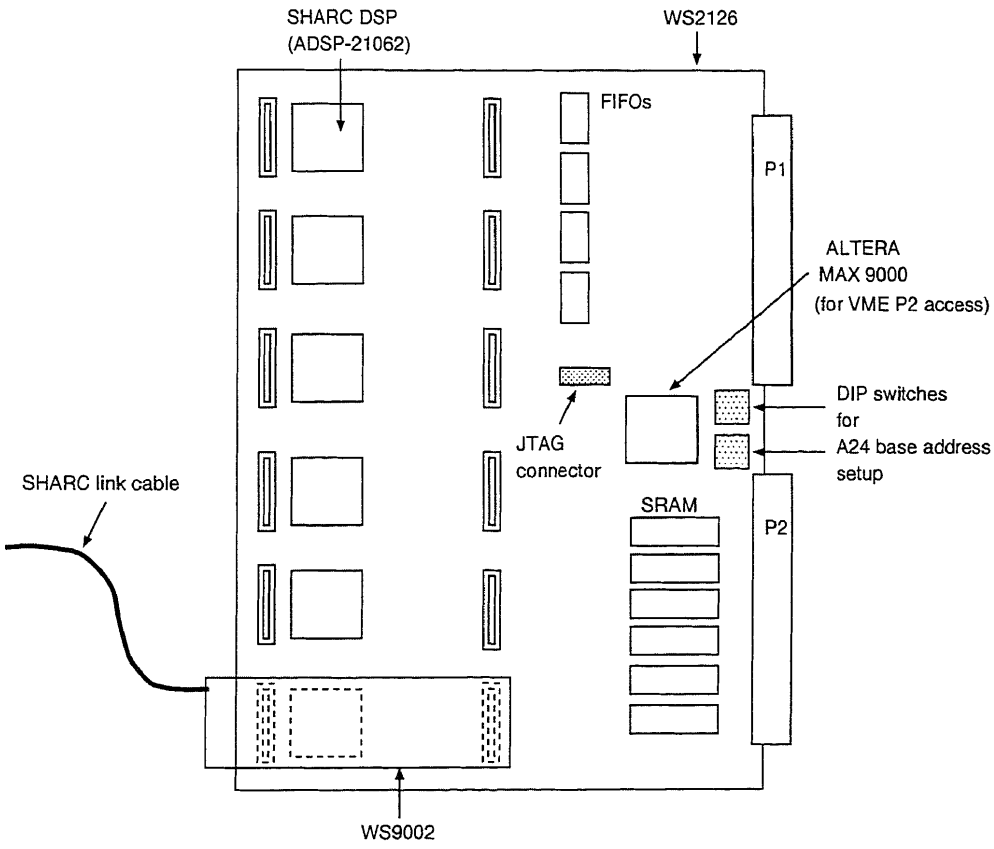


Figure 3.18: Schematic view of a WS2126 with a WS9002.

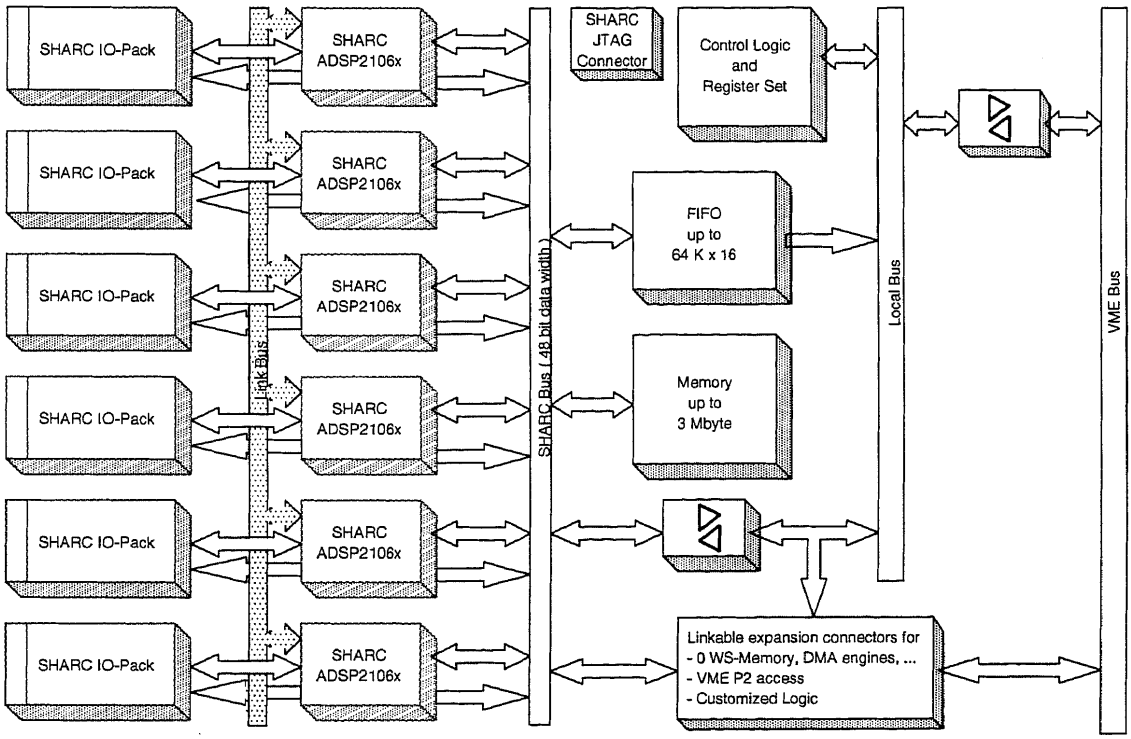


Figure 3.19: Functional diagram of a SHARC VME cluster board, WS2126.

communication between SHARC DSPs on WS2126 is realized by WS9002s which were fabricated by WIESE. A functional diagram of a WS9002 is shown in Fig. 3.20. This link has a 40 MB/s transfer speed. One WS9002 has six link

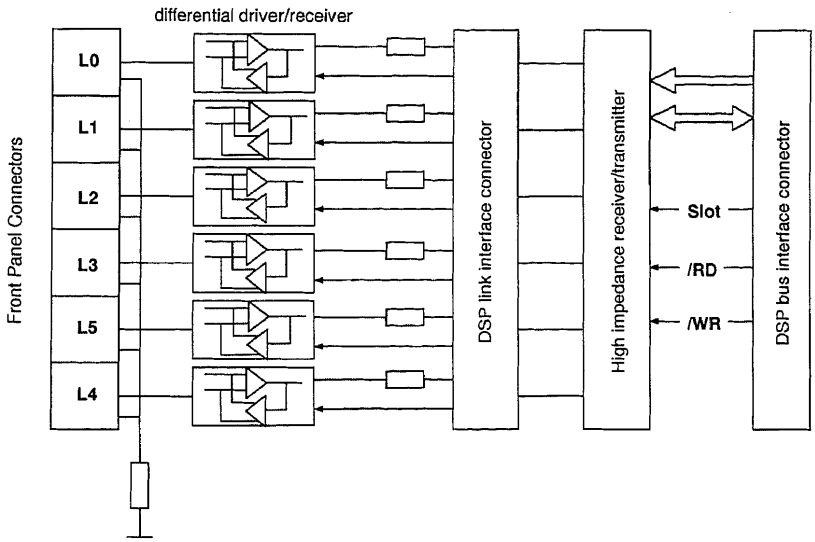


Figure 3.20: Functional diagram of a SHARC IO piggy pack, WS9002.

ports (L0 $\sim$ L5). Because of the hardware design conception, the sequence of the location of link ports of L4 and L5 in Fig. 3.20 is opposite. The number of the link ports on WS9002 and that of the links of SHARC DSP are the same. Using a control register on WS9002, flexible link connection between links of a SHARC DSP and link ports of a WS9002 is realized. The direction of transfer is also configurable by a register on WS9002. The register is accessible from a program on SHARC DSP. In each link port, there is a buffer to store data which will be sent (received) in the transmitter (receiver) case. Each WS2126 can mount up to six WS9002s. A connector of a link cable is suited in the front panel of WS2126. Therefore we can connect between SHARC DSPs by point-to-point connection. Because of the requirement of a stable signal transfer for long length cables, the output signals from WS9002 are differential signals with the help of differential drivers/receivers. Figure 3.21 shows a layout of the connector of a WS9002. Each link port has 4 bit data lines (D0 $\sim$ D3), a clock signal (CLK) and an acknowledge signal (ACK). Two kinds of data can be transferred via the links: 32 bit words

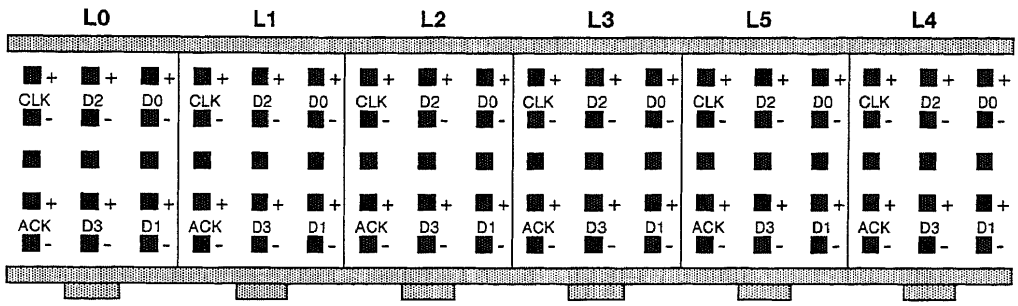


Figure 3.21: Layout of a connector of a WS9002.

(long words) and 48 bit words (very long words). The link logic splits each word into eight or twelve nibbles respectively. The ACK signal is asserted at a transmitter link port and sent to a receiver link port. Each Data on the links are transferred synchronously with this clock signal. The receiver link port toggles the ACK signal after having received the first nibble if its link buffer cannot store the next word. The remaining nibbles of the current word will always fit into the buffer. By this the ACK signal has, in case of short link connections, enough time to arrive at the transmitter before it starts transmitting the next word. In the DAQ system of SVD, because the length of link cables is about 3 m, the time needed for a round trip through the link cables is negligible for the ACK signal to arrive at the transmitter before it starts transmitting the next word.

A DSP program was written in C and a loadable code is created from this program. The loadable code is downloaded from a host computer (Force CPU-7V) to SHARC DSPs via VME bus. Details of the download and control methods are described in Appendix C. VME single word, DMA (direct memory access) and BLT (block transfer) transfer methods are supported in this module

3.5 Data acquisition system for BELLE SVD

In the DAQ system for BELLE, most of all the sub-detector DAQ systems are based on TDC (time-to-digital converter) based systems, whereas for the SVD detector, we selected the FADC based DAQ system. A block diagram of the DAQ system of the BELLE detector is shown in Fig. 3.22. Data from

each sub-detector are gathered in the event builder block [4]. The gathered data are sent to the online computer farm and stored in magnetic tapes in the mass storage system.

The DAQ system of all the sub-detectors, except SVD, is shown in Fig. 3.23. Signals from the detectors are converted from charge to time by Q-to-T converter chips and converted to digital data by FASTBUS TDCs [26]. The data in the FASTBUS TDCs are sent to a dual port memory module in the VME crate via a 68kFPI FASTBUS processor module [27]. The MVME162 module, which has a MC68040 CPU in the VME crate reads data from the dual port memory and send them to the local CPU module (Force Sparc CPU-5V or CPU-7V). Then the data are transferred to central CDAQ via an event builder interface S-bus card.

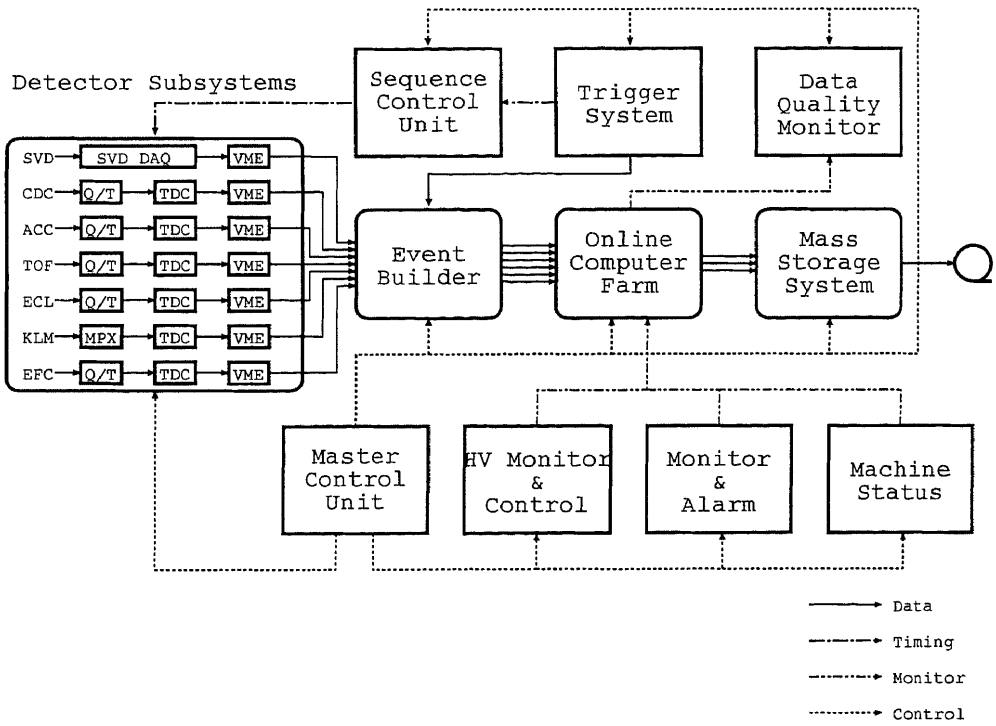


Figure 3.22: Block diagram of the data acquisition system of the BELLE detector.

On the other hand, SVD has a large number of channels ($\sim$ 82,000). One FASTBUS TDC has 96 input channels. If we adopt the FASTBUS TDC

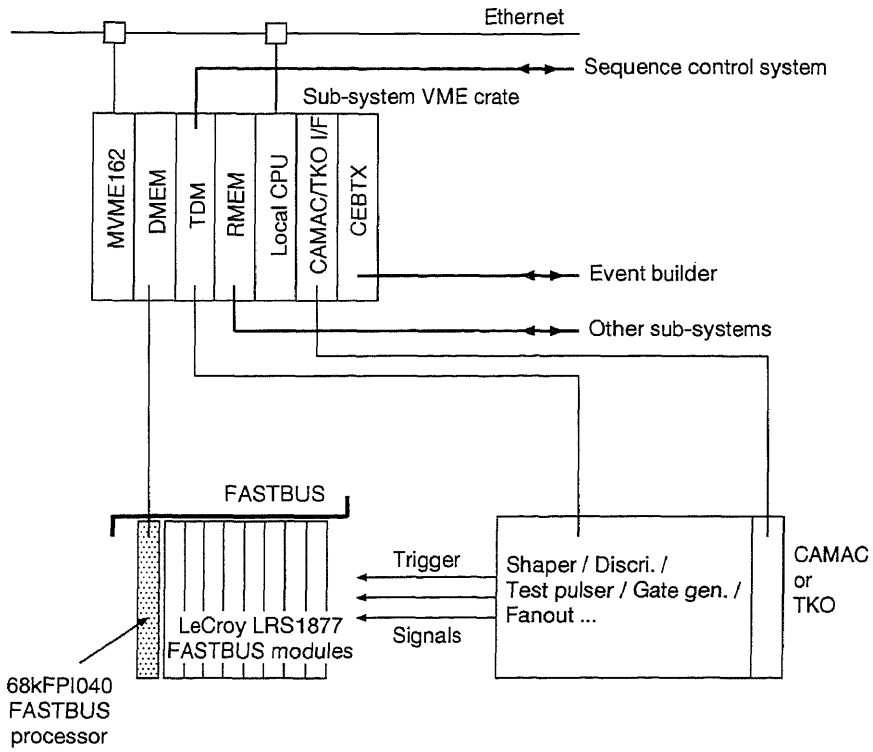


Figure 3.23: Setup of the data acquisition system for BELLE sub-systems, except for SVD.

based DAQ system, the total number of FASTBUS crates may be about 40. In addition, a VA1 chip has an analog multiplexed output mechanism for a limited space. As a result, we can not manage the FASTBUS TDC based system for SVD. Because of the analog multiplexed output mechanism of the preamplifier chip, we selected a sampling FADC based DAQ system. For a fast data transfer, a pipelined FADC module is selected. Figure 3.24 shows the arrangement of the DAQ system for SVD. In the system, we have four VME crates for Halny FADC modules (FADC crate) and one for DAQ control (local control crate). In each of the four FADC crates, there are eight Halny FADC modules, a WS2126 with one SHARC DSP and a CEBTX (central DAQ interface S-bus card and CPU-7V) which is a transmitter to CDAQ. We may set the WS2126 as a master in readout sequence from Halny FADCs and a slave while the CPU-7V reads from the WS2126 after the completion of readout from FADC modules. In the local control crate, there are one CPU-7V, two WS2126s with two SHARC DSPs, one TDM module and nine TTM modules for readout processing. With the SHARC link, we make connection between an FADC crate and a local control crate.

In this system, we can select two different modes; one is a global run mode and the other is a local run mode. The global run mode is a run state in which all the BELLE detectors are activated, while the local run mode is a localized run state with only SVD in operation. In the global run mode, the digital information data stored in a memory of each FADC module are read by WS2126. After WS2126 reads data from FADCs, the CEBTX reads data in a memory of WS2126 and send them to CDAQ. On the other hand, in the local run mode, WS2126 reads data on FADC modules and transfer them to WS2126 in the control crate via SHARC link.

In constructing the DAQ system, we took into account the following things:

- expected nominal data size from Monte-Carlo simulations, and
- transfer rate of the CEBTX.

We selected four independent DAQ systems for SVD according to these things. As the SVD DAQ system is a distributed system, a program on each SHARC DSP is basically the same one. In addition, each SHARC can run independently so that the bottle neck of transfer speed is defined by the limitation due to CEBTX and data size from the silicon detector system. Figure 3.25 shows a data flow scheme within an FADC crate. SHARC

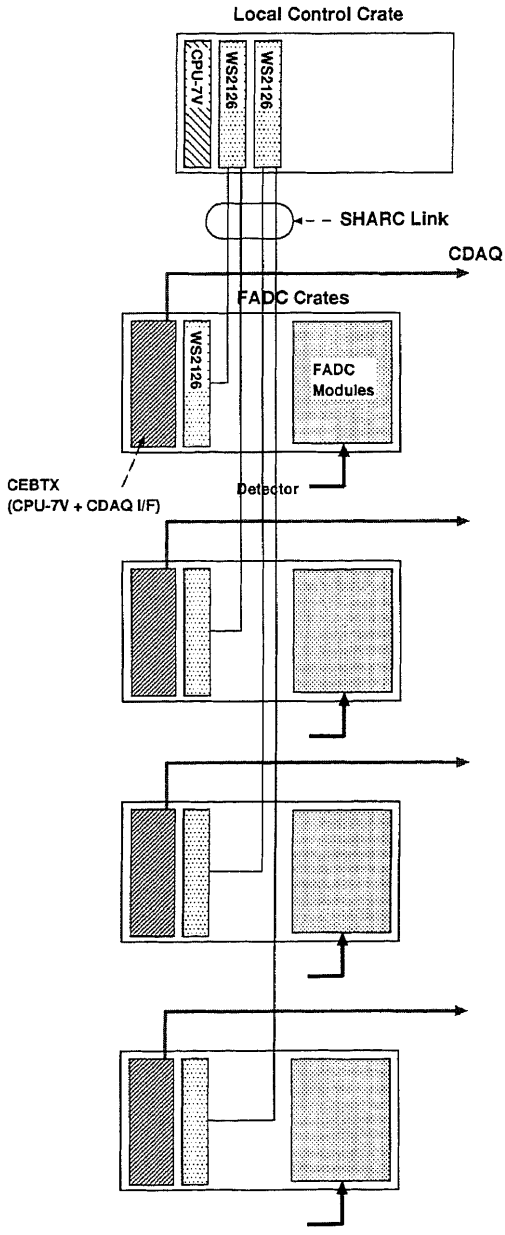


Figure 3.24: Arrangement of the SVD data acquisition system.

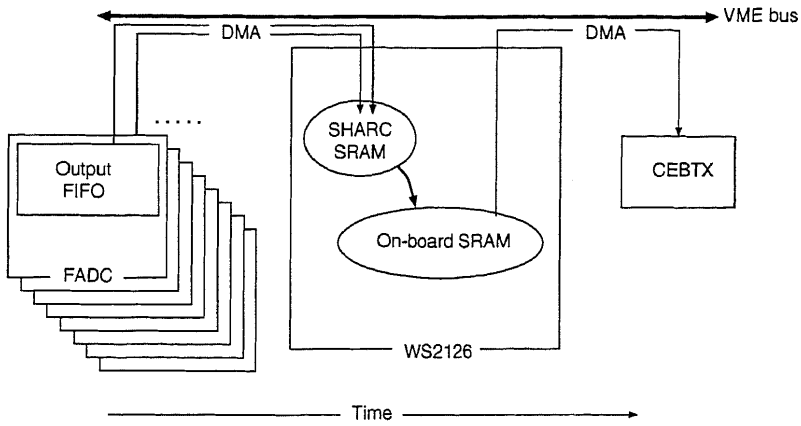


Figure 3.25: Data flow inside the FADC crate.

DSP of type ADSP-21062 has a 2 Mbit on-chip SRAM (static RAM) and WS2126 has an on-board SRAM of 3 Mbyte. The SHARC on-chip SRAM will be used for a buffer to store the FADC data. After completion of storing the data on the memory, the data will be transferred to WS2126 on-board SRAM. After the transfer, the CEBTX will start to read the data from the on-board SRAM. We can not achieve concurrent VME read/write process because WS2126 and CPU-7V uses the same VME bus. Analog signals from the detectors are sent to FADC modules and converted into digital information. Figure 3.26 shows a data flow scheme within a local control crate. Via the SHARC link, the data from each FADC crate are gathered in the link buffer of each SHARC DSP on WS2126. After that, the data will be transferred to the on-chip SRAM of SHARC DSP. Then the whole data are stored in each on-board memory of WS2126. When the WS2126 finishes storing data, CPU-7V starts to read from each on-board memory via VME bus.

Since all the sub-detector DAQ systems in BELLE must be executed synchronously, a synchronous run-control system is required. Figure 3.27 shows a schematic diagram of the run-control system for the BELLE SVD DAQ system. In the global run mode, the run-control commands are asserted from the central run-control system developed by CDAQ group. In the SVD DAQ system, a run-control interface program which runs on a CPU-7V in the local control crate receives control commands from the central control system via TCP/IP network with the help of network shared memory (NSM) [28].

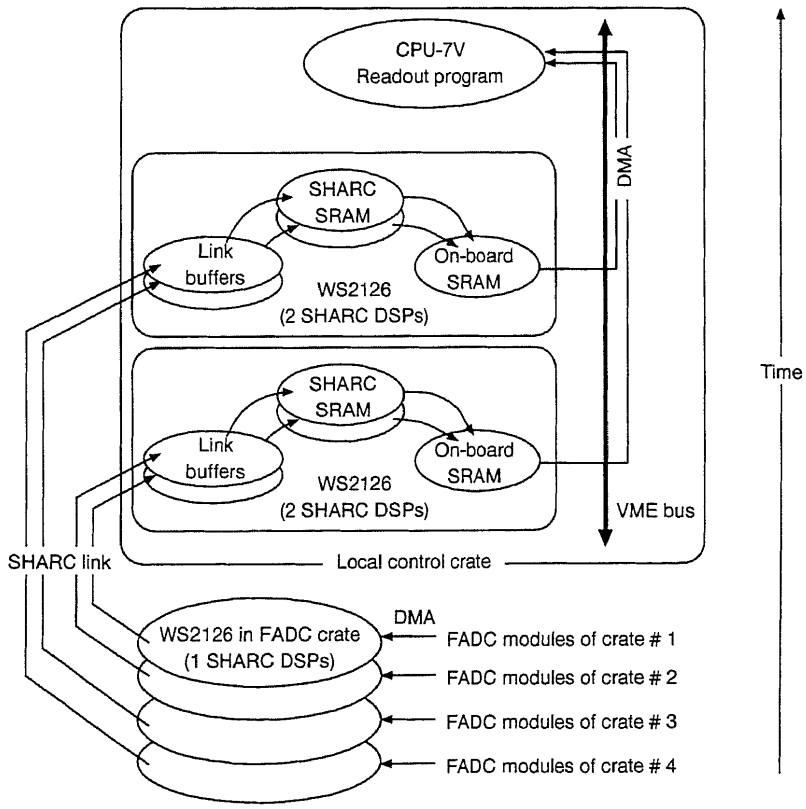


Figure 3.26: Data flow inside the local control crate.

The NSM is a package of a library and a daemon that provides easy-to-use functions of inter-processor shared memory and message passing over a TCP/IP based local area network. After the interface program receives a

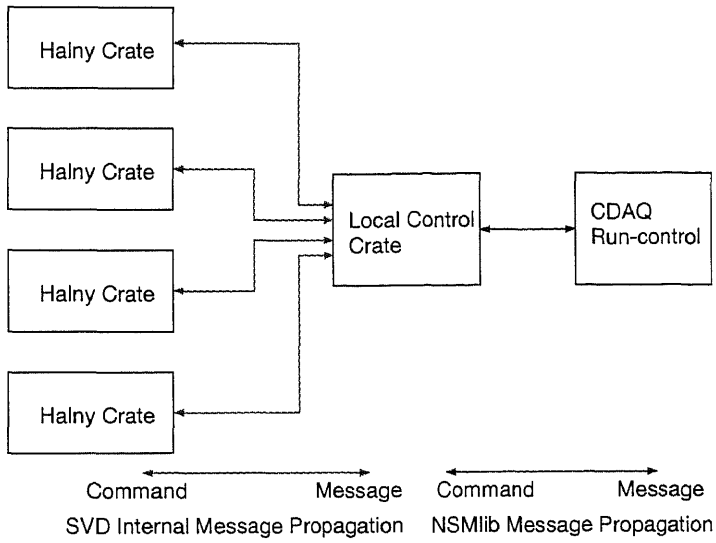


Figure 3.27: Schematic diagram of the run-control system for the BELLE SVD DAQ system.

run-control command, the following tasks are done:

1. The command is distributed to a CPU-7V in each FADC crate via a TCP/IP network with the help of the SVD internal message transfer program developed by SVD DAQ group.

2. After a CPU-7V in each FADC crate receives the command, the CPU-7V sends a message of run-status to the CPU-7V in the local control crate.

3. According to the messages from every CPU-7V in FADC crates, the CPU-7V sends a message of the whole SVD DAQ system run-status to the CDAQ run control system.

The run-control for the SVD DAQ system in the local run mode is also realized by the SVD internal message transfer program. The message-transfer mechanism itself is the same as the mechanism in the global run mode except

for the use of the message transfer program by the NSM between CPU-7V in the local control crate and the CDAQ run-control system.

Figure 3.28 shows a state diagram of the run-control system in the global run mode. In this figure, *base*, *set*, *run*, *daq_reset* and *daq_greset* are actions to be done during state transitions. Relations between the run-control commands and actions at the SVD DAQ system are listed in Table 3.6. Before the data acquisition, the DAQ system is set in the ground state. Status of the DAQ system will be changed according to the commands from the CDAQ run-control system.

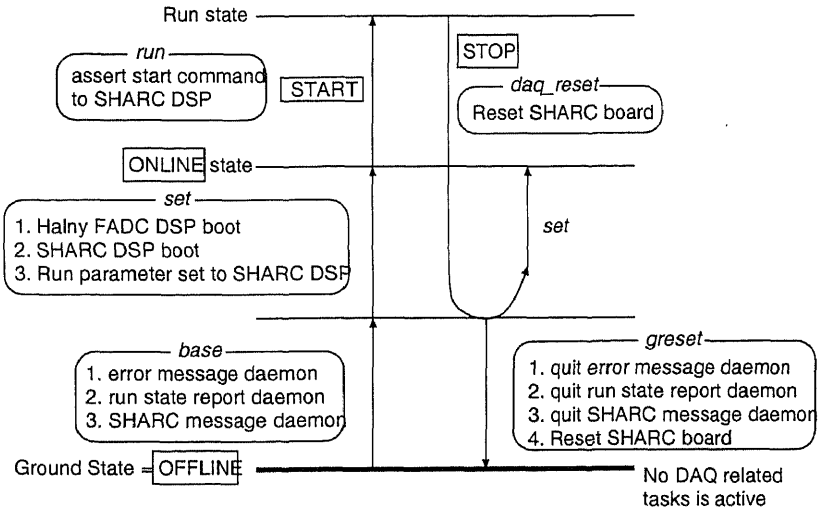


Figure 3.28: State diagram of the run-control system for the BELLE SVD DAQ system.

Since the DAQ program was made of many sub-programs, we must type many commands in executing. To avoid inconvenience for routine workers, we have been developing the GUI-based run control system.

3.6 Buffer management system in the data acquisition

In developing the data acquisition program, we need a pipeline-buffer system or a buffer management system for smooth operation in transferring data.

Table 3.6: Relations between the run control commands from CDAQ and the actions at the SVD DAQ system.

CDAQ control command	Action at the SVD DAQ system
ONLINE	*base* + *set*
START	*run*
STOP	*daq_reset* + *set*
OFFLINE	*daq_reset* + *greset*
SYSTEMRESET	(*daq_reset* +) *greset*

The buffer management system was made in the program which runs on a SHARC DSP in the SVD DAQ system with the help of a circular-buffer method. A typical concept of the circular-buffer is shown in Fig. 3.29. The

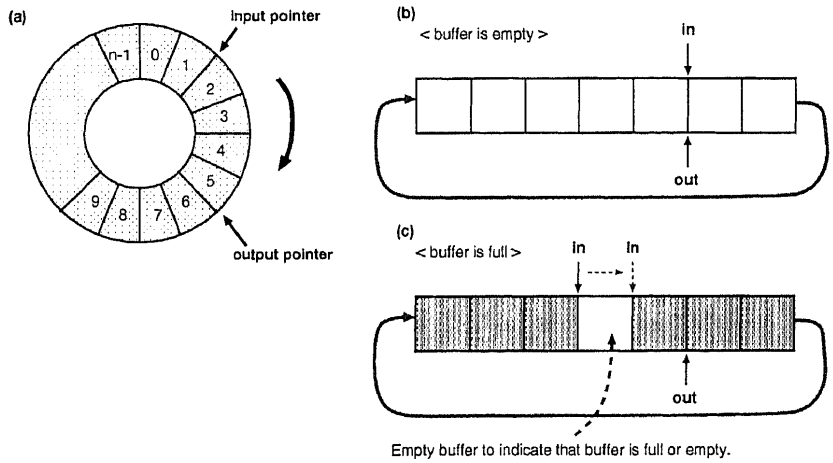


Figure 3.29: Typical concept of a circular-buffer. (a) shows a ring type circular-buffer. (b) and (c) show empty and full status of circular-buffer, respectively.

circular-buffer is segmented into n. One event data are stored in one segment, except a case in which the data length is bigger than the maximum length of the segment. In this figure, the input and output pointers tell the input and output positions to *producer* and *consumer* processes, respectively. The

transferred data to the buffer are inputted to the segment which is indicated by the input pointer. On the other hand, the position of a segment which has data to be sent out of the buffer is indicated by the output pointer.

For manipulating the circular-buffer, a status of the buffer must be checked in each access in order to avoid overwriting. We need to know which segment to be written/read and whether the buffer is accessible or not. To distinguish empty or full status from the indicated position by the input and output pointers, an empty buffer segment is adopted between the newest data segment and the oldest data segment. As shown in Fig. 3.29 (b), the input and output pointers indicate the same segment when the buffer is empty. On the other hand, as shown in Fig. 3.29 (c), the input pointer, which indicates the segment position to be inputted, moves to the previous position of what the output pointer indicates. Thus, these two statuses are distinguished as follows:

$$\text{if } out - in = 0, \text{ buffer is empty}$$

and

$$\text{if } out - in = 1, \text{ buffer is full,}$$

where in and out are the input and output pointers, respectively. While $out - in \neq 1$, the buffer is writable, and while $out - in \neq 0$, the buffer is readable.

A preliminary circular-buffer system was made in a program which runs on CPU-5V with a UNIX system (Solaris 2.4). Performance of the system is not so good because the buffer was assigned in the VME memory module. The VME access speed from CPU-5V in the short length (less than a few kbytes) data transfer is much slower than that in the longer length (more than 50 kbytes) data transfer [29]. In addition, the UNIX system is not a real-time system but a multi-task system. If the number of tasks in a processor increases, the performance of each task becomes poorer with the UNIX system. After this development, the similar system was made in a program on a SHARC DSP. The performance of the system itself was more or less acceptable. But in the construction phase of the SVD DAQ system, we could not implement the circular-buffer system in the SHARC program. The reasons for this are as follows:

- Program on SHARC DSP itself is basically a sequential program. We concluded that there are not so great advantages in the circular-buffer system in the sequential processes.

- We have an interrupt method for the multi-task system on a SHARC DSP, but it was hard to make use of it in a limited time.
- The Halny FADC module has the mechanism of a buffer management system with two FIFOs. There was no requirement to make another buffer management system on a SHARC DSP.

As a result, we did not implement the buffer management system in a program on a SHARC DSP.

3.7 Estimated transfer rate for the BELLE SVD DAQ system

The average transfer rate was estimated by a BELLE Monte-Carlo simulator, GSIM. GSIM is written on the framework of GEANT detector simulation code [30].

When we consider a transfer rate, we must take into account the trigger rate. In BELLE, we plan to implement two categories of triggers: track triggers and calorimeter-energy triggers [4]. These two triggers rely on independent information derived from different detector components, thus providing redundant triggers. The following two redundant triggers are base-line trigger conditions for BELLE:

- track trigger: two or more tracks with $p_t \geq 0.3$ GeV/c in the detector acceptance ($17° < \theta < 150°$), and
- calorimeter trigger: total energy deposit greater than a threshold value of 2 GeV.

With these conditions, the trigger rate for physics processes will be $\sim$ 100 Hz. In BELLE, the mean trigger rate must be kept lower than 500 Hz. The contents of events from e^+e^- collisions are listed in Table 3.7 [4].

In the BELLE SVD system, we have 64 double-sided hybrids. An output of each side of a hybrid is connected to one channel of an FADC module. Thus we have 128 readout sides for all the hybrids. Since on each side there are 5 VA1 chips, we have 640 readout channels on one side of each hybrid. As a result, the total strip number is $640 \times 128 \simeq 82{,}000$. The number of sides of hybrids in one FADC crate is $128/4 = 32$, where the denominator

Table 3.7: Total cross section and trigger rate with $\mathcal{L} = 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ from various physics processes at the $\Upsilon(4S)$: [(a)]pre-scaled by 1/100, [(b)]with restricted condition ($p_t \geq 0.3$ GeV/c).

Physics process	Cross section (nb)	Rate (Hz)
$\Upsilon(4S) \to B\overline{B}$	1.2	12.
Hadron production from continuum	2.8	28.
$\mu^+\mu^- + \tau^+\tau^-$	1.6	16.
Bhabha ($\theta_{lab} \geq 17°$)	44	4.4 [(a)]
$\gamma\gamma$ ($\theta_{lab} \geq 17°$)	2.4	0.24 [(a)]
2γ processes ($\theta_{lab} \geq 17°, p_t \geq 0.1$ GeV)	$\sim$ 15	$\sim$ 35 [(b)]
Total	$\sim$ 67	$\sim$ 96

4 is the number of FADC crates which we use. As one FADC module has four channels, the number of FADC modules in one FADC crate is 32/4 = 8. The number of strips per FADC module is 4 × 640 = 2,560. Therefore the number of strips per FADC crate is 8 × 2,560 = 20,480.

The occupancies for physics and beam background events according to GSIM simulations are listed in Table 3.8 [10, 31]. In this table, the event rate of a physics event is set 100 Hz according to the total trigger rate listed in Table 3.7. In this estimation, it is assumed that one hit cluster includes data from the hit strips and four neighboring strips. An example of clustering is shown in Fig. 3.30. In this figure, signals of the three middle channels are

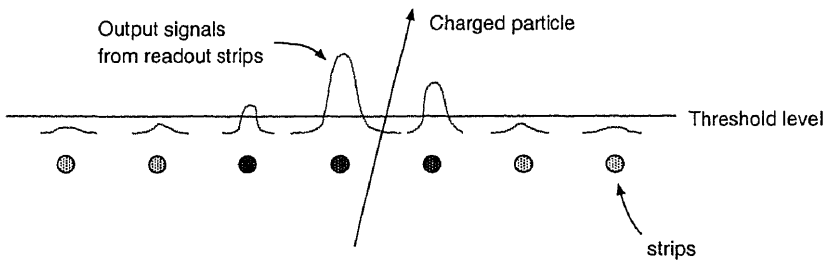


Figure 3.30: Schematic view of signals from each strip when a charged particle penetrates the silicon detector. For vertex reconstruction, we may include some neighboring strips of hit channels.

higher than the threshold level. The data of these strips are read. Besides, the neighboring strips of the hit strips are also read as additional information for vertex reconstruction. In this simulation, two neighboring strips on both sides of the hit strips are included as readout data.

Table 3.8: Estimated occupancy by a Monte-Carlo simulation, GSIM.

	Event rate	Occupancy
Physics events	100 Hz	2.2 %
Beam background events	400 Hz	6.2 % (worst case)

In physics events (background events), the number of hit strips per FADC crate is:

$$20,480 \times 0.022\,(0.062) \simeq 450\,(1270).$$

If we assume that the data size per strip is 4 bytes, then the data size per FADC crate is:

$$450\,(1270) \times 4 \simeq 1.76\,(4.96) \text{ kbytes}.$$

In this calculation, we used the following relation of 1 k $= 2^{10} = 1024$ used in the computational manipulation. If the event rate is 100 Hz (400 Hz), then the transfer rate per FADC crate is:

$$1.76\,(4.96)\text{ (kbytes)} \times 100\,(400)\text{ (Hz)} \simeq 0.172\,(1.94)\text{ MB/s}.$$

Table 3.9: Estimated transfer rate from GSIM in physics events and beam background events.

Physics events	0.172 MB/s
Beam background events	1.94 MB/s

We summarized the transfer rates in Table 3.9. The transfer rate of CEBTX has been measured to be about 3.6 MB/s in a FASTBUS TDC-based DAQ system which the other sub-detector groups will use [32]. Therefore, the simulation results indicate that we can operate the DAQ system of BELLE SVD in these cases assumed in the simulations.

Chapter 4

Background Effects in BELLE SVD

In a real experiment, there are hit channels on DSSD from several concurrent events caused by:

- e^+e^- beam collision (real events),
- electric noises in readout electronics and DSSDs, and
- beam background.

In estimating the real number of hits, the beam background is one of the most important components. In general, beam background events are generated from:

- coulomb scattering processes between the electron (positron) beam and residual gases, and
- bremsstrahlung processes.

We have several event generators (qq, beam background generator and so on). Among these generators, we selected *beam background event generator* [33] to estimate the number of hit channels due to the beam background. With GSIM, beam background effects were studied in the previous design of BELLE SVD [34]. In the current design, the geometry is different from that of the previous design. So far as DAQ is concerned, it is required to estimate approximately the total data size. For this purpose, the number

of hit channels from beam background events was estimated in various different conditions. We have several parameters to operate the SVD system configuration (threshold levels of analog signals, cluster size of hit strips etc.). Varying these parameters, we could study how many channels are hit and which detector unit is the busiest and so on. In this simulation study, the following items were estimated:

- beam background effect,
- electric noise effect,
- occupancies for various threshold levels,
- occupancies for various cluster sizes, and
- single threshold cut and Halny emulation cut.

Halny emulation of this list is the emulation mode for Halny multiple threshold sparsification code.

In a real experiment, particles with different transverse momenta (p_t) will penetrate DSSDs. As shown in Fig. 4.1, a particle with high p_t penetrates DSSD with a near right angle, whereas a particle with low p_t penetrates it with a small angle. This means that high p_t particles make narrow clusters and large analog outputs, whereas low p_t particles make wide clusters and small analog outputs. It is very desirable to accumulate as wide varieties of physics events as possible in an experiment. From this point of view, we must detect both types of signals. For this purpose, we set multiple thresholds for sparsification. Details of this sparsification will be discussed in Appendix D.

Two thresholds are set as follows:

$$\text{thrs1} = a \times (\text{rms noise}), \tag{4.1}$$

$$\text{thrs2} = \sqrt{n} \times \text{thrs1}, \tag{4.2}$$

where thrs1 and thrs2 are threshold levels for the comparison of a single-strip signal and the sum of n strip signals, respectively. First we compare a signal in each strip with thrs1, and if it exceeds thrs1, the strip signal is included as data. Second the sum of each n neighboring strip signals is compared with thrs2, and if it exceeds thrs2, these strip data are also included. In a nominal case, we set a = 4.0 and n = 2. With this method, we can pick up hit channels from physics events as many as desired.

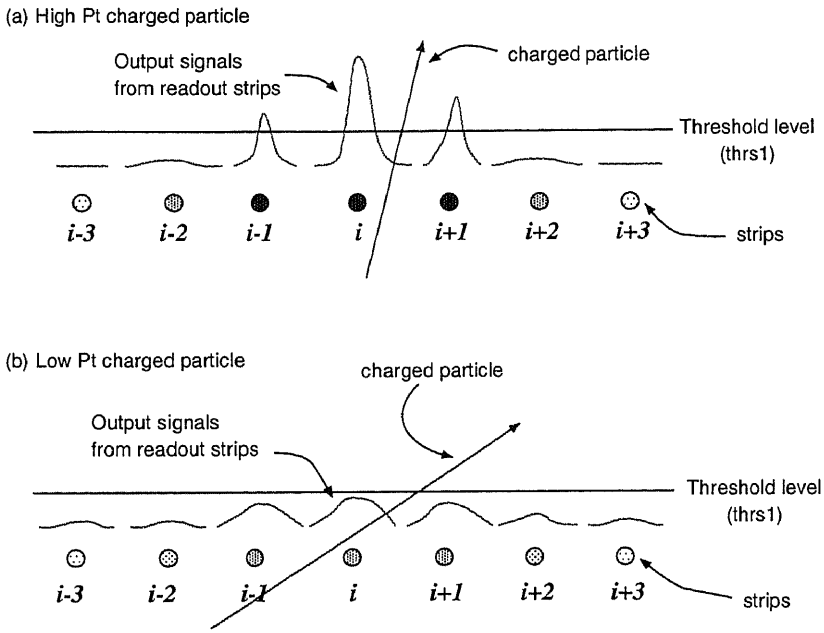


Figure 4.1: Penetrating particles with (a) high transverse momentum and (b) low transverse momentum.

4.1 Beam background effect

Most of beam background events are randomized events. Statistically, a Poisson distribution is formed from random events.

Since beam background events are continual, we must define a time window to include them. Figure 4.2 shows the mean occupancy as a function of beam background time window. In this simulation study, an electric noise

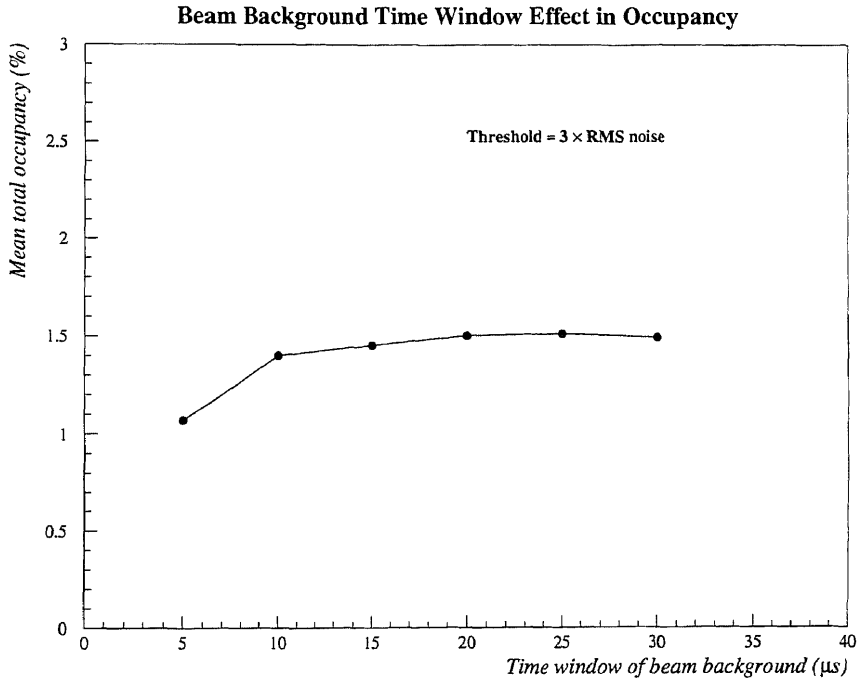


Figure 4.2: Beam background time window effect in occupancy.

effect was included. The electric noise effect was included through the simulation studies if there is no explanation. In this figure, there is no significant increase in occupancy for the time window over 20 μs.

In the real readout sequence, the peaking time of a VA1 chip is 2.5 μs. In the following simulations, the time window of 5.0 μs (2 $\times$ peaking time of VA1) is used.

4.2 Electric noise effect

Electric noises are one of the most significant parameters in signal handling. In GSIM, we can select whether electric noises are included or not. Before starting a simulation, it is very useful to know the magnitude of effects of electric noises in GSIM.

In this simulation, we evaluated two cases with and without electric noises by varying the threshold level. Figure 4.3 shows the total hit channel distributions (a) with and (b) without electric noises as a function of threshold level.

In GSIM, a hit distribution from electric noises is essentially Gaussian, whereas the beam background has a Poisson distribution. The reason for the Poisson distribution is that beam background events are almost random events. Statistically speaking, a Poisson distribution is formed from random events with a small mean value.

4.3 Occupancies for various threshold levels

In this study, we set a cluster size (the total number of neighboring strips at the both ends of hit strips) to be 4. We used realistic and ideal signals from VA1 preamplifier chips. The difference between the realistic and ideal signal cases was whether the base line instability after a hit was included or not. Figure 4.4 shows occupancies vs. several threshold levels. From this figure, we could not find any significant difference between ideal and realistic signal shapes. In the following sections, the realistic signal shape is used as outputs from VA1 preamplifier chips. In the single threshold cut, a nominal threshold value is 3 $\times$ rms noise. In this figure, the occupancy at this threshold is about 1 %. According to $B\overline{B}$ event simulation [10], the occupancy from this type of events is about 2.2 %. Therefore, the total occupancy will be about 3 %. We note that this is just an expected mean value because we can not predict accurately the maximum background rate.

4.4 Occupancies for various cluster sizes

The cluster size is one of the important ingredients to estimate a data size. In this simulation study, a cluster size setup is controlled by the side logic number setup. The side logic number indicates how many neighboring strips

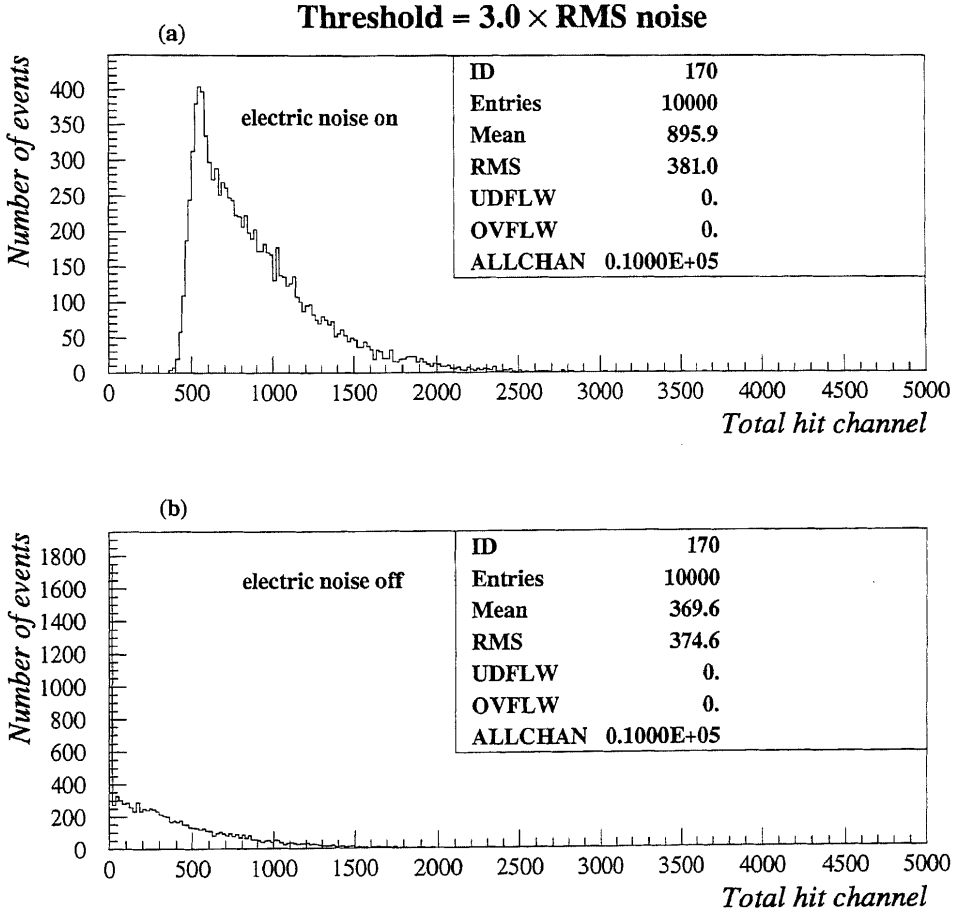


Figure 4.3: Distribution of the number of total hit channels (a) with and (b) without electric noises.

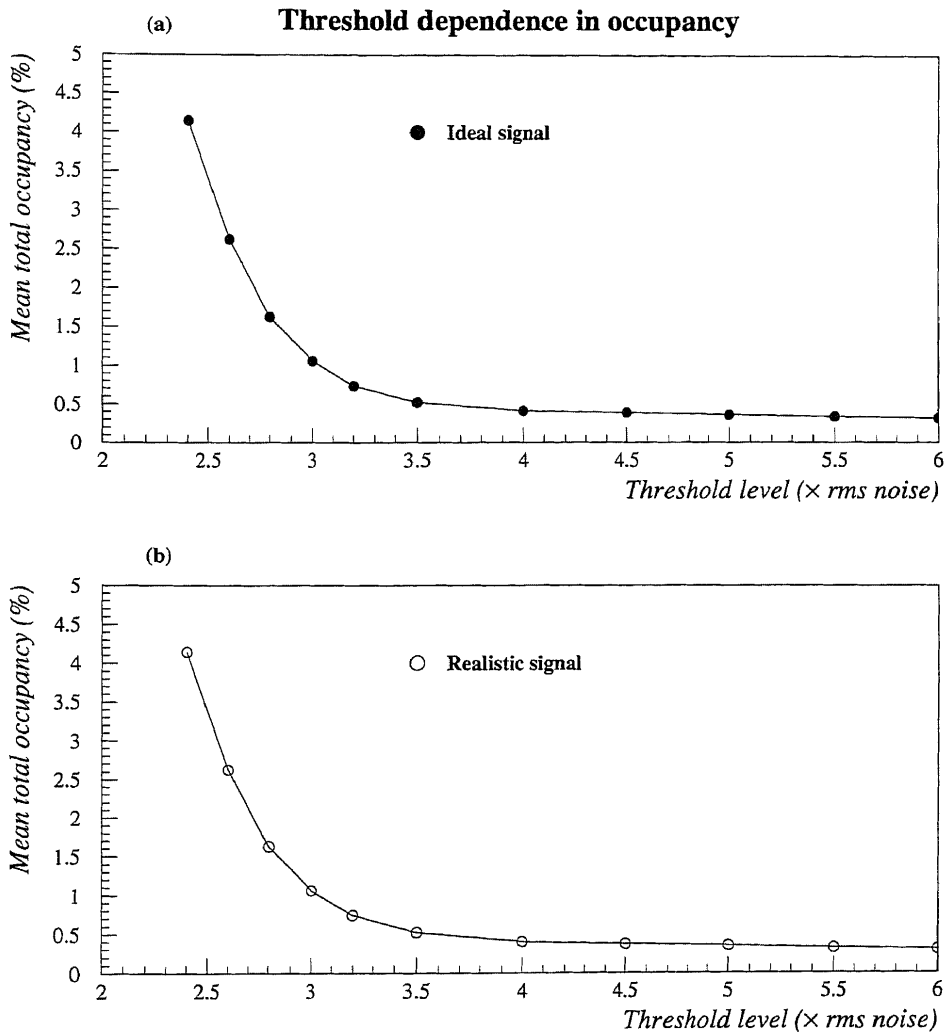


Figure 4.4: Distribution of the mean total occupancy as a function of threshold levels of analog signals from VA1 chips for (a) ideal and (b) realistic signal shapes.

in each side of the hit cluster are included in data. The cluster size is defined by the total number of neighboring strips included as follows:

$$\text{(cluster size)} = 2 \times \text{(side logic number)}.$$

Figure 4.5 shows occupancies vs. side logic number. This figure indicates

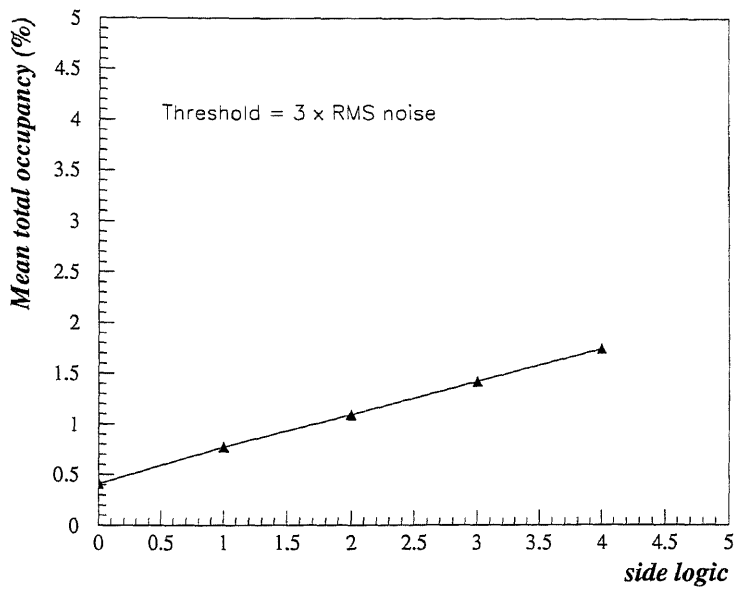


Figure 4.5: Occupancies vs. side logic number.

that the occupancy increases with the cluster size. In a real experiment, we may readout neighboring channels for information to reconstruct tracks of charged particles. We may want information as much as possible, but from the point of view of DAQ, we may not be able to handle a large amount of data at a 500 Hz trigger rate. This result helps us to choose a proper cluster size for the BELLE SVD DAQ system.

4.5 Single threshold and multiple threshold cuts

From the viewpoint of physics analysis, we want to accept hit channels as many as possible, but to reject background hit channels as effectively as possible. As mentioned earlier, in a real experiment, it is hard to realize this situation with a single threshold cut. To pick up real hits from physics events, Halny FADC modules in the SVD DAQ system utilize a multiple threshold cut method. This program is a data sparsification code for SVD. It runs on each DSP of the Halny FADC module. In this sparsification run, offset and rms noise values are updated in each event [40].

In a GSIM simulation study, the Halny FADC sparsification code was used. In this simulation, the two threshold values shown before are used. Figure 4.6 shows the difference of the occupancies from beam background events and electric noises between the single threshold and multiple threshold (Halny emulation) cuts as a function of threshold value. In the Halny emulation mode, a pulse height in each strip is compared with *thrs1* and hit strips are picked up first. Second, the sum value of pulse heights of every two adjacent strips is compared with *thrs2* and hit strips are also picked up. (*thrs1* and *thrs2* are defined by Eqs. 4.1 and 4.2, respectively.)

In the results shown in Fig. 4.6, the occupancy from the beam background is about 0.65 % in Halny emulation with $thrs1 = 4.0 \times$ rms noise and $thrs2 = 5.7$ $(4 \times \sqrt{2}) \times$ rms noise. On the other hand, in the single threshold cut with 3.0 $\times$ rms noise, the occupancy from beam background is about 1.1 %. Concerning the beam background occupancy, the Halny emulation case is less than the single threshold case. For physics events ($\Upsilon(4S) \rightarrow B\overline{B}$), the occupancy in the Halny emulation mode is larger than that in the single threshold cut [31]. From these results, we could conclude that the Halny emulation mode case with $thrs1 = 4.0$ and $thrs2 = 5.7 \times$ rms noise is better than the single threshold cut case with 3.0 $\times$ rms noise for physics analyses. We note that this is just a result from the Monte Carlo simulation and that the real case can be much different.

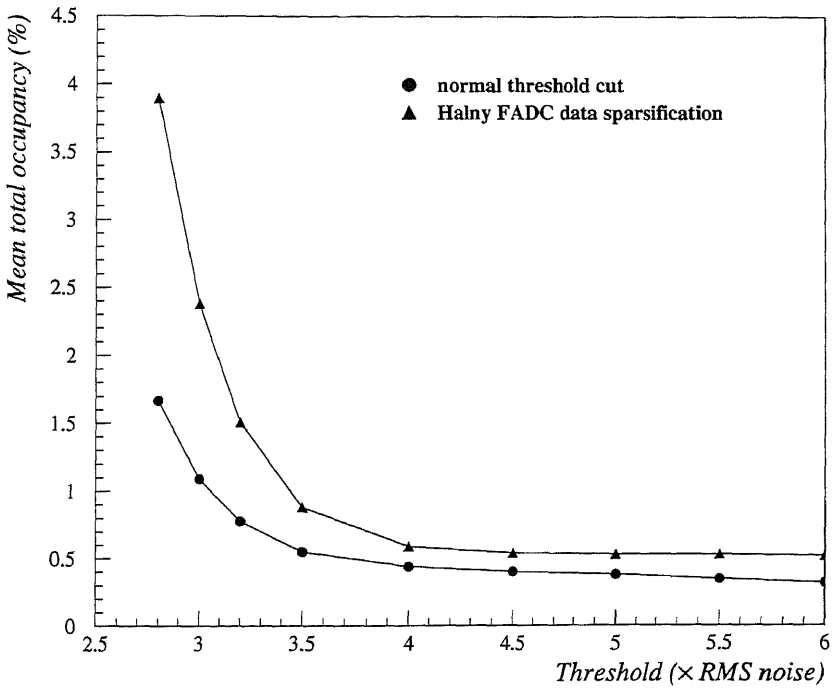


Figure 4.6: Occupancy distributions for the single threshold cut and Halny FADC sparsification as a function of threshold level.

Chapter 5

System Test for BELLE SVD

In October and November 1998, we tested the readout performance of a setup with the whole BELLE SVD components. The purposes of this test were as follows:

- check of readout sequence of real SVD,
- performance check of the DAQ system for SVD, and
- demonstration of hit track reconstruction from detected signals.

5.1 Performance check of the SVD DAQ system

We made the following performance tests of the SVD DAQ system:

- transfer rate of the system, and
- dead-time of the system.

5.1.1 Transfer rate measurement

We measured the transfer rate on the VME bus and SHARC link. As explained in Section 3.5, our DAQ system uses not only VME bus but also SHARC link. This SHARC link is a key in the local run mode. We measured individual transfer rates of WS2126 on VME bus. Figure 5.1 shows a typical VME transfer time of WS2126 with a Halny FADC module as a

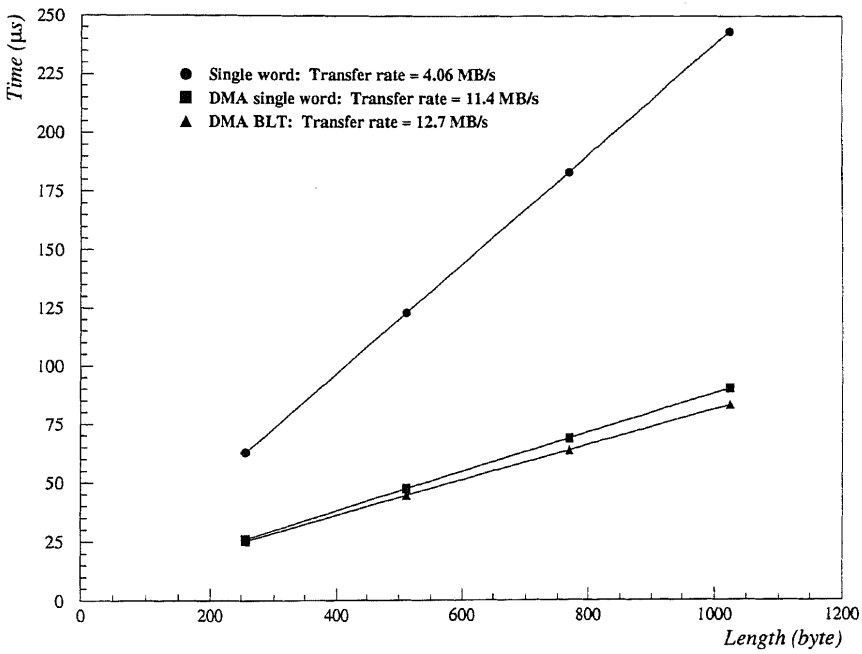


Figure 5.1: Typical VME transfer rate of WS2126 with a Halny FADC module as a VME slave.

VME slave as a function of data size to be transferred. In the single word transfer case, we obtained 4.06 MB/s. We also obtained 11.4 MB/s and 12.7 MB/s in DMA single word transfer and DMA block transfer, respectively.

In the SHARC link transfer, we measured a transfer speed with a simple link transfer program to estimate the basic transfer speed of the link. The transfer time of single word and DMA single word transfer modes of the link as a function of data size is shown in Fig. 5.2. From this measurement, we obtained 9.69 MB/s and 33.7 MB/s in the single word transfer and DMA single word transfer, respectively. The DMA transfer speed is lower than the specification value on the data sheet of the board. We considered this inconsistency was due to the difference of overheads between our link transfer program and that of the manufacturer.

We also measured the transfer speed of link with memory writing. This measurement was done with realistic link transfer in our DAQ system. In this test, the transfer sequence between the transmitter (Tx) and the receiver (Rx) is as follows:

1. Tx sends data length to be transferred in single word transfer.
2. Rx receives data length to be received in single word transfer.
3. Tx sends real data.
4. Rx receives real data.
5. Rx writes the data on an on-board memory on the WS2126.

This sequence was used for both of the transfer modes (single word/DMA). As the on-board memory on the WS2126 is accessible from the VME bus, CEBTX (CPU-7V) can have access to the memory in the DAQ sequence. For this reason, a SHARC DSP transfers data to the on-board memory. Figures 5.3 (a) and (b) show the transfer time as a function of data size which was measured with this sequence without and with writing on the external memory, respectively. We could conclude that the transfer rate in the DMA transfer case shown in Fig. 5.3 (b) was not so fast. Since time for the development of the link transfer program was not sufficient, the program itself was not optimized yet. The transfer rate will be optimized with some modifications if there is enough time to develop. But it was usable for the DAQ system in the local run mode because fast transfer rate was not required in the system.

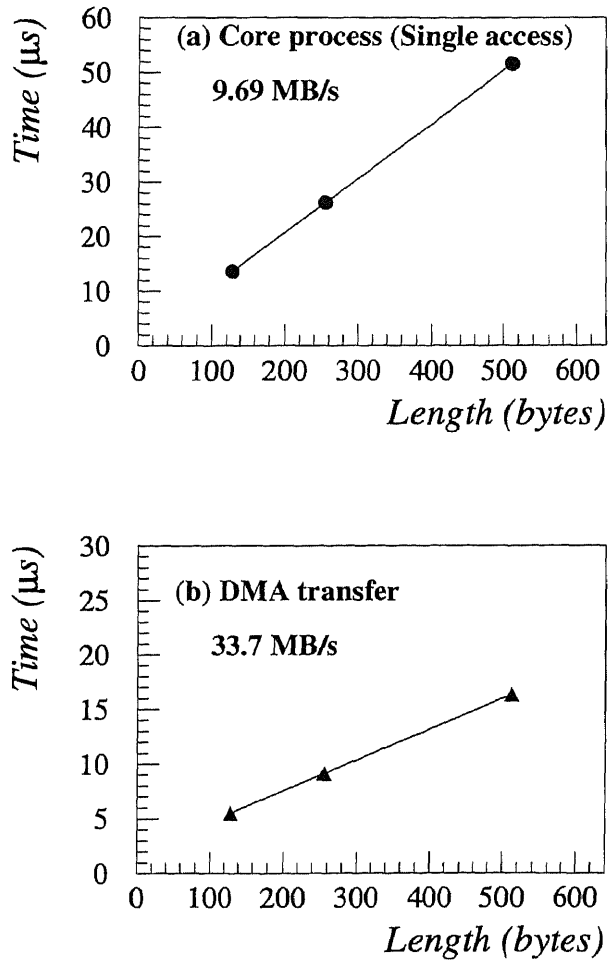


Figure 5.2: Transfer time of SHARC link in (a) single word transfer and (b) DMA single word transfer as a function of data size.

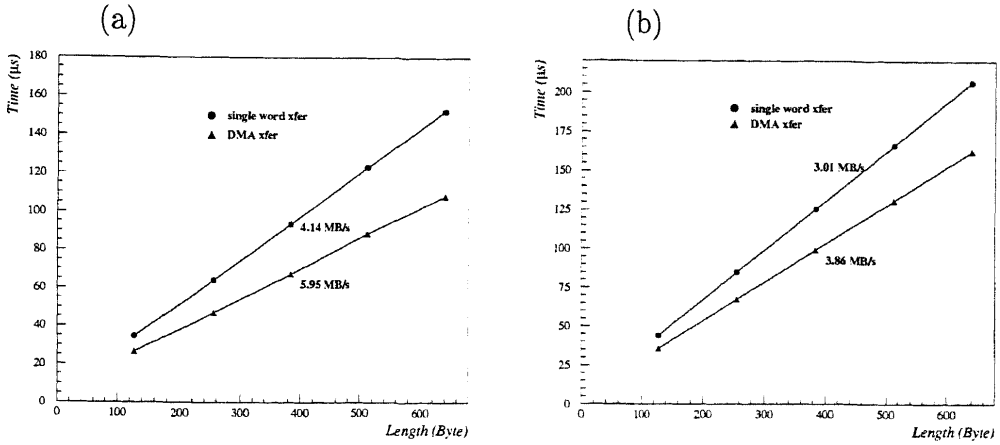


Figure 5.3: Transfer time of SHARC link vs. data size in a realistic transfer method (a) without and (b) with writing on an external memory after receiver SHARC receives data.

5.1.2 Dead-time measurement

The event transfer rate will decrease with the increase of a trigger rate due to the dead time of the readout system. Let r and R be the trigger rates with and without the dead-time, τ, respectively. Then we have the relation:

$$(1 - r\tau)R = r.$$

Rearranging this equation, we obtain the live time fraction:

$$\epsilon \equiv \frac{r}{R} = \frac{1}{1 + R\tau}. \tag{5.1}$$

Using Eq. 5.1, the live time fraction as a function of trigger rate can be calculated. The results are shown in Fig. 5.4. The vertical line in this figure indicates 500 Hz trigger rate. At the 500 Hz trigger rate, the readout system with 100 μs processing time satisfies the requirement of 95 % live time fraction operation, while that with 200 μs processing time does not.

We made a live time fraction measurement with random trigger timing from TDM to evaluate the live time (dead-time) of the BELLE SVD DAQ system. In this test, we use only one FADC crate, which consists of one Sparc CPU-7V, one WS2126 SHARC board and eight Halny FADC modules. WS2126 reads whole channel data from all the FADC modules, and transfer

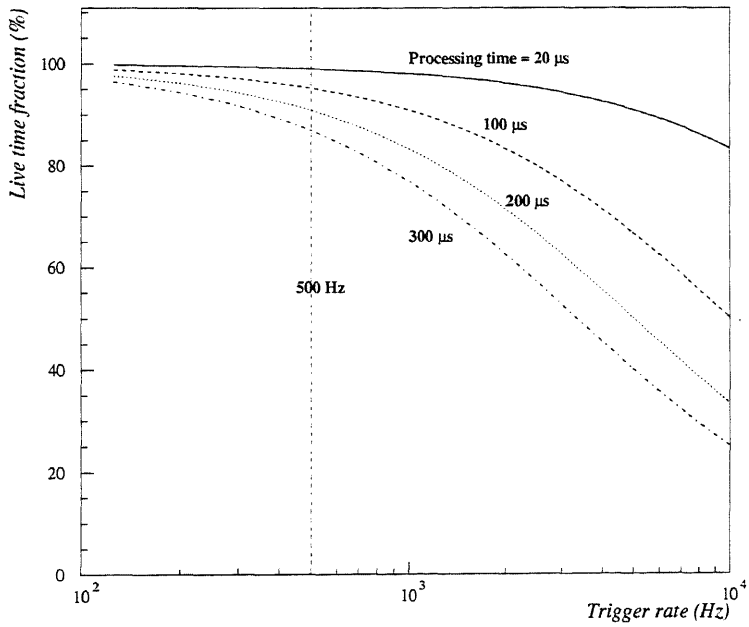


Figure 5.4: Calculated live time fractions as a function of event trigger rate. The vertical line indicates 500 Hz trigger rate.

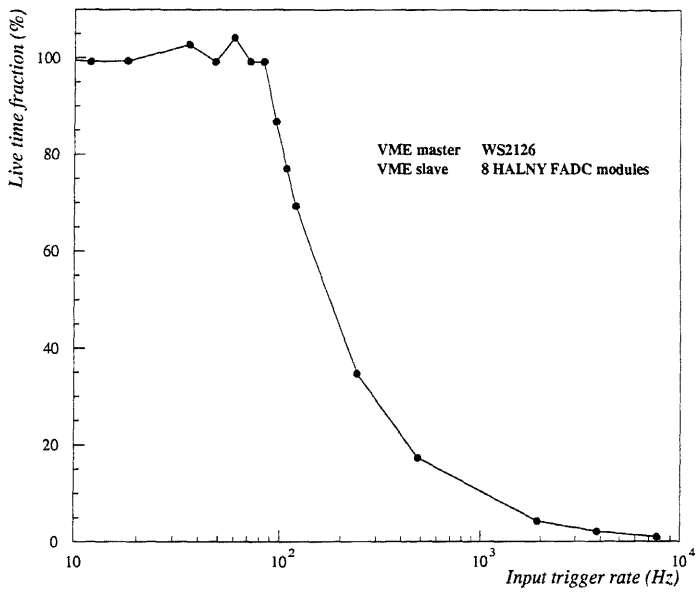


Figure 5.5: Live time fraction for full channel readout in the SVD DAQ system in a case of full channel readout with random trigger timing from TDM.

the data to CPU-7V. The result is shown in Fig. 5.5. In this figure, the live time fraction value in the region smaller than 100 Hz trigger rate was almost 100 %. Although the live time fraction should not exceed 100 %, there are several points of the measured live time fraction over 100 %. This was caused by time jitters of the TDM used in the test. Since the input and output FIFOs in the FADC modules were almost empty, the buffer management system consisting of the two FIFOs acted as a buffer with an infinite depth. On the other hand, the live time fraction value became drastically lower in the region of more than 100 Hz trigger rate. In this case, as the FIFOs had the ultimate size of data at any time, the buffer management system acted as a buffer with a finite depth as shown in Fig. 5.5.

As described in the Section 4.3, the total occupancy with the sparsification method will be about 3 % according to the GSIM simulation study. From this measurement, we can conclude that our DAQ system can run with more than 95 % live time at a 500 Hz trigger rate if we use the sparsification method in the Halny FADC modules.

5.2 Silicon detector test

As a preliminary test before testing real DSSDs, we tested performance of BEAST (**b**eam **e**xorcism for **a** **st**able BELLE experiment) silicon detectors with a radioactive source (β source). Figure 5.6 shows the setup of a preliminary test for the BEAST silicon detector. One SHARC VME cluster, WS2126, and one Halny FADC module were used to read data. A typical analog signal output from the BEAST ladder is shown in Fig. 5.7. As the sampling timing of analog signals in Halny FADC was not optimized in this test, a peak ADC value in this figure was less than the charge optimized for a minimum ionizing particle (MIP) ($\sim$ 22,000 e $\simeq$ 180 mV).

Before installing the SVD detector in the BELLE detector, we checked the performance of the real SVD detector system. The system test was done near the end of November 1998. The setup is shown in Fig. 5.8. In this test, preliminary tuning and testing were required, for example optimization of sampling timing of analog signals in Halny FADCs, electrical treatments for ground problem and so on. After solving these problems, we could see cosmic ray events with the real SVD detectors. Figure 5.9 shows typical hit distributions in all the ladders of the SVD detector system with a cosmic ray. The vertical and horizontal axes indicate ADC values from FADC modules

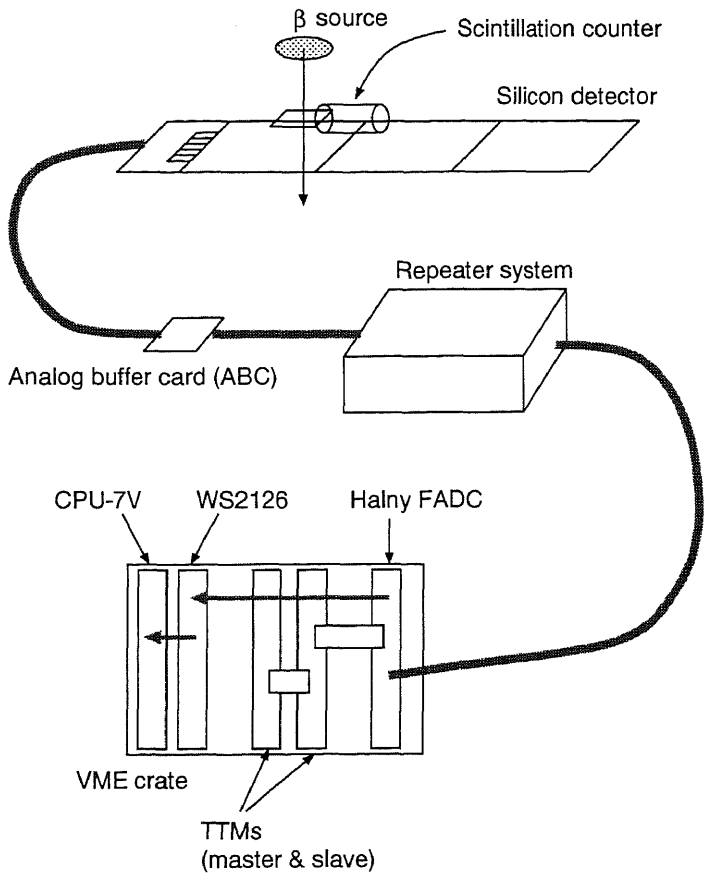


Figure 5.6: Setup of the preliminary test for the BEAST silicon detector with a radioactive source.

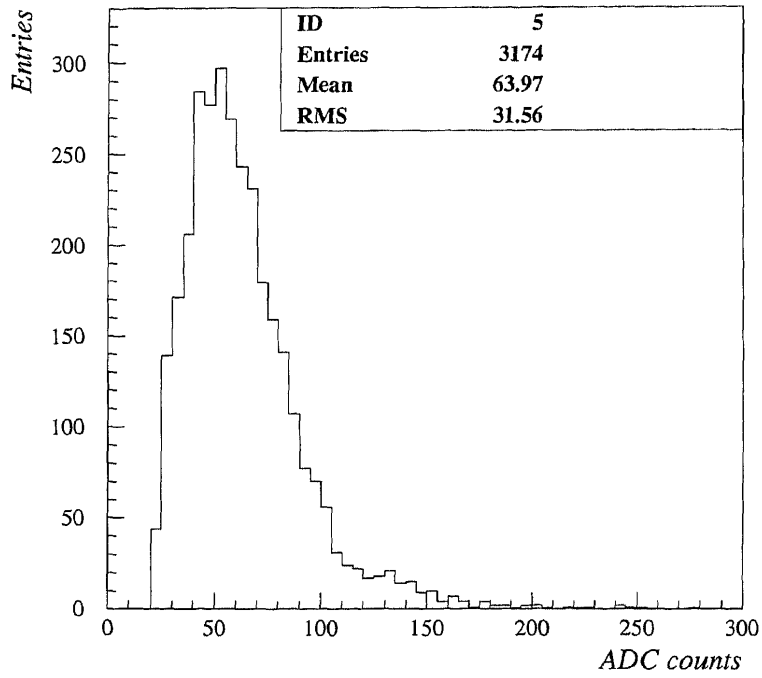


Figure 5.7: Typical ADC count distribution from a BEAST silicon detector with a β source (2 mV/ADC count).

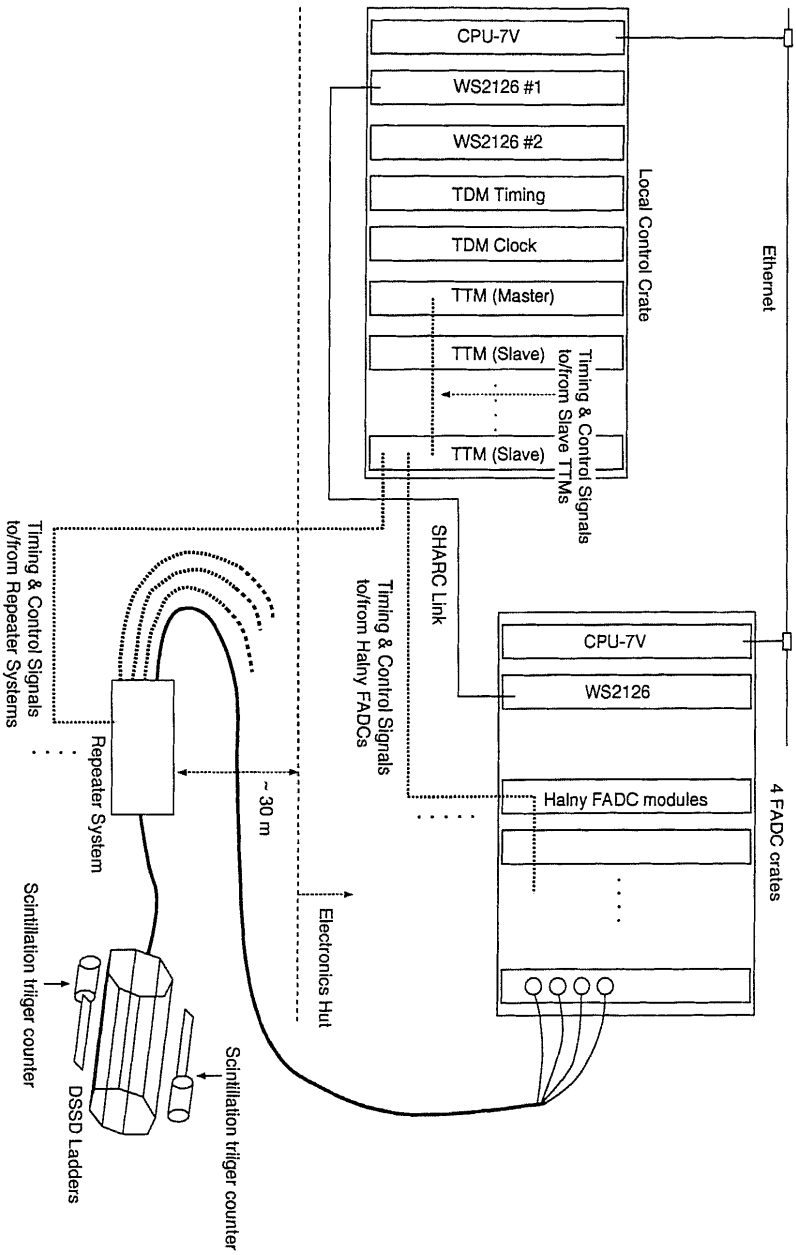


Figure 5.8: Setup for the BELLE SVD system test.

and the channel number, respectively. There are some hit signals in some plots. A typical cosmic ray track reconstructed from hit information of the SVD detectors is shown in Fig. 5.10. In this figure, the numbers at the hit points indicate pulse heights in units of 1000 e^- of the hit strips. In the event display program, the following tasks were done [35]:

1. Find hit channels which exceed the threshold level ($th1$) with noise levels below the reference *noise* level.

2. Find a pair of neighboring channels in which the sum of pulse heights exceeds the other threshold level ($th2$). These pairs are treated as clusters and the center positions of these clusters are defined as hit positions.

In this figure, the values of $th1$, $th2$ and *noise* are chosen to be 5000 e^-, 8000 e^- and 2000 e^-, respectively. [35].

In this event display program, residuals in reconstructing cosmic ray tracks were measured. A schematic view of a residual in the three layers of the silicon detectors is shown in Fig. 5.11. In this figure, the residual of the inner layer is shown. The calculation method of the residual is as follows:

1. draw a reconstructed cosmic ray track by two hit positions in two layers, and

2. measure the distance between the hit position of the remaining layer and the position obtained by extrapolating the line determined by the two other layers.

The residuals of the three layers and the sum of residuals of the three layers are shown in Fig. 5.12. In this figure, we could get the residual distribution with a standard deviation of 42.7 μm as the sum of residuals for the three layers. If we assume the position resolution of each ladder is the same, we get the position resolution of 24.7 $(42.7/\sqrt{3})$ μm. In the real experiment, we determine the positions of the silicon ladders. The position calibration was not done in this test. Although the present measurement was very preliminary, the position resolution obtained can be regarded as acceptable for BELLE SVD to measure vertex points.

We also checked pulse heights and noise levels of each detector in the system test. Figure 5.13 shows distributions of pulse heights of all p-side short half ladders, n-side short half ladders and p-n flipped side half ladders.

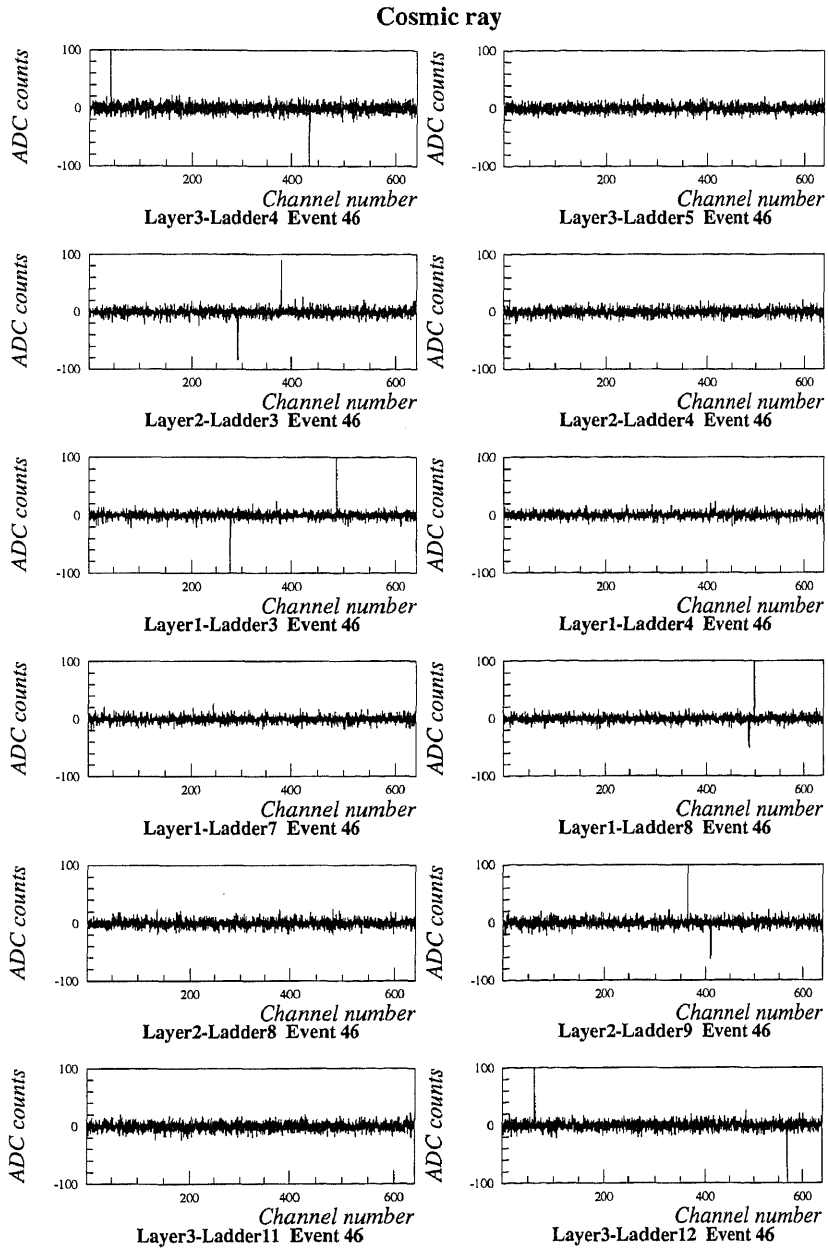


Figure 5.9: Typical hit distributions in the ladders of the SVD detector system with a cosmic ray. The vertical and horizontal axes indicate ADC values from FADC modules and the channel number, respectively. Pulses in these distributions are signals from the cosmic ray. The signals of positive and negative values correspond to the signals on the p-side and n-side, respectively.

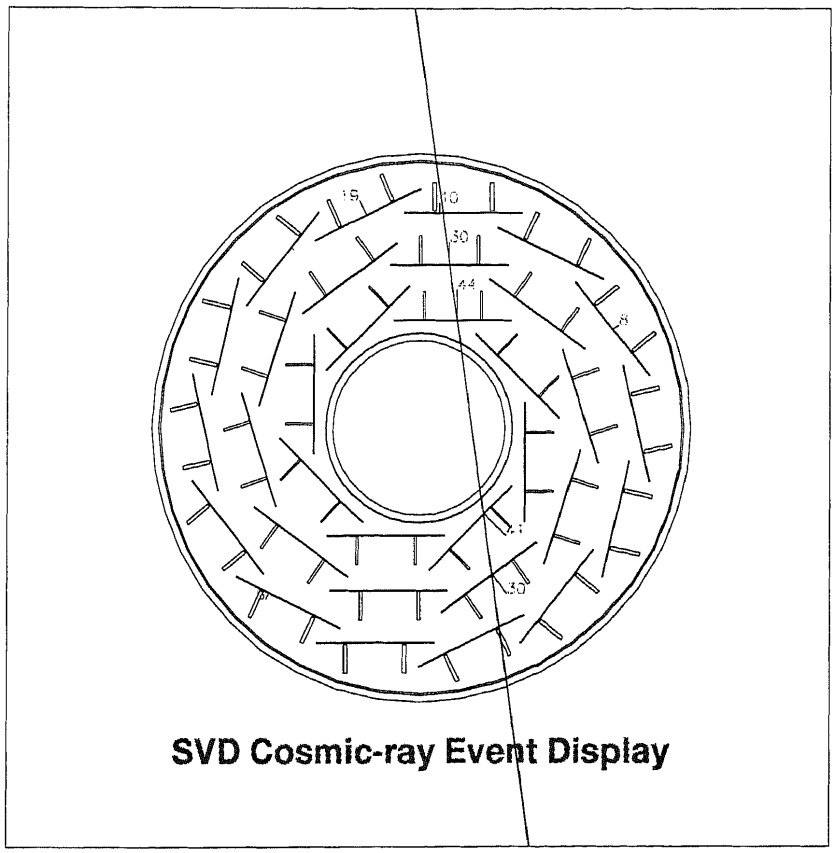


Figure 5.10: Typical reconstructed track in the $r - \phi$ plane by the SVD detector system with a cosmic ray, where the numbers in this figure indicate pulse heights in units of 1000 e^- of the hit strips.

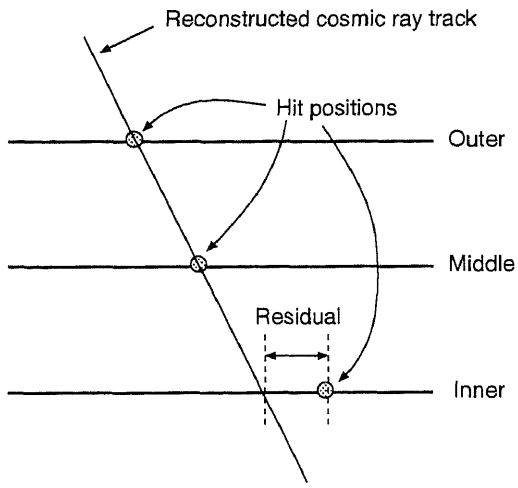


Figure 5.11: Schematic view of a residual in the three layers of the silicon detectors.

In this figure, there are Landau peaks around 20,000 electrons for all the distributions. As the scintillation counters used for a cosmic ray trigger were large, cosmic ray tracks with various incident angles penetrated the detector. Therefore the pulse height distribution was generated by not only MIPs but also by tracks with larger energy deposits than MIPs.

The distributions of the p-side and n-side have pulse height peaks with opposite polarities, whereas the distribution of the p-n flipped side ladder has pulse height peaks with both polarities as expected. The broad pulse height distributions around 0 might be caused by noisy events due to readout electronics problems or noisy channels of the detectors [36]. Figure 5.14 shows distributions of S/N (signal-to-noise ratio) values of each cluster in several ladders in the system test with cosmic rays. The signal is defined by the total charge of each cluster. The horizontal axis corresponds to the S/N ratio of clusters and the vertical axis to the number of clusters. The purpose of these plots is to understand noise characteristics of individual ladders. For example, Fig. 5.14 (a) shows an S/N value distribution of the n-side of the inner layer. The ladders shown in this figure were parallel to the trigger scintillation counters. From this figure, we conclude that we have an S/N ratio around 20 except for the distributions of the p-side of the inner and the backward middle ladders (Fig. 5.14 (b) and (e)) which have peaks around

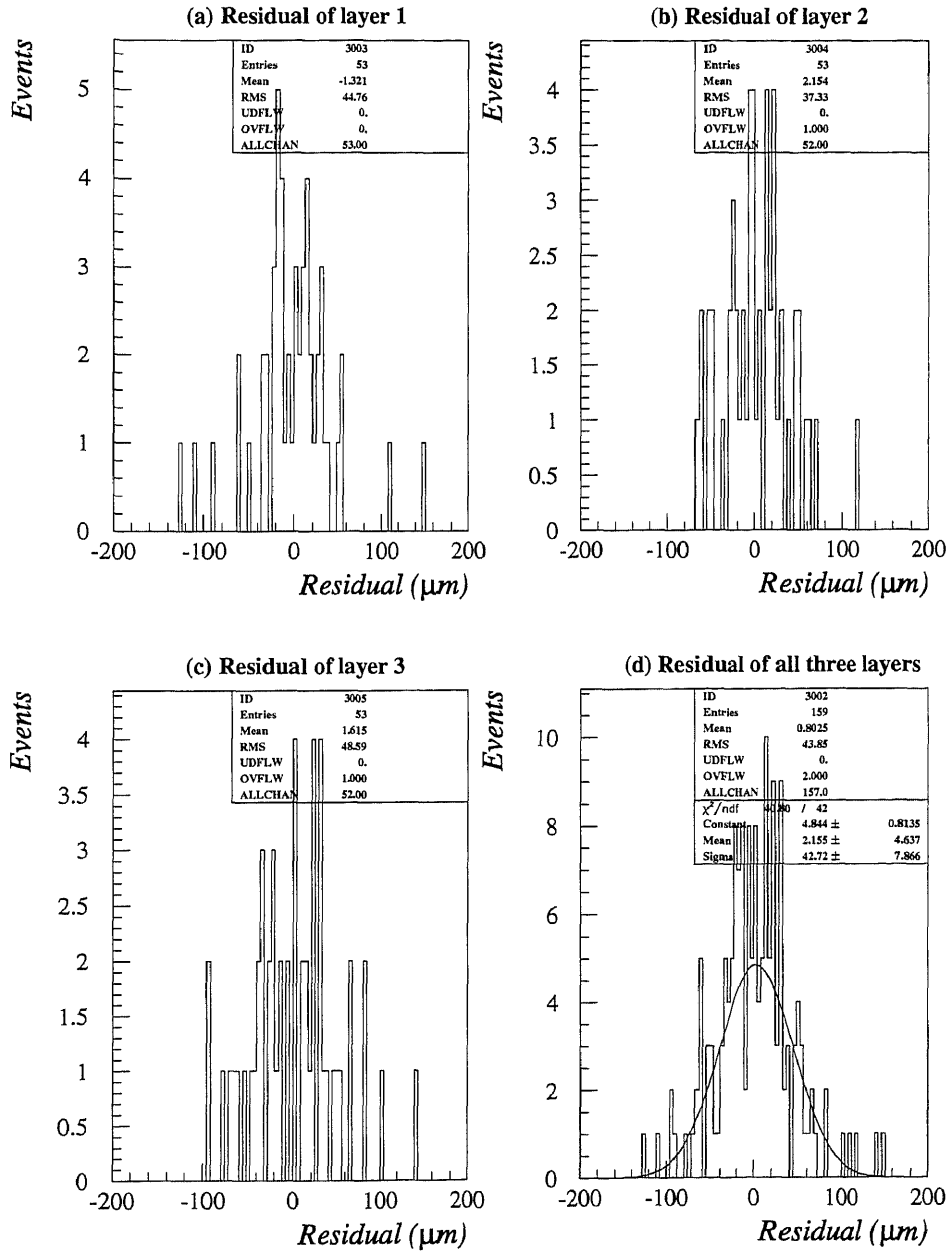


Figure 5.12: Distributions of residuals of (a) layer 1, (b) layer 2, (c) layer 3 and (d) the sum of all three layers.

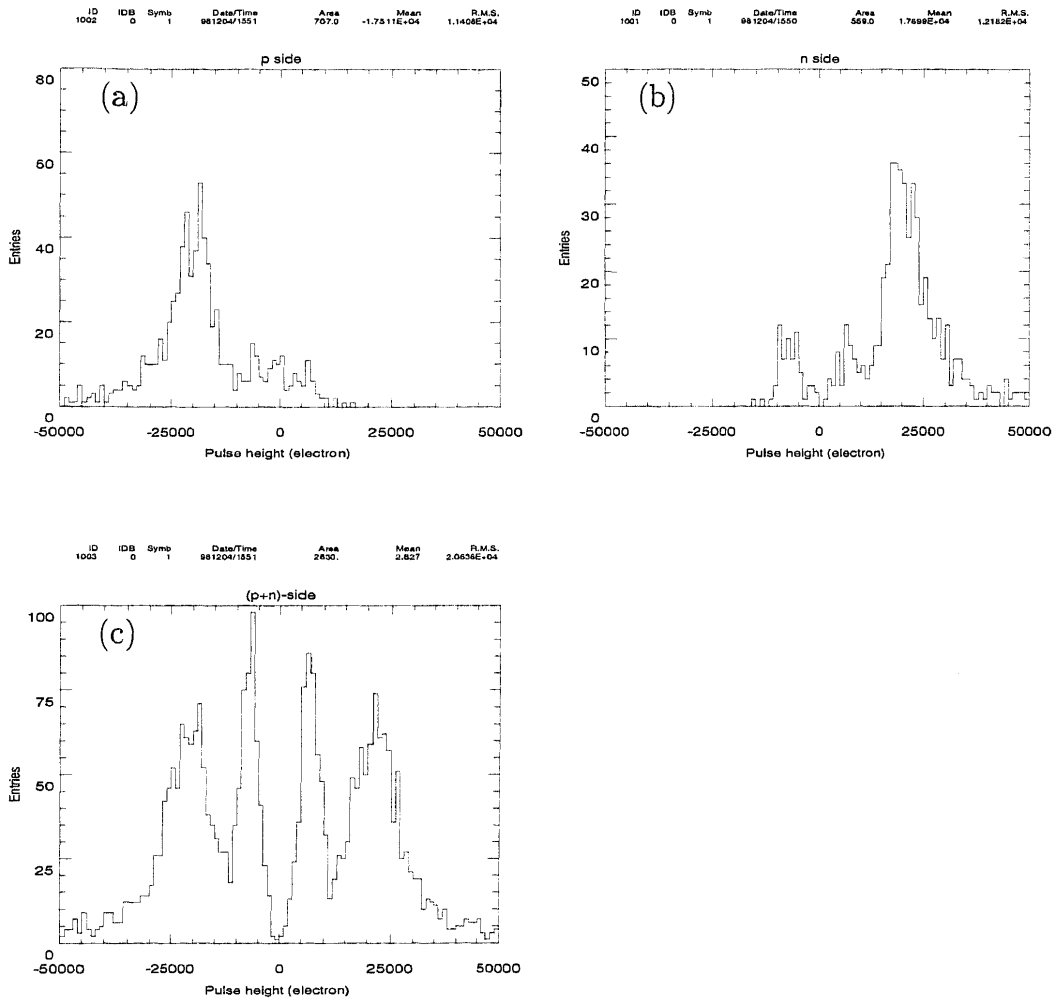


Figure 5.13: Pulse height distributions of (a) all p-side short half ladders, (b) all n-side short half ladders and (c) all p-n flipped side half ladders of the silicon detector for tracks triggered by the scintillation trigger counters.

40. This is due to the geometrical reason of the scintillation counters used for a cosmic ray trigger. As the scintillation counters were large, cosmic ray tracks with various incident angles penetrated the detector. The signals from the silicon detector were generated by not only MIPs but also by tracks with larger energy deposits than MIPs. Peaks in the region below the S/N value of 20 were caused from the inefficiency in the clustering program for tracks with small angles to the detector ladder [31].

In this system test, we conclude that the BELLE SVD detector can give a good performance. After this system test, the SVD detector and the repeater system were installed in the BELLE detector.

5.3 Summary of the system test for BELLE SVD

Through this system test for the silicon detectors for BELLE SVD, we could reach the following conclusions:

- Performance of the VME transfer rate of WS2126 was acceptable.
- Transfer rate of the SHARC link itself was reasonably good but there would be some possibilities of improvement.
- The SVD DAQ system could cope with a long time test.
- Performance of BEAST silicon detectors was acceptable.
- The combined performance of the SVD DAQ system, the repeater system and the silicon detectors was reasonably good. The DAQ system could run synchronously with the trigger timing signals.
- Track reconstruction of a cosmic ray in the $r - \phi$ plane was done successfully.
- The position resolution of the silicon detector ladders was estimated to be 24.7 μm by using the residual distributions.
- According to pulse height distributions, the silicon detectors were reasonably good. We note that the pulse height distribution was not only made by pure MIPs because of the geometrical reason of the trigger counters.

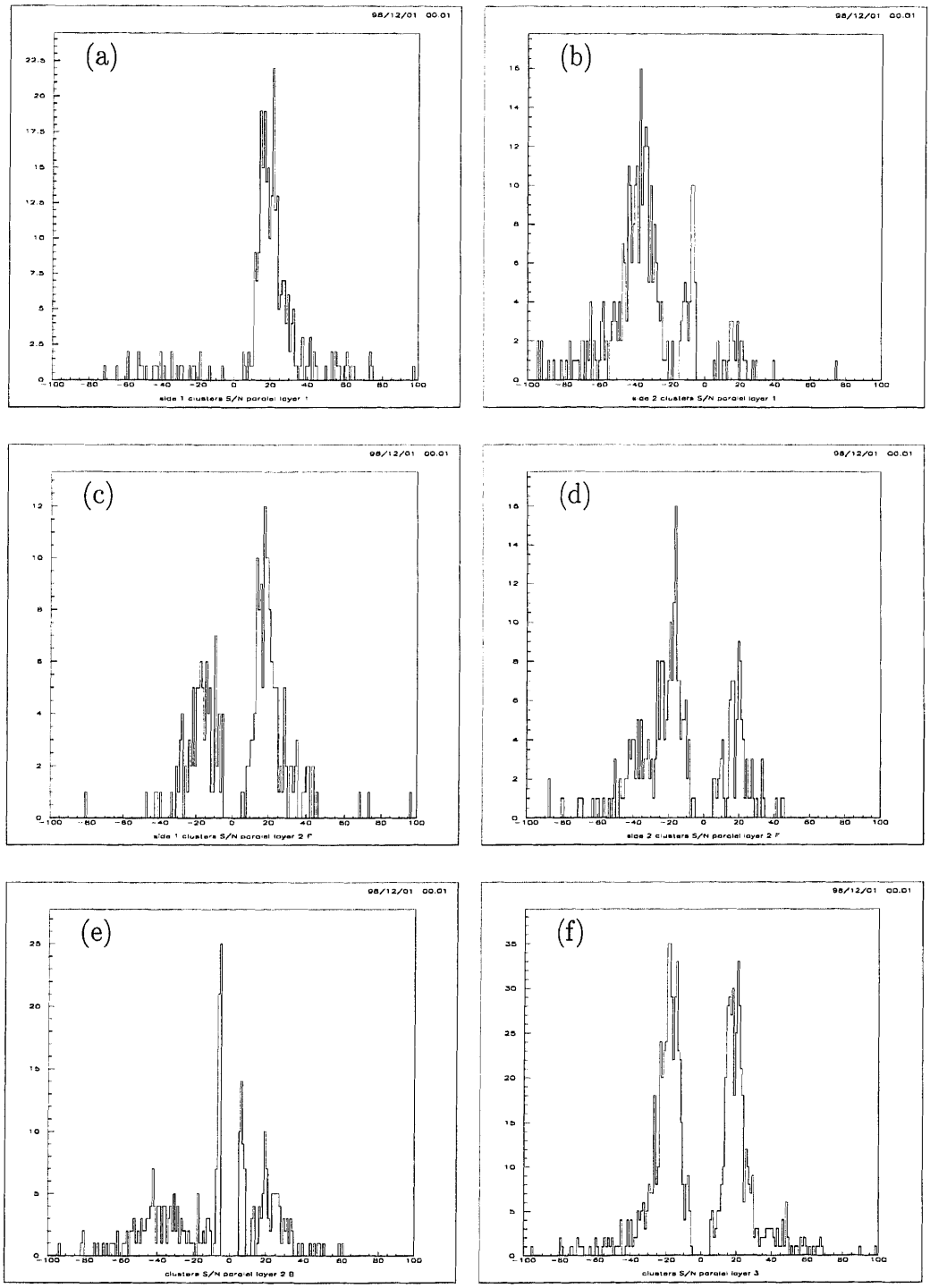


Figure 5.14: Distribution of S/N values of each cluster in the silicon detector ladders of (a) n-side of the inner layer, (b) p-side of the inner layer, (c) n-side of a short half ladder in the middle layer, (d) p-side of a short half ladder in the middle layer, (e) the backward middle layer (p-n flipped half ladder) and (f) the outer layer in the system test with cosmic rays. All the ladders shown in this figure were parallel to the scintillation counters.

- Preliminary data of S/N distributions indicate that the silicon detectors seem to be reasonably good with regard to S/N characteristics.

Chapter 6

Summary

We have committed to construct an SVD DAQ system from a preliminary design work by the BELLE SVD group. According to requirements from Monte-Carlo simulations, we have selected a DSP-based distributed DAQ system. We could construct a compact DAQ system with SHARC DSP VME clusters. With the SHARC link, we could make the centrally controlled local-run mode DAQ system. The system was useful for the BELLE SVD system test held in November 1998.

Concerning beam background effects in BELLE SVD, we obtained the following results. The beam background generator used in the Monte-Carlo simulation study generates pseudo spent electrons caused by residual gases in the beam-pipe, bremsstrahlung and Coulomb scattering. The beam background effects are rather severe in a high luminosity accelerator, such as KEKB, since the beam background events may cause radiation damages to the detector components, increase trigger rates, and obscure tracks of real physics events of interest. For the simulation study, a time window is required. In this study, we set the time window of 5 μs which corresponds to twice the peaking time of VA1 chips. In this simulation study, electric noise effects turned out to be dominant in the occupancy of the SVD detector.

To minimize the data size, a sparsification program is used in Halny FADC modules. The program uses two different threshold levels to determine hit channels. Optimization of the program is very essential for the SVD DAQ system because the DAQ system is required to run at a 500 Hz trigger rate. To evaluate the effects of the program, we made a simulation study of the sparsification code. According to the study, the sparsification code on DSPs of the FADC boards was effective for reducing background events. We

found that a multiple threshold cut was powerful to select physics events as efficiently as possible.

In the system test, we measured a transfer rate of this system with the full channel readout mode. In this test, we could have fast enough VME transfer rate of 4.06 MB/s, 11.4 MB/s and 12.7 MB/s for single word transfer, DMA single word transfer and DMA BLT, respectively. We could also have sufficiently fast transfer rate in the SHARC link of 9.69 MB/s and 33.7 MB/s for single word transfer (core process) and DMA transfer, respectively. But the link transfer program for a realistic use did not perform adequate transfer rate as anticipated. As the current DAQ system does not use the SHARC link in the global run mode, we need not improve the transfer rate at present. But we need to improve the system for the future.

We could also conclude that the buffer management system in FADC VME boards was sufficiently powerful for the high rate event trigger according to the results of a live time fraction plot. In the sparsification mode in a real experiment at a 500 Hz trigger rate, we could conclude that the system would have a good enough performance. The combined performance of the SVD DAQ system, the repeater system and the silicon detectors was reasonably good.

In the cosmic ray test, the silicon detectors showed a required level of performance. According to the pulse height distributions, the detectors showed good characteristics. Landau peaks were observed around 20,000 electrons in this measurement. The pulse height distributions included not only MIPs but also particles with larger energy deposits than MIPs because of the geometrical arrangement of the trigger counters. We measured S/N ratios around 20 for most of the ladders. The position resolution of the silicon detector ladders was estimated to be 24.7 μm according to the residual distributions created for the event display program in the cosmic ray test. In this estimation, we assumed that the position resolution of each ladder was the same.

From these results, we conclude that the silicon detectors can perform the required tasks very adequately in the forthcoming physics experiment.

Appendix A

Silicon Detector and Frontend Electronics

In this chapter, the sequence of signal handling in SVD is discussed.

A.1 Signals from a silicon detector

A charged particle deposits energy when it penetrates matter. The deposit energy of one MIP (minimum ionizing particle) in matter is approximately 2 MeV/ (g/cm^2). In a silicon detector, a charged particle deposits energy in the depletion layer to create electron-hole pairs. The deposit energy is used for excitation of electrons from the valence band to the conduction band. The band gap (V_g) of silicon is about 1.12 eV. On average, only about one third of the deposit energy is used for excitation, and the rest for cluster oscillation energy [37]. The average energy for the excitation of an electron is about 3.36 eV (3 $\times$ 1.12 eV).

In our silicon detector, the thickness of the depletion layer is about 300 μm. When one MIP penetrates the silicon detector, with a 300 μm thick depletion layer, about 25000 electron-hole pairs are created [38]. Thus the output charge caused by one MIP is:

$$25000 \times 1.6 \times 10^{-19}\mathrm{C} = 4 \times 10^{-15}\mathrm{C} = 4\,\mathrm{fC} \qquad \text{(A.1)}$$

A.2 Performance of VA1 preamplifier chips

VA1 preamplifier chips were fabricated by IDEAS, Norway as described in Section 3.2. This preamplifier chip is a charge-sensitive amplifier. The current/charge ratio is 10 μA/fC. In the previous section, we calculated the output charge from one strip of the silicon detector to be about 4 fC for one MIP. Thus the output current of VA1 for one MIP is about 40 μA.

A.3 Output voltage of the repeater system

A first stage amplifier on the repeater system has a 5.1 kΩ resistor for the feedback resistor of an operational amplifier. In this amplifier, the input current is converted to the output voltage. The output voltage for one MIP is estimated to be:

$$5.1\,(\mathrm{k}\Omega) \times 40\,(\mu\mathrm{A}) \simeq 200\,(\mathrm{mV}). \tag{A.2}$$

Appendix B

Digital Signal Processor

B.1 General characteristics of a digital signal processor

A digital signal processor (DSP) is widely used in the digital signal processing field (eg. compact disc player or mini-disc player). DSP is familiar devices in our daily life. It is designed based on Harvard architecture. Figure B.1 shows a typical architecture of DSP. In this architecture, a program memory and a data memory are independent, thus there are two bus lines. One is for the program memory and the other for the data memory. On the other hand, in CPU (central processing unit), a program and data share space in the same memory. A typical architecture of CPU is shown in Fig. B.2. In this architecture, there is only one common bus with which CPU has access to the program and data. An advantage of DSP is bandwidth of this bus. In the DSP case, we can use full bandwidth of the bus in access of program memory and data memory separately.

Since the architecture of a DSP is designed for digital signal processing, DSP has a good performance capability in calculating the following digital signal processing equation:

$$Y = \sum_{n=0} A_n \cdot X_n. \tag{B.1}$$

Thus DSP is good at numerical manipulation, but not at general use.

Concerning a program on DSP, we can select from some languages (assembler or C-language, for example). A program on DSP is compiled on a

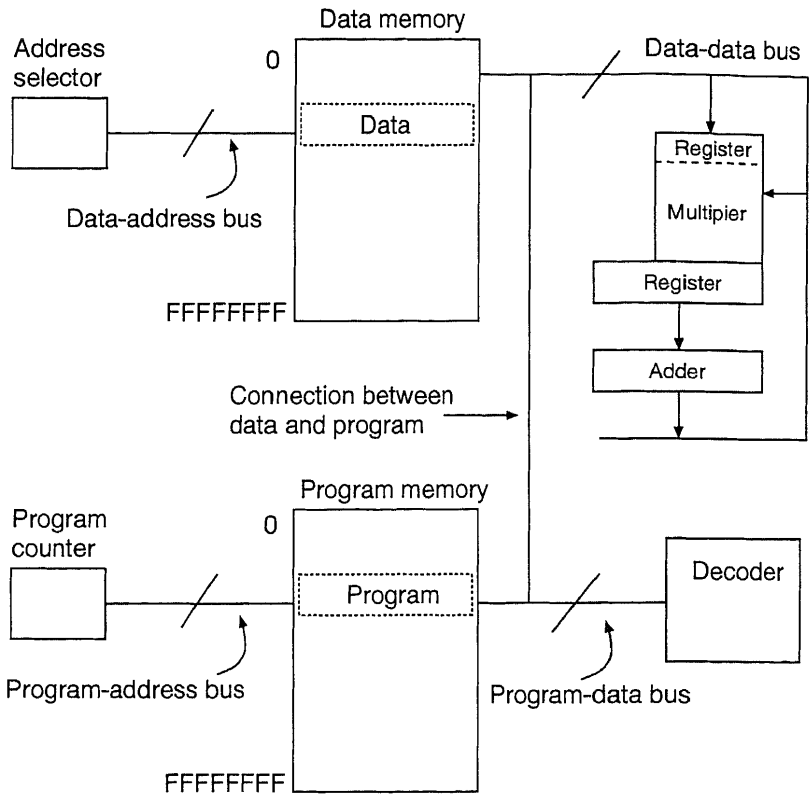


Figure B.1: Architecture of a digital signal processor.

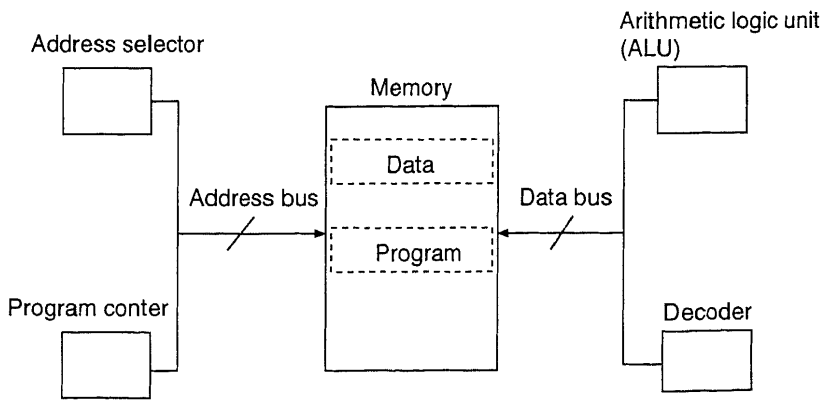


Figure B.2: Architecture of a central processing unit.

host computer (personal computer or work station). After a host computer completes compilation, the code is converted into a loadable code. The host computer downloads it to DSP when we want to start the program.

Many IC vendors supply different types of DSPs. We can select any type from them when its performance matches our requests (processing speed, cost, power usage and so on).

B.2 SHARC DSP

SHARC (**S**uper **H**arvard **Ar**chitecture **C**omputer) is a high speed 32 bit floating point DSP developed by Analog Devices, USA. This DSP has 40 MIPS, 25 ns instruction rate, single cycle instruction execution and 120 MFLOPS peak, 80 MFLOPS sustained performance. It has 6 link transfer lines and a capability of DMA transfer. The transfer speed of this link is up to 40 MB/s (DMA). The DMA transfer mode is used for data handling from external/internal to internal/external memory. This DSP has also the capability of glueless connection for scalable multiprocessing. Figure B.3 shows a block diagram of SHARC DSP (Analog Devices ADSP-21062) architecture. We can see that a program memory and a data memory are separated. This architecture (Harvard Architecture) has an advantage in memory access. Thus DSP has a capability of data manipulation.

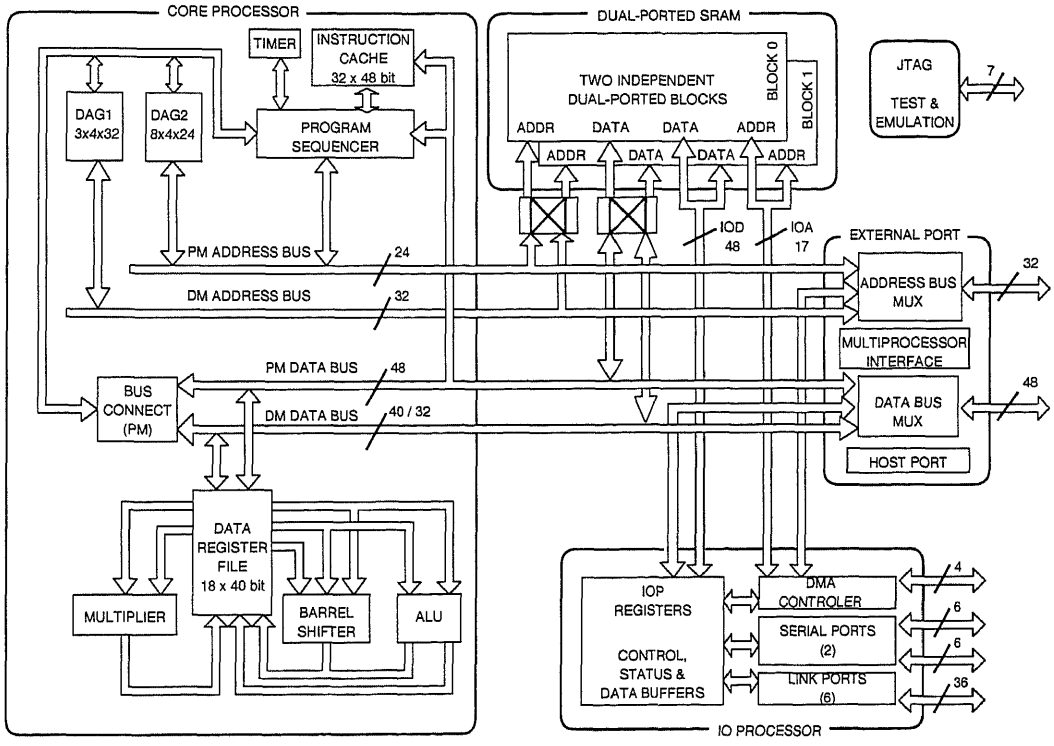


Figure B.3: Block diagram of SHARC DSP (Analog Devices ADSP-21062) architecture.

Appendix C

Usage of SHARC DSP VME Cluster

C.1 Programs for controlling WS2126

The SHARC DSP VME cluster, WS2126, has a capability of acting as the VME slave and the master. A VME A24 address of the board is defined by two screw switches. After power turned on a VME crate, this module is set to A24/D16 VME slave mode. After downloading program, this module is set to a VME master mode by the downloaded program which runs on a SHARC DSP. A downloader program for SHARC DSP was written in C with a FORCE computer VME driver for CPU-7V (Sparc CPU VME board). This program runs on CPU-7V and downloads a loadable code to SHARC DSP. On this module, there are two registers to be set up. One is a control register (**CTRL_REG**) for slave A32 setup and the other is a master control register (**MASTER_CTRL_REG**) which is used in VME master mode.

Before downloading, we must set a boot mode of SHARC DSP with EBOOT, LBOOT and BMS of a DIP-switch on the WS2126 [19]. The setup configurations of these parameters are shown in Table C.1. In the host boot mode, a SHARC DSP waits a DSP program to be written in the host port buffer (EPB0) and reads the program after the host computer write the program on the buffer. In the link boot mode, a SHARC DSP waits a DSP program to be written in a link buffer. The program is transferred via SHARC link. In the DAQ system of SVD, we selected the host boot mode. Thus the CPU-7V downloads a DSP program to SHARC DSPs on a WS2126.

Table C.1: Setup configuration of the boot setup.

EBOOT	LBOOT	BMS	Action
0	0	1	Boot from Host processor
0	1	1	Boot from link port
0	0	0	No booting

A flow chart of the download process is shown in Fig. C.1 and VME slave registers on a WS2126 used in downloading are listed in Table C.2. Subscripts, h, denote hexadecimal values. This notation is used in this chapter. The setup sequence is as follows:

Table C.2: VME slave registers on a WS2126. Subscripts, h, denote hexadecimal values.

Notation	VME A24 address	Name of a register
RESET_REG	0_h + A24_OFFSET	Reset register
CTRL_REG	4_h + A24_OFFSET	Control register
VME_OFFSET_REG	8_h + A24_OFFSET	VME offset register
FIFO_STAT	10_h + A24_OFFSET	FIFO status register
EXT_CTRL_REG	14_h + A24_OFFSET	Extended control register

- Reset every register of SHARC DSPs and WS2126.
- Set a user defined unique A32 base address for the WS2126. Then we write upper 7 bits of the address on **VME_OFFSET_REG** on WS2126.
- Set the A32 access enable bit in **CTRL_REG**.
- Set or reset the VME bus-lock enable bit for VME access.
- Download a program on SHARC.

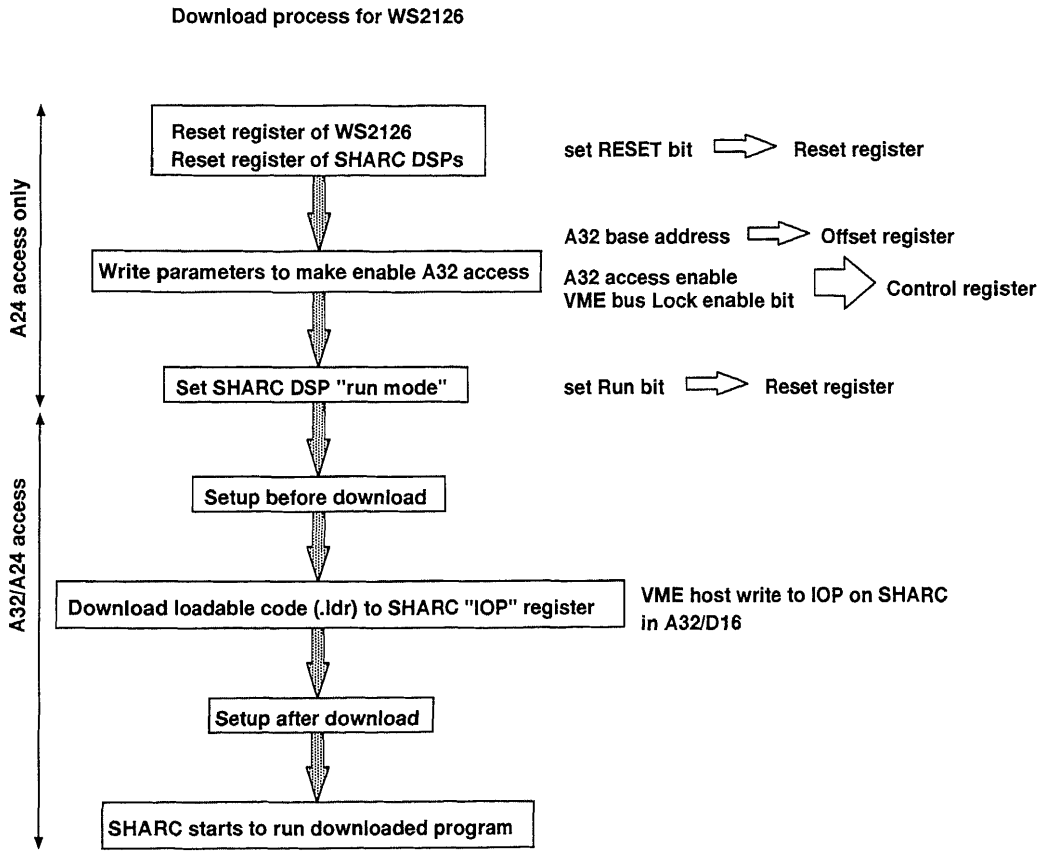


Figure C.1: Flow chart of the download process for WS2126.

VME bus-lock is used for VME DMA transfer by SHARC. If this bit has not been set, SHARC can not execute VME DMA transfer. In our case, we set the VME bus-lock bit for VME DMA usage from SHARC DSP. After this, VME host can have access to WS2126 in A32 mode. Before and after downloading, some preparations are needed as described in Tables C.4 and C.5. Subscripts, b, denotes binary values. This notation is used in this chapter.

Table C.3: Different host packing modes between external bus and SHARC bus. Subscripts, b, denote binary values.

	Packing method
HPM bits in SYSCON	Host bus to/from DSP bus
00_b	no packing/unpacking
01_b	16 bit external bus to/from 32 bit internal packing
10_b	16 bit external bus to/from 48 bit internal packing
11_b	32 bit external bus to/from 48 bit internal packing

Before downloading, several setup tasks are needed. The setup sequence is shown in Table C.4. **HPM** register in SYSCON defines the packing mode between a SHARC DSP bus and a data on VME bus. Table C.1 shows several packing modes between external bus and SHARC bus. The byte-order of data is defined by **HMSWF** in SYSCON. In this setup, the VME memory window size must be defined for the VME master access of WS2126. In our case, the window size is 256 Mbytes (= 2^{28} bytes with the relation of 1 k = 2^{10} = 1024). In general, the **MSIZE** is defined as follows. The window size is:

$$\text{window size } = 2^{EXT\_MSIZE\_EXP} \text{ (bytes)},$$

where the **MSIZE** is defined as:

$$\text{MSIZE} = (\text{EXT\_MSIZE\_EXP} - 13).$$

Thus **MSIZE** = 15 (f_h) in our case. As the external host port (**EPB0**) corresponds to DMA channel 6, we enables the channel. Concerning the instruction method and host packing mode, the DMA channel must also be set with the same method and mode as those set in SYSCON as follows:

Table C.4: Setup sequence before downloading a SHARC program. The sequence proceeds from upper to lower lines of the table.

VME action	Parameter to be set
set 32 bit words direct read/write enable	IWT (SYSCON) = 0
set host bus = 16 bit and memory bus = 32 bit in SYSCON	HPM (SYSCON) = 01_b
set LSW first	HMSWF (SYSCON) = 0
set MSIZE = 256 Mbytes	MSIZE (SYSCON) = f_h
set external bus priority (I/O processor has a priority)	EBPR10 (SYSCON) = 1
write set parameters in SYSCON	
clear SRST	SRST (SYSCON) = 0
write set parameters in SYSCON	
set DMA enable in DMA channel 6	DEN (DMAC6) = 1
write set parameters in DMAC6	
set external address (DSP address) of host port in II6	II6 = 20000_h (DSP address of host port.)
write set parameters in II6	
set DMA channel 6 address modifier 1	IM6 = 1
write set parameters in IM6	
set FLSH bit in DMAC6	FLSH (DMAC6) = 1
write set parameters in DMAC6	
reset FLSH bit in DMAC6	FLSH (DMAC6) = 0
set instruction mode	DTYPE (DMAC6) = 1
set host bus = 16 bit and memory bus = 48 bit in DMAC6	PMODE (DMAC6) = 10_b
write set parameters in DMAC6	
set DMA enable in DMA channel 6	DEN (DMAC6) = 1
write set parameters in DMAC6	
set host bus = 16 bit and memory bus = 48 bit in SYSCON	HPM (SYSCON) = 10_b
write set parameters in SYSCON	
set instruction mode in SYSCON	IWT (SYSCON) = 1
write set parameters in SYSCON	

Table C.5: Setup sequence after downloading a SHARC program. The sequence proceeds from upper to lower lines in the table.

VME action	Parameter to be set
clear instruction mode	IWT(SYSCON) = 0
write set parameters in SYSCON	
set host bus = 16 bit and memory bus = 32 bit	HPM(SYSCON) = 01_b
write set parameters in SYSCON	
set DMA disable in DMA channel 6	DEN(DMAC6) = 0
set FLSH bit in DMAC6	FLSH(DMAC6) = 1

- HPM of SYSCON corresponds to PMODE of DMAC6, and
- IWT of SYSCON corresponds to DTYPE of DMAC6.

The same values are set in a **PMODE** bit and **DTYPE** bits of DMAC6. For downloading, the host packing mode of making 48 bit data from three 16 bit data must be set. The corresponding parameters are set. (PMODE of DMAC6 and HPM of SYSCON). The instruction mode is also enabled (**IWT** bit of SYSCON).

After downloading, several tasks are required. The setup sequence is shown in Table C.5. For the read/write operation, the instruction mode is disabled. The packing mode of making 32 bit data from two 16 bit data is set in this setup. As soon as the downloading has been finished, the DMA channel 6 is disabled and the contents of a buffer of DMA channel 6 are cleared.

The program on SHARC was written in C and assembler language according to the definition of the compiler from Analog Devices. A source program is converted to a binary executable code (.exe) by the compiler and the loader makes loadable code (.ldr) for SHARC from the executable code. Once the loadable code is downloaded successfully, SHARC starts the program.

C.2 VME functionality

WS2126 supports the VME master/slave mode. The memory map of WS2126 in SHARC address and VME address is shown in Fig. C.2. When WS2126 is in the slave mode, a VME master module can have access to WS2126 according to the VME memory map shown in the figure. While WS2126 is in the master mode, SHARC DSP on this board can have access to the VME memory space according to the SHARC memory map shown in the figure.

A schematic diagram of VME master access from SHARC DSP(s) on WS2126 is shown in Fig. C.3. Each SHARC can perform VME master access via a VME master control register by the VME control program on ALTERA MAX 9000. The address is converted from a DSP bus format to a VME bus format by this register. In Table C.6, the conversion methods between the SHARC bus format and the VME bus format are shown. In this table, **VME_ADDR_WINDOW** is the VME address of VME address window when SHARC makes access in the VME bus (SHARC is a master.) and **SHC_VME_BASE** is a VME base address when the other host makes access to SHARC on WS2126. (One of other modules is a master.) VME_ADDR_WINDOW and SHC_VME_BASE are defined by VME slave register setup on WS2126 [19]. As described in the previous section, VME_ADDR_WINDOW is set as 256 Mbytes by the setup of **MSIZE** bits in a DSP register, SYSCON. SHC_VME_BASE is set by a program which runs on a SHARC DSP.

Table C.6: Conversion method between the SHARC DSP bus format and VME bus format.

Host	Direction	Address
SHARC	SHARC → VME	(VME_ADDR_WINDOW) + (SHARC address << 2)
Other module	VME → SHARC	(SHC_VME_BASE) + (VME address >> 2)

Each DSP on a WS2126 can have access to a master control register on a WS2126. The contents of the register are listed in Table C.7. Upper 6 bits are used for a VME A32 address setup for VME master access from WS2126. The BLT32 bit enables the VME DMA block transfer in a master access mode.

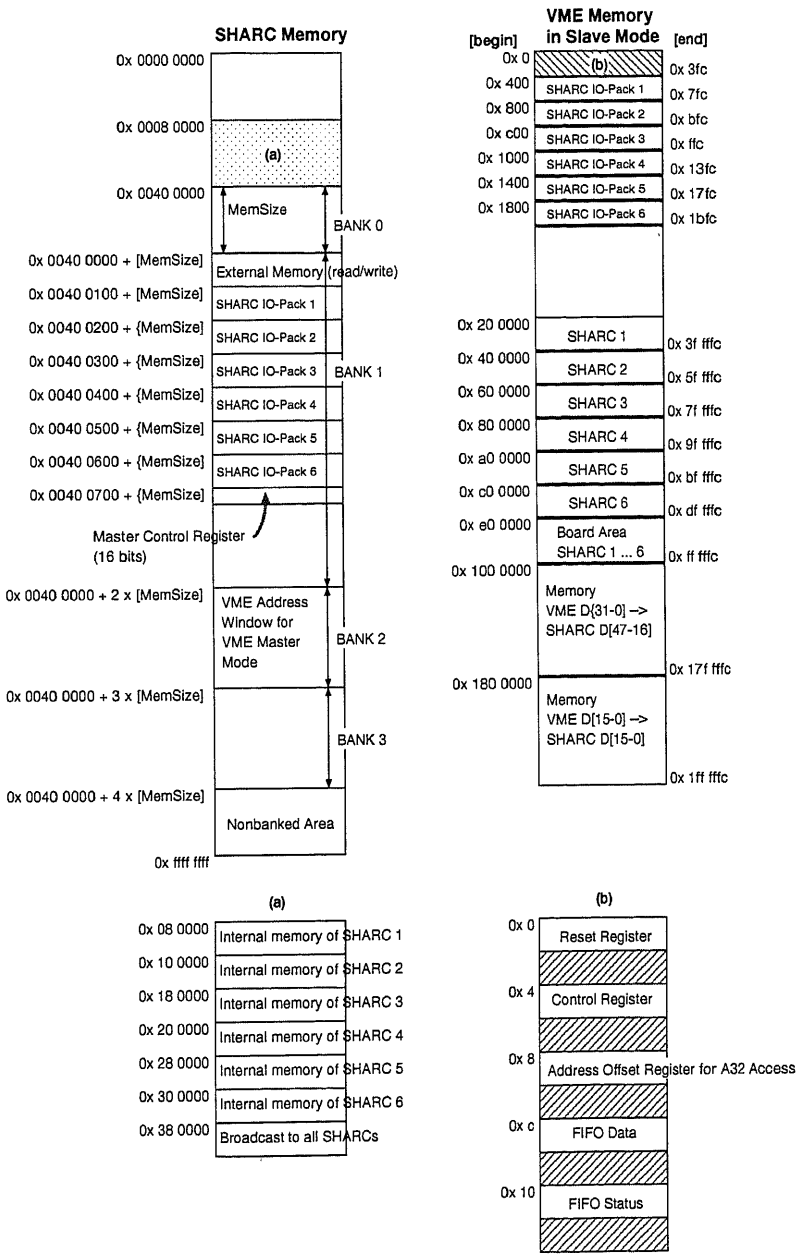


Figure C.2: Memory map of WS2126 in SHARC address and VME address.

Table C.7: Contents of a master control register on a WS2126.

Bit number	Contents
15	VME A31
14	VME A30
13	VME A29
12	VME A28
11	VME A27
10	VME A26
9	BLT32
8	VME bus-lock
7	LWORD
6	VME A1
5	Address modifier: AM5
4	Address modifier: AM4
3	Address modifier: AM3
2	Address modifier: AM2
1	Address modifier: AM1
0	Address modifier: AM0

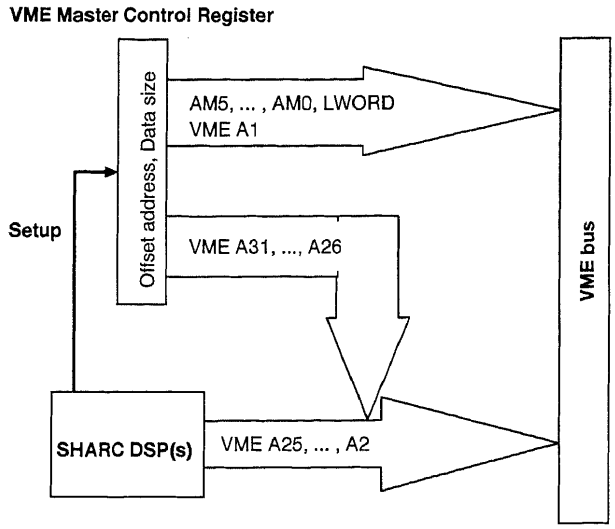


Figure C.3: Schematic diagram of VME master access from SHARC(s).

The VME bus-lock bit is set for DMA transfer. The LWORD, A1 and address modifier (AM) are set according to the VME transfer mode. Details of the LWORD and the AM are described in ref. [39]. This register is accessible from only SHARC DSPs. An upper 16 bits of VME address to which SHARC DSPs will have access are written on the register. A SHARC DSP can have access to the VME memory space by the access to the SHC_VME_BASE. For example, in the case of VME memory access from a SHARC DSP in an address of VME_BASE_ADDR + VME_OFFSET, where VME_BASE_ADDR is written in the master control register, the SHARC DSP will have access to the memory in an address of SHC_VME_BASE + SHC_OFFSET. According to the address exchange defined in Table C.6, SHC_OFFSET is a two-bits shifted value of the VME_OFFSET in the right direction (divided by 4).

In the master mode, this module can perform VME single and DMA read, and DMA BLT (block transfer) is supported by the control program. In a VME master access, the setup of AM (address modifier code) and $\overline{\text{LWORD}}$ is important. In the VME single word transfer mode, AM (address modifier) and $\overline{\text{LWORD}}$ are set to $0d_h$ and 0_h, respectively. On the other hand, in the DMA BLT mode, AM and $\overline{\text{LWORD}}$ are set to $0f_h$ and 0_h, respectively.

In the single word transfer and BLT mode, a SHARC DSP only has access to the SHC_VME_BASE + SHC_OFFSET. The data length is limited up to

256 bytes (64 long words) in the BLT mode. In the DMA transfer mode, some setup tasks listed in Table C.8 are required. The parameter, x, in this table denotes a DMA channel number ($x = 0 \sim 10$). After these setup tasks,

Table C.8: Setup sequence of VME DMA transfer, where x denotes a DMA channel number. The sequence proceeds from upper to lower lines of the table.

Action	Parameters to be set
Clear buffer	Set FLSH bit in DMACx
Set internal memory address	IIx = internal memory address
Set internal address modifier 1	IMx = 1
Set data length	Cx = data length
Set external memory address	EIx = external memory address
Set external address modifier 1	EMx = 1
Set data length	ECx = data length
Set DMA master mode	Set MASTER bit in DMACx
Set transfer direction	Write 0 (read from external memory) or 1 (write to external memory) in TRAN bit of DMACx

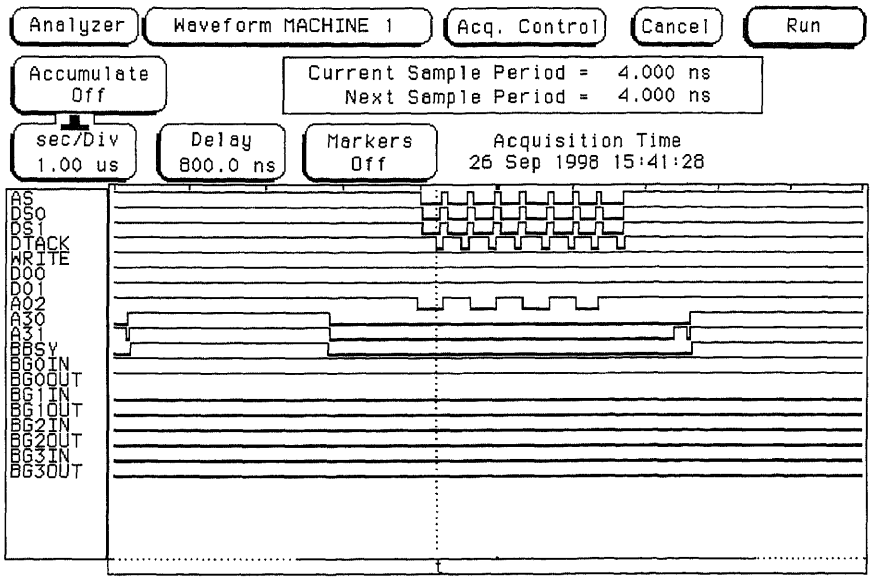
the VME DMA transfer is available. When we start the DMA sequence, the VME bus grant is done. If the bus is free to have access, the host packing mode (HPM) in the SYSCON register is set in the same one in DMACx. In this case, since HPM in DMACx is set in no packing mode (00_b), the HPM in SYSCON is set in the same mode. Next DMA enable bit (DEN) in DMACx is set, then VME DMA transfer starts.

Figures C.4 (a) and (b) show signals on a VME bus when WS2126 reads Halny FADC in DMA single word and DMA BLT modes, respectively. In Fig. C.4 (a), the AS signal is asserted in each long word transfer, whereas in Fig. C.4 (b), the AS signal is low while the whole data is transferred.

C.3 SHARC link transfer

For the communication between different WS2126 boards, a SHARC link is supported. When we use the SHARC link on WS2126, a WS9002, SHARC

(a)



(b)

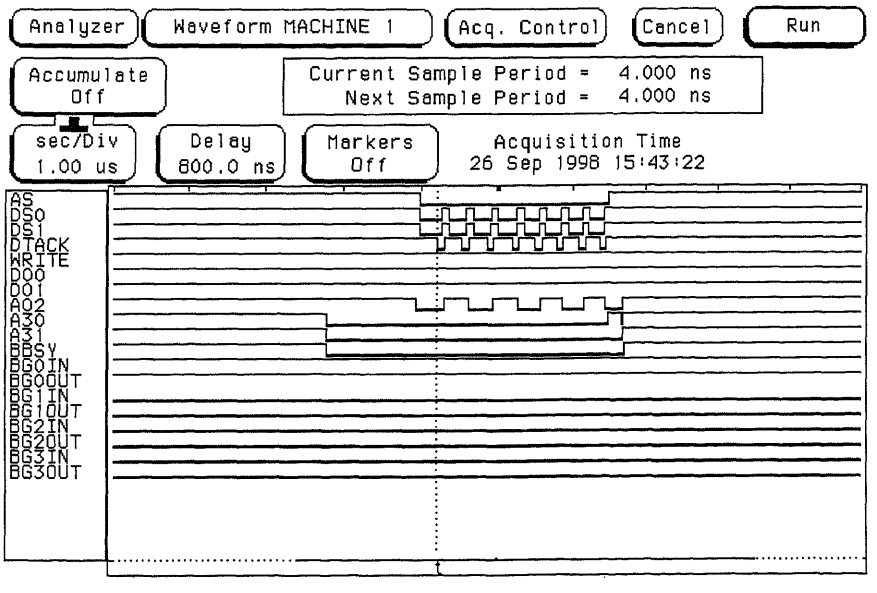


Figure C.4: Signals on VME bus when WS2126 read from Halny FADC in (a) DMA single mode and (b) DMA BLT mode.

IO piggy pack, is used. Figure C.5 shows the configuration of a SHARC link between different SHARC DSPs using WS9002s. As described in Subsec-

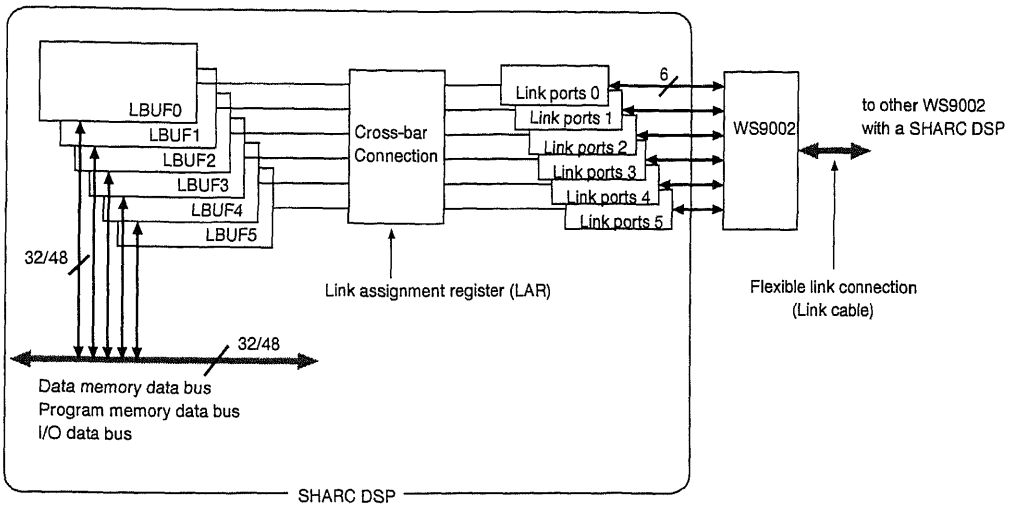


Figure C.5: Configuration of a SHARC link between SHARC DSPs using WS9002s.

tion 3.4.4, the link connection is flexible and it is configured by a register on a WS9002. The register setup is done by a software which runs on a SHARC DSP.

Some setup tasks are required for the link transfer. The setup sequence of the link transfer is shown in Table C.9. The items in the center and right columns are parameters to be written or read on SHARC DSP and WS9002 sides, respectively. The parameter, x, denotes a link buffer number. IOPACK_CTRL is a control register of a WS9002. Details of the registers on a WS9002 used in this setup are described in ref. [20].

First, some registers on a SHARC DSP is cleared and a link port is disabled to be connected. The three-state outputs of link ports on WS9002 are set in high-impedance. To configure the link connection, the direction of a link transfer is set in IOPACK_CTRL. A DMA transfer is used between a SHARC DSP internal RAM and a link buffer when the DMA transfer is selected. For this DMA transfer, DMA channel number is set. In fact, the channel number is defined from the link buffer number of a SHARC DSP.

Table C.9: Setup sequence of a SHARC link transfer, where IOPACK_CTRL is a control register of a WS9002, where x in this table denotes a link buffer number ($0 \sim 5$).

Setup action	Parameter to be set	
	SHARC DSP	WS9002
Reset the SHARC links and the related registers	LAR = ffffffff_h LCOM = 0 LCTL = 0	
Disable link ports	LAR = 3ffff_h	
Set link port output high-impedance		IOPACK_CTRL = 0
Assign transfer direction		Set 01_b (receive) or 10_b (transmit) in assigned link port bits of IOPACK_CTRL
Assign DMA channel	Set DMA channel	
Assign link port	Write link port number in AxLB bits of LAR	
Select clock cycle (1 × or 2 × system clock)	Set LCLKX2x bits in LCOM	
Set link buffer enable	Set LxEN in LCTL	
Define transfer direction	Set LxTRAN in LCTL	

The link port number which is used is set in AxLB bits in LAR. The link transfer clock cycle is set in LCLKX2x bit in LCOM. The direction of this link transfer is also set in the LxTRAN bit in the LCTL. The setup sequence listed in this table is done on a transmitter and a receiver link sides. The transfer direction must not be the same between the transmitter and the receiver sides.

We have two link transfer modes; one is a core process transfer mode and the other a DMA transfer mode. In the core process transfer mode, write/readout sequence of a SHARC link is simple. The data to be transferred from the transmitter are written on the link buffer (LBUFx; $x = 0 \sim 5$) which is assigned for the transmitter link port. On the other hand, the data to be received on the receiver are read from the link buffer which is assigned for the receiver link port. The transfer sequence of DMA link transfer is shown in Table. C.10. The parameter, x, in this table denotes a link buffer number. As described before, the DMA channel is defined from the link

Table C.10: Sequence of a SHARC link DMA transfer, where x in this table denotes a link buffer number.

Setup action	Parameter to be set in a SHARC DSP
Set DMA channel	Set DMA channel number
Set link buffer enable	Set LxEN in LCTL
Set transfer direction	Write 1 (transmit mode) or 0 (receive mode) in LxTRAN of LCTL
Set internal SHARC memory address	IIx = memory address
Set DMA address modifier 1	IMx = 1
Set data length	Cx = data length
Start DMA transfer	Set LxDEN in LCTL

buffer number. The link buffer used has been already defined in the link transfer setup. We must use the assigned link buffer and link port. According to the DMA channel, an internal SHARC memory address, an address modifier number and length of data to be transferred are set in IIx, IMx and Cx, respectively. When we start the DMA transfer, we set a LxDEN bit in LCTL.

In general cases of the DMA link transfer, a combination with these methods of core process transfer and DMA transfer is used for synchronous transfer. The sequence is as follows:

1. Transmitter sends the data length of data to be transferred in DMA (core process transfer).
2. Receiver receives the data length from the link buffer via a SHARC link (core process transfer).
3. Transmitter sends the data in DMA transfer.
4. Receiver receives the data in DMA transfer.

The data length is variable in each transfer and the receiver and transmitter must respond, otherwise the transferred data will be neglected.

Appendix D

Halny FADC Module

D.1 Introduction to FADC

Halny Flash ADC (FADC) modules were designed and fabricated by Krakow and Princeton groups. Figure 3.17 shows a block diagram of a Halny FADC module. This module has four input channels, four Motorola DSP56302s. Two Xilinx FPGAs are placed on the module. Each DSP operates a readout task on each channel and calculates pedestal and offset values. From these values and threshold levels, sparse data scan is done by each DSP. Two Xilinx chips manage VME interface and control and data handling. This module supports A32/D32 VME slave access and BLT (block transfer).

D.2 Functionality of Halny FADC

Each readout channel of Halny FADC incorporates:

- input differential amplifier,
- serial 12-bit DAC and level shifter,
- a 10-bit, 20 MHz ADC (Analog Devices AD9200),
- a front multi-event FIFO buffer (Cypress CY7C4265-15AC: 16 k $\times$ 18 bits),
- a digital signal processor (Motorola DSP56302: 66 MHz/66 MIPS, internal 0 wait states 100 kbytes SRAM),

- an output multi-event FIFO buffer (Cypress CY7C4265-15AC: 16 k × 18 bits), and
- a field programmable gate array based control unit (Xilinx XC4005E)

There are two Xilinx chips on this module. One is for VME control, DSP host port control and output FIFOs control logic, and the other is for control of writing digitized data on the input FIFOs.

D.3 Common mode subtraction by DSPs on Halny

In BELLE SVD, we have about 82,000 readout channels, whereas CsI has about 10,000 channels, for example. It is hard to manage the huge number of readout channels of SVD at a 500 Hz trigger rate. The FADC module has a capability of data sparsification to select real hit channels as precisely as possible. The data sparsification is done by DSPs on the board. Particles with various momenta will penetrate DSSDs. Signal shape and hit channel distribution depend on the direction of a penetrating particle. Figure 4.1 shows two examples of particles with high transverse momentum (P_t) and low P_t.

In a Halny FADC, data sparsification shown in Fig. D.1 is done in each strip. In this figure, numbers 128 and 5 denote the number of channels in one VA1 chip and the number of VA1 chips in one side of a hybrid, respectively. For this sparsification, data of at least 16 events are required before real data acquisition [40]. From input signals, offset and noise levels are calculated in each strip and stored in the pedestal and noise tables, respectively. With the data taken before real data acquisition, offset and noise levels are calculated for real data acquisition. Contents of the tables are updated in each event. Pedestal values are subtracted from signals in each strip. Pedestal subtracted signals are put in the noise calculation and discriminating block. After these manipulations, hit strips are selected. Selected channel data are formated. Calculated pedestals and noises are fed into the formated data. The data are put into output FIFO. Through this method, the common mode subtraction and pedestal subtraction are done.

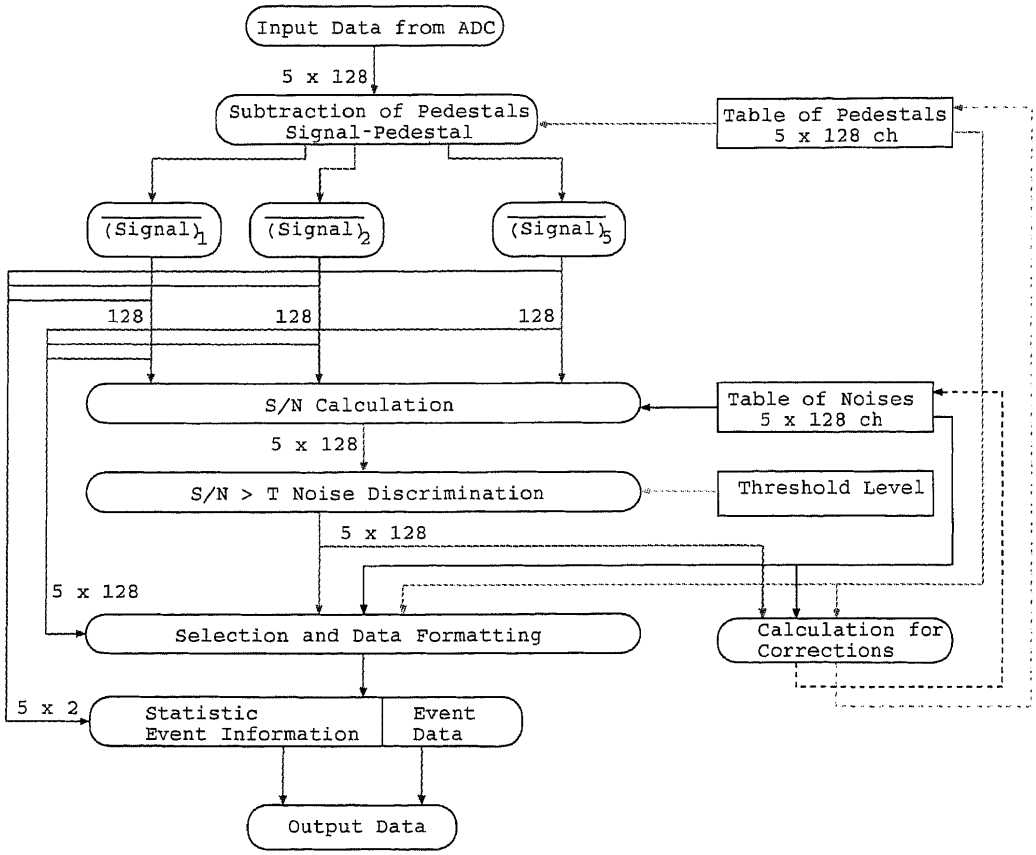


Figure D.1: Sparsification method in a Halny FADC.

D.4 Cluster finding method

In the sparsification of Halny FADC, the cluster finding is one of the most important features. Figure D.2 shows a cluster finding method of a Halny FADC. As shown in Fig. D.1, pedestal and noise levels are subtracted from

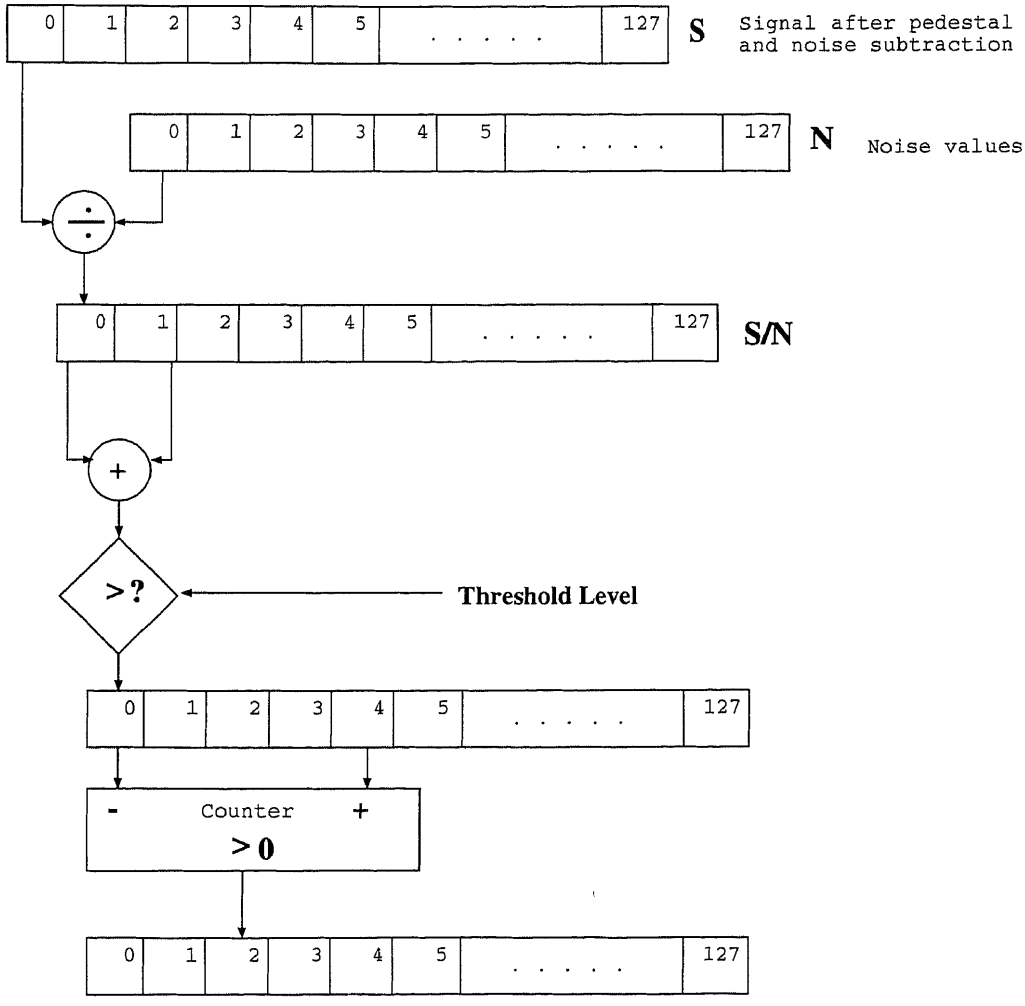


Figure D.2: Cluster finding method of a Halny FADC module.

signals in each strip. The subtracted values are divided by noise levels in each strip. Then, S/N (signal-to-noise ratio) value is calculated. After this calculation, S/N values of neighboring channels are added and compared with

the threshold level. After this, cluster information is prepared. Through these manipulations, hit clusters are found.

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