Vertically Aligned Group-IV Semiconductor Nanowires and Nanotubes for Electronic and Optoelectronic Applications

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Abstract

Group IV semiconductor nanostructures are widely used in the electronic and optoelectronic fields due to their excellent material compatibility, reliability, and manufacturability. Reducing the size and dimensions of semiconductors not only increases the packing density, but also tailors electrical and optical properties, leading to new functionalities.

Vertically aligned one-dimensional (1-D) nanostructures, including nanowires (NWs) and nanotubes (NTs), have a high specific surface area, allowing transistors to be integrated perpendicular to the surrounding gates to achieve excellent performance and high packing density. Their large junction area and light-trapping effect make them ideal materials for optoelectronic devices such as solar cells and photodetectors.

First, we succeeded in fabricating $Ge_{1-x}Sn_x$ NWs with high Sn content (~5 at.%) using Au–Sn catalyst. The Sn incorporation, crystallinity, and growth direction were investigated and controlled. Boron doping of $Ge_{1-x}Sn_x$ NWs was also demonstrated. The high Sn% catalyst promotes the incorporation of Sn and improves the crystallinity of NWs, but also induced twinning defects in the NWs. NWs grown by high Sn catalysts grow in the ⟨110⟩ direction, while NWs grown by low Sn catalysts grow in the ⟨111⟩ direction.

Next, Ge NW arrays and Ge/p-Si core–shell NW arrays with different lengths and diameters were fabricated successfully by nanoimprint lithography (NIL) and Bosch etching, and hole gas accumulation in the Ge region was demonstrated.

Next, a simple and low-cost method was developed to fabricate vertically oriented SiNTs and GeNTs by wet etching the ZnO of ZnO/Si(Ge) core–shell NWs. The growth, morphology, crystallinity, and stress were investigated.

Lastly, Si NT arrays with different lengths, diameters, and wall thicknesses were successfully fabricated using NIL with spacer patterning, and the surface defect density and reflectance were studied. The defect density and reflectance of fabricated NT arrays are lower than NW arrays.

Contents

Chapter 1

Introduction

1.1 Background and motivation

Today's world economy is supported by nothing less than high-performance electronics products. Since J. Kilby proposed the concept of integrated circuits (ICs) in 1958, the number of electronic components on microchips has increased exponentially over time, and the miniaturization of complementary metal–oxide–semiconductor (CMOS) technology has been the fundamental key to the continued progress of the silicon-based semiconductor industry. In 1965, Gordon Moore predicted that the number of transistors on a chip would double every 18 months, a prediction that has held true for the past 40 years [1]. However, the scaling down may be reaching its physical limit, and further performance improvement of conventional metal–oxide–semiconductor field-effect transistor (MOSFET) structures has become difficult due to the short-channel effects (SCEs), which causes the drain-induced barrier lowering, deteriorated subthreshold swing, increased off-state leakage current and the threshold voltage roll-off in device.

To overcome these inherent scaling limits as technology node shrinks, the architecture of the MOSFET has been shifted from single-gate to multi-gate such as fin field-effect transistors (FinFET) and gate-all-around (GAA) FET. In GAAFETs, the gate completely surrounds the nanowire channel, which allows for optimal electrostatic control, resulting in a significant reduction in SCE and improved drive current.

Despite the architecture of the MOSFET, another approach to meet the increasing performance requirements is to use a better channel material than Si. The comparison of the electric properties for Si and Ge in Table 1.1. shows that Ge has a lower carrier effective mass (electrons and holes) and thus a higher charge carrier mobility. This high electron and hole mobility (about twice and four times that of Si), makes it an ideal channel material for next-generation electronic and optoelectronic devices that are compatible with Si.

Table 1.1. Comparison of the electric properties for silicon and germanium.

Property	Silicon	Germanium
Electron bulk mobility (cm^2/Vs)	1450	3900
Hole bulk mobility (cm^2/Vs)	450	1900
Electron effective mass, m^*/m_0	m_l^*=0.98 m_l^*=0.19	m_l^*=1.64 m_l^*=0.082
Hole effective mass, m^*/m_0	m_{lh}^*=0.16 m_{hh}^*=0.49	m_{lh}^*=0.044 m_{hh}^*=0.28
Melting point (℃)	1415	937
Band gap (eV)	1.12	0.66

1.2 Nanowires and nanotubes

Group-IV semiconductor nanostructures have been widely used in electronic and optoelectronic applications due to their great material compatibility, reliability, and manufacturability. Reducing the size and dimensionality of semiconductor not only increase the packing density but also lead to tailored electrical and optical properties, and thus new functions. Vertically aligned one-dimensional (1D) nanostructure including nanowires (NWs) and nanotubes (NTs) provide a high specific area that allows integrating the transistors vertically with a surrounding gate to achieve excellent performance and high packing density. The large junction area and light trap effect make them ideal for optoelectronic devices such as solar cells and photodetectors. On the other side, vertically aligned 1D architecture can achieve superior performance and high-density packaging by integrating transistors perpendicular to the surrounding gates.

Nanowire

NW structures have desirable properties such as optical confinement, large junction area, and high integration, making it possible to realize highly efficient optoelectronic devices [2], [3], and vertical-gate all-around FETs. The illustration of a vertically stacked NW GAAFET is shown in Figure 1.1a. A vertical NW, as a channel, is completely surrounded by the gate with the source and gate stacked vertically. This kind of vertical NW GAAFET was predicted to occupy less area, consume less power, and be 300% faster than lateral NW GAAFET [4].

In the case of application in solar cells, conventional solar cells require anti-reflection layers and thick substrates to reduce reflection loss and transmission loss, which increases the manufacturing cost of the device[5]–[7]. NW structure can effectively enhance the absorption of light due to its anti-reflection and light-trapping effect. On the other hand, the radial p-n junction of the NWs provides a short carrier collection path, which is particularly advantageous for rapid charge separation and efficient carrier collection [8]–[10]. Figure 1.1b shows the anti-reflection of NWs. The NW region represents an effective refractive index value between that of the air and substrate and acts as an anti-reflection coating layer.

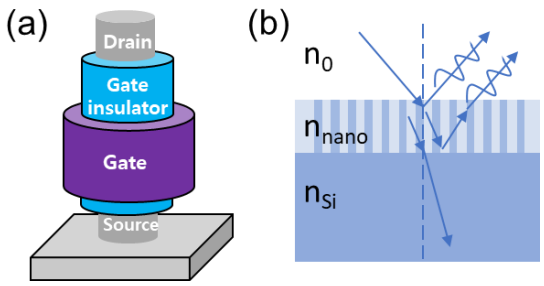

Figure 1.1. (a) Illustration of Si NW FET. (b) Illustration of anti-reflection of NWs

Nanotube

Nanotubular structures are characterized by a large specific surface area with more exposed active sites, giving them unique physical properties. Si NTs and Ge NTs are highly promising semiconductor materials due to their potential application as solar cells with enhanced light absorption [11] and nanotube FET with higher switch speed and better controllability [12] than the NWs. The nanotube FET shown in Figure 1.2 has an inner core and outer shell gate with vertically stacked source, channel, and drain regions. It is also supposed that the NT architecture for FET has a higher area efficiency than the vertical NW GAAFET [13]. The electric field intensity distribution in Figure 1.2 shows that the NW reflects more light than the NT structure, indicating a higher anti-reflective effect of NT. On the other hand, the NT solar cells are also considered to further shorten the carrier collection path for higher charge collection efficiency.

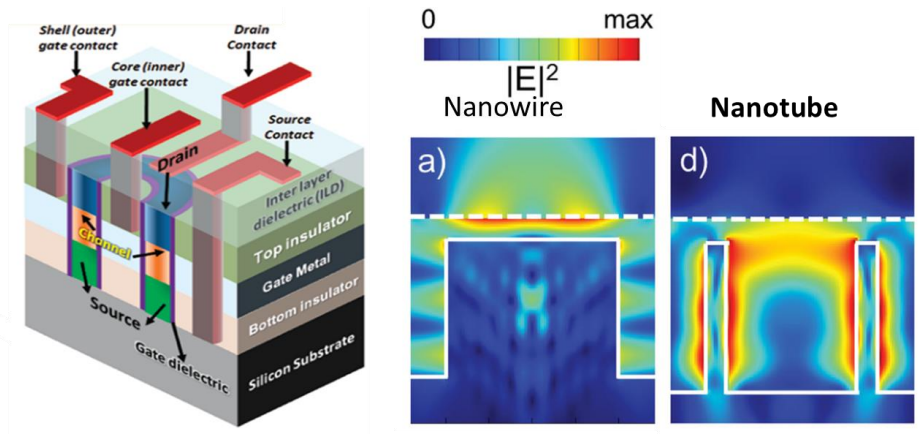

Figure 1.2. Left: illustration of Si NT FET [12]. Right: simulated electric field intensity $|E|^2$ distribution in the (a) NW and (b) NT at a wavelength of 600 nm [11].

Other applications

In addition to electronic and optoelectronic applications, NTs are gaining increasing attention due to their potential applications in energy storage, biosensors, and chemical transport. The axial hollow space within SiNTs can be used to improve the electrochemical performance of Li-ion batteries. This is because it provides additional free space to accommodate the massive volume expansion that occurs during the lithiation/delithiation process and prevents the pulverization of Si [14]–[20]. In addition, SiNTs have a large specific surface area, which results in a short diffusion length of lithium ions and a large ion flux. Another application is as an

intracellular sensor by allowing biological molecular species to flow directly into the inner cavity and gating a SiNT transistor [21]. The inner and outer surfaces of the NT structures can also be functionalized in different ways to allow selective transport, separation, and filtering [22], [23].

Compared to Si, Ge is also a promising material as an anode material for high-capacity lithium-ion batteries due to its excellent volumetric capacity, high electrical conductivity [24] (two orders of magnitude higher than Si), and fast lithium-ion diffusion rate (four orders of magnitude higher than Si) [25]–[28]. Ge-based 1-D nanostructures such as NWs [24], [29]–[31], core–shell NWs, [32]–[35] and NTs [36], [37] can achieve a high specific surface area that provides a free volume to prevent powdering during the lithiation/delithiation process.

In the case of NT structures, wall thickness and diameter are important parameters that affect the maximum hoop stress, and the degree of crystallinity has a significant effect on the expansion behavior of the NT structure during the lithiation process [20]. Single crystal NTs expand anisotropically with structural breakdown, while amorphous NTs expand isotropically without breakdown. Therefore, it is important to understand and control the growth and crystallinity of Si and Ge NTs to improve their structural stability. Incidentally, the surface roughness of one-dimensional nanostructures is also thought to have a significant effect on elastic properties [38].

1.3 Alloy nanowires

Alloying Ge with other elements can provide a platform for the creation and development of innovative materials with desirable and interesting properties.

For example, in SiGe alloy systems, the difference in electronic properties between Si and Ge may allow us to tune the electronic band gap and carrier mobility of the materials. In addition, the lattice mismatch between Si and Ge provides a way to strain Si and further improve its physical properties. The fabrication of SiGe alloy NWs has been reported by our group by thermal annealing of Ge/Si core–shell NWs [39]. As shown in Figure 1.3, The peak corresponding to the SiGe alloy appears at Raman shift of about 400 cm^{-1} after thermal annealing. The intensity of the SiGe peak increased with the annealing temperature up to 700 °C and then decreased due to the fracture of NWs shown in Figure 1.3f.

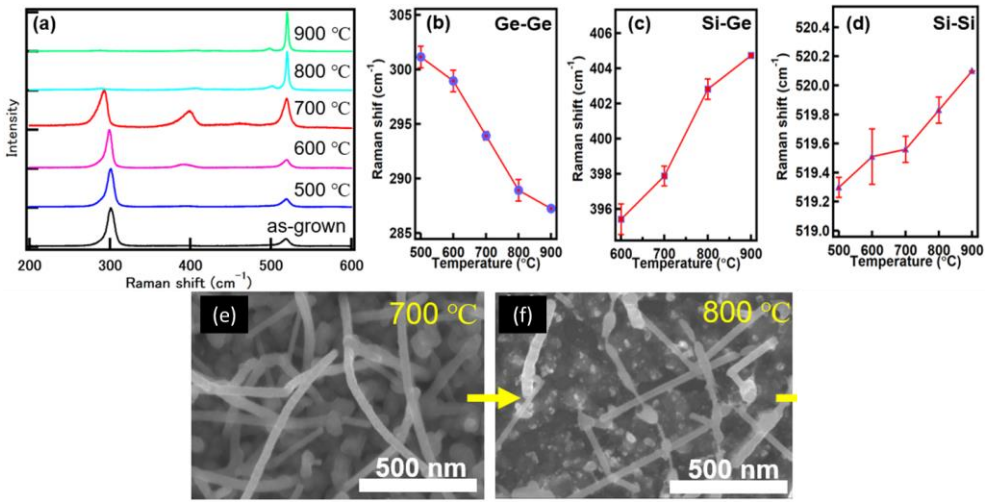

Figure 1.3. (a) Raman spectra of NWs showing SiGe alloy peaks appeared after thermal annealing. Raman shift of (b) Ge, (c) SiGe, and (d) Si optical phonon peaks as a function of annealing temperature. SEM images of SiGe NWs annealed at (e) 700 and (f) 800 °C [39].

GeSn alloy nanowires

The incorporation of Sn into the Ge lattice has received much attention in recent years due to its high carrier mobility, Si-compatibility, and accessibility to achieve direct bandgap structures [40], [41]. Ge has an indirect bandgap property because the minimum value of the indirect conduction band at the L-point of the Brillouin zone (L-valley) is about 140 meV lower than the minimum value of the direct conduction band at the Γ-point (Γ-valley). By introducing Sn, the energy separation between the indirect valley (L) and the direct valley (Γ) becomes smaller, and if the energy of the Γ valley is smaller than that of the L valley, a direct bandgap structure can be realized (Figure 1.4a).

Theoretically, indirect-direct bandgap transitions are predicted to occur when Sn is increased above 6.5–11 at.% in unstrained $Ge_{1-x}Sn_x$ [42], [43]. In addition, direct bandgap emission in the near-infrared region has been experimentally observed with the addition of Sn above 10 at.% [44], [45]. Such narrow bandgap properties of $Ge_{1-x}Sn_x$ alloys make them suitable as luminescent devices for infrared photodetectors and optical data communications [46], [47]. On the other hand, the incorporation of Sn into Ge increases the mobility of electrons and holes by lowering the effective mass of the carriers [43], [48], making $Ge_{1-x}Sn_x$ an ideal material for high-speed MOSFETs. As a group IV semiconductor, the $Ge_{1-x}Sn_x$ alloy is also compatible with CMOS processes based on Si technology.

However, $Ge_{1-x}Sn_x$ thin films grown on Ge or Si substrates can cause compressive strain in the $Ge_{1-x}Sn_x$ layer due to the lattice mismatch between the film and the substrate, resulting in a higher Sn% required for the indirect-to-direct bandgap transition [42]. This problem can be solved by choosing nanowire (NW) structures, as NW structures can accommodate elastic strain due to their large surface area.

In Chapter 3, we will investigate the fabrication of $Ge_{1-x}Sn_x$ NWs using Au–Sn catalysts by CVD method. The morphology, crystallinity, and Sn concentration will be characterized and estimated.

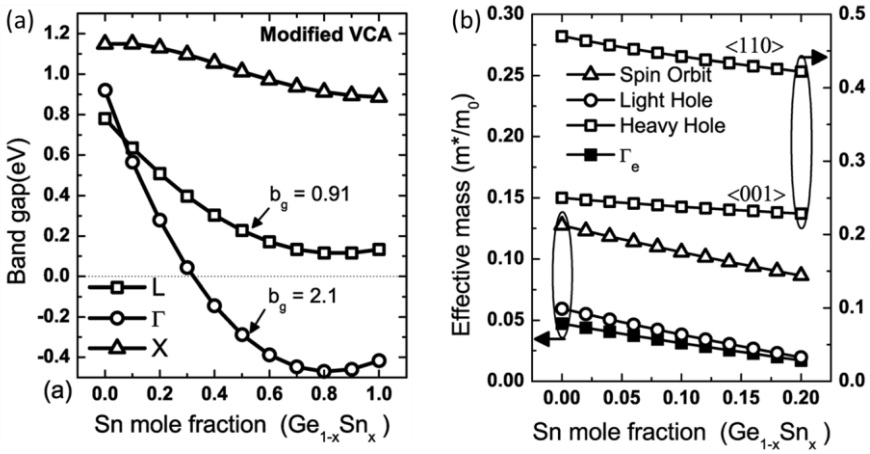

Figure 1.4. Calculated (a) Sn composition-dependent band gap at L, Γ, and X points in the Brillouin zone and (b) Sn composition-dependent electron and hole effective masses at Γ point in GeSn alloy [42].

1.4 Core–shell heterostructures

In heterostructures, materials with different lattice constants need to be matched, but this can only be done up to the limited thickness (critical thickness) before the dislocations happen at the interface [49]. NWs with small size can minimize the lattice mismatch energy through elastic deformation with no misfit dislocation, making them the perfect materials to grow shell layers on them.

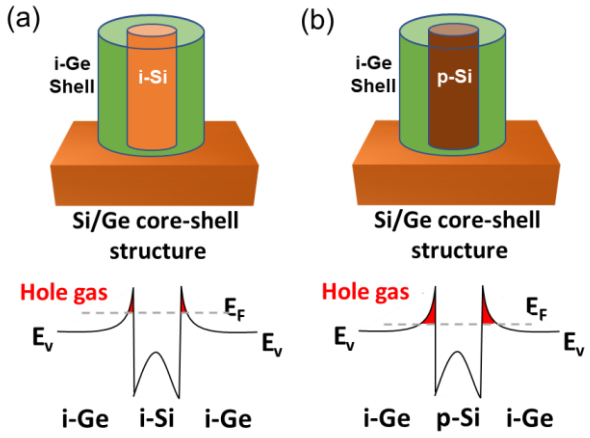

Figure 1.5. Schematic illustration of (a) i-Si/Ge and (b) p-Si/Ge core–shell NWs with corresponding band diagrams. EV and EF are the valence band edge and the Fermi energy, respectively. The hole gas accumulation is represented by red color.

By constructing a heterostructure of Si and Ge, quantum wells can be formed due to the difference in band structures. Therefore, the impurity doping region and the carrier transport region can be separated, and impurity scattering can be suppressed. Figure 1.5 shows the band diagram of the Si/Ge core–shell structure. Hole gas shown in red in Figure 1.5a is generated in the Ge region. When the core of i-Si was changed to p-type Si, the Fermi energy of Si was lowered

and the area where hole gases accumulate was expanded, resulting in an increase in carrier concentration.

In a previous study, our group has demonstrated the hole gas accumulation in i-Ge/p-Si core–shell NWs (Figure 1.6) [50]. As the p-Si shell growth time increases, the Ge optical phonon shift to the lower wavenumber with an asymmetric broadening. This redshift and negative skewness of the Raman line shape is corresponding to Fano effect, which can be used to estimate the carrier concentration of semiconductors. The presence of the Fano effect indicates an increase in carrier concentration, demonstrating the hole gas accumulation in i-Ge/p-Si core–shell NWs.

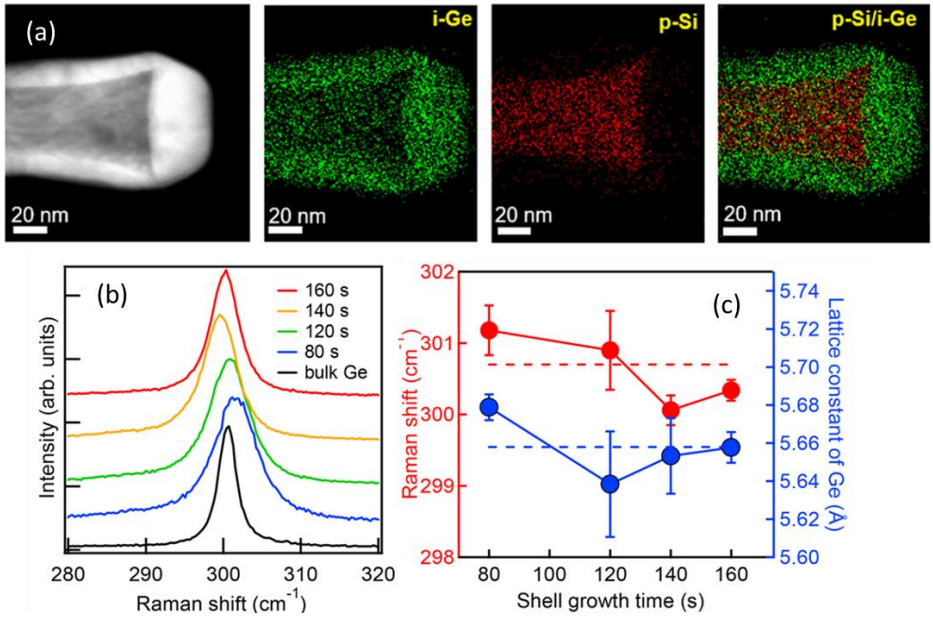

Figure 1.6. (a) STEM image and EDX mappings for Ge and Si of a i-Ge/p-Si core–shell NWs. (b) Raman spectra of the NWs with different shell growth times. (c) Corresponding Raman shifts of Ge optical phonon and lattice constant of Ge shell [50].

However, it is more beneficial to use Ge as the core since Ge NWs can be fabricated by top-down method with very good crystallinity (Chapter 4). On the other hand, hole gas accumulation can be easily controlled by adjusting the dopant concentration of the Si shell during shell formation.

In Chapter 4, We will investigate the fabrication of Ge/p-Si core–shell NW arrays by depositing p-Si shell on the Ge NW arrays, and the hole accumulation in Ge region will be studied and estimated.

In addition, other core–shell NWs, such as ZnO/Si and ZnO/Ge heterostructures, are attracting increasing attention due to their potential applications in energy storage and electronics. ZnO/Ge core–shell NWs significantly improve the cycling stability of Ge anodes in Li-ion batteries by supporting the structure and accommodating volume changes [51]. It was also reported that ZnO/Ge heterojunctions have high on-state current in tunneling field-effect transistors (TFETs) due to their type II band alignment and small effective barrier height [52]. Furthermore, by applying a selective wet etching process, ZnO/Ge core–shell nanowires can be used to fabricate vertically formed Ge NTs with low energy and time consumption [53]. By

increasing the internal space, the NT structure is expected to be able to accommodate its volume changes more effectively [54].

In Chapter 5, we will investigate the fabrication ZnO/Si and ZnO/Ge core–shell NWs. The morphology, crystallinity, and strain will be characterized.

1.5 Fabrication methods

1.5.1 Nanowire fabrication

Vertically aligned nanowire (NWs) fabrication approaches can usually be divided into two categories: bottom-up and top-down. Bottom-up approaches include vapor-liquid-solid (VLS), vapor-solid-solid (VSS), non-catalytic growth, etc. Au-catalyzed VLS growth is the most common method to fabricate group-IV semiconductor NWs with high NW density and high aspect ratio. Au-catalyzed SiNWs [55], GeNWs [56], SiGe NWs and their doping characteristics have been studied thoroughly, and GeSn NWs have become a highly promising semiconductor material due to their superior properties.

Top-down approaches include nanoimprint lithography (NIL), electron beam lithography (EBL), metal-catalyzed electroless etching (MCEE) method, etc. NIL is considered to be among the most desirable for its low cost, high throughput, and zero metal contamination. NIL and Bosch processes have been widely used to achieve SiNW arrays with small diameters and a high aspect ratio [57].

Vapor-liquid-solid growth

Vapor-liquid-solid (VLS) growth is the most widely used bottom-up method for the synthesis of group IV, III-V, and II-VI semiconductor NWs. In the case of growing Si and Ge NWs, VLS growth is usually applied by chemical vapor deposition (CVD), molecular beam epitaxy (MBE), and laser ablation. Wagner first proposed a VLS mechanism of NW growth [58], which is shown in Figure 1.7a. Gaseous Si and Ge precursors, such as silane and germane, flow together with Au and other metal nanoparticle catalysts on the substrate. Given a sufficient temperature, the catalyst can form a liquid eutectic with the growing species. The gaseous precursor then cracks at the surface of the droplet catalyst, thereby supplying additional Si or Ge to the catalyst.

When the concentration of the feed species is higher than the equilibrium concentration, this supersaturation forces the droplet catalyst to precipitate excess Si and Ge, causing them to crystallize layer by layer at the droplet-solid interface. Continuous supply of precursor gas causes the NWs to grow. Since the supply species goes from the gas phase to the liquid phase and then to the solid phase, this process is called the VLS process.

However, when VLS growth is performed, another process called VS (Vapor-Liquid) growth also occurs. This process illustrates the case where the precursor gas cracks directly on the solid surface to form a solid film, as shown schematically in Figure 1.7b. Compared to VLS growth,

VS growth is usually more dramatic at higher temperatures. Figure 1.7c shows a typical NW grown by both VLS and VS processes, where the wire is tapered.

Au nanoparticles are the most commonly used metal catalysts for the growth of Ge NWs by the VLS process. They can be easily synthesized and have excellent chemical stability [59]. The main reason for using Au is the Au–Si and Au–Ge binary phase diagram shown in Figure 1.8. The eutectic point is present at a composition of about 19 at.% Si and 28 at.% Ge and a temperature of 363 °C, and 360 °C, respectively. This eutectic temperature is much lower than the melting point of pure Au, Si, and Ge, which enables the growth of Si and Ge NWs at low temperatures.

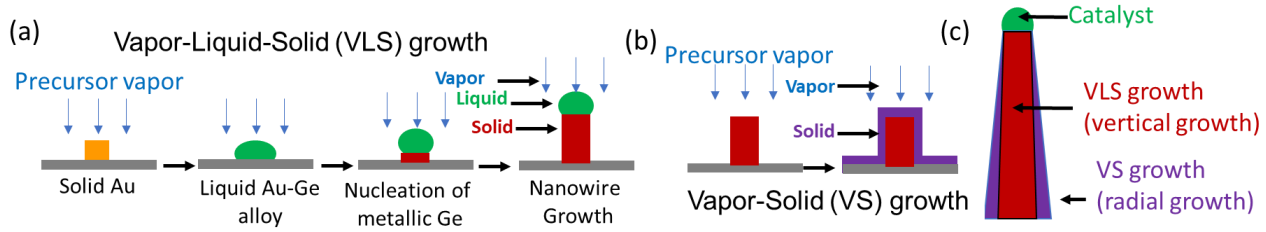

Figure 1.7. Schematic illustrations of (a) the vapor-liquid-solid (VLS) and (b) vapor-solid (VS) growth mechanism. (c) Longitudinal schematic illustration showing a grown NW with both VLS and VS growths involved.

In the VLS mechanism, the growth temperature of NWs should be above the eutectic melting point. However, there are reports of NWs grown at temperatures below the eutectic point [60], [61]. In nanoscale droplets, the capillary effect increases the free energy and decreases the eutectic melting point. The dashed line in Figure 1.8b shows the equilibrium phase diagram of the Au–Ge binary alloy system at the nanoscale. Using this property, NWs can be grown at temperatures 90°C below the eutectic point [62], with no difference in crystallinity.

In Chapter 3, we will investigate the VLS growth of $Ge_{1-x}Sn_x$ NWs using Au–Sn catalysts. The VLS process is believed to have the ability to overcome the solubility of Sn in Ge.

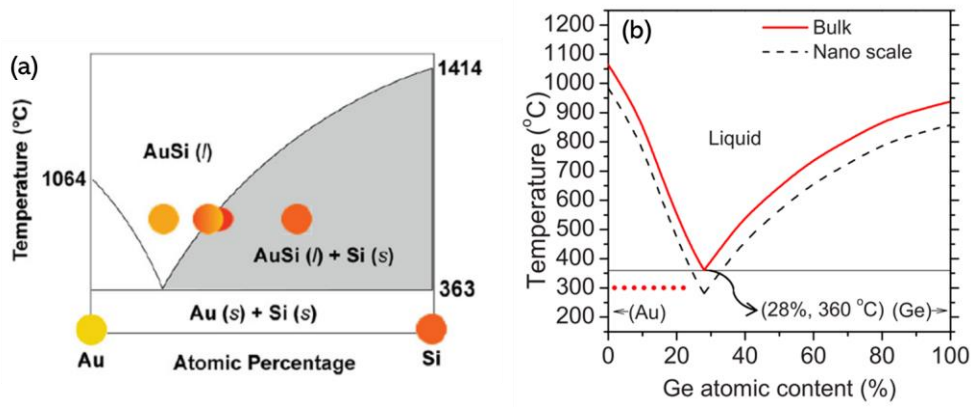

Figure 1.8. (a) Au–Si and (b) Au–Ge binary alloy diagram for nanoscale compared to bulk [63], [64].

Nanoimprint lithography and Bosch etching

Top-down approaches include nanoimprint lithography (NIL), electron beam lithography (EBL), metal-catalyzed electroless etching (MCEE) method, etc. NIL is considered to be among the most

desirable for its low cost, high throughput, and zero metal contamination. NIL and Bosch processes have been widely used to achieve SiNW arrays with small diameters and a high aspect ratio [57].

Nanoimprint lithography is a type of top-down manufacturing method for RIEs, in which a mold is used to transfer patterns for the fabrication of nanostructures [65], [66]. The molds can be fabricated in the desired configuration and used many times, thus achieving high throughput and low cost, which is important for mass production and industrial applications.

The process of nanoimprint lithography is illustrated in Figure 1.9. Since this process is surface sensitive, the surface of the wafer is cleaned using an excimer to avoid defects during the imprinting and etching processes. a UV-curable imprint photoresist was spin-coated onto the substrate. the thickness of the resist layer can be controlled by the composition of the resist and the spin rate. Next, a quartz stamp with a pattern was placed in contact with the photoresist layer and formed a reversed pattern in the photoresist. Then, the transparent quartz mold is irradiated with UV light to cure the photoresist. After detaching the stamp, the reversed pattern is imprinted on the resist. Since there is a thin residual layer of photoresist at the bottom of the imprint hole, a reactive ion etching (RIE) process is carried out to remove the residual layer until the substrate surface is exposed. Next, a thin mask layer is deposited on the imprinted resist pattern. The mask on the top of the resist is lifted-off by chemical, and the mask in contact with the Si surface remains, leaving a patterned hard mask on the substrate.

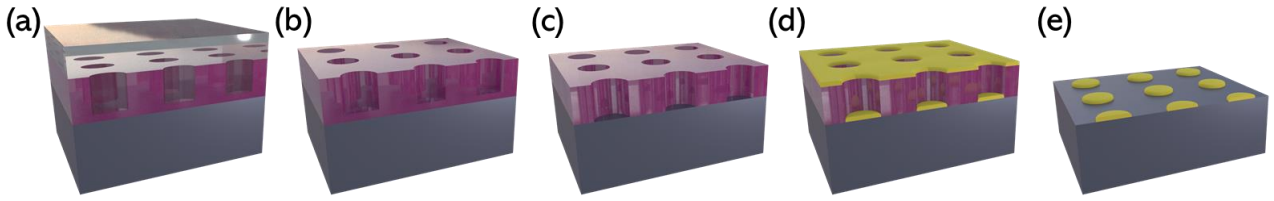

Figure 1.9. Illustration of the process of nanoimprint lithography. (a) Quartz mold attaches to the photoresist coated substrate follower by a UV irradiation. (b) Mold is detached from the substrate with a cured resist. (c) Residual resist is removed by RIE. (d) A hard mask is deposited on the imprinted pattern. (e) resist is lifted-off.

Bosch etching

Deep reactive ion etching (DRIE) of semiconductors is important to form nanostructures with a high aspect ratio. However, conventional plasma etching processes suffer from short etching depths with a tapered shape. In order to fabricate semiconductor NW with a high aspect ratio and non-tapered shape, Bosch etching is introduced to the NW fabrication process.

Bosch process shown in Figure 1.10 consists of a three-step cycle: substrate etching, passivation film deposition, and underlayer passivation film etching. Here, the passivation film is homogeneously deposited on both the top and side walls of the NW, acting as protection during the substrate etching step and suppressing the etching of the side walls. The substrate etching step uses anisotropic etching, in which the sidewalls are etched lee than the bottom surface. By repeating this cycle, long and non-tapered NWs can be achieved. In this thesis, C_4F_8 is used as precursor gas for the passivation, and SF_6 is used as the etching gas.

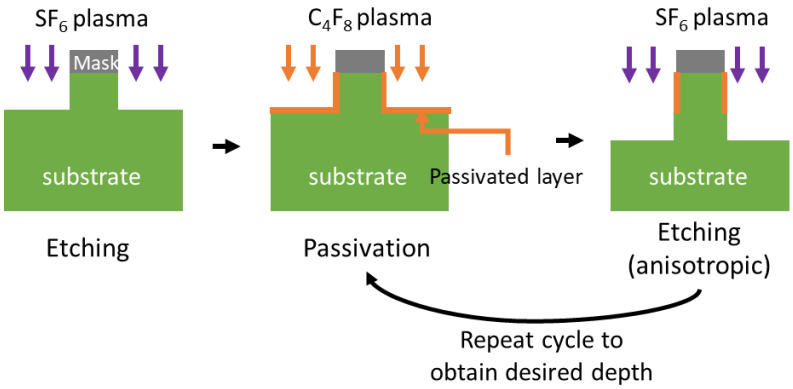

Figure 1.10. Illustration of a Bosch process cycle

Si NW arrays have been successfully fabricated by NIL and Bosch process in our group [50], as shown in Figure 1.11. The fabricated Si NWs show a non-tapered shape with a smooth surface, and the diameter can be reduced down to 50 nm by thermal oxidation and etching process.

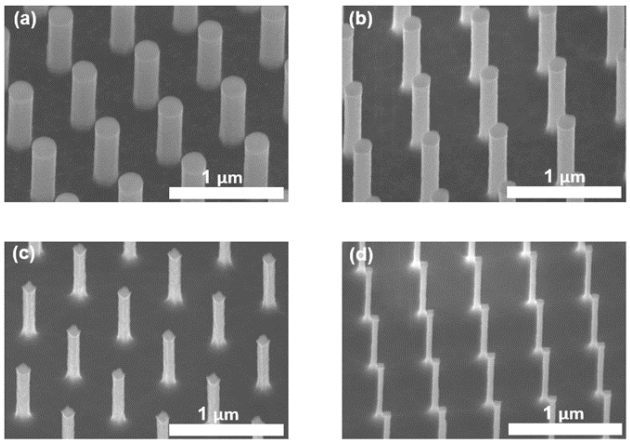

Figure 1.11. (a) 30°-tilted SEM images of Si NW arrays fabricated by NIL and Bosch etching. (b–d) Si NWs after thermal oxidation and wet etching process [50].

Compare to Si, Ge has excellent electronic transport properties, which make it a prime candidate material for fabricating next-generation Si-compatible electronic and optoelectronic devices. Vertical Ge NW arrays are of particular interest due to their large surface-to-volume ratio and high integration that has been proposed to be an ideal material for a high-speed vertical gate-all-around field-effect transistor (FET). However, there are few reports on the top-down fabrication of Ge NW array. This study aims to develop a method to fabricate uniform Ge NW arrays with a smooth surface and a controlled diameter by nanoimprint lithography and wet etching.

In Chapter 4, We will investigate the fabrication of Ge NW arrays by NIL and Bosch etching process. To reduce the diameter of Ge NW, the wet chemical etching will be studied.

1.5.2 Nanotube fabrication

SiNTs are mainly synthesized using one-dimensional sacrificial templates: Si shell layers are deposited on templates such as ZnO [15], [18], Ge [22], [67], and MgO [68] NWs, and then the templates are selectively etched to form SiNTs.

On the other side, top-down techniques using lithography [69]–[71] and self-assembled nanosphere bead templates [72]–[74] have been developed to fabricate SiNTs. The fabricating processes usually require complex fabrication processes, long processing times, or the use of precious metals.

In addition, other methods such as chemical etching [75] and electrochemical formation [76] cannot produce vertically aligned SiNTs, which limits their applications.

One-dimensional sacrificial templates approach

Among all the one-dimensional sacrificial templates methods, using ZnO nanowire (NW) is regarded as a low-cost, convenient, and controllable method for the fabrication of SiNTs and GeNTs. As shown in Figure 1.12, Vertically aligned ZnO NWs are synthesized by hydrothermal method at a temperature below 100 °C, followed by the deposition on the ZnO template with a Si shell layer using chemical vapor deposition (CVD) methods. Finally, the ZnO core is selectively etched by a reduction process at 600 °C with 50% H_2 in N_2 for 24 hours [15]. However, this etching process is very time and energy-consuming, hindering the mass production of NTs in the future.

In Chapter 5, we will investigate the fabrication of SiNTs and GeNTs by wet etching the ZnO of ZnO/Si(Ge) core–shell NWs. The morphology, crystallinity, and strain will be characterized.

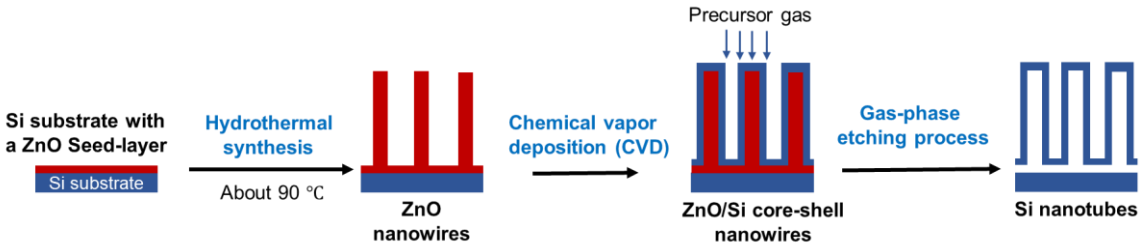

Figure 1.12. Illustration of the fabrication process of vertically aligned Si and Ge NT using ZnO NW sacrificial templates method.

Top-down approach

Unlike sacrificial templates methods, top-down approaches provide vertical 1D structure with smooth surface, high crystal quality, and highly ordered arrangement, which make them suitable for electronic applications. Lithography [69], [71], and self-assembled nanosphere bead templates [72]–[74] have more recently been developed to fabricate SiNTs, but the fabricating process is complicated and has a long processing time or disordered arrangement.

Recently, Si NTs fabricated by using spacer patterning technique and metal-assisted chemical etching (MCEE) have been reported [70]. Spacer patterning is known as one of the techniques used to overcome the resolution limit in the semiconductor industry [77].

As shown in Figure 1.13, The spacer is a layer deposited to cover a pattern made by conventional lithography. Next, the spacers are etched anisotropically so that the horizontal spacer layer is etched away, leaving the remaining spacers on the side walls. The remaining spacers act as a new mask with the pattern doubled, giving a higher resolution than the original mask. In the case of nanohole pattern, the spacer patterning technique can result in a ring-like mask, which can be used for NT etching.

In Chapter 6, we will develop a fabrication method depending on NIL and spacer patterning technique to fabricate Si NT arrays. The geometry of NT will be investigated and controlled.

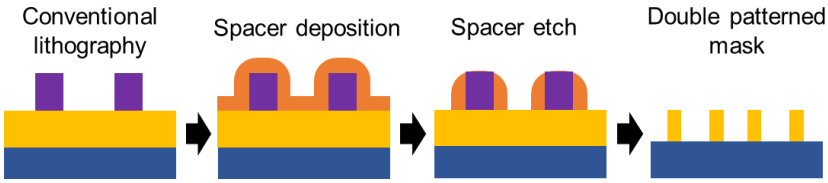

Figure 1.13. Illustration of spacer patterning technique.

1.6 Characterization techniques

Scanning electron microscopy (SEM) was used to study the morphology (geometry shape, surface roughness, number density, and growth direction) of the samples. Transmission electron microscopy (TEM) was used to investigate the morphology (detailed shape, heterostructure, and growth direction), crystallinity (strain, grain size, dislocation, defects, etc.) of samples. TEM-Selected area electron diffraction (SAED) was used to investigate the crystallinity of the samples. TEM-electron dispersive X-ray (EDX) spectroscopy was used to study and estimate the elemental distribution and composition in the samples. Electron spin resonance (ESR) spectroscopy was used to investigate the dangling band-type defects of the samples. Ultraviolet-visible near-infrared (UV-vis-NIR) spectroscopy was used to measure the reflectance of the samples. Raman scattering and X-ray diffraction (XRD) will be discussed below.

1.6.1 Raman scattering

Raman scattering spectroscopy is a non-destructive and contactless analysis technique that can provide detailed information on the strain, composition, impurity doping, and crystallinity of semiconductors. Due to the short penetration depth (10 nm) of 355 nm excitation light in Si, micro-Raman scattering is able to probe the surface of nanostructures.

Strains in crystal can be defined in terms of changes in the lattice constant, which will cause the Raman shift of the phonon peaks. Normal compressive strain corresponds to unit cell

shrinkage, resulting in a blueshift of the peak. On the other hand, tensile strain corresponds to enlargement of the unit cell and leads to a redshift of the peak.

The compositional dependence of Raman shift in alloys can be derived by analyzing the atomic distribution information. For group-IV semiconductor alloys (such as $Si_{1-x}Ge_x$ and $Ge_{1-x}Sn_x$), the Raman shift of the host materials can be expressed as the sum of a mass-disorder term and a bond distortion term as follows [78]

$$\Delta\omega_{alloy}(x) = -A\omega_0 x - B\frac{\Delta R(x)}{R_0}\omega_0 \qquad 1.1$$

Where ω_0 is the Raman frequency of the host materials and R_0 is the bond length of the host materials. Here, $R(x)$ is related to the lattice constant

$$\frac{\Delta R(x)}{R_0} = (1 - a^{**})\frac{\Delta a(x)}{a_0}) \qquad 1.2$$

Where a^{**} is bond rigidity parameter and a_0 is the lattice constant of host materials. Since $\Delta a(x)$ is leaner in x according to Vegard's law, Equation 1.1 and 1.2 result in a linear compositional dependence for the Raman frequency and can be used to estimate the composition of semiconductor alloys.

Raman scattering also can be used to investigate the electrical activity of dopant atoms with the Fano effect.

Fano interference

The energy of Raman optical phonon overlaps with the intervalence band excitations (continuum), which are generated by doped semiconductors. As a result, the overlap between the discrete level and the continuum causes interference effects, a phenomenon is known as Fano interference. This interference causes asymmetry, broadening, and peak shift in the Raman line shape [79]–[84], which can be described by the Fano function as follows

$$I(\omega) = I_0\frac{(q+\varepsilon)^2}{(1+\varepsilon^2)} \qquad 1.3$$

where ω is the wavenumber, I_0 is the prefactor, q is the asymmetry parameter, and $\varepsilon = (\omega - \omega_p)/\Gamma$. Here, ω_p is the phonon wavenumber and Γ is the line width-related parameter [80]. These Fano parameters represent the shape of Raman phonon peaks, which can be used to estimate the doping concentration in semiconductors. As shown in Figure 1.14, As the Si doping concentration increases, the phonon peak shifts to the higher wave number and becomes broadened with positive skewness (Fano parameter $q > 0$). While the phonon peak of doped Ge exhibits a redshift with negative skewness ($q < 0$).

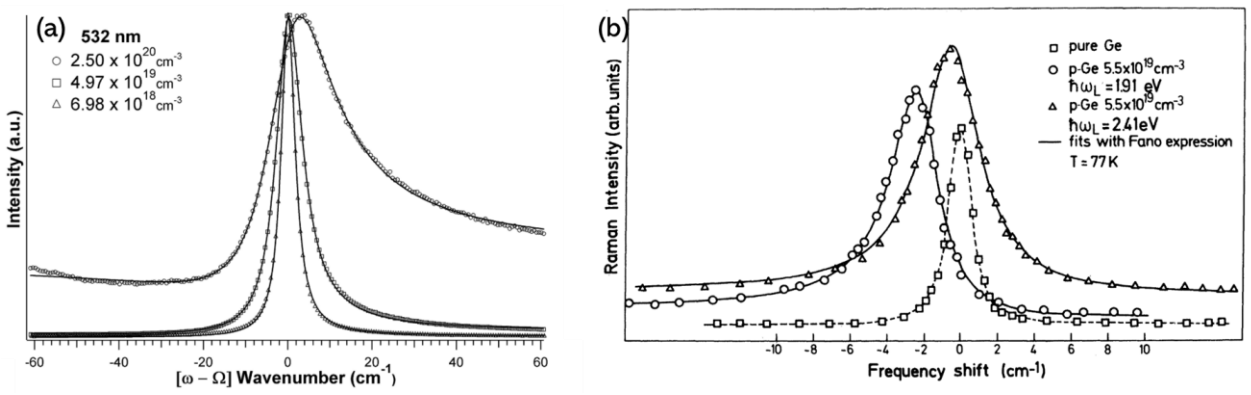

Figure 1.14. (a) Raman spectra for p-Si with different doping concentrations at an excitation wavelength of 532 nm [79]. (b) Raman spectra for p-Ge using different energies of excitation light [85].

Phonon confinement

It is observed that as the size of nanostructure decreases, the peak of the optical phonon broadens and shifts to the lower wavenumber side (Figure 1.15a). These downshifts and asymmetric broadening can be explained by the phonon confinement [86]–[89].

According to the Heisenberg uncertainty principle, when the uncertainty of position becomes small, the possible wavenumber of phonon becomes wide. This is called phonon confinement. Richter et al. [90] and Campbell and Fauchet [91] (RCF) reported that the phonon confinement model and the Raman intensity are given by

$$I(\omega) = \int \frac{|C(0,q)|^2}{[\omega - \omega(q)]^2 + (\Gamma_0/2)^2} d^3q \qquad 1.4$$

where $C(0,q)$ is the Fourier coefficient of the confinement function, $\omega(q)$ is the phonon dispersion, and Γ_0 is the full width at half maximum (FWHM) of the reference bulk material.

In the case of Ge NWs, $|C(0,q)|^2 = \exp(-q^2D^2/16\pi^2)$ and $\omega(q) = \{X + Y\cos[q(a/2)]\}^{0.5} + Z$, with $A = 0.69 \times 10^5$ cm^{-2} and $B = 0.195 \times 10^5$ cm^{-2} [89].D is the diameter of GeNWs, Z is an adjustment parameter for reference samples. The X and Y values are derived from fitting the $\omega(q)$ with the Ge TO dispersion. From the calculated Raman shift and FWHM in Figure 1.15b,c, we can see that the optical phonon peak broadens and shifts to lower wavenumbers as the diameter decreases.

For materials with a small grain size, its phonon peak also shows redshift and asymmetric broadening due to the phonon confinement effect.

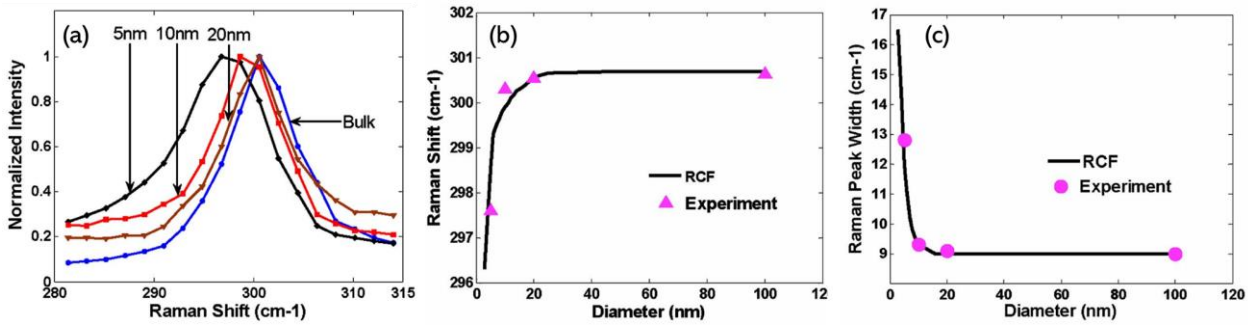

Figure 1.15. (a) Raman spectra of GeNWs with different diameters. Comparison of experiment results and RCF model results in terms of (b) Raman shift and (c) FWHM [89].

1.6.2 X-ray diffraction

X-ray diffraction (XRD) is widely used to characterize and analyze the material by its characteristic peaks. In this thesis, the diffraction peaks are fitted with the Pseudo-Voigt function, and the peak position and width are used to study the composition, crystallinity, and strain of the samples.

For the same crystal structure, Vegard's discovered that the lattice constant of a solid mixture of two materials ($A_{1-x}B_x$) is approximately a weighted mean of the lattice constants of materials A and B, which can be used to estimate the composition of alloy materials. This Vegard's law can be written as:

$$a\mathrm{A}_{(1-x)}\mathrm{B}_x = a_\mathrm{A}(1-x) + a_\mathrm{B}x \qquad 1.5$$

In the case of $Ge_{1-x}Sn_x$ alloy, the Sn composition x can be estimated linearly according to Vegard's law.

$$a\mathrm{Ge}_{(1-x)}\mathrm{Sn}_x = a_\mathrm{Ge}(1-x) + a_\mathrm{Sn}x \qquad 1.6$$

Here, the a_Ge lattice constant of the bulk Ge (0.56576 nm) and a_Sn is the lattice constant of bulk α-Sn (0.64892 nm).

It is well known that as the grain size becomes smaller, the X-ray diffraction peaks broaden according to Scherrer's equation. This is due to the fact that imperfections such as misfit dislocations, small grains, twin defects in the crystal lead to lattice size inhomogeneity, which contributes to the width of the diffraction peak. The width of the peak can be used to characterize the crystallinity of the materials.

Compressive and tensile strain in the materials can be estimated from the change in lattice constant. Since Si, Ge, and α-Sn are all diamond structures (FCC), the lattice constant can be calculated by

$$d = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \qquad 1.7$$

Where d is the d-spacing, a is the lattice constant, and h, k, and l are the Miller indices. If the lattice value is less than the bulk value, it indicates compressive strain of the material, and vice versa, tensile strain.

1.7 Aims and outline

The aim of this thesis was to investigate the fabrication of vertically aligned group-IV semiconductor NWs and NTs and study their morphology, crystallinity, strain, doping, and other electrical and optical properties for the application in electronics and optoelectronics in the future.

In this thesis, NWs including alloy NWs ($Ge_{1-x}Sn_x$ NWs), core–shell heterostructure NWs (ZnO/Si and ZnO/Ge core–shell NWs), and ordered top-down NW arrays (Ge NW arrays) were investigated. NTs including low-cost NTs (Si NTs and Ge NTs) and ordered top-down NT arrays (Si NT arrays) were investigated.

The outline of this thesis is the following.

Chapter 2 introduced the experimental techniques.

In Chapter 3, the growth of $Ge_{1-x}Sn_x$ NWs using Au–Sn catalysts by CVD method was investigated. The results are divided into the following parts:

- We studied the effect of the deposition order and growth temperature on VLS growth. The morphology of the sample surface after VLS growth was investigated by SEM.
- We studied the morphology and crystallinity of the fabricated $Ge_{1-x}Sn_x$ NWs by SEM, TEM, and SAED analysis. Twining defects in the NWs are discussed in detail.
- We studied the elemental distribution, Sn content, and crystallinity of $Ge_{1-x}Sn_x$ NWs by Raman scattering, EDX, and XRD analysis. The obtained Sn content is much higher than the equilibrium solubility of Sn in Ge.
- The growth direction preference of $Ge_{1-x}Sn_x$ NWs was studied by SEM. The contribution of Sn to the free energy of NW was investigated using Schmidt's model.
- Growth and doping concentration of Boron-doped $Ge_{1-x}Sn_x$ NWs were investigated by SEM and Raman scattering analysis. The doping effect on the Sn corporation was also discussed.

In Chapter 4, the fabrication of Ge NW and Ge/p-Si core–shell arrays by NIL method was investigated. The results are divided into the following parts:

- We studied the morphology of the fabricated Ge NW array by SEM. H_2O_2 solution was used to reduce the diameter of the NWs.
- We studied the morphology of fabricated Ge/p-Si core–shell arrays. The hole gas accumulation in Ge region was investigated by Raman scattering.

In Chapter 5, the fabrication of SiNTs and GeNTs by wet etching the ZnO of ZnO/Si(Ge) core–shell NWs was investigated. The results are divided into the following parts:

- We studied the growth of ZnO NW templates fabricated by hydrothermal synthesis.
- We studied the growth, morphology, crystallinity, and elemental distribution of ZnO/Si core–shell NWs and Si NTs by SEM, TEM, SAED, EDX, Raman, and XRD. Thermal annealing is performed to crystalized the Si.
- We studied the growth, morphology, crystallinity, and elemental distribution of ZnO/Ge core–shell NWs and Ge NTs by SEM, TEM, SAED, EDX, Raman, and XRD.

In Chapter 6, the fabrication of Si NT arrays using NIL with spacer patterning were investigated. The results are divided into the following parts:

- We studied the fabrication process of Si NT arrays by controlling their lengths, diameters, and wall thicknesses.
- The morphology of fabricated Si NT arrays was investigated by SEM from top- and cross-sectional views. The geometry was measured and quantified using ImageJ.
- ESR was carried out to study and estimate the dangling bond-type defects in NTs.
- The reflectance of the NT arrays was measured by UV-vis-NIR spectroscopy. The results are compared with Si NT arrays.

Chapter 2

Experimental

In this chapter, a brief overview of the experimental and characterization techniques used in this thesis is given.

2.1.1 Chemical vapor deposition

A cold-wall ultra-high vacuum chemical vapor deposition (UHV-CVD) system was used to perform ultra-high vacuum Si or Ge thin film deposition. The system consists of a load-lock chamber for loading samples and the main chamber for performing the CVD process. The sample is loaded into the load-lock chamber, then transferred to the main chamber for deposition, and finally transferred back to the load-lock to be unloaded. A schematic of the system layout of the system is shown in Figure 2.1.

Ultra-high vacuum is obtained using multiple turbo molecular pumps (TMPs) to ensure the low impurities in the chamber before the deposition. The system is equipped with silane, germane, diborane, hydrogen, nitrogen, etc. for intrinsic or doped semiconductor film deposition.

The sample is set on a holder upside down in the load-lock and then pumped using a TMP-backed rotary pump (RP). After reaching the desired vacuum level, the sample is transferred to the main chamber using a transfer arm. The holder is set to separate the main chamber for preventing the precursor gas from entering the upper area of the chamber during the growth. The main chamber is pumped by two TMPs backed by a dry pump (DP) to maintain a pressure of 2×10^{-6} Pa. Prior to the growth process, the TMPs and DP are stopped and 30 sccm of N_2 is injected into the main chamber. The temperature during growth can be controlled by a heater at the top of the sample holder, and after the desired temperature is reached, the precursor gas is injected keeping the total pressure at about 700 Pa. To stop the growth, turn off all the gases and heaters, and turn on the DP and TMP to pump out any residual gas in the main chamber.

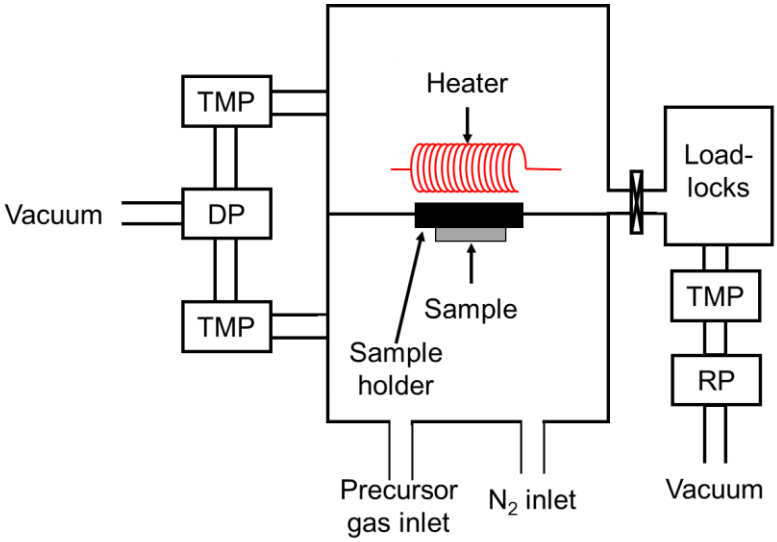

Figure 2.1. Schematic diagram of a chemical vapor deposition (CVD) system.

2.1.2 Scanning electron microscopy

A scanning electron microscopy (SEM) is a tool for observing the surface of a sample by scanning the surface of the sample with a focused electron beam. A schematic diagram of the SEM is shown in Figure 2.2. The SEM consists of four main components: a vacuum system that maintains the high vacuum necessary for the propagation of electrons; an electron optical system that converges the electron beams emitted from the electron gun and irradiates them while scanning the sample in two dimensions; a detection system that detects the electrons emitted from the sample and converts them into electrical signals; and a system that displays the electrical signals as images.

The electron beam emitted from the electron gun at the top of the SEM passes through the Wehnelt electrode, is focused to an extremely small spot by the condenser lens and objective lens, and finally enters the sample. Between the condenser lens and the objective lens is a scan coil, which controls the entering position of the electron beam on the sample. When a specimen interacts with an electron beam, various signals are emitted such as secondary electrons, back-scattered electrons, Auger electrons, X-rays, and photons. Here, the detector detects the secondary electrons, which have the largest amount of signal. The secondary electron image is obtained by displaying the intensity of the secondary electrons on a cathode-ray tube (CRT) in synchronization with the primary electron beam scanning over the sample surface. The convex part of the surface is brighter because it generates more secondary electrons, while the concave part is darker. Here, a Hitachi SU8000 cold field emission SEM (FE-SEM) with a spatial resolution of about 1 nm was used at an acceleration voltage of 5 and 10 kV to characterize the morphology of the samples.

The sample must be conductive to be observed by SEM. If the sample is not conductive, incident electrons will accumulate and inhibit the scattering and transmission of incident electrons. This is called charge-up, and the SEM images will show abnormal contrast and distortion. In order

to produce better quality images, the non-conductive sample needs to be sputter coated with conductive materials.

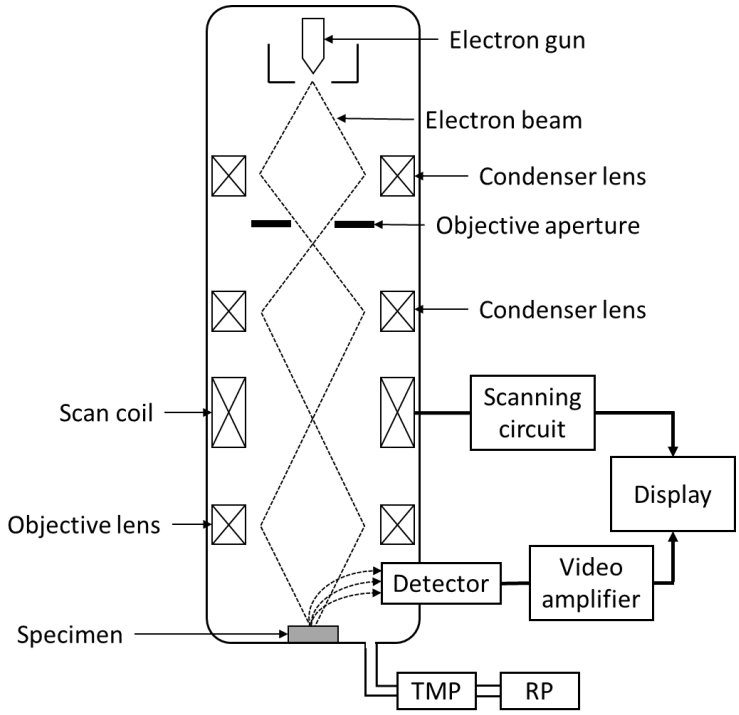

Figure 2.2. Schematic illustration of a scanning electron microscope (SEM).

2.1.3 Transmission electron microscopy

Transmission electron microscopy (TEM) is a type of microscopy technique that uses an electron beam accelerated at tens to hundreds of kV to transmit electrons through a sample and obtain a magnified image of fine detail. A schematic diagram of the SEM is shown in Figure 2.3. The A TEM consists of three main components: A vacuum system that maintains the high vacuum necessary for the propagation of electrons; an electron emission system that uses an electron gun and multiple lenses to emit and control the electron beam; and a recording system that observes the image on a fluorescent plate and records it with a CCD.

Another operation mode in TEM is shown in Figure 2.3b. When switching to diffraction mode, electron diffraction can occur if the atoms are arranged periodically. Some electrons are scattered at a specific angle determined by the crystal structure, while others pass through without being deflected. As a result, we can obtain diffraction patterns with a variety of information about the crystal, such as lattice constants, symmetry, and defects. On the other side, Energy dispersive X-Ray (EDX) analysis can be performed simultaneously with TEM observation, enabling distribution and quantitative analysis of the elemental composition of materials. Here, a JEOL 2100F TEM was used at an acceleration voltage of 200 kV to characterize the morphology, crystallinity of the samples. The selected area electron diffraction (SAED) and EDX analysis were used to study the crystal structure and elemental composition of the samples.

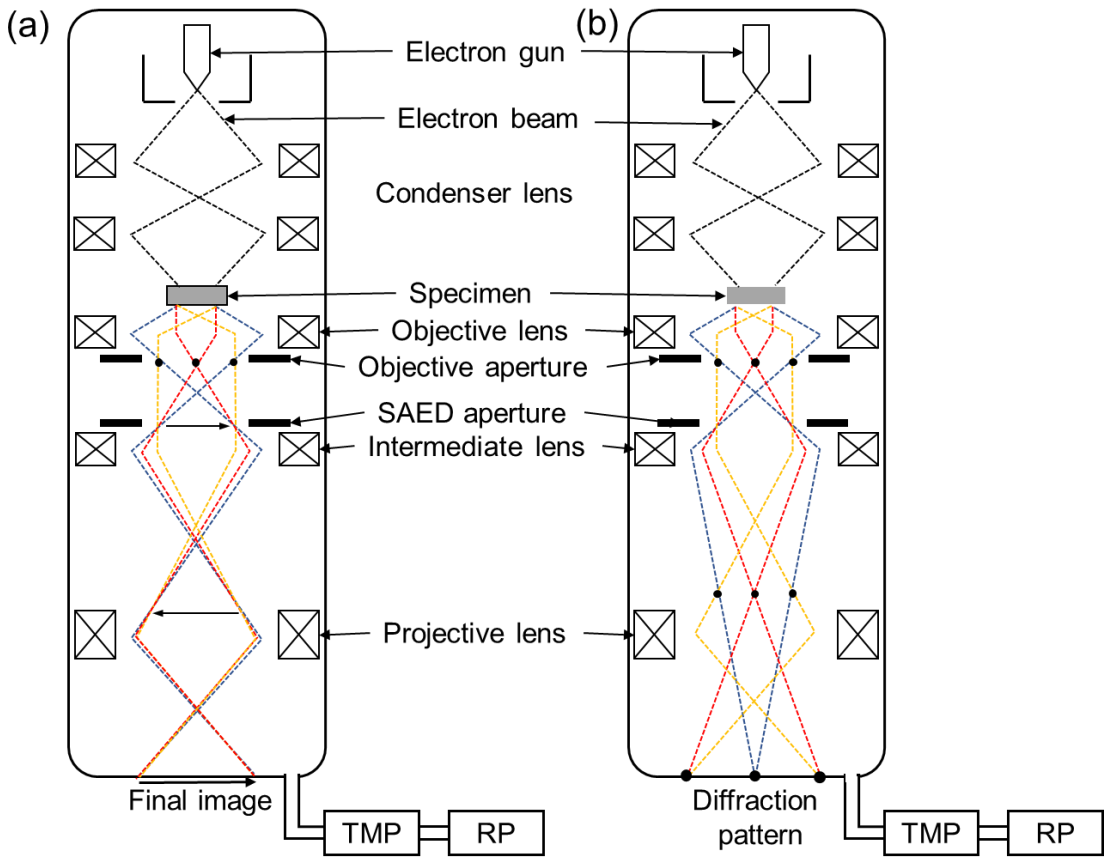

Figure 2.3. Schematic illustration of a transmission electron microscope (TEM) and ray diagrams in (a) imaging mode and (b) diffraction mode.

2.1.4 Raman spectroscopy

The energy of the incident excitation light induces a polarization of the molecules in the material, and the molecules can be excited to a higher energy state, which is called the virtual state. when the molecules drop back to the ground state, two types of luminescence are generated. The first is that the energy of the emitted light is the same as the incident light, which is called elastic or Rayleigh scattering. The other is called Raman scattering, where energy transfer occurs between molecules and scattered photons. If the molecules return to a different energy level, the photon loses or gains energy as a Stokes or anti-Stokes scattering shift. The Jablonski diagram and the corresponding spectra are shown in Figure 2.4.

Micro-Raman scattering measurements (Photon Design) with a spectral resolution of about 0.3 cm^{-1} were performed at room temperature. Three types of excitation light sources (355 nm, 532nm, and 633 nm) are used according to the sample and purpose. The scattered photons are passed through a filter to remove elastically scattered components, and a diffraction grating is used to separate the photons with different energy of the inelastic components. The photons are recorded by a CCD detector, which is cooled to −125 K by liquid nitrogen. The computer then plots the difference between Raman and Rayleigh scattered light against wavenumber. In the

case of measuring nanostructure, the power of the incident light was set to about 0.02 mW to avoid local heating effects [86], [92].

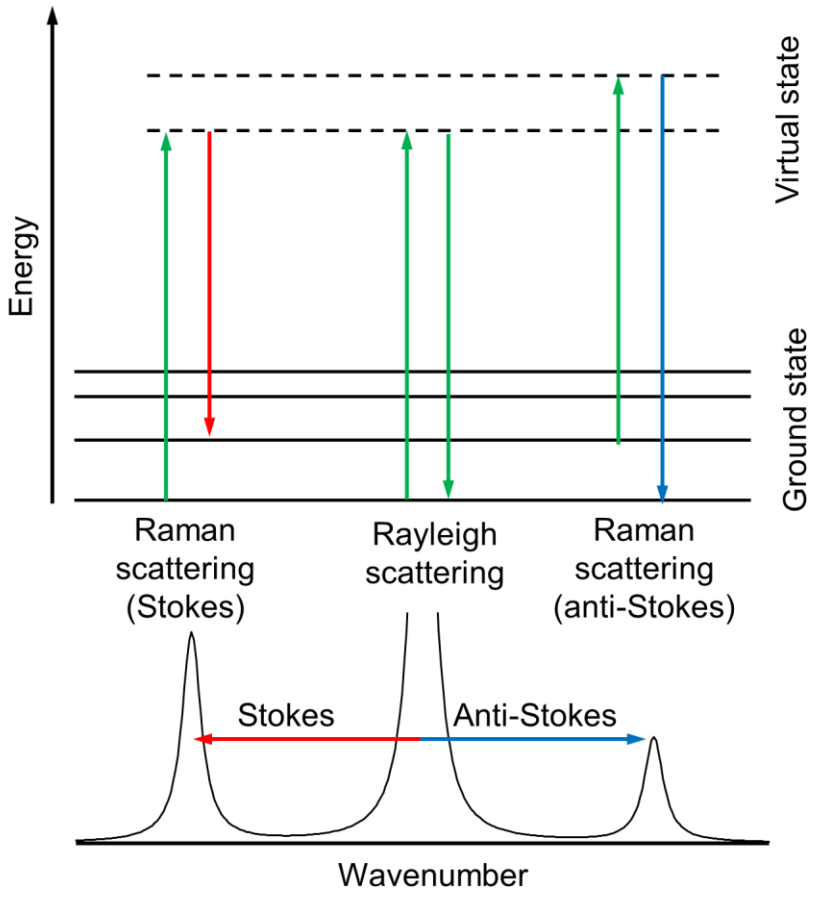

Figure 2.4. Jablonski diagram and spectra of Raman (stokes and anti-stokes) and Rayleigh scattering.

2.1.5 X-ray diffraction

X-ray diffraction (XRD) is an analytical technique that uses the diffraction of X-rays by crystals to measure the distance between atoms. When X-rays with a wavelength equivalent to the atomic spacing are incident on a material in which atoms are regularly arranged, they may be diffracted and interfere with each other and cause constructive interference. The relationship between the diffraction angle and the atomic spacing can be described using the following Bragg's law.

$$2d\ sin\ \theta = n\lambda \qquad 2.1$$

where d is the crystal parallel plane distance, θ is the angle of incident X-ray, n is an integer, and λ is the X-ray wavelength. By moving the X-ray tube or detector, this constructive interference with respect to the angle can be recorded. The spectrum consists of multiple peaks

corresponding to multiple crystal planes with different d values, which can be used to identify different crystalline materials.

A PANalytical X'Pert Pro MRD XRD system was used to investigate the strain and crystallinity of the samples. A voltage of 45 kV is applied between the filament (current: 40 mA) and the Cu source, and the emitted X-rays (Cu Kα1 wavelength: 1.540598 nm) are focused and extracted at a single wavelength with high directionality. the scattered waves are detected by the detector. The schematic illustration of the optical arrangement is shown in Figure 2.5, where ω is the incident angle (between X-ray source and sample) and 2θ is the diffraction angle (between the incident beam and detector).

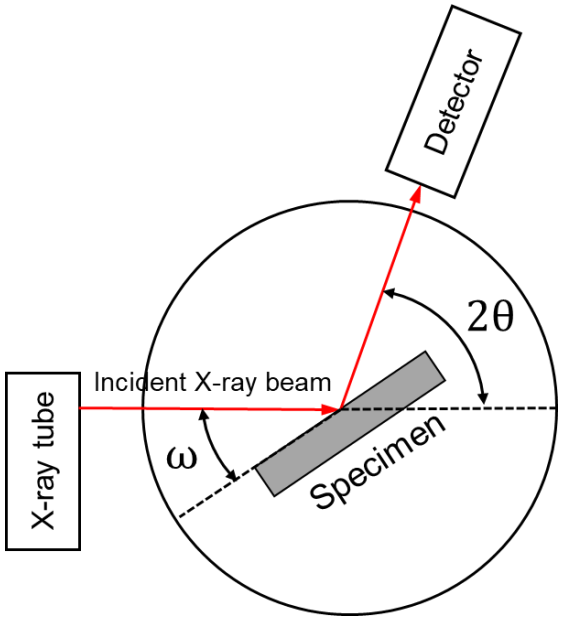

Figure 2.5. Diffraction beam path in an X-ray diffraction (XRD) system.

2.1.6 Electron spin resonance spectroscopy

An external magnetic field can split the spin states of unpaired electrons in materials. The transition between these spin states can be induced by applying electromagnetic energy, such as microwave, and its absorption spectrum is expressed as electron spin resonance (ESR).

Consider the case of an isolated electron with angular momentum $S = 1/2$. The electron is placed in an external magnetic field H_0, and an electromagnetic wave of frequency υ is applied perpendicular to this field. The degenerated energy splits into two levels (Zeeman effect), and the spin quantum number $m_s = \pm 1/2$. The energy here is

$$E = g\beta H_0 m_s \qquad 2.2$$

where g is called the g-factor (g = 2 for an isolated electron), β is the Bohr magneton. When $\Delta m_s = 1$ between, the energy difference between the two levels is

$$\Delta E = g\beta H_0 \qquad 2.3$$

When the transition occurs, the energy hυ of the electromagnetic wave is equal to the energy difference between the levels.

$$h\upsilon = g\beta H_0 \qquad 2.4$$

The above discussion only considers a simple system of isolated electrons. However, in reality, unpaired electrons rarely exist in isolation but interact with other atoms. This contribution appears as a correction to the g-factor.

$$g = g_e + \Delta g \qquad 2.5$$

where g_e is the value for free electron with relativistic correction, and Δg includes the contribution from the interaction of unpaired electrons with other electrons.

Electron spin resonance spectroscopy (ESR) is a useful tool to study the behavior of defects with unpaired electrons in Si NWs [93]–[95]. The line shape of the ESR absorption spectrum can be approximated expressed as a Gaussian or Lorentzian function [96]. Here we will use the Pseudo-Voigt function, which is a linear combination of Gaussian function and Lorentzian function.

$$Y(H) = A\left[m_u \frac{2}{\pi}\frac{w}{4(H-H_0)^2+w^2} + (1-m_u)\frac{\sqrt{4\ln 2}}{\sqrt{\pi}w}\mathrm{e}^{-\frac{4\ln 2}{w^2}(H-H_0)^2}\right] \qquad 2.6$$

where A is area under the curve, m_u is the ratio of the Lorentzian and Gaussian function. H_0 is the magnetic field value at the center, and w is the full width at half maximum (FWHM). Since the ESR spectrum is the first derivative of the absorption spectrum, a derivative from of Equation 2.6 was used to fit the experimental data. In this thesis, the A value of the defect signal (g = 2.005) is used as the ESR signal intensity to estimate the defects in the samples.

Here, we used a JEOL JES-FA200 (100 kHz) ESR system at 4.2 K with a micropower of 1 mW to detect the defect in samples. Figure 2.6 shows a schematic diagram of the ESR system. A Gunn diode with X-band was used as the microwave source. The microwaves emitted from the source pass through an isolator, and are then separated by a directional coupler into a signal and reference microwave. For the signal side, a microwave attenuator adjusts the power of the microwaves and a circulator guides them to the cavity resonator.

When ESR absorption occurs, the Q-value of the cavity resonator changes, and so does the reflection of the microwave, which is modulated by the magnetic field and detected by a balanced mixer consisting of a magic T and two detector diodes. The detected signal passes through amplifiers and a lock-in detector, where the waveform is measured.

The sample was placed in a fused silica tube and inserted into the center of the cavity. The signal intensity in each measurement was normalized by the ESR signal intensity measured from $MgO:Mn^{2+}$ maker.

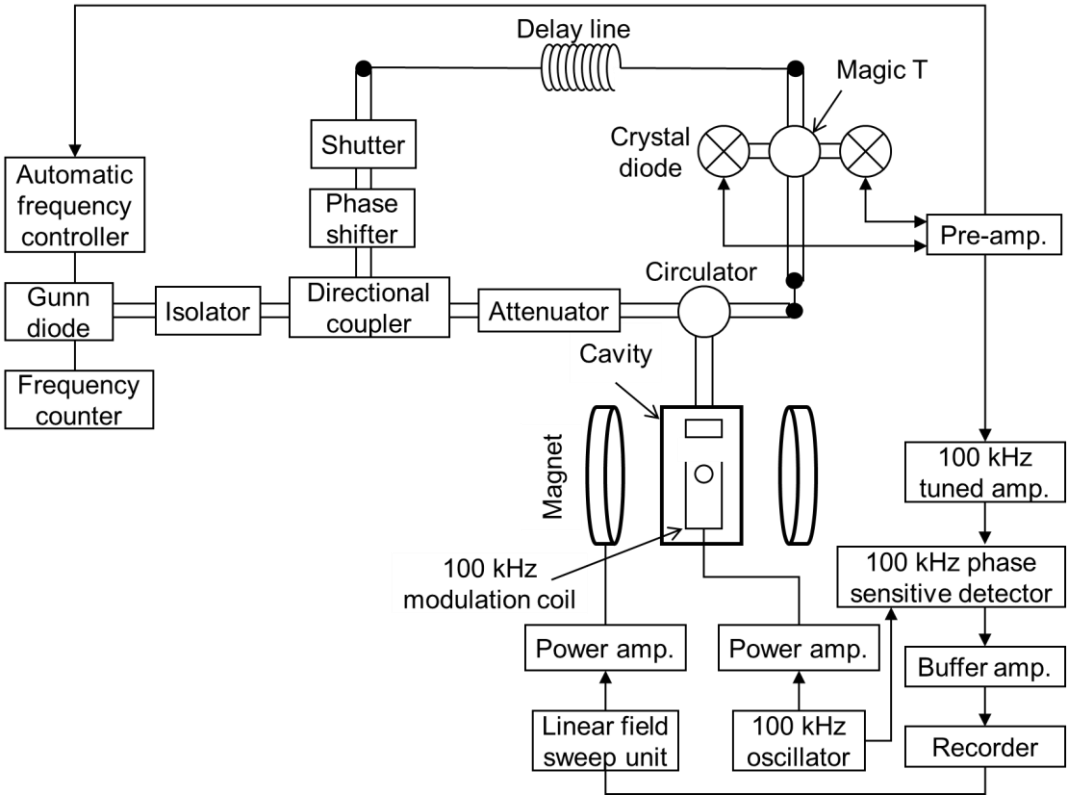

Figure 2.6. Scheme of a standard (X-band) electron spin resonance (ESR) spectrometer

Chapter 3

Au–Sn catalyzed $Ge_{1-x}Sn_x$ nanowires

$Ge_{1-x}Sn_x$ nanowires (NWs) have attracted much research attention for their potential to realize next-generation electronic and optoelectronic devices that are compatible with Si. In order to control the growth of NWs and to increase their Sn content, it is necessary to understand their growth mechanism.

The fabrication of $Ge_{1-x}Sn_x$ NWs requires low temperature to minimize Sn segregation and a non-equilibrium incorporation mechanism due to the very low (<1%) equilibrium solubility of Sn with respect to Ge [97]. These requirements can be met by a VLS growth mechanism that provides a growth temperature lower than the eutectic point [60], and over-equilibrium Sn incorporation by a solute trapping process performed in a step-flow kinetic [98], [99].

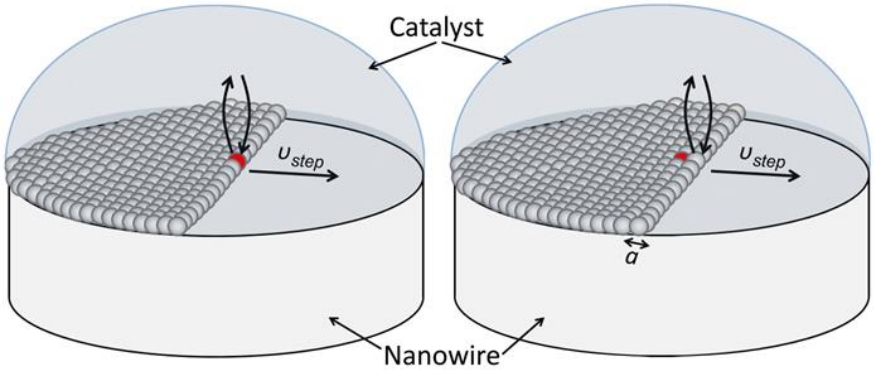

Figure 3.1. Schematic illustration of step-growth process in the catalyst during VLS growth [98].

A simple schematic of step-growth is shown in Figure 3.1, where Sn atoms are represented by red balls and Ge atoms are represented by gray balls the Sn atoms can be confined between successively growing rows of Ge atoms. The time to add a sequence of atom can be written as $\tau_e = a/v_{step}$, where a is the width of a single atomic row and v_{step} is the step velocity. τ_e can also be used to represent the time that Sn atoms at the end of a row of Ge atoms can still return to the catalyst.

To date, growth of $Ge_{1-x}Sn_x$ NWs with Sn concentration in the range of 9–12 at.% has been achieved via VLS process [100], [101], [102]. Growth kinetics such as the temperature

dependence of Sn incorporation into NWs [103] and the dependence of NW growth rate on the concentration of Sn in the catalyst [101] have also been studied. However, in these reports, the concentration of Sn in the catalyst is difficult to control and cannot exceed 50% because a Ge–Sn mixture gas is used as a precursor [101]. High Sn concentration in the catalysts has always been considered as an important fact due to the anomalous Sn incorporation into $Ge_{1-x}Sn_x$ NWs. To further increase the Sn content in $Ge_{1-x}Sn_x$ NWs, there is an urgent need to understand the growth kinetics by clarifying the effect of catalysts with a wide range of Sn concentrations on Sn incorporation. On the other hand, significant Sn incorporation may lead to problems such as misfit dislocations, Sn segregation, and twinning defects in NWs, resulting in low-quality crystals. Therefore, it is necessary to consider the change in crystallinity in $Ge_{1-x}Sn_x$ NWs with different Sn content.

On the other hand, when the composition of the catalyst is changed, the ratio between different growth directions of NWs changes significantly [104]. NWs with different growth directions can result in different electronic properties [105], and controlling and manipulating the growth direction of $Ge_{1-x}Sn_x$ NWs can be beneficial to further tune the band structure and tailor the physical properties for specific applications. In terms of applications, NW-based 3D electronic devices such as gate-around field-effect transistors (FETs) require vertical orientation of NWs [106]. Therefore, it becomes essential to investigate the effect of the Sn concentration in the catalyst on the growth direction of $Ge_{1-x}Sn_x$ NWs.

In this work, the Sn incorporation, crystallinity and growth direction of $Ge_{1-x}Sn_x$ NWs were investigated over a wide range (0–86%) as a function of Sn concentration. $Ge_{1-x}Sn_x$ NWs were prepared using germane (GeH_4) precursor and Au–Sn catalysts by the VLS process. The Sn concentration in the catalyst was controlled by varying the ratio of deposited Au to Sn. Here, metallic Sn in the catalyst was used as the Sn source instead of the precursor gas, and Au was used to induce Sn incorporation into NWs during the VLS growth process. Schmidt's model [107], which takes into account the change in the surface tension of the catalyst, is used to discuss the effect of the catalyst on the growth direction. Sn incorporation and crystallinity are evaluated by transmission electron microscopy (TEM), Energy dispersive X-ray (EDX) spectroscopy, Raman scattering, and X-ray diffraction (XRD) analyses.

3.1 Nanowires growth

3.1.1 VLS growth by using Au–Sn catalysts

Sn nanoparticles and Au film were sequentially deposited on Si(111) substrate by thermal evaporation, and the volume ratio of Au to Sn was adjusted by varying the deposition thickness of each metal at a rate of 0.05 nm/sec, monitored by a crystal oscillator. A schematic diagram of the catalyst preparation is shown in Figure 3.2. The effect of the order of metal deposition will be discussed in Chapter 3.1.2.

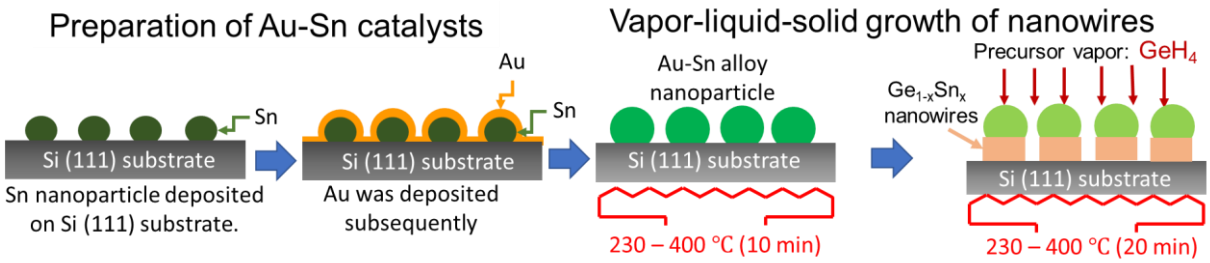

Figure 3.2. Schematic illustration of Au−Sn catalyzed $Ge_{1-x}Sn_x$ NW growth procedure.

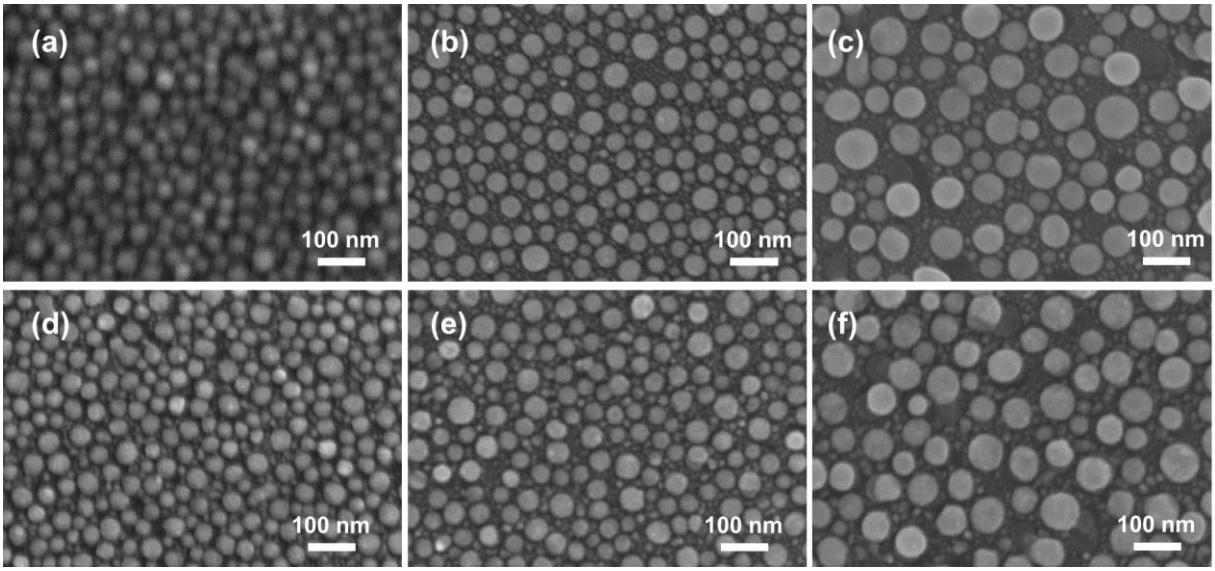

Figure 3.3. SEM images of Au−Sn catalysts with Au:Sn ratios of (a,d) 2:5 (b,e) 1:5 (c,f) 1:10 annealed at (a−c) 320 ˚C and (d−f) 360 ˚C [30].

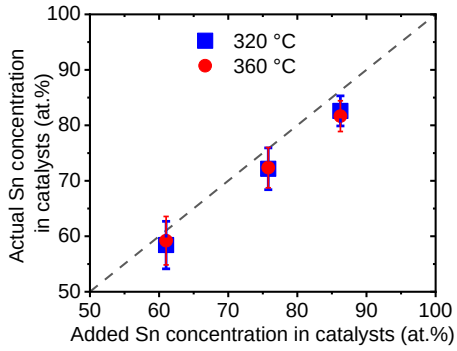

Figure 3.4. Sn concentration in Au−Sn catalysts estimated by EDX annealed at 320 ˚C and 360 ˚C [30].

The morphology and the actual Sn concentration of Au−Sn catalysts were investigated by SEM and EDX. The Au:Sn ratio was controlled by varying the deposition thickness of each metal. The actual thickness used here were 2 nm Au (5 nm Sn), 1 nm Au (5 nm Sn), and 1 nm Au (10 nm Sn), corresponding to Au:Sn ratio of 2:5, 1:5, and 1:10, respectively. Figure 3.3 shows that the shape and size of Au−Sn catalyst are very similar for the samples annealed at 320 ˚C and 360 ˚C, indicating that the surface diffusion of Sn and Au atoms is not significantly enhanced. The bigger size of the catalysts with Au:Sn ratios of 1:10 is due to the larger total thickness of Au

and Sn. The large catalyst with a diameter of about 70 nm is not suitable for VLS NW growth, which is probably the reason for the low density of $Ge_{1-x}Sn_x$ NWs in Figure 3.9c,f.

In order to investigate the actual Sn concentration in these Au–Sn catalysts, EDX multipoint measurements were performed. All the measurement points were placed at the center of each catalyst (10 points for each condition). The Sn concentration in the catalysts was evaluated using Au-M and Sn-Lα. From the result shown in Figure 3.4, it can be seen that the actual Sn concentration at 320 ˚C and 360 ˚C is consistent with the amount added. According to the Au–Sn binary phase diagram, there is no limit of Sn incorporation into Au catalyst at temperature above 320 ˚C [108].

After preparing the nanoparticle catalysts, these samples were loaded into a chemical vapor deposition (CVD) chamber for VLS growth (in Figure 3.2). 10 min pre-annealing at 230–400°C was followed by the growth of $Ge_{1-x}Sn_x$ NWs using 10 sccm of GeH_4 as precursor gas for 20 min at the same temperature. The total pressure was set to 700 Pa by mixing with 30 sccm of N_2. For the growth of GeNWs, a Au film (2 nm) was first deposited on an Si(111) substrate, immersed in HF solution (1%) for 2 min, and then immediately loaded into a CVD chamber to perform VLS growth.

Table 3.1. Experiment results for different growth temperatures and Au:Sn ratios in catalysts.

		Growth temperature				
		230 ℃	280 ℃	320 ℃	360 ℃	400 ℃
Au:Sn ratios in catalysts (Sn content in at.%)	Au:Sn = 2:0 (0%)	—	×	○	○	○
	Au:Sn = 5:2 (20%)	—	×	○	○	—
	Au:Sn = 2:2 (39%)	—	×	○	○	—
	Au:Sn = 1:2 (56%)	×	—	—	○	—
	Au:Sn = 2:5 (61%)	×	—	○	○	—
	Au:Sn = 1:5 (79%)	×	—	○	○	×
	Au:Sn = 1:10 (86%)	×	—	○	○	×
	Au:Sn = 0:5 (100%)	—	×	×	×	×

○, nanowire growth; ×, no nanowires growth; —, no data.

The growth results are shown in Table 3.1, where ○ indicates successful growth of NWs, × indicates failure, and — indicates no experimental data. If the growth temperature is too low or too high, the growth may not be successful. The effect of growth temperature will be discussed in Chapter 3.1.3 and Chapter 3.2.

3.1.2 Effect of the deposition sequence of Au and Sn

There is a significant difference in the growth of Au-on-Sn and Sn-on-Au catalyzed. In Figure 3.5, the Au-on-Sn catalyst successfully grows NWs. However, when Au was deposited first, only a continuous island or a partially expanded catalyst was observed on the sample surface after VLS growth.

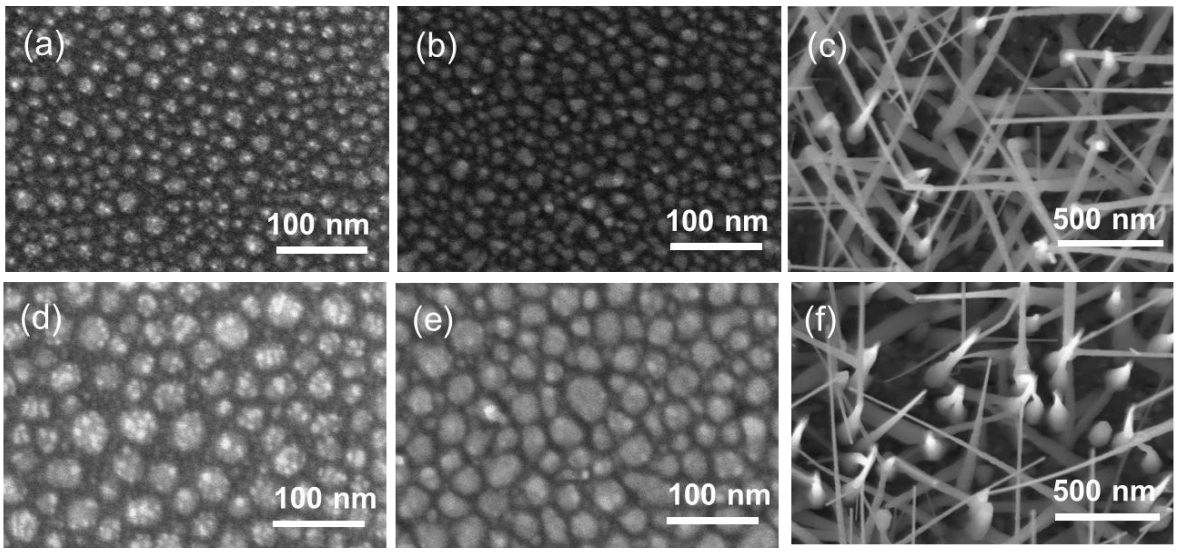

Figure 3.5. Top-view SEM images of the sample surface (a.d) as-deposited (b,e) after annealing (c,f) after performing CVD process at 360 °C using catalysts with (a−c) 1 nm Au on 2 nm Sn and (d−f) 2 nm Au on 5 nm Sn.

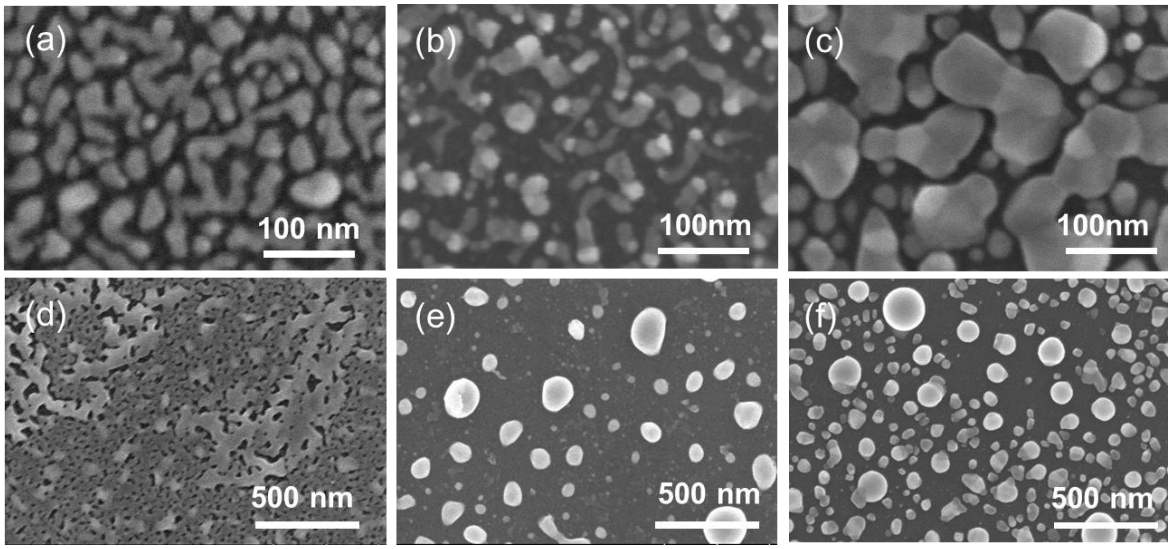

Figure 3.6. Top-view SEM images of the sample surface (a,d) as-deposited (b,e) after annealing (c,f) after performing CVD process at 360 °C using catalysts with (a−c) 2 nm Sn on 1 nm Au and (d−f) 5 nm Sn on 2 nm Au.

To illustrate this phenomenon, SEM images were taken of the sample surface after catalyst deposition, annealing, and VLS growth. Figure 3.5a,d show the nano-islands shapes of two Au-on-Sn catalysts with different thicknesses. When the order of deposition was changed, the shape of the catalyst changed from a continuous island to a film with small openings as shown in Figure 3.6a,d. After annealing at 360 °C for 10 min, the shapes of Au-on-Sn catalysts did not

change (Figure 3.5b,e), but the Sn-on-Au catalysts aggregate by forming tadpole-like islands and larger islands as shown in Figure 3.6b,e. After 20 min of VLS growth, the Sn-on-Au catalysts became bigger, suggesting the incorporation of the germane gas precursor.

A possible mechanism is shown below: In the case of Au on Sn, the nano-island-shaped catalysts are separated from each other, allowing the NWs to grow separately. In the case of Sn on Au, the catalysts are not separated from each other. If the catalysts are continuous, the Ge deposited will be continuous instead of NW-like. Incidentally, the Au layer remaining between the Sn of the substrate may also slow down the process of Ge deposition and nucleation.

3.1.3 Effect of growth temperature

In this experiment, the growth temperature also plays an important role in the NW growth. As shown in Figure 3.7, the growth temperature of 230 °C is much lower than the eutectic temperature of the Au–Ge binary system, so only a small amount of NW can be grown.

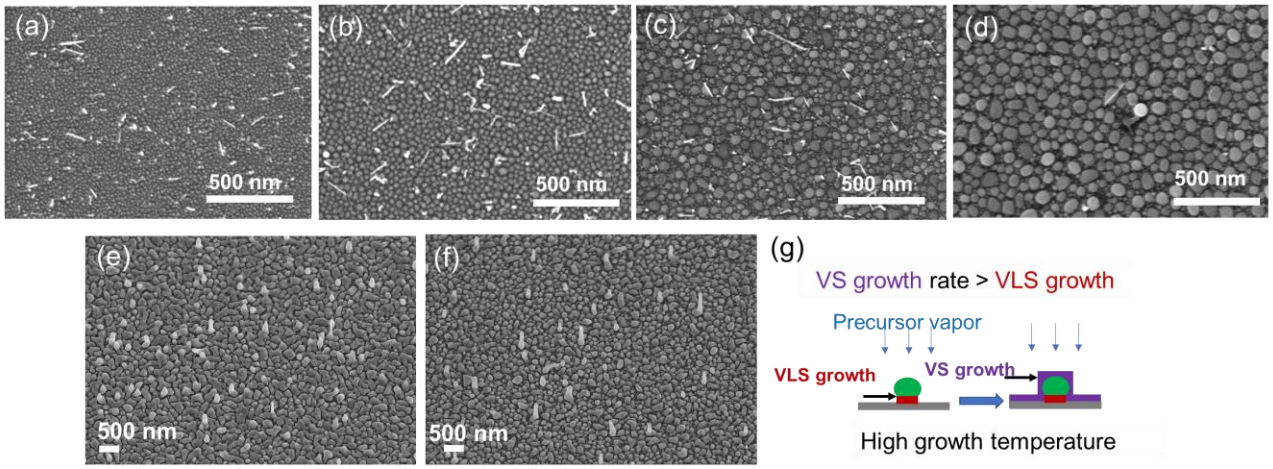

Figure 3.7. Top-view SEM images of the sample surface after performing CVD process at 230 °C using catalysts with Au:Sn ratios of (a) 1:2 (b) 2:5 (c) 1:5 (d) 1:10. 30°-tilted SEM images of sample surface after performing CVD process at 400 °C using catalysts with Au:Sn ratios of (e) 1:5 (f) 1:10. (g) Schematic Illustration of the NW grown with high VS growth rate.

When the growth temperature is 400 °C, the SEM image in Figure 3.7 shows that the substrate surface is covered with a continuous island and the wire can hardly grow. This can be explained by Figure 3.7g: if the VS growth rate is smaller than the VLS growth rate (which usually happens at lower temperatures), the grown NWs are covered by the VS growth layer and become tapered in shape. Instead, if the VS growth rate is too fast, the VLS growth may stop because the excess VS layer covers the catalyst and prevents the precursor gas from contacting the catalyst surface.

3.2 Morphology

3.2.1 Scanning electron microscope

A Hitachi SU8000 scanning electron microscope (SEM) with an acceleration voltage of 5 kV was used to evaluate the morphology of the $Ge_{1-x}Sn_x$ NWs.

From the 30° tilted SEM images in Figure 3.8, it can be seen that $Ge_{1-x}Sn_x$ NWs grown at 280 °C have a disordered growth direction and an irregular shape. Since the growth temperature is still lower than the eutectic temperature (around 300 °C due to the melting point depression for nanoparticles), vapor-solid-solid (VSS) growth may be involved in the VLS growth process.

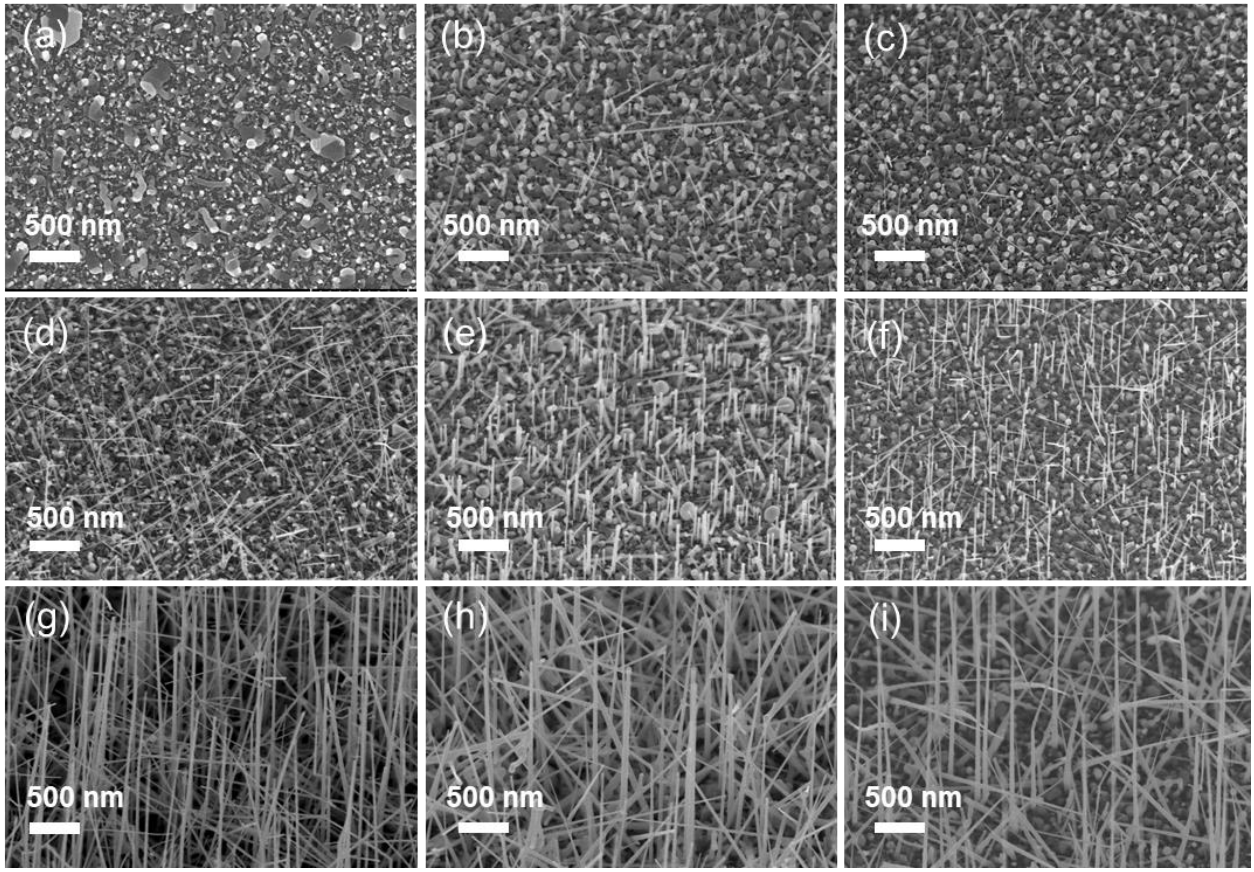

Figure 3.8. 30°-tilted SEM images of $Ge_{1-x}Sn_x$ NWs grown at (a−c) 280 °C, (d−f) 320 °C, and (g−i) 360 °C using catalysts with Au:Sn ratios of (a,d,g) 2:0 (b,e,h) 5:2 (c,f,i) 2:2.

When the growth temperature was increased to 320°C, NWs with a regular shape and a growth direction of ⟨111⟩ were obtained. Furthermore, when the growth temperature was increased to 360°C, the diameter of the grown NWs became larger due to the gas phase growth (VS) and catalyst enlargement. On the other hand, at the same growth temperature, the number density of NWs seemed to decrease with increasing Sn content in the catalyst.

As shown in the SEM image in Figure 3.9, Au−Sn catalyzed growth of $Ge_{1-x}Sn_x$ NWs was successfully achieved at 320 °C and 360 °C. The reason for the unusually low NW density in

Figure 3.9a is that the growth temperature is lower (320 °C) than the eutectic temperature (360 °C with 60 at.% Sn) [108]. The NWs grown at 360 °C show a larger diameter (80 nm) than those at 320 °C (20 nm). This is probably because the decomposition rate of the germane precursor is faster at higher temperatures, resulting in vapor-solid (VS) growth and larger catalyst droplets.

Except for Figure 3.9a, the density of NWs decreases with increasing Sn concentration in the catalyst at each growth temperature, and Figure 3.9f shows an extremely low NW density of 0.4 μm^{-2}. This can be explained by the instability of the catalyst droplets [59]. Liquid Sn in the catalyst lowers the surface tension of the Au–Sn–Ge droplets and any disturbance causes the droplets to wet the sidewalls of the NWs, making NW growth difficult for Sn-rich catalysts.

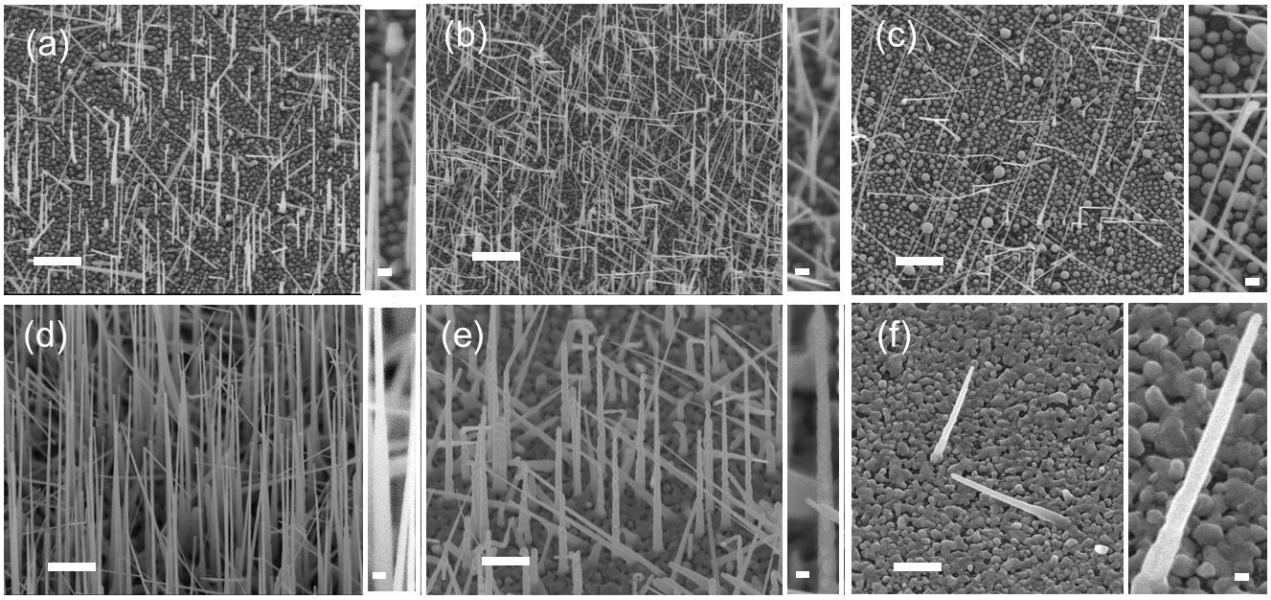

Figure 3.9. 30°-tilted SEM images of $Ge_{1-x}Sn_x$ NWs grown at (a–c) 320 °C and (d–f) 360 °C using catalysts with Au:Sn ratios of (a,d) 2:5 (b,e) 1:5 (c,f) 1:10 (Scale bar, 500 nm).The insets show the magnification SEM images of a typical NW. Scale bar, 50 nm [30].

3.2.2 Transmission electron microscopy

The morphological properties of $Ge_{1-x}Sn_x$ NWs were characterized by transmission electron microscopy (TEM) and energy dispersive X-ray (EDX) spectroscopy analysis using a JEOL 2100F transmission electron microscope operating at 200 kV.

As shown in Figure 3.10a–c, a NW with a spherical seed at the tip was observed, confirming the involvement of the Au–Sn catalyst in the VLS growth mechanism. Figure 3.10d–f show the ⟨111⟩-oriented NWs with an oxide layer of about 3 nm thick, and corresponding diffraction patterns show the high crystallinity of the NWs.

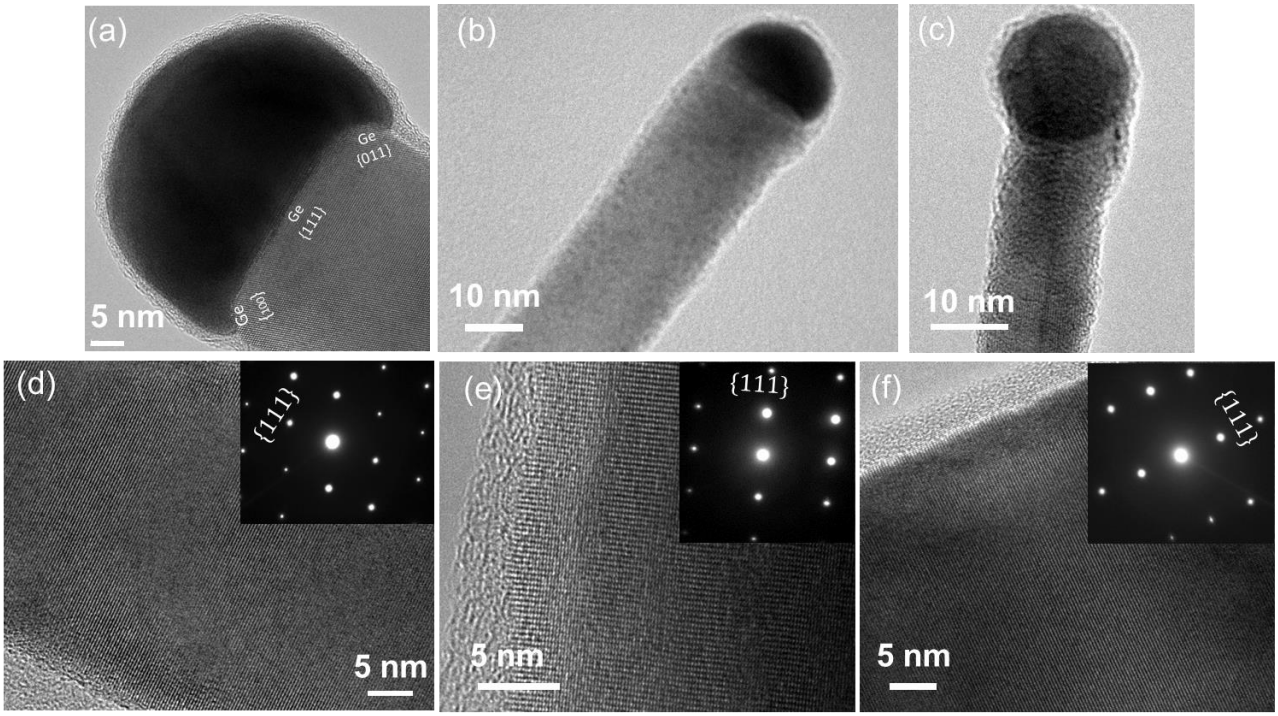

Figure 3.10. HRTEM images of the (a) top and (d) middle of the NWs grown at 320 °C using catalysts with Au:Sn ratios of 5:2. HRTEM images of the (b) top and (e) middle of the NWs grown at 360 °C using catalysts with Au:Sn ratios of 2:5. (c) TEM image of a NW (Au:Sn = 1:10, 320 °C). (f) TEM image of a NW (Au:Sn = 1:5, 360 °C). SAED patterns in the inset demonstrating the single crystalline and growth orientation of the NWs [30].

High-resolution transmission electron microscopy (HRTEM) images and the corresponding selected area electron diffraction (SAED) patterns were taken to investigate the crystallinity of the NWs with the highest Sn doping rate in the catalyst. From the high-resolution TEM image in Figure 3.11b, the NWs were considered to be single crystals covered with a 2 nm oxide film, but extra spots indicating hidden defects within the NWs were observed in the SAED pattern. Figure 3.12a shows an odd numbered HRTEM image with three different regions. Fast Fourier Transform (FFT) analysis was performed in regions A and B of the HRTEM image in Figure 3.12a, and different crystallographic grains were identified. In the central region, the periodicity of the three {111} planes gradually appear, with the highest contrast in the center, followed by a change to a different grain. The SAED pattern in Figure 3.12b shows the pseudo-hexagonal symmetry.

These strange phenomena can be explained by the superposition of two twinned grains [109]. As shown in Figure 3.12c, grains A and B partially overlap along the incident electron beam, spontaneously generating a $3d_{111}$ period, which is in good agreement with TEM observations. Figure 3.12d shows the possible arrangements of grains A and B in NWs. The ratio of grain A decreases from left to right and becomes 0.5 in the center, resulting in the contrast change observed in the TEM image. The SAED pattern can also be explained by the superposition of the FFT images of regions A and B in Figure 3.12b, indicating that the presence of many additional spots is due to the double diffraction effect. Figure 3.11a. Figure 3.11a shows that the two twins also appear at the tip of the NW, indicating the longitudinal twin plane along the growth axis of the NW.

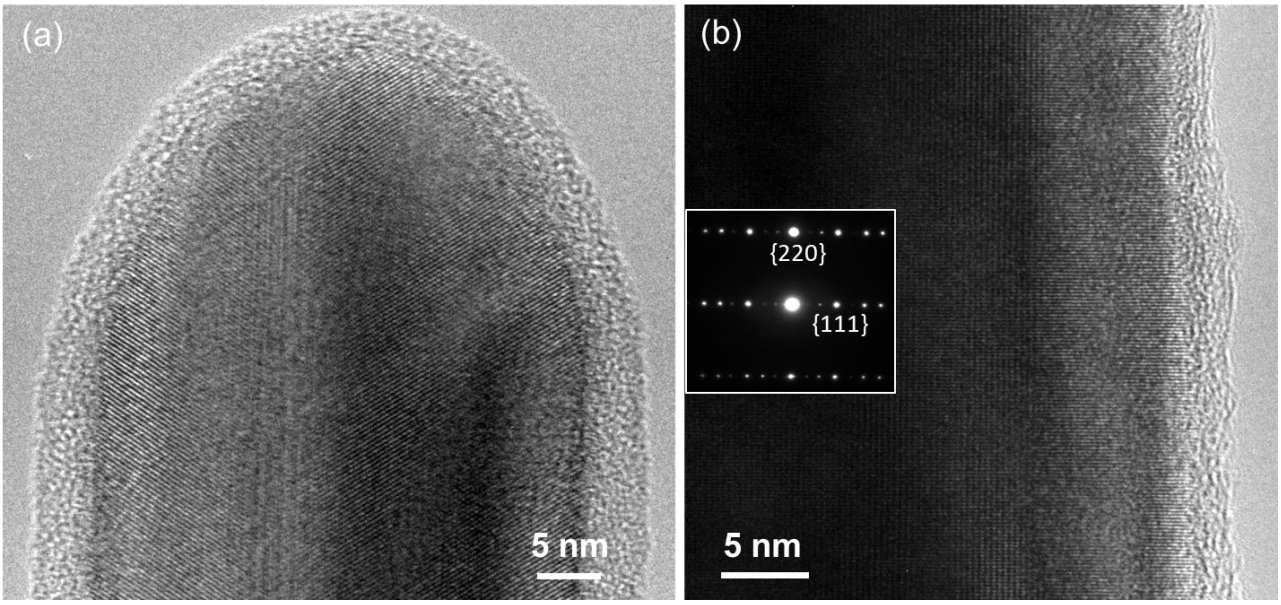

Figure 3.11. HRTEM image of (a) the tip and (b) bottom of a $Ge_{1-x}Sn_x$ NW (Au:Sn = 1:10, 360 °C). The inset in (b) shows the corresponding SAED pattern [30].

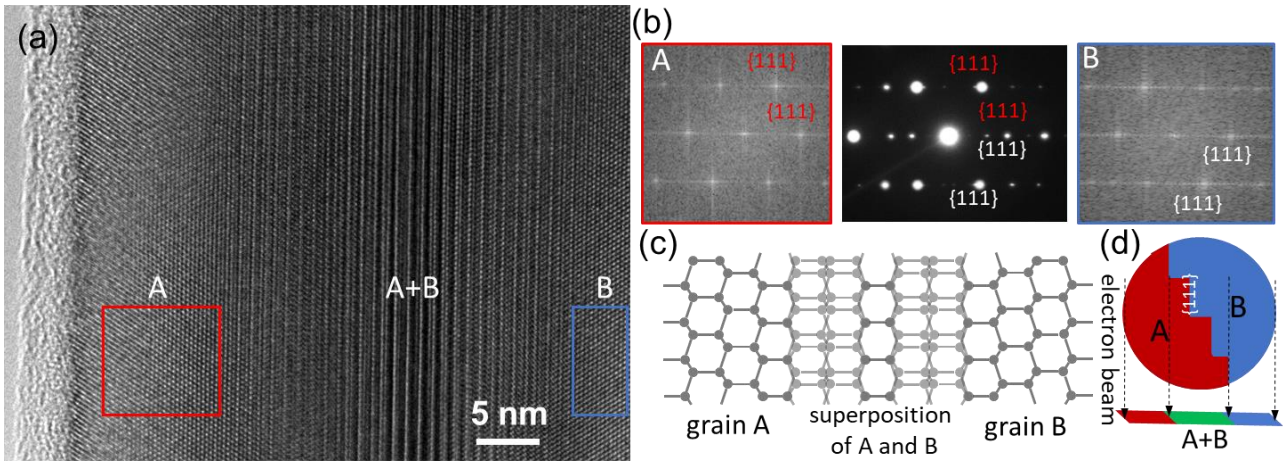

Figure 3.12. (a) HRTEM image taken from the middle of the $Ge_{1-x}Sn_x$ NW (Au:Sn = 1:10, 360 °C). (b) FFT patterns A and B corresponding to the region A (red rectangle), and region B (blue rectangle) in (a) rectangle, respectively. Corresponding SAED pattern in the middle of (b) showing a pseudo-hexagonal symmetry. (c) Illustration shows an atomic model of the {111}-twined grain A and B, generating a partial superposition in the middle. (d) Cross-sectional schematic illustration showing a possible configuration of grain A and B in the NW under the electron beam [30].

If the twin energy of the catalyst is smaller than $\Delta\mu/S$, twin defects can be induced in GeNW [110]. Here $\Delta\mu$ is supersaturation, which is defined as the difference between the chemical potential of Ge in catalyst droplet and Ge in NW. S is the inverse of the nucleus density on a {111} plane. According to Biswas et al. [111], supersaturation can be expressed as

$$\Delta\mu = kT\ ln\left(\frac{C}{C_e}\right) \qquad 3.1$$

where k is Boltzmann constant, T is temperature, C is the concentration of the growth species (in this case Ge) in liquid or solid and C_e is the equilibrium concentration of the growth species. If the Sn concentration in the catalyst is high, the C_e will be extremely low due to the low

solubility of Ge in the Au–Sn liquid on the Sn-rich side [[112], leading to a high degree of supersaturation, which ultimately promotes the formation of twins. On the other hand, the Au–Sn alloy has a lower stacking defect energy than Au [113], and the twin density usually increases with decreasing stacking defect energy [114], which could also be the reason.

3.3 Sn incorporation

Energy dispersive X-ray (EDX) analysis was performed on a JEOL 2100F transmission electron microscope operating at 200 kV.

Micro-Raman scattering analyses were carried out at room temperature using a 532 nm excitation light source, focused to a spot size of about 1 µm with a 100× objective lens. The power of the light was set to about 0.02 mW to avoid local heating effects due to the excitation laser [86], [92]. All data were recorded with a spectral resolution of about 0.3 cm^{-1}. The optical phonon Raman peak of Ge shifts to the lower wavenumber side as the Sn concentration in Ge increases. The composition dependence of the Raman mode of this group IV alloy can be explained as the sum of a mass-disorder term and a bond-distortion term, both of which decrease linearly with increasing Sn concentration.

XRD data were collected on a PANalytical X'Pert Pro MRD system with a parallel Cu Kα beam. The incorporation of a heterogeneous element with a large lattice constant increases the lattice size of Ge, giving the left shift of Ge(111) peak (see Vegard's law in Section 1.6.2).

3.3.1 Energy-dispersive X-ray analysis

It is essential to investigate the quantitative incorporation of Sn in $Ge_{1-x}Sn_x$ NWs. Therefore, TEM-energy dispersive X-ray (EDX) analysis was performed to study the composition and distribution of the element in NWs. Figure 3.13 shows TEM-EDX spectra recorded from the catalyst and body regions of a $Ge_{1-x}Sn_x$ NW (Au:Sn = 5:2, 320 ˚C). There are three main peaks associated with Ge, Sn, and Au in the catalytic region. The quantitative analysis shows that the Sn concentration is 13.8 at.% and the Au concentration is about 82.5 at.%. The XRD pattern recorded from the NWs shows three $Au_{17}Sn_3$ alloy peaks compared to the Au-catalyzed GeNWs, which is in good agreement with the EDX results. For the body region, the main peaks are associated with Ge and Sn and not with Au, indicating that the Au contamination is negligible. The Sn concentration is estimated to be 0.6 at.%, which is lower than the equilibrium solubility of Sn in Ge [97]. By the way, the Cu peaks here originate from the TEM grid.

Figure 3.14a shows a STEM image and EDX mapping of the tip of a $Ge_{1-x}Sn_x$ NW (Au:Sn = 5:2, 320 ˚C). The EDX mapping data show that Sn is uniformly distributed inside the body of the $Ge_{1-x}Sn_x$ NW and there is no observable segregation. The mapping of Au, Sn, and Ge in the catalyst also demonstrates the participation of the Au–Sn–Ge catalysts in the Au–Sn catalyzed

growth process. Figure 3.14b shows an EDX linescan along the length of the NW, where Sn-L indicates continuous Sn incorporation along the length of NW.

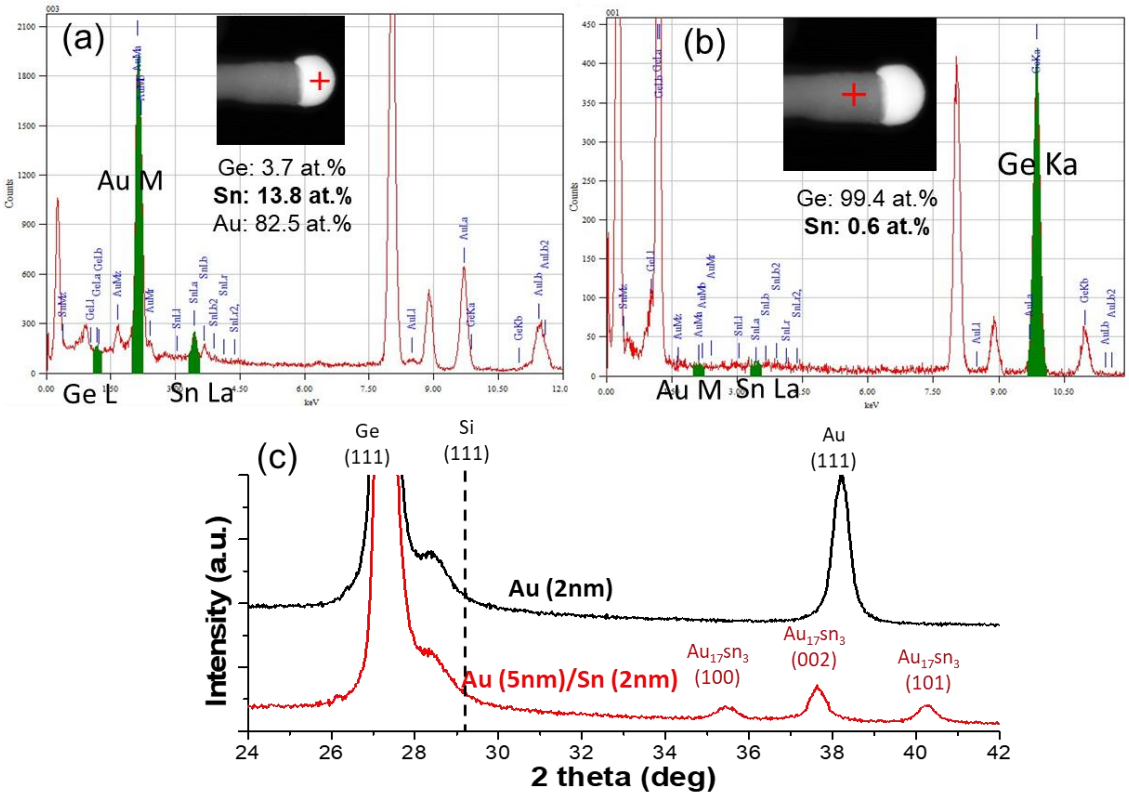

Figure 3.13. (a) TEM-EDX spectrum recorded from the catalyst region of the $Ge_{1-x}Sn_x$ NW (Au:Sn = 5:2, 320 ˚C). (b) TEM-EDX spectrum recorded from the NW body region. (c) XRD patterns of NWs using catalysts with Au:Sn ratios of 2:0 and 5:2, indicating that the catalysts of the $Ge_{1-x}Sn_x$ NW (Au:Sn = 5:2, 320 ˚C) are composed of $Au_{17}Sn_3$ alloys.

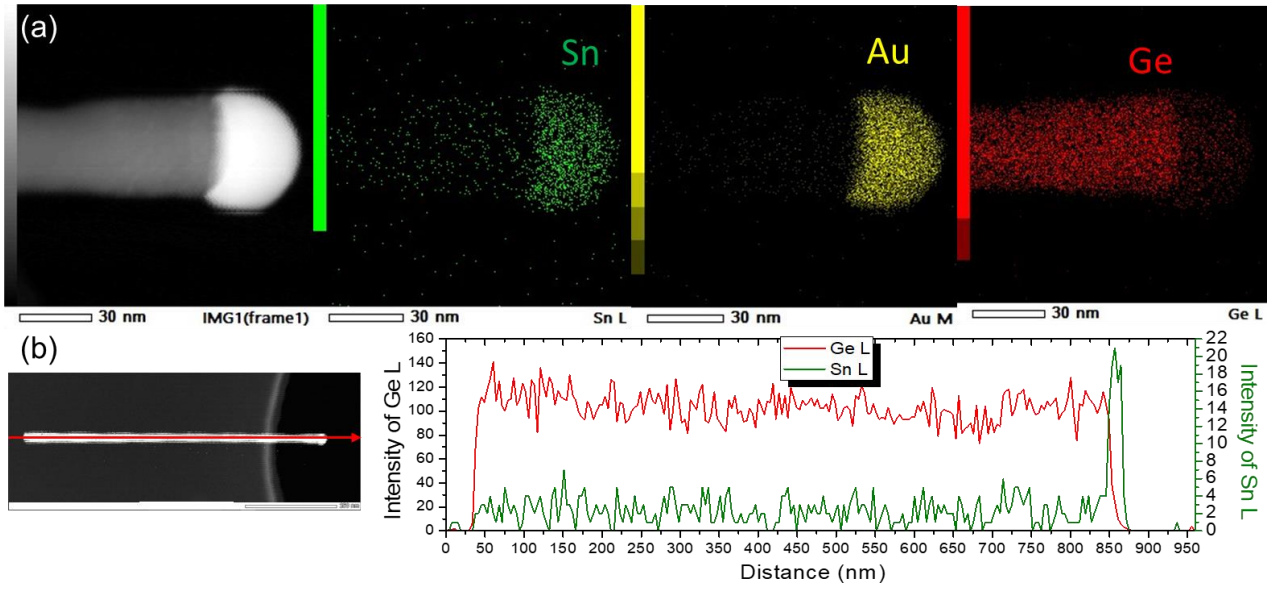

Figure 3.14. (a) STEM image and EDX mapping for Sn, Au, and Ge at the tip of the $Ge_{1-x}Sn_x$ NW (Au:Sn = 5:2, 320 ˚C). (b) EDX linescan for Ge and Sn along the length of the NW.

The amount of Sn in the catalyst was varied from 0 to 86 at.% (Au:Sn thickness ratio from 2:0 to 1:10), giving an increase of Sn content in NWs (in Figure 3.15). By using 61% and 76% of Sn

in the catalyst, 1.3 at.% and 2.2 at.% of Sn were incorporated into the NWs, respectively. By increasing the Sn content to 86%, 5 at.% of Sn was estimated to be incorporated into the body of NWs. This value is much higher than the equilibrium solubility of Sn in Ge [97].

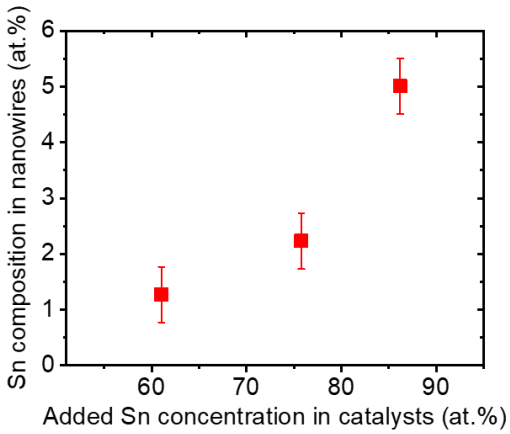

Figure 3.15. TEM-EDX Sn composition in $Ge_{1-x}Sn_x$ NW grown at 360 °C as a function of added Sn concentration in catalysts [30].

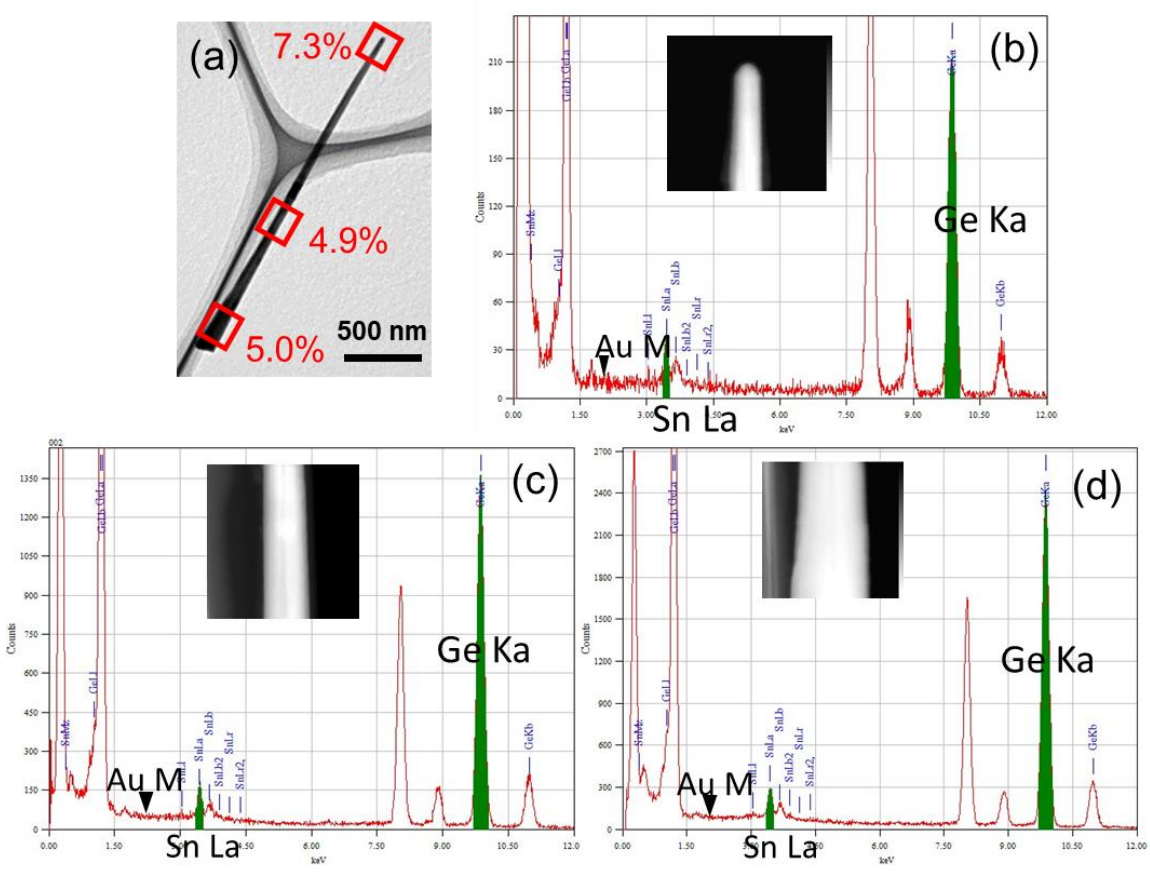

Figure 3.16. (a) TEM image of the $Ge_{1-x}Sn_x$ NW (Au:Sn = 1:10, 360 °C) and the average Sn composition measured by TEM-EDX for three different regions of the NW (indicated by red rectangles). TEM-EDX spectrum recorded from the (b) tip, (c) middle, and (d) bottom of the NW. Au was under the detection limit in all three regions [30].

Sn distribution in NWs (5 at.% of Sn) is characterized in detail in Figure 3.16. Figure 3.16b–d show TEM-EDX spectra recorded from the top, middle, and bottom of the $Ge_{1-x}Sn_x$ NW (Au:Sn

= 1:10, 360 ˚C). The bottom of the NW contains an average Sn content of 5 at.% and negligible Au contamination. The middle part of the NW shows almost the same Sn composition, while the tip is estimated to have an anomalous Sn content of 7.3 at.%. No catalyst was detected in the TEM image (Figure 3.11a) or the elemental mapping (Figure 3.17a), so this high value cannot be attributed to the residual catalyst. The reason for this could be the higher Sn content at the tip due to the thinner radial growth shell compared to the bottom, but it could also be overestimated due to the high noise (Figure 3.16b). The EDX mappings in Figure 3.17a,b show that Sn is uniformly distributed inside the NWs and no segregation is observed. Figure 3.17d shows an EDX line scan along the length of the NW. Sn-L indicates continuous Sn incorporation along the length of the NW, and the increase in Ge-K intensity toward the bottom of the NW is attributed to the tapered shape of the NW. A line scan along the width of the NWs (Figure 3.17c) also showed that there was no Sn segregation on the surface of the NWs.

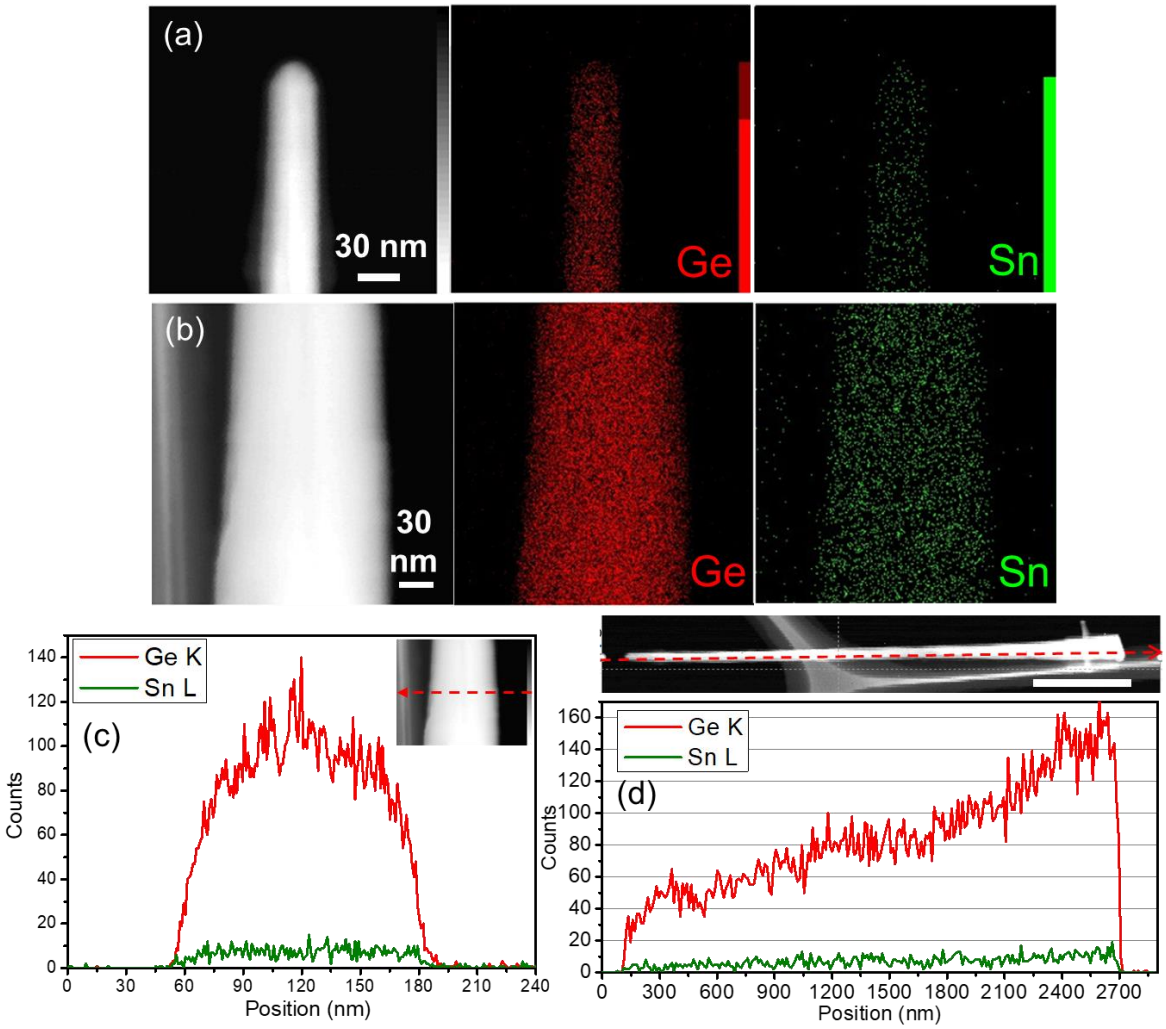

Figure 3.17. TEM image and EDX mapping for Ge and Sn at the (a) tip and (b) bottom of the $Ge_{1-x}Sn_x$ NW (Au:Sn = 1:10, 360 °C). EDX linescan for Ge and Sn along with the (c) width and (d) length of the $Ge_{1-x}Sn_x$ NW (Au:Sn = 1:10, 360 °C). Decreased Ge intensity toward the tip resulting from the tapered shape of the NW [30].

3.3.2 Raman scattering and X-ray diffraction analysis

Raman spectroscopy is an effective technique to investigate local chemical bonding and crystallinity inside the NWs. The dependence of Raman frequency on Sn composition in $Ge_{1-x}Sn_x$ alloys has been published by many research groups, giving a way to estimate the amount of Sn located at substitution sites in alloy NWs. Figure 3.18a,c show the Raman spectra of NWs grown at 320°C and 360°C, respectively. The strong peak around 300.2 cm^{-1} in bulk Ge is attributed to the Ge optical phonon mode. The Ge optical phonon peak generally shifts to the lower wavenumber side with increasing Sn content in the catalyst. In Figure 3.18b, the Ge optical phonon peaks from the NWs with 1.3 and 2.2 at.% Sn (estimated by TEM-EDX spectroscopy) were found to be shifted by −0.32, and −1.02 cm^{-1} compared to bulk Ge, respectively.

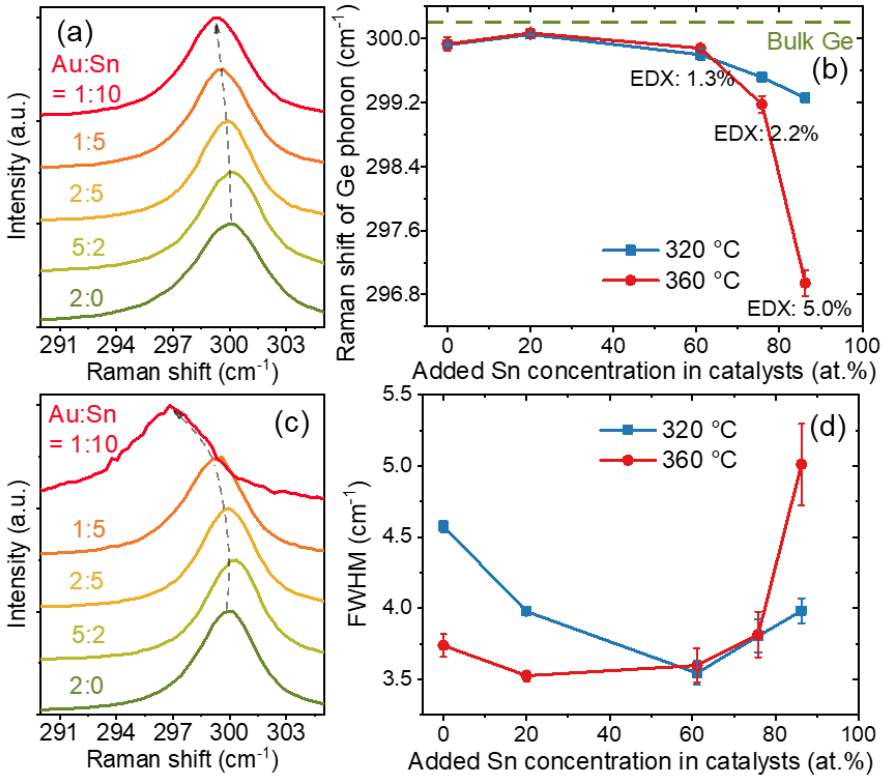

Figure 3.18. Raman spectra of $Ge_{1-x}Sn_x$ NWs grown at (a) 320 °C and (c) 360 °C with different Au:Sn ratios in catalysts. The tendency of the peak shift is indicated by black dashed line. (b) Raman shift and (d) corresponding FWHM fitted from the Ge optical phonon peaks. The Ge bulk value is represented by green dashed line. The actual Sn composition of NWs (measured by TEM-EDX) are indicated in (b). Standard deviation in Raman measurements is represented by the error bars in (b,d) [30].

For the NWs grown at an Au:Sn ratio of 1:10, micro-Raman scattering was performed to separate the NW signal from the background because the signal from the wetting layer was negligible due to the extremely low NW density (Figure 3.9f). As shown in Figure 3.19, the regions with and without NWs were probed using excitation light with a diameter of 1 µm. The intensity of the Ge optical phonon peak observed from the NW region is about twice that from the region without NWs. The Raman spectrum of the NW-free region is subtracted from the Raman spectrum of the NW-containing region to obtain the NW component, which gives a Raman shift of −3.26 cm^{-1}.

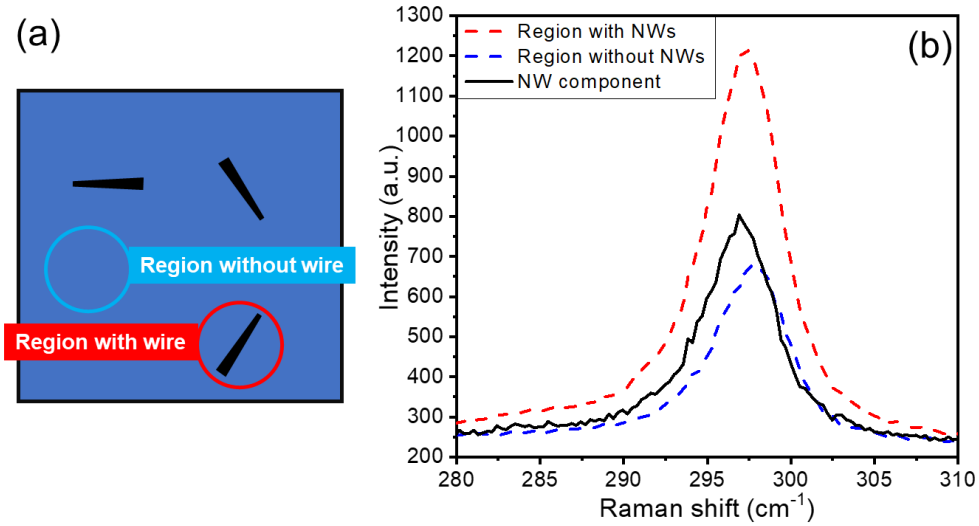

Figure 3.19. (a) Schematic illustration of Raman measurement for the samples with a low NW density. (b) Raman spectra of the $Ge_{1-x}Sn_x$ NWs (Au:Sn = 1:10, 360 °C). Spectra measured at the region with NWs, the region without NWs, and NW component are indicated by red, blue, and black lines, respectively [30].

Raman shift of the Ge optical phonon peak in $Ge_{1-x}Sn_x$ alloys is affected by the compositional variations and strain. Here, the stain effect is not considered because strain can be released with a one-dimensional nanostructure. The compositional dependence of the Raman shift in $Ge_{1-x}Sn_x$ alloys (ω_{alloy}) can be expressed by the linear equation: $\omega_{alloy} = \omega_{Bulk} + \Delta\omega_{alloy}x$ with ω_{Bulk} being the Raman shift of bulk Ge and x being the Sn concentration. Fitting the Raman shift (ω_{alloy}) as a function of Sn concentration (x) with this equation, we obtain $\Delta\omega_{alloy} = -(60.0 \pm 7.5)\ cm^{-1}$. This value can be compared with $-(64.3 \pm 0.1)\ cm^{-1}$ for $Ge_{1-x}Sn_x$ NW [100] and $-(68 \pm 5)\ cm^{-1}$ for unstrained $Ge_{1-x}Sn_x$ alloy film [78]. This consistency further confirms the substitutional incorporation of Sn in our samples. The decrease in full width at half maximum (FWHM) in Figure 3.19d indicates that the crystallinity of the NWs has increased. The change in FWHM can be attributed to the competition between the increase in crystallinity and the broadening effect due to the incorporation of Sn, resulting in a first decrease of FWHM for low Sn content and then an increase for high Sn content. The slight blueshift of Raman peak of NWs with 20% added Sn compared with 0% in Figure 3.19b can be attributed to the increase in crystallinity, since the Raman peak red-shifts when the crystallinity is low.

X-ray diffraction (XRD) was performed to further confirm the Sn incorporation and crystallinity in $Ge_{1-x}Sn_x$ NWs (Figure 3.20). The Ge(111) reflection shift and the corresponding lattice constant show that the unit cell increase with the increase in added Sn%. This enlargement of unit cell is associated with the incorporation of Sn atoms into the Ge lattice according to Vegard's law (see Section 1.6.2). The significant lattice constant change of the sample (Au:Sn = 1:10, 360 °C) compare to the bulk Ge gives a Sn content of 4.1 at.%, which is comparable to the actual Sn content of 5 at.% (determined by TEM-EDX measurements). The FWHM of Ge(111) peak in Figure 3.20d shows a similar trend to the results obtained by Raman measurements, confirming that the crystallinity is enhanced when Sn% is low and Sn incorporation is increased when Sn% is high. One possible explanation for the improved crystallinity is that the supersaturation of Ge significantly suppresses the homogeneous nucleation rate of the Au [61]. The addition of Sn to the Au catalyst decreases the solubility of Ge and thus increases the Ge

supersaturation (Equation 3.1), resulting in less Au incorporation and higher crystallinity. Furthermore, the overall smaller FWHM of the Ge(111) peak of NWs grown at 360°C compared to 320 °C can be attributed to the lower nucleation rate of Au at higher temperatures [61].

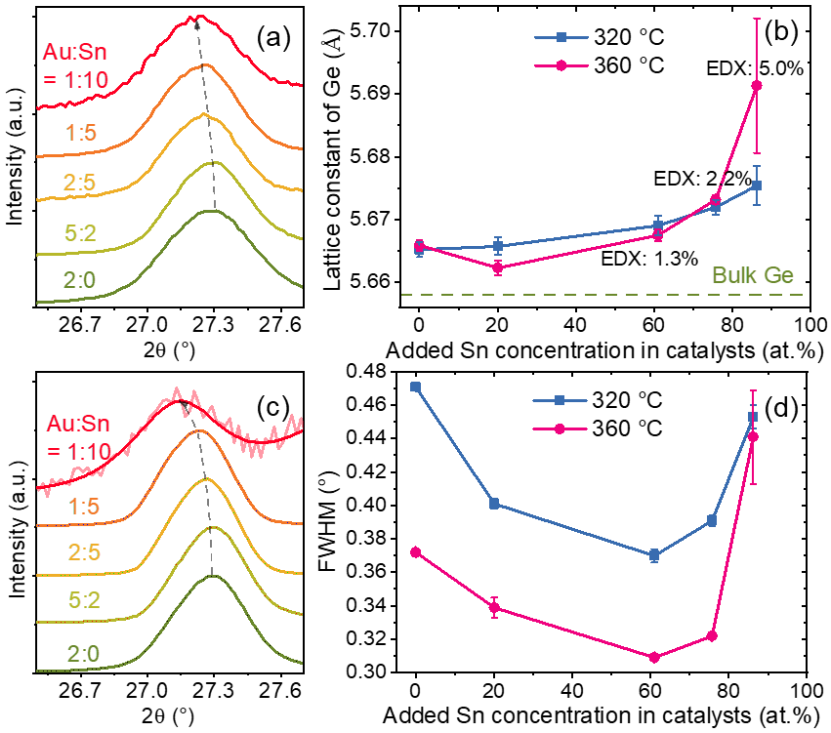

Figure 3.20. XRD patterns of $Ge_{1-x}Sn_x$ NWs grown at (a) 320 °C and (c) 360 °C with different Au:Sn ratios in catalysts. The tendency of the peak shift is indicated by black dashed line. (b) Lattice constant and (d) corresponding FWHM calculated from Ge(111) peaks. The Ge bulk value is represented by green dashed line. The actual Sn composition of NWs (measured by TEM-EDX) is indicated in (b). Standard deviation of the fitting of XRD spectra is represented by the error bars in (b,d) [30].

Non-equilibrium incorporation of Sn during the Ge NW growth is considered by a solute trapping mechanism that takes place in a step-flow kinetic [98]. The step-flow cycle involves an accumulation of chemical potential, called the incubation process, followed by a rapid addition of layers, called step flow, then the impurities in the catalyst droplet can be trapped by the rapid growth of the host layers. The amount of impurity incorporation increases with the trapping rate, which implies a faster step velocity. Since the system size is one of the factors determining the step velocity [99], it can be used to explain the higher Sn content in the NWs grown at 360 °C compared to 320 °C. The higher growth temperature resulted in a larger diameter and therefore a faster step velocity, which in turn increased the Sn% in the NWs.

Another thing to mention is that for quick step flow, the Ge supersaturation in catalysts needs to be high [99]. Higher growth temperature (due to faster cracking rate of precursor) and larger diameter (due to Gibbs-Thomson effect) [115] will result in higher Ge supersaturation and consequently higher Sn content in the NW. On the other hand, a higher Sn concentration in catalysts results in a faster growth rate of $Ge_{1-x}Sn_x$ NWs [101], indicating a higher Sn incorporation into the NWs due to a faster step velocity. Incidentally, the twin defects observed in our samples do not seem to affect the Sn incorporation, since the impurities in the catalyst

are first incorporated into the NWs in a uniform distribution and then segregate to the defects [116].

3.4 Growth direction

Change in the direction of NWs can be attributed to several causes: the diameter of NWs [117], supersaturation of catalyst droplets [118], different types of catalysts [119], and catalyst coverage on NW sidewalls [120]. In order to make the integration of $Ge_{1-x}Sn_x$ NWs on Si platforms more practical, the growth direction of $Ge_{1-x}Sn_x$ NWs needs to be controlled and manipulated.

3.4.1 Variation of growth direction with respect to added Sn% in the catalysts

Figure 3.9a–f show that the growth direction of NWs depends on the Sn concentration in the catalyst. GeNWs grow mainly in the ⟨111⟩ and ⟨110⟩ orientations, while the ⟨112⟩ orientation is rarely observed [121], [62]. In Figure 3.21a,b, the 3D models of NWs with ⟨111⟩ and ⟨110⟩ orientations on (111) substrate were constructed to simulate the same view as the 30° tilted SEM images for comparison (indistinguishable in the top view). The results are shown in Figure 3.21c,d. As the Sn% in the catalyst increases, the relative proportion of ⟨110⟩ orientation increases significantly, and the crossover Sn% is about 75, and 80 in the ⟨111⟩ direction at the growth temperature of 320 °C, and 360 °C, respectively.

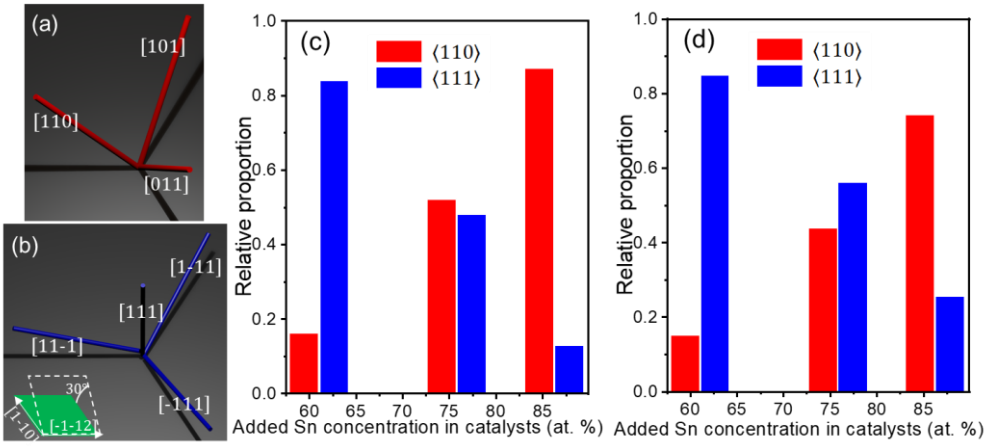

Figure 3.21. Schematic 30°-tilted view of (a) ⟨110⟩-oriented and (b) ⟨111⟩-oriented NWs grown on Si(111) substrate. The viewing direction is presented in the inset. Relative proportion of ⟨110⟩-oriented and ⟨111⟩-oriented NW numbers at the growth temperature of (c) 320 °C and (d) 360 °C as a function of added Sn concentration in catalysts [30].

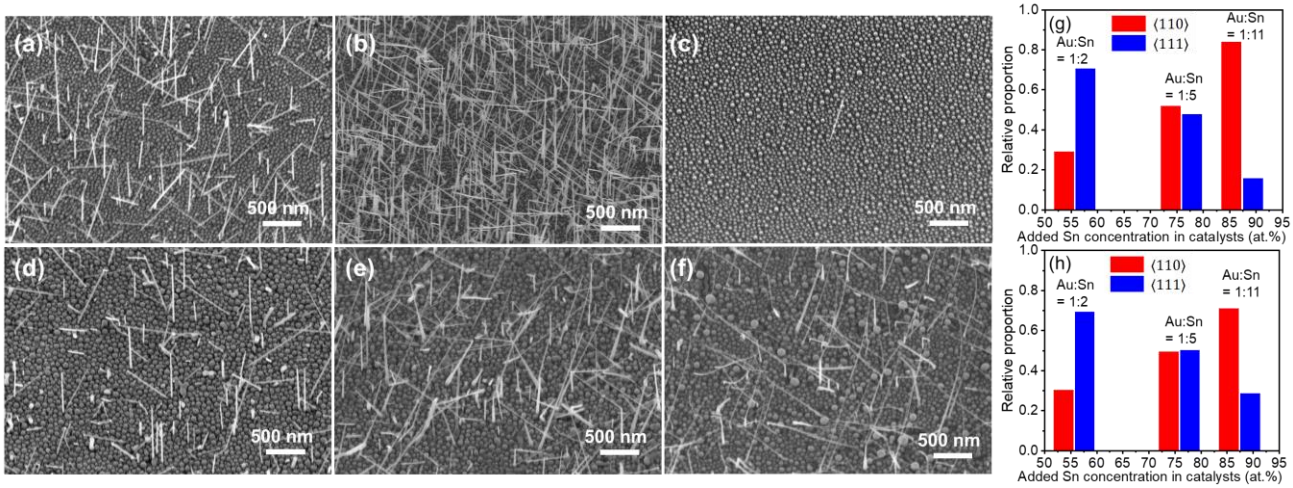

Figure 3.22. 30°-tilted SEM images of $Ge_{1-x}Sn_x$ NWs grown at 320 °C using catalysts with Au:Sn ratios of (a,d) 2:5 (b,e) 1:5 (c,f) 1:10. The NWs were grown by keeping the same total catalyst deposition thickness of (a−c) 6 nm and (d−f) 12 nm. Relative proportion of ⟨110⟩-oriented and ⟨111⟩-oriented NW numbers with the catalyst deposition thickness of (g) 6 nm (h) 12 nm as a function of added Sn concentration in catalysts [30].

In order to eliminate the effect of the total Au−Sn thickness on the growth direction of the $Ge_{1-x}Sn_x$ NWs, we performed an experiment in which the Sn concentration was varied while maintaining the total catalyst thickness, and a control experiment in which the total thickness was varied while maintaining the Sn concentration. Figure 3.22 shows the SEM images of the fabricated NWs and the relative ratios of the number of these two growth directions. The results show that the total thickness of Au−Sn has little effect on the growth direction of $Ge_{1-x}Sn_x$ NWs. To explain this phenomenon, a detailed discussion is given below.

3.4.2 Calculation of free energy

While the diameter dependence of the growth direction of Si NWs has been demonstrated [107], it is unknown for $Ge_{1-x}Sn_x$ NWs. Here we assume that the direction of $Ge_{1-x}Sn_x$ NWs depends on both the diameter of the Si NWs and the Sn concentration in the catalyst, and we will use the model established by Schmidt et al [107] to make it Sn concentration dependent.

Since the growth occurs at the liquid-solid interface, all the contributions from the liquid-solid transition region must be taken into account [107], which is consists of six parts: bulk energy of $Ge_{1-x}Sn_x$ and Au−Ge−Sn droplets, surface tension of $Ge_{1-x}Sn_x$ NWs and droplets, interfacial tension at the liquid-solid interface, and line tension at the vapor-liquid-solid triple-phase line. Assuming that the bulk energy, as well as the surface tension of the droplet catalysts, keep the same for different growth directions, a change in the growth direction of NW will affect the surface tension of the NW, the interfacial tension, and the line tension. On the other hand, varying the composition of droplet catalysts will affect the bulk energy of droplet, the surface tension of droplet, the interfacial tension, and the line tension.

Since we are interested in the energy separation between two different growth directions, the two bulk energies of the droplet and the surface tension can be neglected. The Line tension term

also can be removed due to its small absolute value [107]. The contribution of NW surface tension can be expressed as a product of circumference L, the thickness of the interface Δz, and the surface tension $\sigma_s^{\langle uvw \rangle}$. By introducing the geometrical parameter $a^{\langle uvw \rangle}$, the free energy per circumference can be expressed as below:

$$f^{\langle uvw \rangle} = \Delta z \sigma_s^{\langle uvw \rangle} + a^{\langle uvw \rangle} \sigma_{ls}^{\langle uvw \rangle} r \qquad 3.2$$

where, $f^{\langle uvw \rangle}$ is the free energy per circumference of $\langle uvw \rangle$ oriented NWs, $\sigma_s^{\langle uvw \rangle}$ is the surface energy of $\langle uvw \rangle$-oriented NWs, $a^{\langle uvw \rangle}$ is the geometrical parameter of the cross-section of $\langle uvw \rangle$-oriented NWs, $\sigma_{ls}^{\langle uvw \rangle}$ is the interfacial tension of the liquid-solid interface, and r is the radius of the NW. A schematic representation of these terms is shown in Figure 3.23a.

The mixed region of Si and Au in Au thin films on Si substrates has been calculated by molecular dynamics simulations [122], and Schmidt et al. considered the results of simulation and set Δz to 1 nm for the growth of SiNWs to explain the relationship between the diameter of SiNWs and the growth direction. The intermixed region thickness of $Ge_{1-x}Sn_x$ NWs is estimated to be about 1 nm using high-resolution EELS mapping by Biswas et al. [123]. Based on these results, we set Δz to 1 nm for the growth of $Ge_{1-x}Sn_x$ NWs. Here, we only consider NWs with ⟨111⟩ and ⟨110⟩-orientations. The preferred growth direction can be estimated from the difference between the $f^{\langle 111 \rangle}$ and $f^{\langle 110 \rangle}$. The calculations to estimate the surface energy of $f^{\langle 111 \rangle}$ and $f^{\langle 110 \rangle}$ alloys are described in detail below.

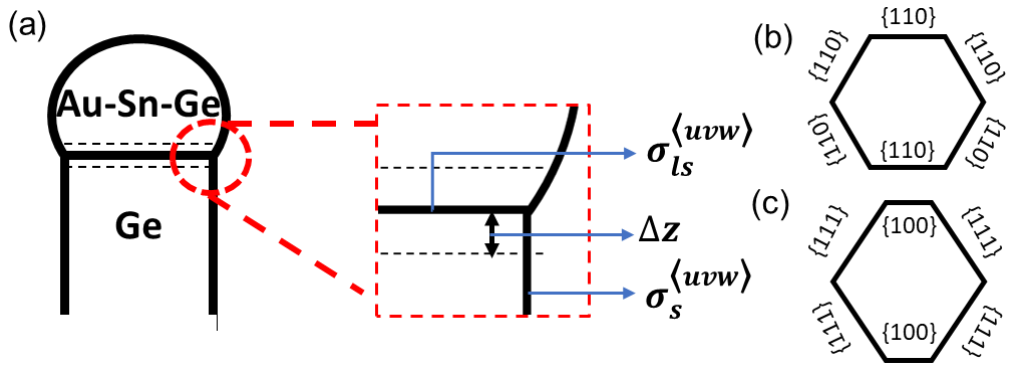

Figure 3.23. (a) Schematic illustration of the liquid-solid interfacial region of a $Ge_{1-x}Sn_x$ NW. Cross-sectional illustration of a (b) ⟨111⟩-oriented NW and (c) ⟨110⟩-oriented NW.

In our case, since only a small amount of Sn is incorporated in NW, we consider the NW as a Ge NW for the sake of simplicity. Using the surface energy of Ge of the different planes in Table 3.2, $\sigma_s^{\langle 111 \rangle}$ can be calculated by assuming a hexagonal cross-section with six (110) surface planes (see Figure 3.23b) to be 1.41 $J \cdot m^{-2}$. The Ge NW with a ⟨110⟩ orientation has two (100) and four (111) surface planes (see Figure 3.23c) [121]. By Wulff theorem, the surface energy of $\sigma_s^{\langle 110 \rangle}$ is deduced to be 1.21 $J \cdot m^{-2}$. From the hexagonal interface of the ⟨111⟩-oriented NW, and the cross-sectional shape of ⟨111⟩-oriented Ge NWs [121], the geometrical parameter $a^{\langle 111 \rangle} = 0.43$, and $a^{\langle 110 \rangle} = 0.40$ are deduced, respectively.

Table 3.2. Calculated surface energy values (J·m^{-2}) for germanium [124].

(*hkl*)	(100)	(110)	(111)
Ge	1.66	1.41	1.15

Since the sides of the NW are perpendicular to the interface, the interfacial tension between the catalyst droplet and the NW $\sigma_{ls}^{\langle 111\rangle}$ can be expressed as

$$\sigma_{ls}^{\langle 111\rangle} = -\sigma_l \cos(\theta)^{\langle 111\rangle} \qquad 3.3$$

derived from young' equation, where σ_l is the surface tension of droplet and θ is the contact angle. Here, we assume these three types of atoms contribute to the surface tension in the same way, and σ_l can be defined as follows

$$\sigma_l = (1 - x^{Sn} - y^{Ge})\sigma_l^{Au} + x^{Sn}\sigma_l^{Sn} + y^{Ge}\sigma_l^{Ge} \qquad 3.4$$

with x^{Sn} and y^{Ge} being the Sn, and Ge concentration in the droplet, respectively. The surface tension values of pure elements at 600K is taken from Keene [125], and the concentration is varied according to the route from e_{AB} to e_{BC} approximately by the phase diagram of Au–Sn–Ge ternary system [126]. The contact angle θ is assumed to decrease linearly with decreasing $1/\sigma_l$ [127]. The initial contact angle of 126° was deduced from Au-catalyzed ⟨111⟩-oriented GeNWs [61], and a final contact angle of 115° was measured from Sn-catalyzed ⟨111⟩-oriented GeNWs [29] with assuming it will remain unchanged after solidification [61]. The interfacial tension for the ⟨110⟩-oriented NW $\sigma_{ls}^{\langle 110\rangle}$ can be easily calculated by multiplying $\sigma_{ls}^{\langle 111\rangle}$ by $\sqrt{3/2}$ [107].

3.4.3 Discussion

The contour plot of the energy separation between $f^{\langle 111\rangle}$ and $f^{\langle 110\rangle}$ is shown in Figure 3.24, where positive values indicate a preference for ⟨110⟩ direction and negative values indicate a preference for ⟨111⟩ direction. The solid black line at the position where the energy separation is zero shows that radius r_0 increases as the Sn% increases, meaning that the NW tends to grow in the ⟨110⟩ direction rather than the ⟨111⟩ direction as Sn% increases. This is because the higher the Sn%, the lower the liquid-solid interfacial energy becomes, and the surface energy of the NW becomes more dominant than the interfacial energy, and vice versa. r_0 is about 6 nm when Sn% is zero, which is smaller than that of SiNW (10 nm) [107]. In the case of NWs grown at 320° C, the crossover Sn% of 75 in Figure 3.24 corresponds to a radius $r_0 \approx 10$ nm at the energy separation of zero. This value is in good agreement with the average diameter of 20 nm (measured from the bottom of the NW).

However, when the growth temperature is 360 °C, the crossover Sn% is 80, and the radius $r_0 \approx 10$ nm, which did not match the average diameter of the NWs. This discrepancy could be explained by the Au and Sn coating on the NW surface. Sn-rich catalyst droplets are unstable due to their low surface tension. As a result, they wet the sidewall of the NW and the catalyst

disappears at the tip (Figure 3.11a). The catalyst covering the sidewall of NWs will strongly change the surface free energy of the system, leading to ⟨110⟩-oriented growth [120].

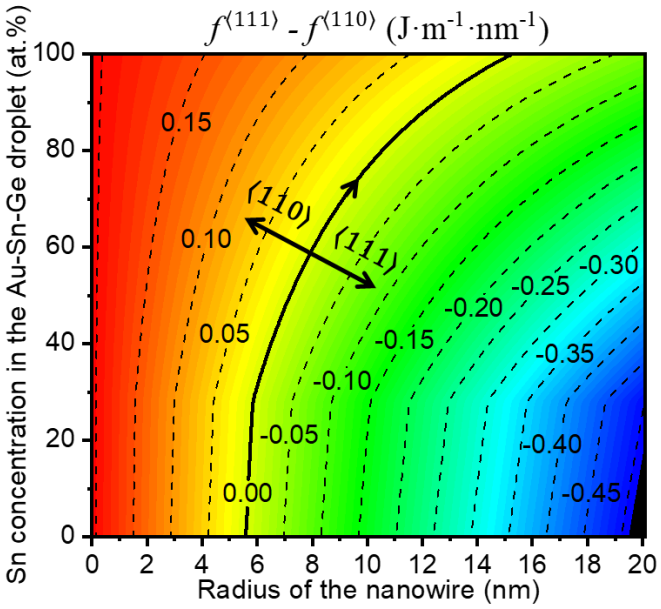

Figure 3.24 Contour plot of the free energy separation of the ⟨111⟩ and ⟨110⟩-oriented NWs as functions of Sn concentration in catalyst droplet and radius of NWs. Energy separation of zero is indicated by the black solid line [30].

3.5 Boron doping

Impurity doping is an important technique for functionalizing group-IV semiconductor nanowires (NWs) for electronic and optoelectronic applications. However, controlling the concentration of impurities in the NWs and characterizing their properties has been a major challenge. Here, boron doping in $Ge_{1-x}Sn_x$ NWs was studied by Raman scattering and X-ray diffraction (XRD).

3.5.1 Morphology

After preparing the nanoparticle catalysts, these samples were loaded into a chemical vapor deposition (CVD) chamber for VLS growth. 10 min pre-annealing at 320–360°C was followed by the growth of boron-doped $Ge_{1-x}Sn_x$ NWs using 10 sccm of GeH_4 (100%) and 0.2 sccm of B_2H_6 (1% in H_2) as precursor gases for 20 min. The total pressure was set at 700 Pa by mixing with 30 sccm of nitrogen gas. For the growth of boron-doped GeNWs, an Au film (2 nm thick) was first deposited on a Si(111) substrate, immersed in HF solution (1%) for 2 min, and then immediately loaded into a CVD chamber for VLS growth. Figure 3.25a shows a schematic diagram of the NW fabrication.

As shown in the SEM image in Figure 3.25, Au–Sn catalyzed growth of boron-doped $Ge_{1-x}Sn_x$ NWs was successfully achieved at 320 °C. Compared to the case without B_2H_6, the size of boron-

doped NWs is larger due to the increased vapor solid (VS) growth at the sidewall of the NWs. The boron doping does not seem to change the orientation of the NWs, suggesting that boron in the catalyst does not have much effect on the free energy of the NWs.

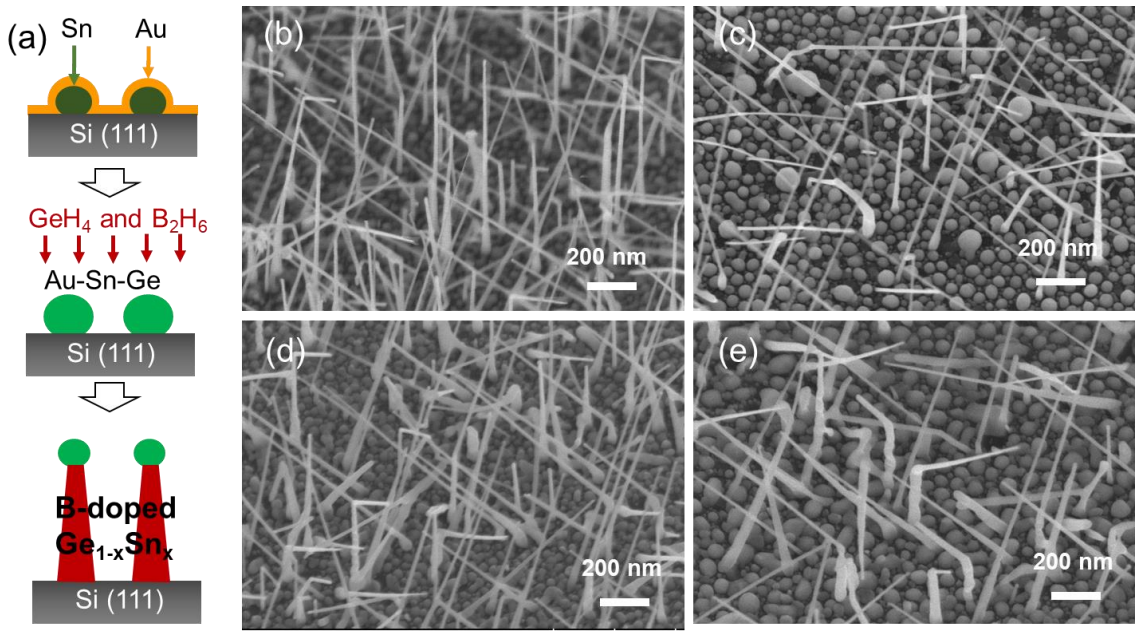

Figure 3.25. Illustration of boron-doped $Ge_{1-x}Sn_x$ NWs growth. 30°-tilted SEM images of (b,c) undoped and (d,e) boron-doped NWs grown at 320 °C with different Au:Sn ratios of (b,d) 1:5 and (c,e) 1:10 in the catalysts.

For the growth temperature of 360 °C in Figure 3.26, the SEM images show that the substrate surface is covered with a continuous island and the wire can hardly grow. This can be explained by the fact that if the VS growth rate is too fast, as in the case of the undoped $Ge_{1-x}Sn_x$ NWs grown at the temperature over 400 °C in Figure 3.7g, the excess VS layer covers the catalyst surface, which may stop the VLS growth. Here, the introduction of boron accelerated the VS growth and lowered the no-growth temperature to 360 °C.

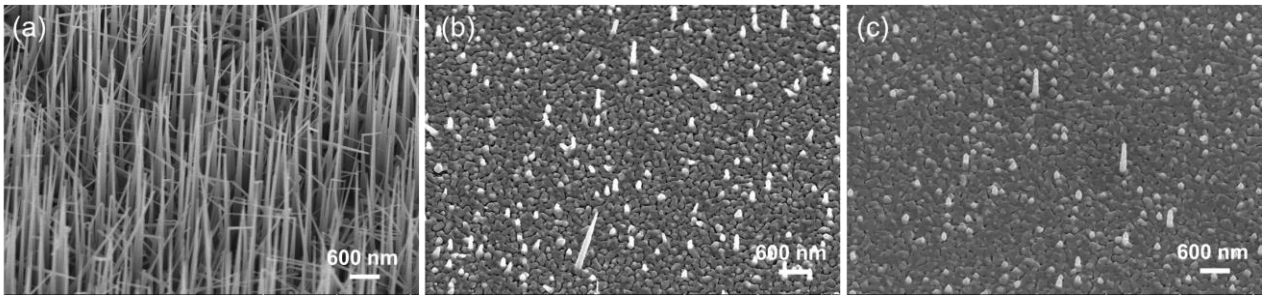

Figure 3.26. 30°-tilted SEM images of boron-doped $Ge_{1-x}Sn_x$ NWs grown at 360 °C with different Au:Sn ratios of (a) 2:0 (b) 1:5 and (c) 1:10 in the catalysts.

3.5.2 X-ray diffraction and Raman scattering analysis

Adding small atom like boron into the $Ge_{1-x}Sn_x$ NWs is expected to accommodate the stress caused by the Sn incorporation, then reduce the Sn segregation, misfit dislocation, and increase the Sn incorporation in NWs. Here, X-ray diffraction (XRD) of boron-doped $Ge_{1-x}Sn_x$ NWs was performed to compare the amount of Sn incorporation and crystallinity with that of non-doped NWs (Figure 3.27).

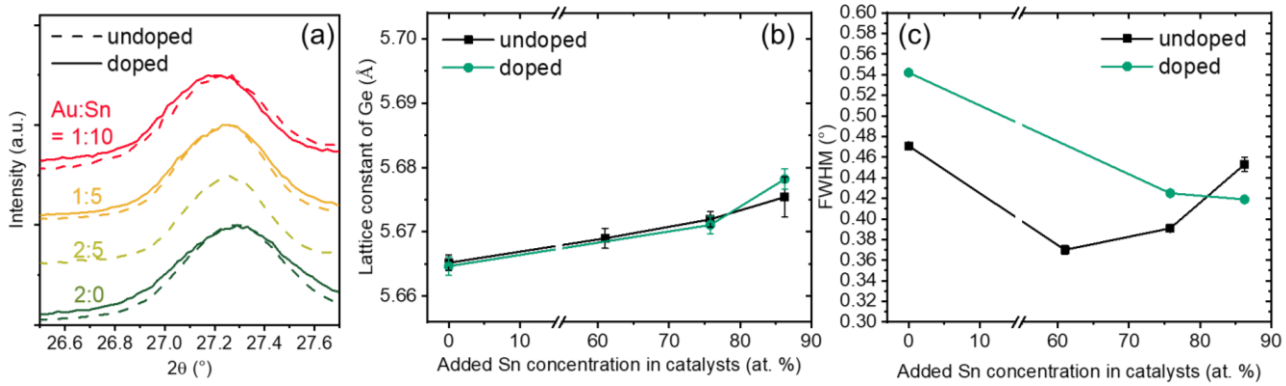

Figure 3.27. (a) XRD patterns recorded from undoped and boron-doped $Ge_{1-x}Sn_x$ NWs grown at 320 °C with different Au:Sn ratios in the catalysts. (b) Lattice constant and (c) corresponding FWHM calculated from Ge(111) peaks. Standard deviation of the fitting of XRD spectra is represented by the error bars.

XRD patterns in Figure 3.27a show an overall broadened spectrum with almost the same peak position after the boron doping. The lattice constant calculated from Ge(111) peaks is within the error bar, indicating that the boron doping does not affect the incorporation of Sn into NWs during VLS growth. The FWHM in Figure 3.27c shows an overall increment after doping, indicating a decrease in the crystallinity of the NWs due to the incorporation of boron atoms. In the case of NWs under growth conditions of using the highest Sn concentration in catalysts, the FWHM of the doped NWs is lower than that of undoped. This indicates that the addition of boron has the effect of accommodating the stress generated by the Sn incorporation and improving the crystallinity.

Micro-Raman scattering measurements were performed at room temperature using a 100x objective and 532 nm excitation light to investigate the states of dopant atoms in NWs. The spectral resolution of all data was about 0.3 cm^{-1}. The excitation power was set to about 0.02 mW to avoid local heating effects. Figure 3.28a shows the asymmetric broadening and downshift of Ge optical phonon peaks after boron doping. This phenomenon is caused by Fano interference and the electrical active boron concentration can be estimated by fitting the Fano equation (Section 1.6.1, Equation 1.3). Figure 3.28c–e show overall downshifts of wavenumber and increase of the Fano parameters q and Γ of boron-doped $Ge_{1-x}Sn_x$ NWs compared to that of undoped NWs. However, such asymmetric broadening and downshift of the Ge optical phonon peak may also be caused by phonon confinement effects if the crystallinity of NWs differs from one growth condition to another. Therefore, we also performed Raman measurements using

excitation light at 633 nm to eliminate the phonon confinement effects and demonstrate the Fano interference in boron-doped $Ge_{1-x}Sn_x$ NWs.

Figure 3.28b shows a spectrum using 355 nm light, which has greater asymmetry, broadening, and downshift compared to 532 nm light. In Figure 3.28c–e, the Ge optical phonon peaks show lower wavenumber shifts, and the Fano parameters q and Γ are also increased overall. These demonstrate the successful doping of boron into $Ge_{1-x}Sn_x$ NWs, and the electrical active boron concentration in the NWs is estimated to be roughly in the order of 10^{19} cm^{-3} [85].

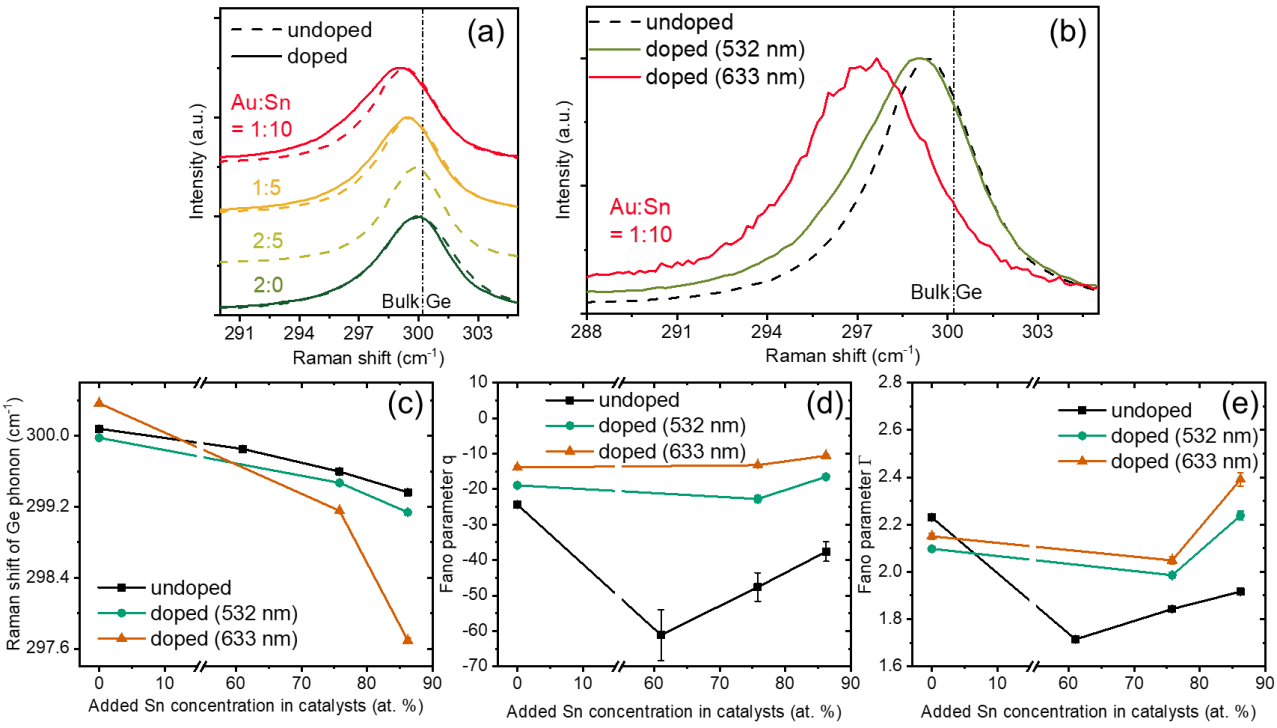

Figure 3.28. (a) Raman spectra of undoped and boron-doped $Ge_{1-x}Sn_x$ NWs grown at 320 °C with different Au:Sn ratios in the catalysts. (b) Raman spectra of the NWs using different wavelengths of excitation laser beam. (c) Raman shift, (d) Fano parameter q, and (e) Fano parameter Γ obtained by fitting corresponding Ge optical phonon peaks with the Fano function. Standard deviation in Raman measurements is represented by the error bars.

3.6 Summary

Using Au–Sn catalysts in different deposition sequences affects growth of $Ge_{1-x}Sn_x$ NWs because of the different catalyst geometries. Au-on-Sn catalysts can lead to the successful growth of $Ge_{1-x}Sn_x$ NWs, while Sn-on-Au catalysts do not.

The growth temperature plays an important role in the growth of $Ge_{1-x}Sn_x$ NWs. The appropriate growth temperature for $Ge_{1-x}Sn_x$ NWs is in the range of 320–360 °C. If the temperature is too low or too high, the shape will be irregular and the NWs will not grow.

The use of Au–Sn alloy catalysts with high Sn content causes twin defects in NWs. High Sn content in the catalyst results in an extremely low C_e and high supersaturation, facilitating twin

formation in NWs. Manipulation and control of the twinning of $Ge_{1-x}Sn_x$ NWs can lead to interesting electrical, optical, and thermoelectric properties. Understanding the role of twinning in VLS growth is a useful tool for morphology and band structure engineering. understanding the role of twins in VLS growth will provide a useful tool for nanostructure and band structure engineering.

Using an Au–Sn catalyst, $Ge_{1-x}Sn_x$ NWs with Sn contents up to 5% were successfully grown at 360 °C. Although 86% of Sn was present inside the NWs, the NW density was very low. On the other hand, twinning defects were observed in these NWs, which may have been induced by the low surface tension of Sn.

It was also confirmed that the use of Au–Sn catalyst promoted the incorporation of Sn into NWs and improved the crystallinity of NWs. On the other hand, high Sn% in the catalyst makes the growth of NWs more difficult and reduces the number density of $Ge_{1-x}Sn_x$ NWs.

$Ge_{1-x}Sn_x$ NWs grown with Sn-rich catalysts prefer the ⟨110⟩ growth direction, while NWs with low Sn content prefer the ⟨111⟩ direction. This reorientation can be explained by calculating the energy separation between these two growth directions.

Boron-doped $Ge_{1-x}Sn_x$ NWs were successfully grown at 360 °C using CVD. Raman scattering analysis showed that the NWs were doped with boron atoms and electrically activated. The concentration of electrical active boron in the NWs was estimated to be in the order of approximately 10^{19} cm^{-3}.

Chapter 4

Ge nanowire arrays fabricated by nanoimprint lithography

Ge has a lower carrier effective mass (electrons and holes), thus higher charge carrier mobility than Si. Its excellent electronic transport properties make it a prime candidate material for fabricating next-generation Si-compatible electronic and optoelectronic devices. Vertical Ge nanowire (NW) arrays are of particular interest due to their large surface-to-volume ratio and high integration that has been proposed to be an ideal material for a high-speed vertical gate-all-around field-effect transistor (FET). However, there are few reports on the top-down fabrication of Ge NW array. This study aims to develop a method to fabricate uniform Ge NW arrays with a smooth surface by nanoimprint lithography and control the diameter of NW by chemical wet etching. To functionalize the Ge NW arrays, Ge/p-Si core–shell structure was fabricated by chemical vapor deposition (CVD) method to introduce and separate the carrier. The hole accumulation in the NW was investigated by X-ray diffraction (XRD) and Raman scattering.

4.1 Ge nanowire arrays fabrication

Figure 4.1 shows the fabrication schematics of Ge NW arrays. The process can be divided into two parts: the fabrication of photoresist nanohole arrays and the fabrication of NW arrays.

Fabrication of photoresist nanohole arrays: prior to the nanoimprint lithography, the p-Ge(100) wafers were cleaned at 110 °C for 5 min using an excimer UV irradiation system (Multiply EXC-1201). Next, 3–4 ml of UV-curable imprint photoresist (NIAC70920-DSN2) was spin-coated onto the Ge substrate at 3000 rpm for 40 seconds. After prebaking at 70 °C for 20 s, a quartz stamp with periodic NWs with the pitch size of 500 nm or 600 nm was placed in contact with the photoresist layer at a pressure of 3.05 kN and then irradiated with UV light. This process was carried out using a nanoimprint system (Toshiba Machine ST50). After detaching the stamp,

the cured photoresist was baked again at 70 °C for 5 min. The thickness of the residual photoresist layer in the nanoholes was measured by a scanning electron microscope (SEM) with the cross-sectional view. Next, the residual layer was removed by a capacitively coupled plasma reactive ion etching (CCP-RIE) system (SAMCO RIE-200NL) using O_2 plasma (N_2 5 sccm, O_2 5 sccm, process pressure 0.1 Pa). The radio frequency inductively coupled plasma (RF ICP) was set to 20 W with the bias of 100 W and the dry etching time was set to 3–8 min with respect to the thickness of the residual layer until the Si surface was exposed.

Fabrication of nanowire arrays: MgO (30 nm) was deposited onto the imprinted photoresist nanohole arrays using an electron beam evaporator (R-DEC RDEB-1206K). The resist was then removed by N-Methyl-2-pyrrolidone (NMP) at 80 °C for one hour with ultrasonic and another hour without ultrasonic, and cleaned by acetone and IPA. Next, SF_6 plasma followed by C_4F_8 plasma (Bosch process) was applied for deep etching of Ge NW structure using a Si deep etcher (Sumitomo Precision Products MUC-21 ASE-SRE). The flow rates of SF_6 and C_4F_8 were both fixed at 35 sccm, the chamber pressure was 0.75 Pa, and the RF power was 100W. The number of Bosch cycles was set from 15 to 60 for adjusting the length of NW arrays. Finally, the MgO mask was removed by H_3PO_4 (DI-water: 97 ml, H_3PO_4: 3 ml) at room temperature over 30 seconds, followed by plasma ashing (>100 °C) to remove organic contamination.

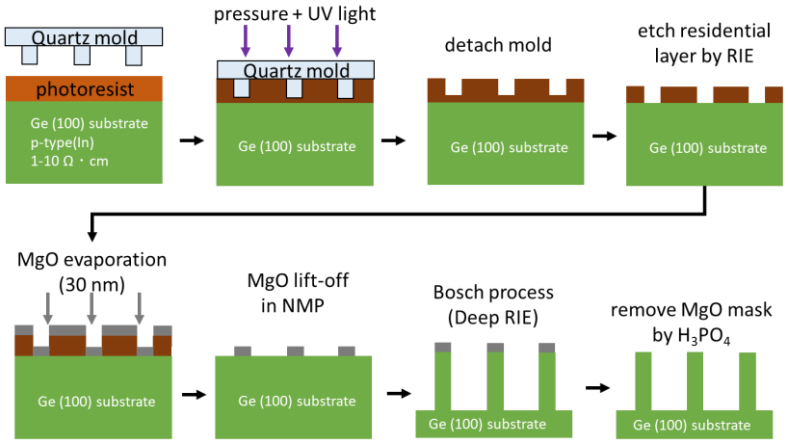

Figure 4.1. Schematic illustration of the fabrication procedure for Ge NW arrays using nanoimprint lithography (NIL).

4.1.1 Morphology

The morphology of the fabricated Ge NW arrays was characterized by a Hitachi SU8000 SEM with an acceleration voltage of 10 kV. Figure 4.2 shows the successful fabrication of Ge NWs with well-ordered arrays and smooth surfaces. The diameter is about 220 nm and the pitch size is 600 nm. Bosch processing of 15, 25, and 60 cycles yielded NW arrays with heights of 500, 830, and 2140 nm, respectively. The NW appears to exhibit almost no taper even at its highest length (Figure 4.2c), indicating a much longer Ge NWs can be achieved with more Bosch cycles. The

length of Si NW and Ge NW length for the Bosch process cycle is shown in Figure 4.2d, indicating that the Bosch etching rate of Ge is approximately twice that of Si.

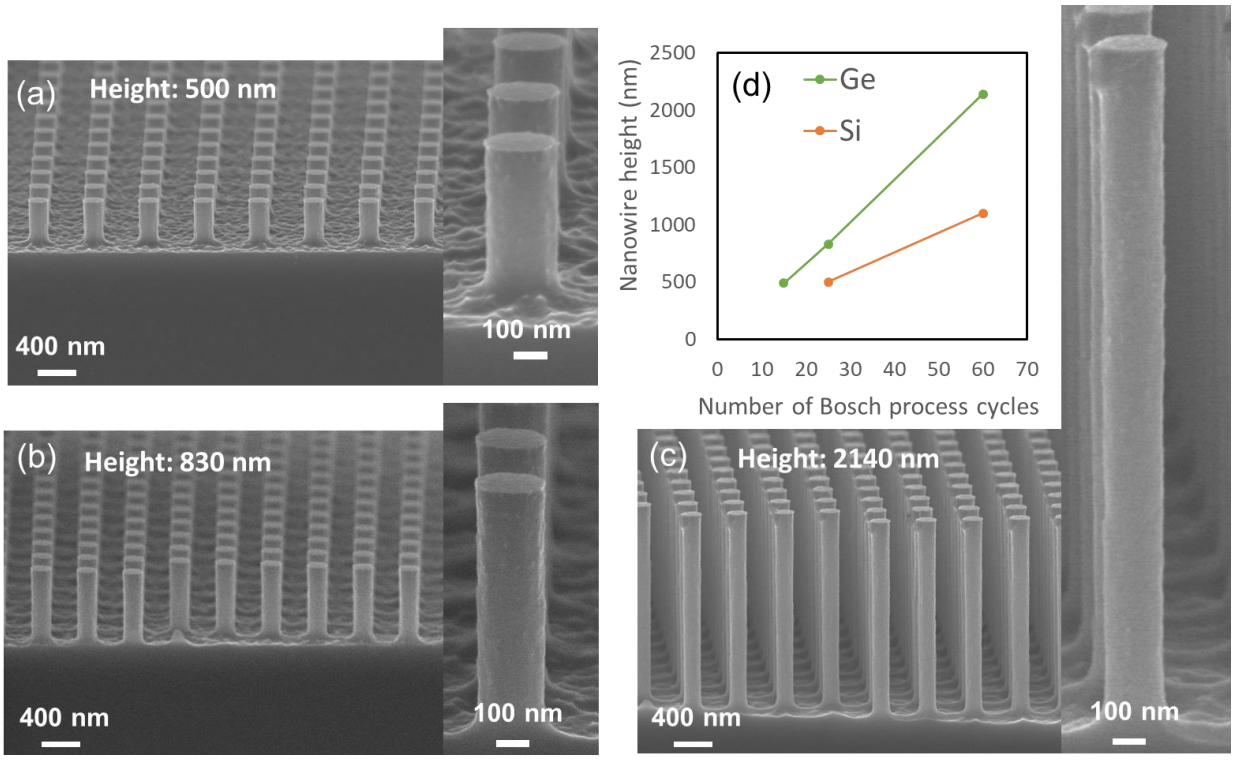

Figure 4.2. 75°-tilted SEM images of Ge NW arrays by NIL with Bosch process cycle numbers of (a) 15, (b) 25, and (c) 60. The insets show the magnification SEM images of the NW. (d) Ge and Si NW height as a function of Bosch process cycles.

4.1.2 Size reduction by etching in H_2O_2 solution

Since the electrical and optical properties of NWs highly are dependent on their size, it is important to control the size of NW for tuning the physical properties as well as increasing the integration level. Thermal oxidation at high temperature (950°C) for a long time (8 hours) is necessary to reduce the diameter of Si NW arrays with a smooth surface [50]. Unlike Si, Ge can be etched easily with chemicals [128], [129]. Here, H_2O_2 was chosen because of its appropriate etching rate at room temperature. The fabricated Ge NW arrays were first immersed in DI-water for 30 seconds to roughly remove the native oxide and then immersed in H_2O_2 (H_2O_2/H_2O: 1/10) solution for 0–240 seconds at room temperature to reduce the size of the NWs. After that, the NWs were washed with DI water and their morphology was evaluated by SEM.

The SEM images in Figure 4.3 show the morphology of Ge NW arrays after H_2O_2 treatment. The diameter was reduced from 220 nm to 30 nm successfully, and the surface of NWs is smooth after etching. The etching rate of Ge by H_2O_2 is about 20 nm/min, which is in good agreement with the value reported by D. P. Brunco et al. [128]. Incidentally, if the diameter is too small (less than 50 nm), they will be damaged by capillary force during drying. Therefore, in the case of fabricating Ge NW arrays shown in Figure 4.3d, the sample was washed with IPA after H_2O_2 etching.

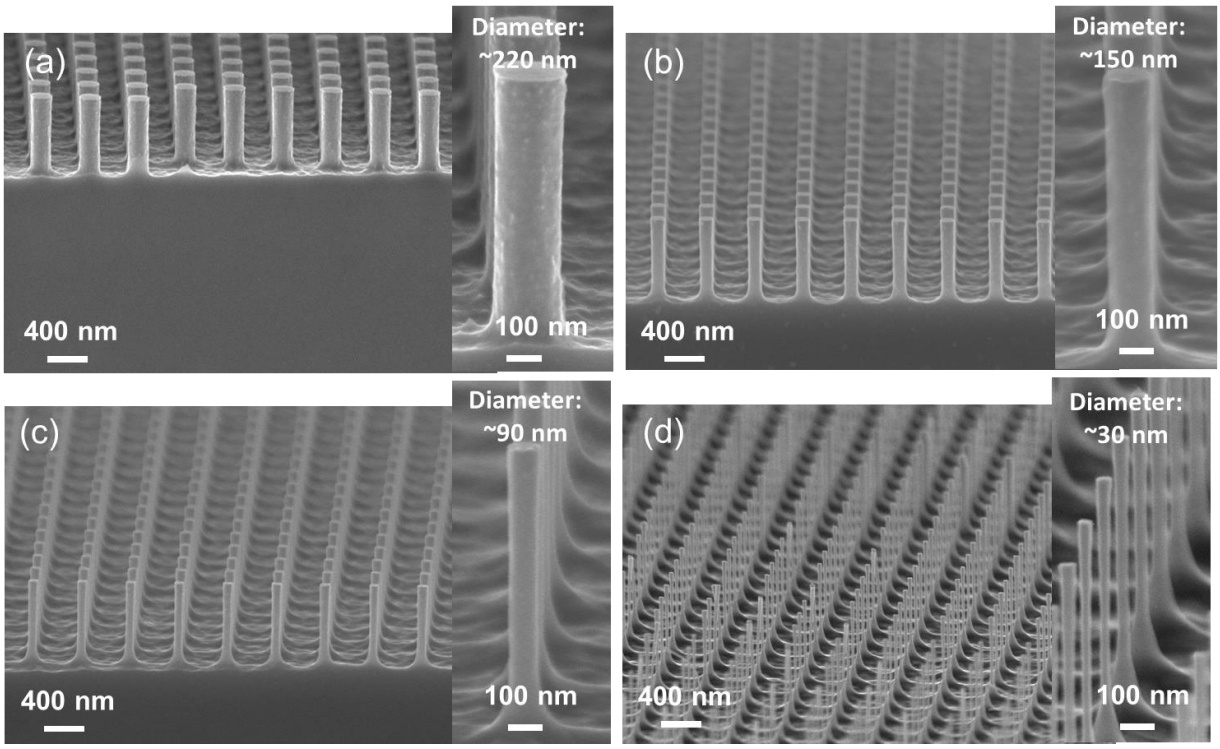

Figure 4.3. 75°-tilted SEM images of Ge NW arrays treated by wet chemical etching with etching times of (a) 0 s, (b) 100 s, (c) 200s, and (d) 240s for reducing the NW size. The insets show the magnification SEM images of the NW.

4.2 Ge/p-Si core–shell nanowire arrays

In order to functionalize the Ge NW arrays, the Ge/p-Si core–shell heterostructure is utilized to generate the hole gas and separate the carrier. As shown in Figure 4.4a, the previous p-Si/Ge core–shell NW structure accumulates the hole gas in the Ge shell region, which is grown by CVD method. Contamination of the Si surface and the lattice mismatch between Ge and Si result in the growth of a Ge shell with a high density of defects such as misfit dislocations, which reduce the carrier mobility in the Ge shell. Conversely, Figure 4.4b shows a Ge/p-Si core–shell NW structure with holes accumulated in the Ge core region. Since Ge NWs (the core region) are fabricated top-down from the substrate and have very good crystallinity, the Ge/p-Si core–shell NW structure is expected to have higher carrier mobility than the p-Si/Ge core–shell NW structure. On the other hand, reducing the size of Si requires higher temperatures, longer times, and more expensive equipment, so it is much easier to adjust the size of the core with Ge than with Si as the core. Furthermore, the doping concentration can be easily controlled by adjusting the flow rate of dopant precursor gas during shell formation.

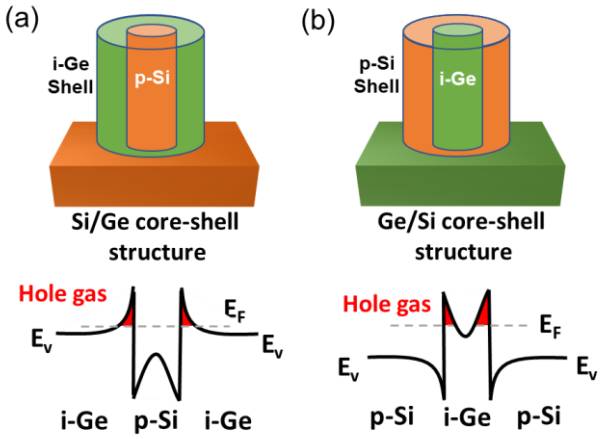

Figure 4.4. Schematic illustration of (a) p-Si/Ge and (b) Ge/p-Si core–shell NWs with corresponding band diagrams. E_V and E_F are the valence band edge and the Fermi energy, respectively. The hole gas accumulation is represented by red color.

4.2.1 Growth

The fabrication schematics of Ge/p-Si core–shell NW arrays are shown in Figure 4.5. First, Ge NW arrays with two different diameters (220 nm and 70 nm) were fabricated by H_2O_2 etching. These samples were immersed in HCl solution for 10 seconds at room temperature to roughly remove the native oxide, and then loaded into a chemical vapor deposition (CVD) chamber with a background pressure of 2×10^{-6} Pa. After pre-annealing at 800 °C or higher for 10 min to remove most of the oxide, boron-doped Si shell growth was carried out for 2 min at 700 °C using 19 sccm of SiH_4 (100%) and 0.5 sccm of B_2H_6 (1% in H_2) as precursor gases. The total pressure was set at 700 Pa by mixing with nitrogen gas. After shell formation, the samples were post-annealed at 800 °C for 10 min to activate the dopant.

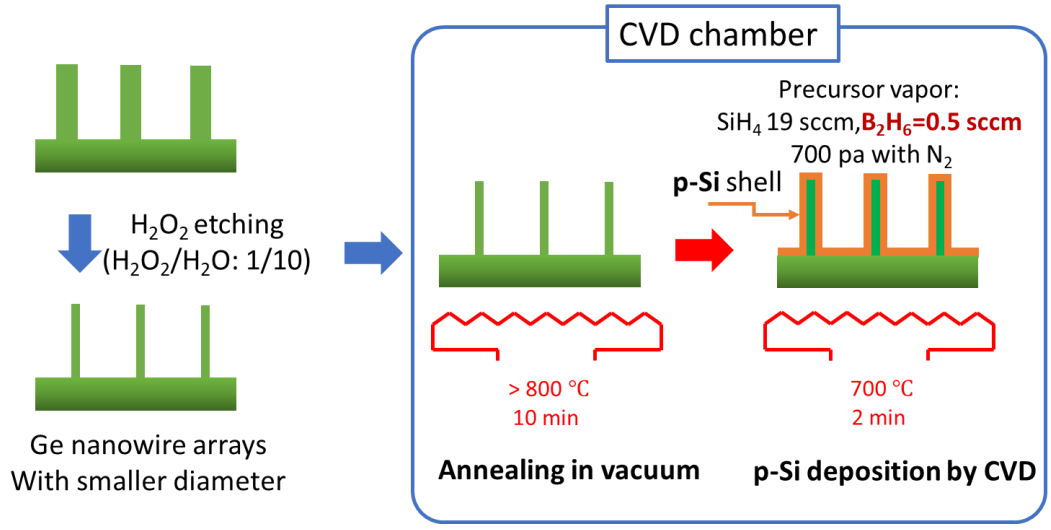

Figure 4.5. Schematic illustration of the procedure for p-Si shell growth on Ge NW arrays with different core diameter by CVD.

Figure 4.6 shows the morphology of the fabricated Ge/p-Si core–shell NW arrays. For both core sizes, the grown p-Si shell is about 40 nm thick and has a smooth surface. The growth rate of p-Si is comparable with the previous report of p-Si shells grown on Si/Ge core–shell NW arrays [50].

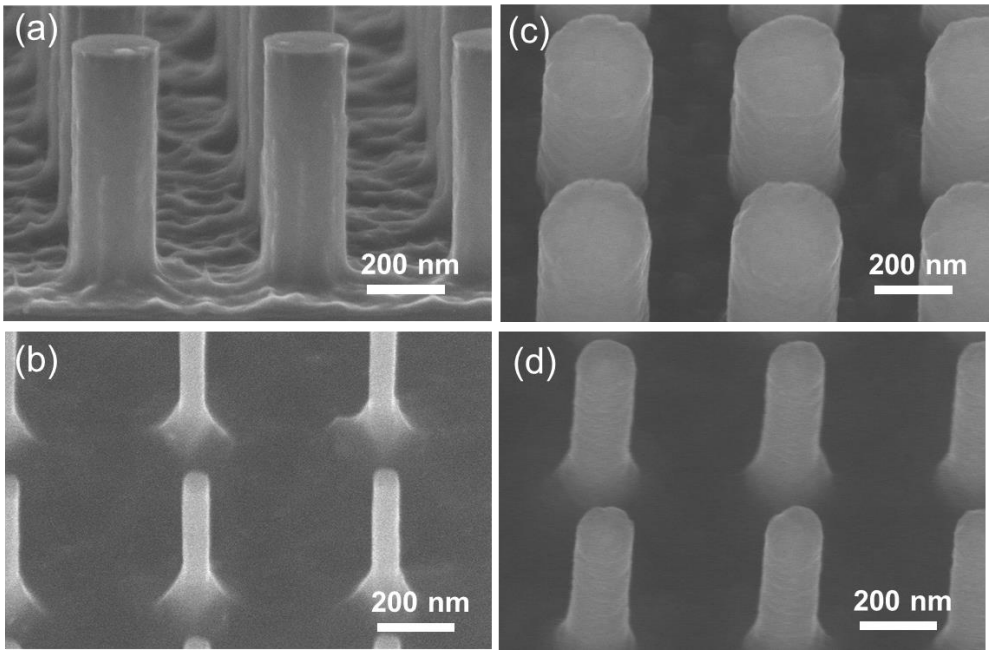

Figure 4.6. (a) 75°-tilted SEM image of Ge NW arrays (Bosch cycles: 30) before p-Si shell formation. (b) 30°-tilted SEM image of Ge NW arrays before p-Si shell formation with a core size of 70 nm. (c) 30°-tilted SEM images of Ge/p-Si NW arrays. (d) 30°-tilted SEM images of Ge/p-Si NW arrays with a core size of 70 nm.

4.2.2 Hole gas accumulation observed by Raman spectroscopy

Micro-Raman scattering measurements were performed at room temperature using a 532-nm excitation beam. The excitation laser beam was focused to a spot size of ~1 μm with a 100× objective lens, and the power was set to about 0.02 mW to prevent local heating effects. All the data were recorded with a spectral resolution of about 0.3 cm^{-1}. Figure 4.7a shows the asymmetric broadening and downshift of Ge optical phonon peaks after boron doping in Si shells. This phenomenon is caused by Fano interference and the hole gas concentration can be estimated by fitting the Fano equation (Section 1.6.1, Equation 1.3). The Fano parameters fitted from the Ge peaks using the Fano equation are shown in Figure 4.7b–d. The peak position for Ge/p-Si core–shell NW arrays is downshifted, and Fano parameters q and Γ are increased compared to the Ge/i-Si core–shell NW arrays, demonstrating hole gas accumulation in the Ge region. Here, the peak shift and asymmetric broadening due to phonon confinement effects can be ignored because the crystal quality is the same and the size is too large to observe phonon confinement effects. In the case of big-core NW arrays, the peak position is upshifted, and Fano parameters q and Γ are decreased compared to the small-core NW arrays, indicating a decrease of hole gas concentration in Ge region. This can be explained by the increase of the component in the Ge region where no hole gas is accumulated. Incidentally, the Raman shift of the Ge/i-Si

core–shell NW arrays is larger than that of the bulk Ge, which is attributed to the compressive stress due to the Si shell.

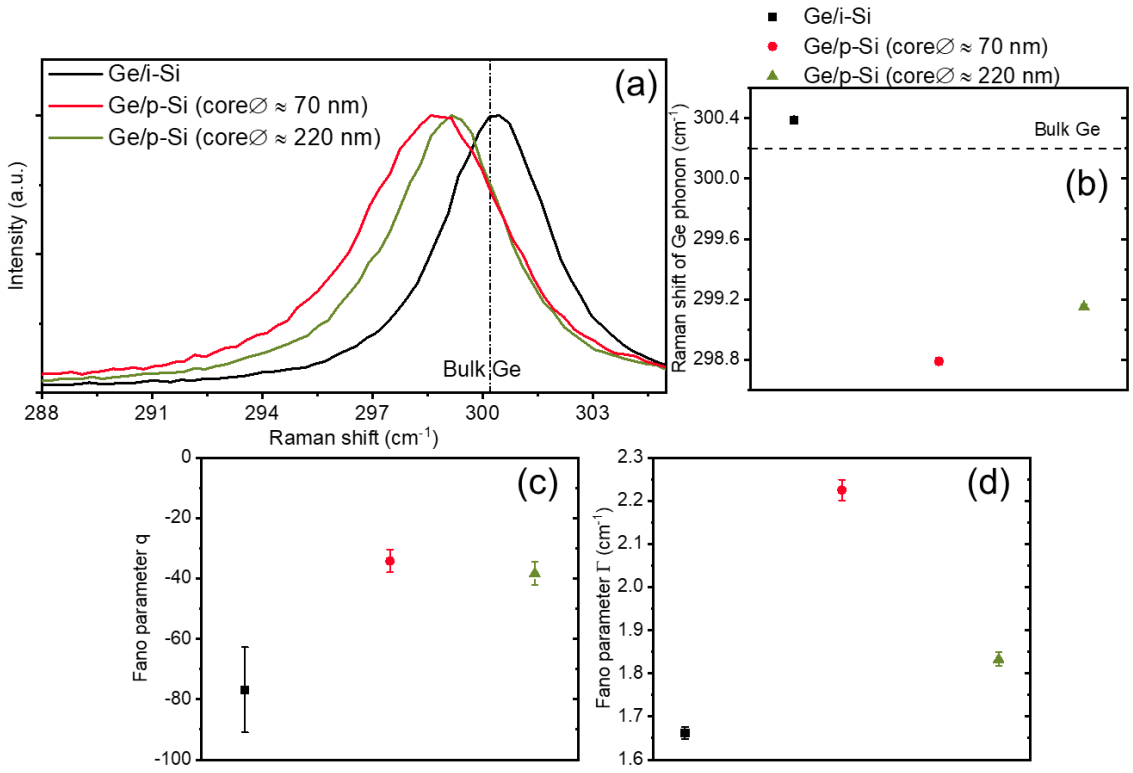

Figure 4.7. (a) Raman spectra of Ge/i-Si NW arrays and Ge/p-Si NW arrays with different core sizes. (b) Raman shift, (c) Fano parameter q, and (d) Fano parameter Γ obtained by fitting corresponding Ge optical phonon peaks with the Fano function. Standard deviation in Raman measurements is represented by the error bars.

4.3 Summary

Ge NW arrays with smooth surface were successfully fabricated using NIL and different lengths (from 500 nm to 2140 nm) can be achieved by varying the Bosch process cycles. The diameter of the Ge NW arrays can be controlled from 220 nm to 30 nm by chemical etching at room temperature using an H_2O_2 solution.

Ge/p-Si core–shell NW arrays were fabricated successfully by forming a p-Si shell layer on Ge NWs using CVD method. Hole gas accumulation in the Ge region was demonstrated by Raman scattering analysis, and the hole gas concentration is higher in the small-core than in the big-core.

Chapter 5

Si and Ge nanotubes fabricated by chemical vapor deposition and wet etching

Nanotube (NT) structures have unique physical properties, characterized by larger specific surface areas and more exposed active sites. Si nanotubes (SiNTs) and Ge nanotubes (GeNTs) are very promising semiconducting materials with potential applications as solar cells with enhanced light absorption [11] and faster and more controllable nanotube field-effect transistors (FETs) [12].

Here, we propose a low-cost, convenient, and time-saving method for fabricating vertically oriented GeNTs and SiNTs by using wet chemical etching to remove the ZnO template instead of a gas-phase etching process.

In the SiNTs session, the Si shell growth rate was investigated as a function of growth temperature and precursor gas flux in order to adjust the wall thickness of SiNTs. The morphology, elemental composition, and crystallinity of SiNTs were also evaluated. The crystallization of ZnO/Si core–shell NWs with different Si shell thicknesses by thermal annealing was also investigated.

In the GeNTs session, different growth times and temperatures were investigated to control the thickness, crystallinity, and morphology of the Ge shell layer. Since mechanical stresses in heterostructures will affect the electrical properties, stress in core–shell NW was investigated by X-ray diffraction (XRD) and Raman scattering. Finally, the ZnO core was removed from the core–shell NWs by wet etching to fabricate GeNTs, and the changes in composition and stress were investigated.

5.1 ZnO nanowire templates growth

In order to fabricate SiNTs and GeNTs, ZnO NWs are used as template materials. Therefore, in this part, we aim to synthesize ZnO NWs with a high aspect ratio and sufficient spacing. ZnO NWs can be prepared by the thermal vapor transport process [130]–[132], which always requires a high temperature [133]. On the other hand, the hydrothermal synthesis method can be performed at less than 100 ℃. Hydrothermal synthesis was first reported by Andres-Vergés et al. [134] for the growth of ZnO nanostructures, and Vayssieres et al. [135] successfully fabricated ZnO NWs on Si substrate by the thermal decomposition of hexamethylenetetramine (HMTA) and zinc nitrate. The growth process of ZnO NWs is based on the following reactions [136]–[138]:

$$
\begin{aligned}
(CH_2)_6N_4 + 6\,H_2O &\leftrightarrow 4\,NH_3 + 6\,HCHO \\
NH_3 + H_2O &\leftrightarrow NH_3 \cdot H_2O \\
NH_3 \cdot H_2O &\leftrightarrow NH_4^+ + OH^- \\
Zn^{2+} + 2\,OH^- &\leftrightarrow Zn(OH)_2 \\
Zn(OH)_2 &\rightarrow ZnO + H_2O
\end{aligned}
\qquad 5.1
$$

The chemicals to be prepared in this method are zinc nitrate, HMTA, ammonium hydroxide, and sodium citrate. Ken C. Pradel et al reported the synthesis of NWs by using a mixture of zinc nitrate and HMTA in the ratio of 2:1 [139]. As Equation 5.1 shows, HMTA is hydrolyzed to formaldehyde and ammonia, then ZnO nuclei are formed by dehydration of these hydroxyl groups. After the nucleation process, ZnO crystals continue to grow by condensation of hydroxyl groups on the surface [140], [141].

Various studies have been done on the addition of HMTA. Ashfold et al [142] reported that HMTA acts as a buffer. While HMTA decomposes slowly, the decomposition products provide a gradual and controlled supply of ammonia. It has been suggested that HMTA can adhere to the non-polar face of ZnO and expose the polar face to the growth solution, so that the Zn^{2+} ions remain only on the polar face (001) and continue further crystal growth along the c direction [143]. Figure 5.1 shows the attachment mechanism of hexamine to the non-polar plane.

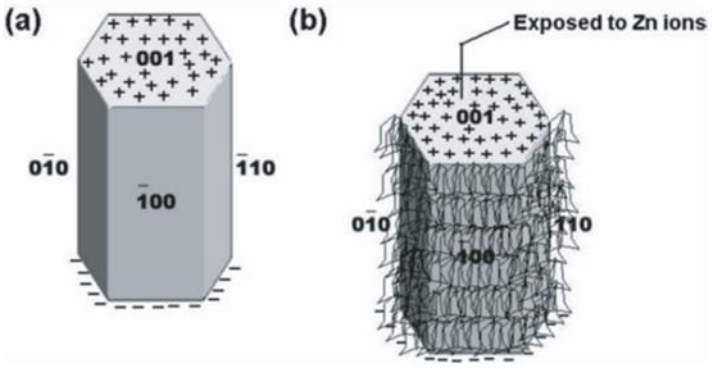

Figure 5.1. Schematic illustrations of (a) hexagonal ZnO and (b) ZnO with HMTA attached to the no-polar facets [143].

The supersaturation of Zn^{2+} in the solution is very high, and the Zn ions tend to nucleate homogeneously as a white precipitate at the bottom of the reaction vessel. When ammonium hydroxide is introduced into the solution, the homogeneous nucleation can be greatly suppressed [136]. With the addition of ammonium hydroxide, complexes $Zn(NH_3)_4{}^{2+}$ and $Zn(OH)_4{}^{2-}$ are generated [144]. This process reduces the supersaturation of free Zn^{2+} in the growth solution and suppresses the homogeneous nucleation of ZnO.

5.1.1 Growth

ZnO was sputtered 100 nm on n-type Si(100) substrate and used as a seed layer for NW growth. The growth solution consisted of zinc nitrate (10 mM), hexamethylenetetramine (HMTA) (5 mM), and ammonium hydroxide (0.6 M) with a small amount of sodium citrate (0.08 mM) to maintain the hexagonal cross-sectional shape of the NWs. All the aqueous solutions were prepared using ion-exchanged water, and all chemicals were purchased from FUJIFILM Wako Pure Chemical Corporation. The substrate was then floated on the solution surface with the front side down. Hydrothermal growth was carried out in an oven at 95 °C to activate the reaction for the first 30 min, followed by 6 hours to grow ZnO NWs. By optimizing the growth conditions, we were able to fabricate ZnO NWs with a high aspect ratio and large wire-to-wire spacing. After the growth of ZnO NWs, the morphology was evaluated using a Hitachi SU8000 scanning electron microscope (SEM) at an acceleration voltage of 5 kV.

Figure 5.2 shows that the ZnO NWs with a high aspect ratio and sufficient spacing were successfully grown, making them suitable for the next step of NT fabrication.

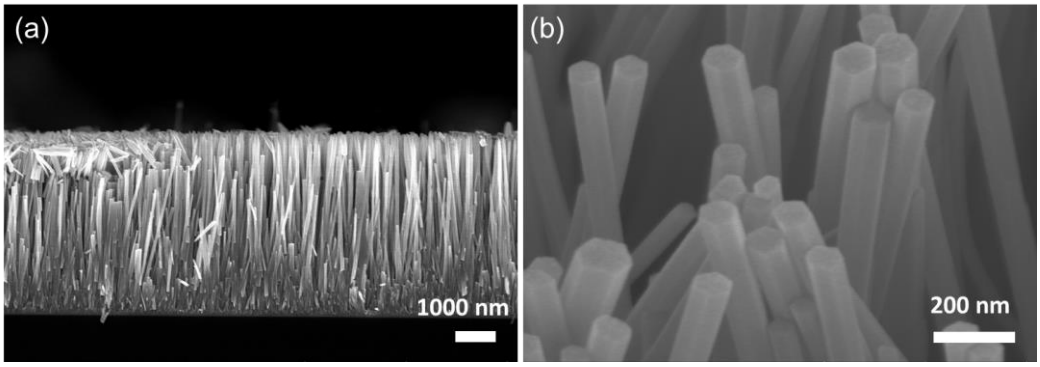

Figure 5.2. (a) Cross-sectional and (b) 30˚-tilted SEM images of hydrothermal synthesized ZnO NWs showing the hexagonal cross-sectional shape.

5.2 Si nanotubes

Silicon nanotubes (SiNTs) are of great interest due to their synthesis and potential applications in electronics, high-capacity energy storage, biosensors, and selective transport.

5.2.1 ZnO/Si core–shell nanowires growth

After cleaning with deionized water (DI-water) and isopropyl alcohol (IPA), the Si substrate on which ZnO NWs were formed was loaded into an ultra-high vacuum chemical vapor deposition (UHV-CVD) system with a background pressure of 2×10^{-6} Pa. Si shell layers were coated on ZnO NWs at temperatures of 650°C and 700°C using SiH_4 as the precursor gas. The growth time was increased from 6 min to 20 min. The SiH_4 gas flow rate was adjusted from 6 to 20 sccm and mixed with nitrogen gas to make the total pressure 700 Pa.

The ZnO core was selectively etched in phosphoric acid solution (85%) for 6 min at room temperature, followed by repeated washing with DI-water to remove residual acid to finally grow Si NT structures. Furthermore, the ZnO/Si core–shell NWs were treated by a rapid thermal annealing (RTA) at 800 °C for 5 min under N_2 atmosphere to study the crystallization of the Si shell layer. The whole fabrication procedure is shown in Figure 5.7.

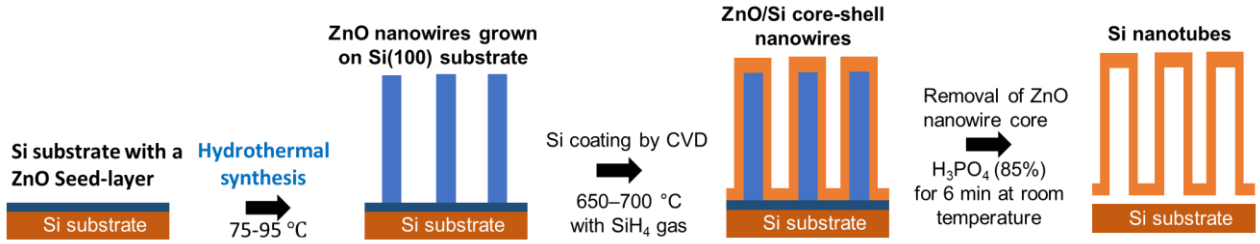

Figure 5.3. Schematic illustration of procedure for fabricating vertically aligned SiNTs [53].

5.2.2 Morphology of ZnO/Si core–shell nanowires

Figure 5.4 shows scanning electron microscopy (SEM) images of ZnO/Si core–shell NWs versus Si shell growth temperature and SiH_4 gas flux. The CVD process resulted in the formation of Si shell layers with thicknesses ranging from 12 to 21 nm on the ZnO core. The growth rate of the Si shells increased with SiH_4 gas flux, which was attributed to the high density of source materials available for its formation. When the growth temperature was increased from 650°C to 700°C, the decomposition rate of the precursor gas became faster and the growth rate of Si shells became faster. In order to obtain the appropriate shell thickness under each growth condition, the growth times of the samples shown in Figure 5.4a–f were set to 20, 20, 10, 15, 6, and 5 min, respectively.

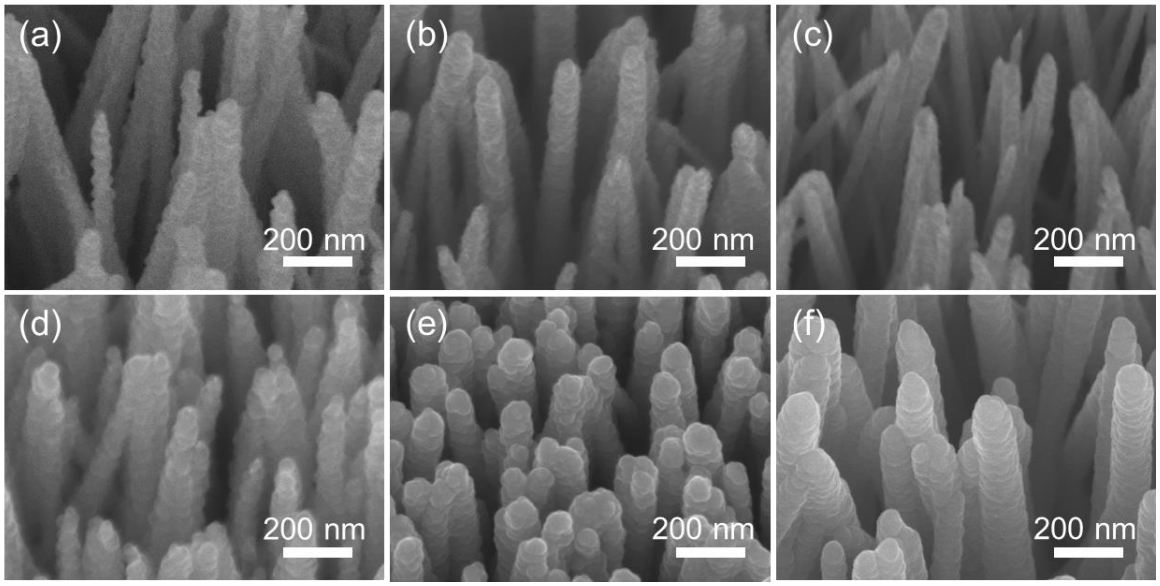

Figure 5.4. 30°-tilted SEM images of ZnO/Si core–shell NWs with the shell layer grown at 650 °C using (a) 10, (b) 20, and (c) 40 sccm of SiH_4 gas flux. 30°-tilted SEM images of ZnO/Si core–shell NWs with Si shell grown at 700 °C using (d) 6, (e) 20, and (f) 40 sccm of SiH_4 gas flux [53].

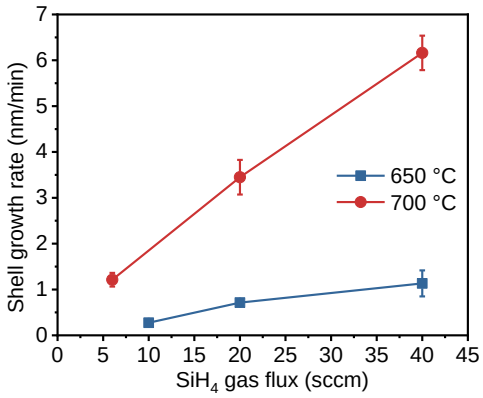

Figure 5.5. Si shell growth rate as a function of the SiH_4 gas flux at 650 °C and 700 °C [53].

5.2.3 Thermal annealing of ZnO/Si core–shell nanowires

In order to improve the electrical and optical performance, ZnO/Si core–shell NWs were thermal annealed to crystallize their Si shell layers. Figure 5.6a,b show that there is little change in the morphology of the NWs after rapid thermal annealing at 800 °C for 5 min. Figure 5.6c,d show the results of Raman scattering analysis using a 355 nm excitation light. This wavelength was chosen for its short penetration depth to suppress the signal from the ZnO core. No Raman peaks were observed before annealing for either the thick (20 nm) or thin (12 nm) Si shell layer samples, indicating that the Si shell layer is amorphous rather than crystalline. After annealing, the Si optical phonon peaks shifted to higher wavenumber and reached the bulk value (520.1 cm^{-1}) with increasing the thickness of the Si shell. The downshift to lower wavenumbers and asymmetric broadening observed in core–shell NWs with thin shell layers can be explained by the phonon confinement [86], [90], [91], [93], [145].

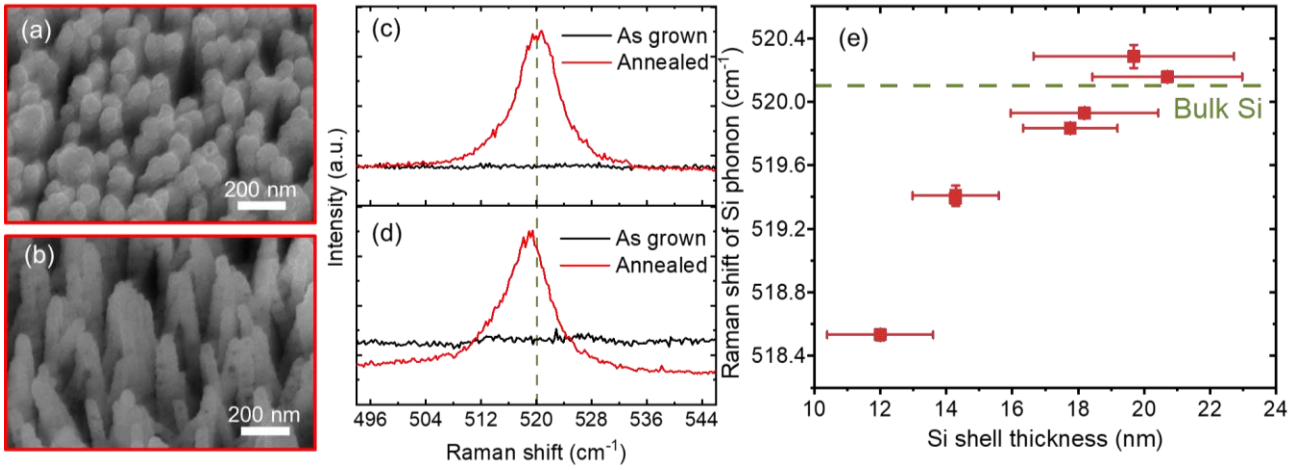

Figure 5.6. 30°-tilted SEM images of ZnO/Si core–shell NWs with a Si shell thickness of (a) 20 nm and (b) 12 nm after thermal annealing at 800 °C for 5 min. Corresponding Raman spectra for the NWs with the Si shell thickness of (c) 20 nm and (d) 12 nm before and after annealing. (e) Raman shift of Si optical phonon peaks for NWs as a function of Si shell thicknesses after annealing. The error bar indicates the standard deviation of Raman measurements and shell thickness. Bulk Si value is indicated by the green dashed line [53].

The phonon confinement model (RCF model) and the Raman intensity are given as Equation 1.4 in Section 1.6.1, where $C(0,q)$ is the Fourier coefficient of the confinement function, $\omega(q)$ is the Si phonon dispersion, and Γ_0 is the full width at half maximum (FWHM) of the Bulk Si. Here, we used the following relations: $|C(0,q)|^2 = \exp(-q^2d^2/16\pi^2)$ and $\omega(q) = [A + B\cos(q\pi/2)]^{0.5} + D$, with $A = 1.714 \times 10^{15}$ cm^{-2} and $B = 10^5$ cm^{-2} [92]. D is an adjustment parameter for reference samples. In the case of one-dimensional nanostructures such as NW and NT, $d^3q \propto qdq$. After removing the ZnO core, the Si shell structure is an NT structure, which is different from the general NW structure. Considering the small diameter of the Si/ZnO core–shell NW, the Si shell structure was treated as a pseudo-NW structure. The fitting results are shown in Figure 5.7. The phonon correlation length estimated by the fitting was about 7–8 nm, which is in good agreement with the thickness of the Si shell layer.

However, the fitting is not so good on the low and high wavenumber sides. There are several possible reasons for this. First, the relation used for the approximation is the one adopted for NW. Secondly, there is the issue of the crystallinity of the Si shell. This is considered to be the main reason for the incomplete fitting on the low-wavenumber side. Thirdly, the effect of strain from the ZnO/Si heterojunction, mainly incomplete fitting at the high wavenumber side, may be a factor. As shown in Figure 5.6g, the optical phonon peak of Si shell was found to have a higher Raman shift than the bulk Si. This upshift implies that compressive stress is induced in the Si shell from the ZnO core.

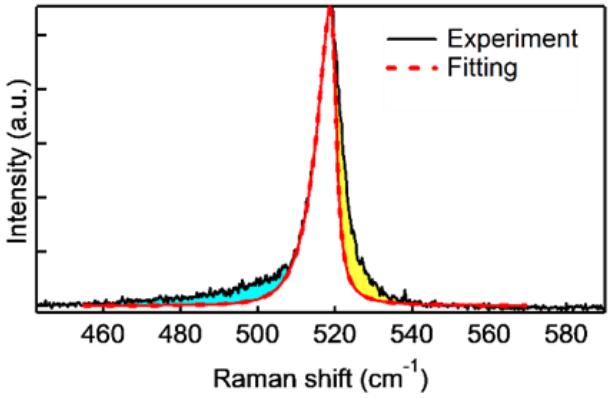

Figure 5.7. Fitting result of Si optical phonon peak observed for ZnO/Si core–shell NWs (Si shell thickness:12 nm) using phonon confinement theory [53].

5.2.4 Si nanotubes fabrication by wet etching

Figure 5.8 shows the SEM images of Si-shelled NWs grown at 700 °C for 6 min using SiH_4 gas (20 sccm) flux without thermal annealing. The SEM image in Figure 5.8b shows darker areas in the center of all single NWs compared to Figure 5.8a, indicating the formation of cavities after the wet etch process. In Figure 5.8c, the XRD pattern recorded from the NWs shows that there is no ZnO peak after etching, confirming that the ZnO core has been removed. The presence of the Si peak is mainly from the Si substrate, as the growth on the ZnO surface has made the Si shell less than perfectly crystalline and closer to amorphous.

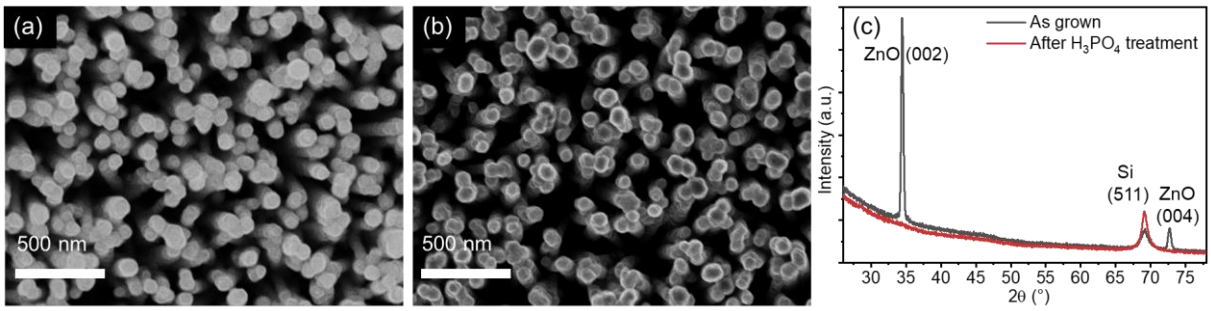

Figure 5.8. Top-view SEM images of ZnO/Si core–shell NWs (a) before and (b) after the H_3PO_4 etching. (c) Corresponding XRD pattern recorded from NWs [53].

The TEM images in Figure 5.9a,b show a sealed tube structure with a wall thickness of about 20 nm. The selected area electron diffraction (SAED) pattern in Figure 5.9b shows a hazy halo ring, which indicates that the Si shell layer is amorphous. The cross-sectional TEM image through the bottom of the NW in Figure 5.9c shows a hexagonal cavity derived from the cross-sectional shape of the ZnO NWs. Elemental mapping and line scans of the SiNTs in Figure 5.9d,e show that the SiNTs were successfully synthesized, and the TEM-EDX spectrum in Figure 5.9f shows that the ZnO core was completely etched. Furthermore, by etching the caps of these vertical-aligned SiNTs with reactive ion etching (RIE) [19], open-cap SiNTs can be obtained and a wider range of applications can be expected.

It is expected to be a promising approach in the development of anode materials for Lithium-ion batteries that require high capacity at low cost. This technique can be applied to materials that can be selectively etched. For example, replacing ZnO with a material such as Ge [32], [35] enables epitaxial growth of Si shell, which is expected to form NT structures with a smoother surface. Impurity doping is also important in functionate the Si NTs [93], [146], [147]. Since this CVD method can be used for doping impurities, various applications are expected in the future.

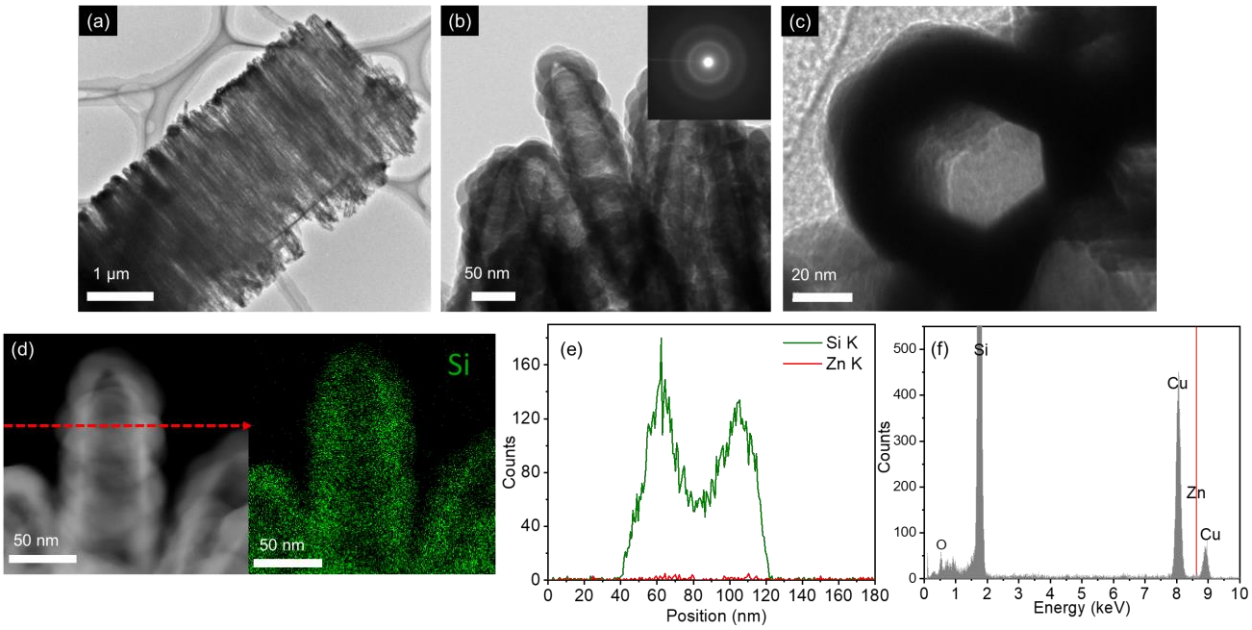

Figure 5.9. (a) Low- and (b) high-magnification TEM images of the SiNTs. The inset shows corresponding selected area electron diffraction (SAED) pattern indicating its amorphous nature. (c) Cross-sectional TEM image showing the hexagonal inner shape of the SiNTs. (d) STEM image and EDX mapping for Si of the SiNTs. (e) EDX linescan for Si and Zn along the width of a SiNT. The dashed line in (d) indicates the scan position and direction. (f) TEM-EDX spectrum recorded from the SiNTs showing the absence of Zn composition [53]. Note that the Cu peaks in the spectra originate from the Cu grid.

5.3 Ge nanotubes

One-dimensional germanium (Ge)-related nanostructures, such as nanotubes (NTs) with high specific surface area, show high performance in energy storage and electronic devices, and their structural control is important for further performance improvement and stabilization.

5.3.1 ZnO/Ge core–shell nanowires fabrication

The ZnO NWs were first washed with DI-water and isopropyl alcohol (IPA) to remove the by-products. Ge shell layers were grown on ZnO NWs using a UHV-CVD system (background pressure: 2×10^{-6} Pa). with GeH_4 as the precursor gas, a gas flow rate of 10 sccm, and nitrogen mixed with the precursor gas to keep the total pressure at 700 Pa. The growth temperature was varied from 400 °C to 500 °C and the time from 1 min to 5 min. The whole fabrication procedure is shown in Figure 5.10.

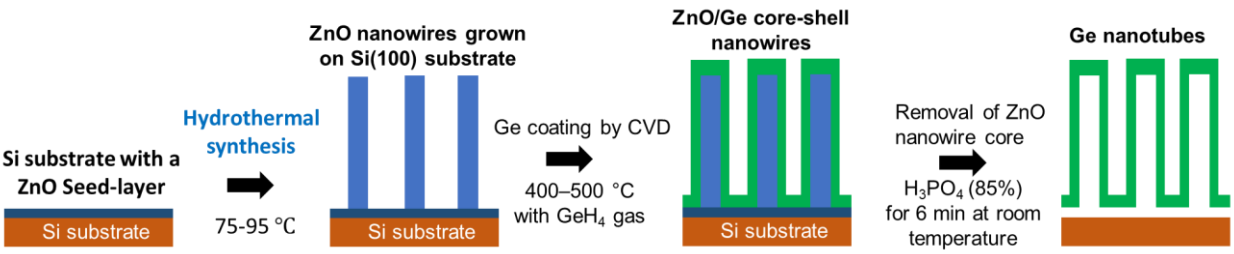

Figure 5.10. Schematic illustration of the procedure for fabricating GeNTs.

5.3.2 Morphology of ZnO/Ge core–shell nanowires

Scanning electron microscopy (SEM) images of ZnO/Ge core–shell NWs are shown in Figure 5.11a–i. The Ge shell layer was grown by CVD on the ZnO NW core with an average thickness of 0–422 nm. The surface of the core–shell NWs appears rougher at higher growth temperatures, which may be due to the higher surface migration rate of the Ge adatoms, resulting in larger grain size. The lack of shell coverage on the NW tip in Figure 5.11e is probably due to the low Ge deposition rate on the {0001} plane of ZnO.

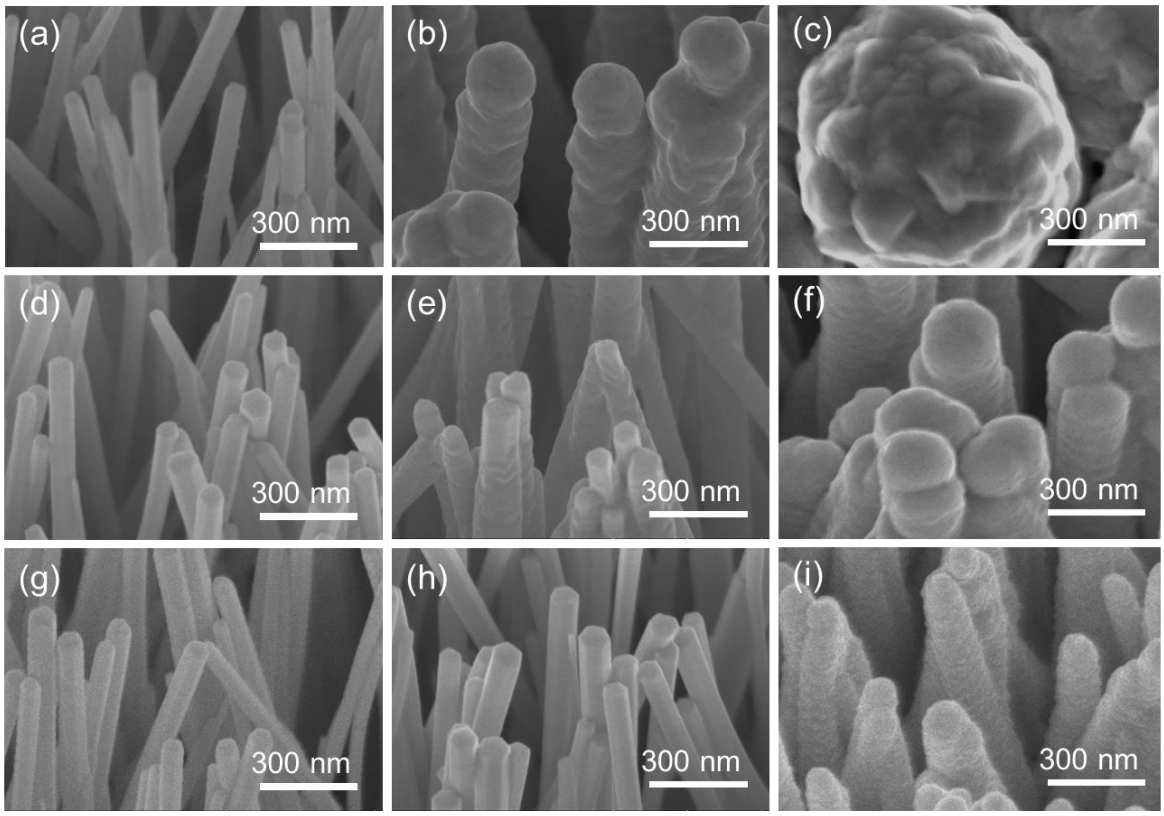

Figure 5.11. 30°-tilted SEM images of vertically aligned ZnO/Ge core–shell NWs with the Ge shell layer grown at (a–c) 500 °C, (d–f) 450 °C , and (g–i) 400 °C for (a,d,g) 1 min, (b,e,h) 2 min, and (c,f,i) 5 min.

Figure 5.12j shows that the growth rate of the Ge shell increases with the growth temperature, which is attributed to the faster decomposition rate of the precursor gas. The shell thickness is

estimated to be zero for the first minute and then increases superlinearly with growth time, indicating that there is an incubation process for the initial nucleation of Ge on ZnO.

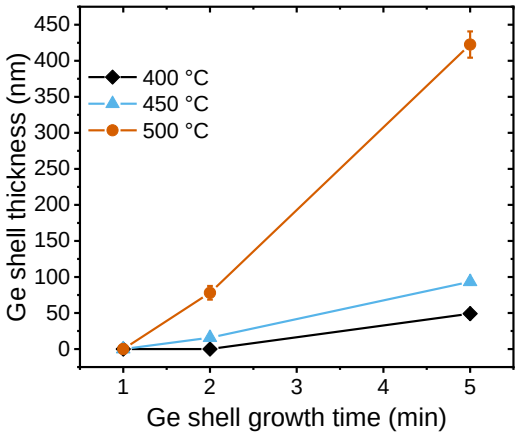

Figure 5.12. Ge shell thickness as a function of the shell growth time at 400 °C, 450 °C, and 500 °C. The shell thickness here was estimated by subtracting the radius of NWs before and after shell growth.

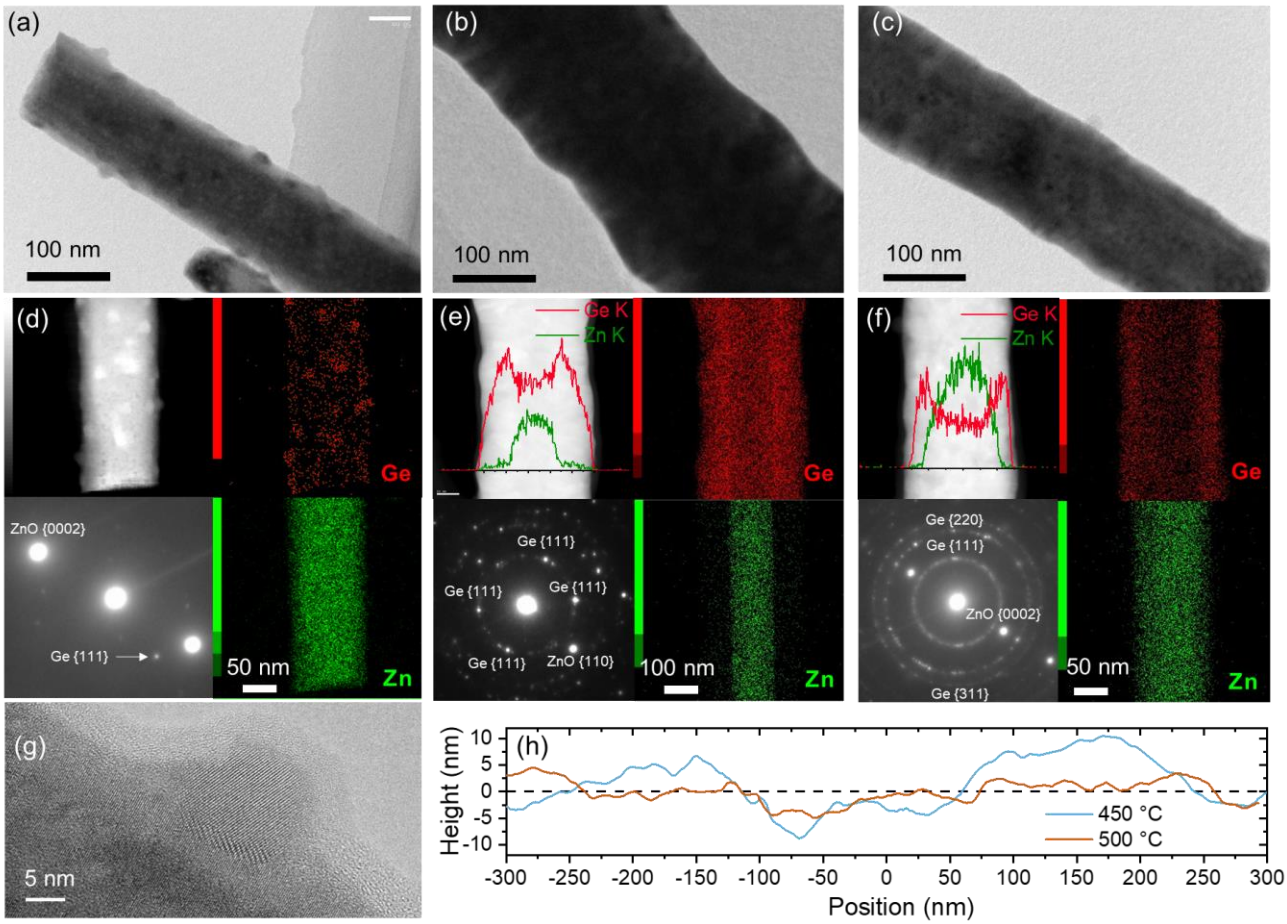

Figure 5.13. TEM images of the ZnO/Ge core–shell NWs with Ge shell layer grown at 500 °C for (a) 1 min and (b) 2 min. (c) TEM images of the ZnO/Ge core–shell NWs with Ge shell layer grown at 450 °C for 2 min. (d–f) Corresponding STEM, overlapped EDX linescan images, SAED patterns, and EDX mapping images for Ge and Zn. (e) Surface profiles of the NWs grown at 450 °C and 500 °C for 2 min.

Next, transmission electron microscopy (TEM), selected area electron diffraction (SAED), and energy-dispersive X-ray spectroscopy (EDX) analysis were performed to investigate the morphology, crystallinity, and elemental distribution of the NWs. Ge shell formation was carried out at 500 °C for 1 min for the core–shell NWs shown in Figure 5.13a. The core–shell NWs are covered with islands with an average diameter of 18 nm. These islands were confirmed to be Ge nanodots by EDX mapping and high-resolution TEM (HRTEM) in Figure 5.13d,g. Due to the detection limit and low spatial resolution of EDX analysis, it is unclear whether a Ge thin film is formed on the ZnO NW surface.

When the shell growth time was increased to 2 minutes, the thickness of the Ge shell was confirmed to be 75 nm from the EDX mapping in Figure 5.13e. This core–shell structure was further confirmed by EDX line scan analysis on the left side of Figure 5.13e. The ring-like pattern in the SAED image reveals the polycrystalline nature of the Ge shell. For Ge shells grown at a lower growth temperature (450°C), the rings become hazy in the SAED pattern, indicating a smaller grain size of the Ge shell. The surface profile of the core–shell NWs is plotted in Figure 5.13h to quantify the surface roughness. The Ge shell grown at 450 °C has a smoother surface (RMS: 2.2 nm) compared to 500 °C (RMS: 4.6 nm), which can be attributed to its smaller grain size.

5.3.3 Internal stress of ZnO/Ge core–shell nanowires

X-ray diffraction (XRD) measurements were performed to estimate the lattice constant and internal stress of the core–shell NWs. As the lattice constant moves away from the bulk value, the stress increases. As shown in Figure 5.14a,b, the ZnO core of the core–shell NWs has a larger lattice constant than that of the general ZnO NWs, indicating tensile stress in the ZnO core. This stress increases as the thickness of the Ge shell increases. Among the three growth temperatures, the NWs grown at 500 °C have the lowest stress due to the stress relaxation of the shell layer at high temperature. The internal stress of the core–shell NWs grown at 400 °C is smaller than that of those grown at 450 °C, which can be explained by the grain boundary relaxation due to the small grain size of the Ge shell. Here, the grain size of the Ge shell is discussed in the following Raman study.

The internal stress and crystallinity of core–shell NWs can also be evaluated by Raman scattering analysis. In general, compressive stress shifts the Ge phonon peak to the higher wavenumber side, and the smaller the grain size of the material, the lower the wavenumber (phonon confinement effect) [86], [90], [91], [93], [145]. Figure 5.15 shows the dependence of the Ge phonon peak on shell growth temperature and time. It can be seen that the shift of the peak is smaller than the bulk value (520.1 cm^{-1}) and then increases as the shell thickness increases. As the shell thickness increases, the phonon confinement effect weakens and the stress-induced shift becomes dominant, resulting in a Raman shift that exceeds the bulk value. After reaching the maximum value, the Raman shift eventually returns to the bulk value, which is due to the relaxation of stress due to the large thickness of the shell. The FWHM in Figure 5.15c shows that the crystallinity of Ge shell increases as the growth temperature increases. Unlike the

results of the XRD analysis, the NWs grown at 450 °C and 500 °C show almost the same Raman shift. This may be due to the strong phonon confinement effect at 450 °C due to the small grain size, which compensates for the shift caused by stress (discussed in the TEM analysis part). The particularly low Raman shift at 400 °C also indicates that the grain size of the shell layer is extremely small.

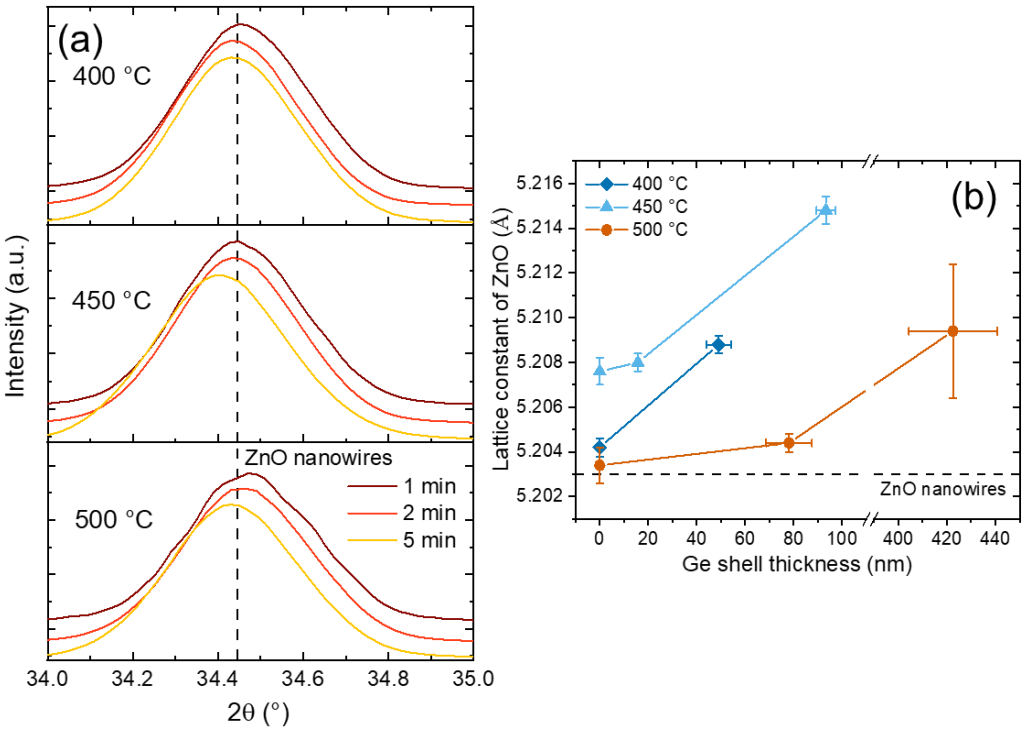

Figure 5.14. (a) XRD patterns of ZnO/Ge core–shell NWs with different Ge shell growth times and temperatures. (b) Corresponding lattice constant calculated from the ZnO(002) peaks. Lattice constant of ZnO NWs is indicated by the black dashed line. The spectra were normalized and stacked with vertical offsets for comparison. The error bar indicates the standard deviation of fitting of XRD spectra and shell thickness.

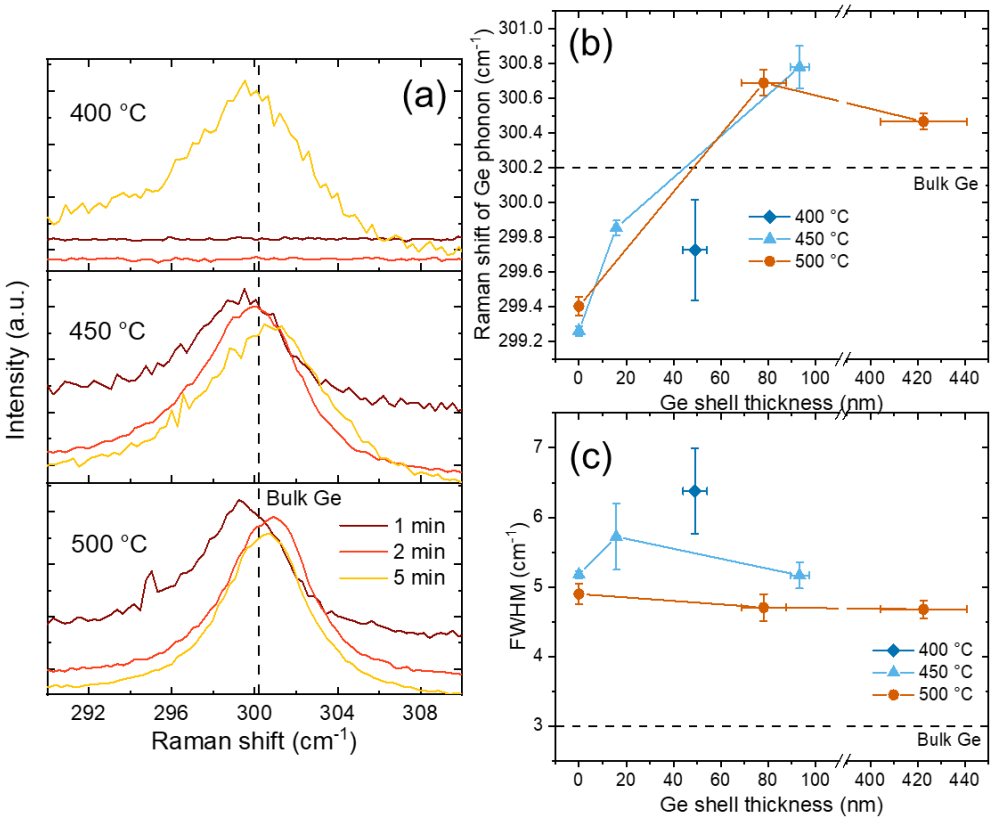

Figure 5.15. (a) Raman spectra of ZnO/Ge core–shell NWs with different Ge shell growth times and temperatures. Corresponding (b) Raman shift and (c) FWHM of Ge optical phonon as a function of Ge shell thickness. Bulk Ge value is indicated by the black dashed line. The spectra were normalized and stacked with vertical offsets for comparison. The error bar indicates the standard deviation of Raman measurements and shell thickness.

5.3.4 Ge nanotubes fabrication by wet etching

The as-grown ZnO/Ge core–shell NWs were subjected to a wet chemical etching process in which they were immersed in phosphoric acid (85%) at room temperature. After etching for 6 min, they were washed several times with DI-water to remove any residual acid. Here, phosphoric acid was chosen for the wet etching process due to the relatively low etching rate of Ge (less than 0.002 nm/min) [128].

To fabricate Ge NTs, phosphoric acid (H_3PO_4) was used to selectively etch away the ZnO core from the as-grown core–shell NWs. The open-cap tubular structures in Figure 5.16a–c show that the Ge NTs were successfully fabricated. The removal of ZnO was also confirmed by XRD shown in Figure 5.16d. The spectrum of the NWs after phosphoric acid treatment showed the disappearance of the ZnO(201) peak and a significant decrease in the ZnO(002) peak. Note that the spectra here are normalized by the Ge peak for comparison. In order to investigate the stress in the Ge NTs, Raman measurements were performed again. The Raman shift of the Ge optical phonon in Figure 5.16e shows an overall downshift compared to the as-grown core–shell NWs. This downshift is attributed to the relaxation of the tensile stress inside the Ge due to the removal of the ZnO core. Incidentally, the Raman peak is upshifted compared to the bulk value due to the residual stress left inside the NT by the ZnO left after etching.

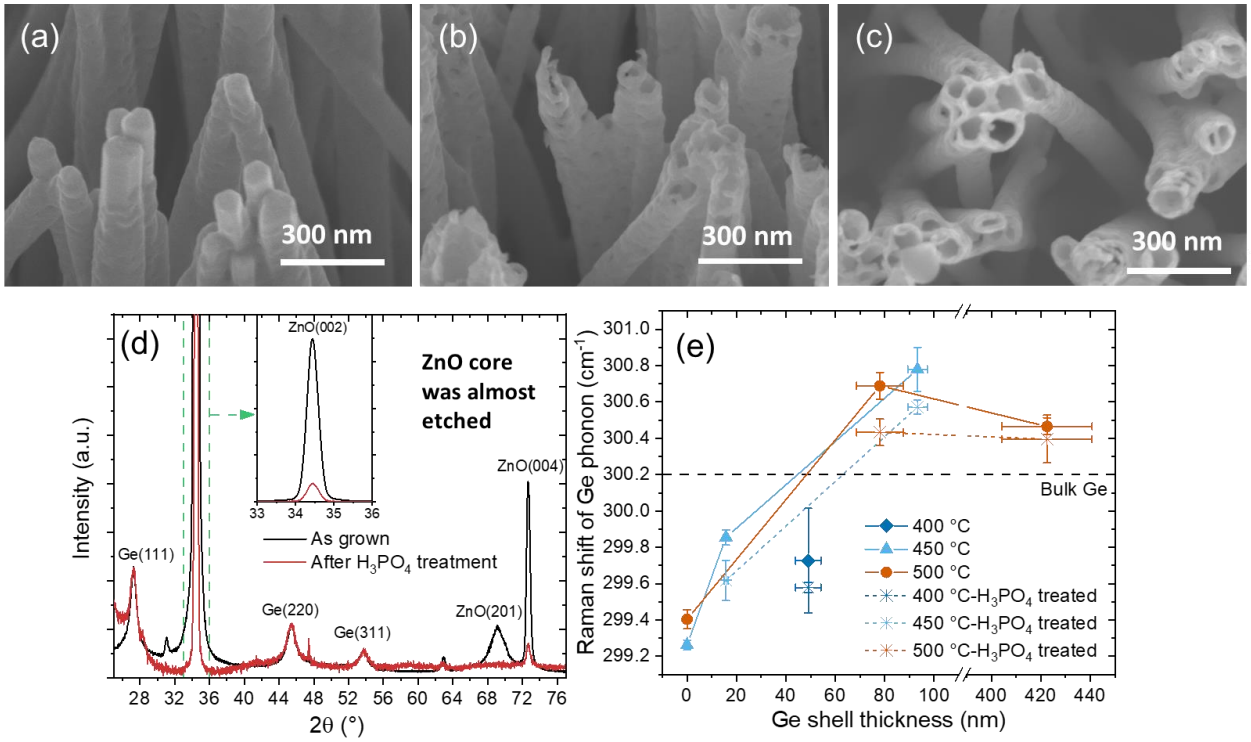

Figure 5.16. 30°-tilted SEM images of ZnO/Ge core–shell NWs (Ge shell thickness: 16 nm) (a) before and (b) after H_3PO_4 treatment. (c) Top-view SEM image of (b). (d) Corresponding XRD pattern recorded from the NWs. The inset shows the overall shape of ZnO(002) peaks. (e) Raman shift of Ge optical phonon before and after the H_3PO_4 treatment as a function of Ge shell thickness.

These vertically aligned Ge NTs can be further improved by coating them with a shell layer to form a NT heterostructure. For example, adding a Si shell layer to the outer or both sides of Ge NTs can improve their performance and stability and increase their lithiumation capacity [37]. High electronic or ionic conduction layers by atomic layer deposition (ALD) can prevent solid electrolyte interface (SEI) buildup and improve capacity retention and cycling stability [17]. The inner diameter of the NTs can be tuned in the future by adjusting the hydrothermal growth conditions of ZnO NWs and optimizing the stress to improve the electrochemical performance.

5.4 Summary

We have developed a simple and low-cost route to fabricate vertically oriented Si NTs and Ge NTs by applying a wet etching process to the ZnO region of ZnO/Si(Ge) core–shell NWs.

The growth rate of Si shells can be controlled by adjusting the flux of the precursor gas and the growth temperature. The dependence of the crystallization of the Si shell layer on the thermal annealing of ZnO/Si core–shell NWs was investigated. The Si optical phonon peak shifted to the higher wavenumber side as the thickness of the Si shell increased. In order to demonstrate the phonon confinement effect of Si NTs, the Si optical phonon peak was fitted with a phonon confinement model. After selective etching of the ZnO core from ZnO/Ge core–shell NWs, the fabricated SiNTs showed amorphous nature with hexagonal hollow.

Ge shell growth on ZnO NWs was studied by varying the growth time and temperature. The morphology, crystallinity, and stress of the grown ZnO/Ge core–shell NWs were thoroughly investigated. At higher growth temperatures, the growth rate is faster and the Ge shell has a larger gain size, higher crystallinity but a rougher surface. The shell thickness was estimated to be zero for the first minute and then increased superlinearly with the growth time. Tensile and compressive stresses were observed in the ZnO core and Ge shell, respectively, and increased with increasing shell thickness. the ZnO/Ge. The stress in the shell decreased after selective etching of the ZnO core from the core–shell NWs.

Chapter 6

Si nanotube arrays fabricated by nanoimprint lithography with spacer patterning

Unlike sacrificial templates methods, top-down approaches provide vertical 1D structure with smooth surface, high crystal quality, and highly ordered arrangement, which make them suitable for electronic applications. Spacer patterning is known as one of the techniques used to overcome the resolution limit in the semiconductor industry [77]. However, the fabrication of Si nanotube (NT) arrays with smooth surface and well-ordered arrays is still a challenge. Here, we propose the use of nanoimprint lithography (NIL) and spacer patterning technique atomic layer deposition (ALD) to fabricate Si NT arrays with a high aspect ratio and nano-scale wall thickness. The morphology of NTs of different diameters and lengths was characterized by scanning electron microscopy (SEM). For the application in the field of electronics and optoelectronics, defects on the NT surface, and reflectance of NT arrays were evaluated by electron spin resonance spectroscopy (ESR), and UV-vis-NIR spectrophotometer, respectively.

6.1 Si nanotube arrays fabrication

Figure 6.1 shows the schematic diagram of the Si NT arrays fabrication process. The process can be divided into two parts: the fabrication of photoresist nanohole arrays and the fabrication of NT arrays.

Fabrication of photoresist nanohole arrays: first, the n-Si(100) wafers were cleaned by an excimer UV irradiation system. Next, a UV-curable imprint photoresist was spin-coated onto the Si substrate and prebaked. A quartz stamp with periodic NWs was brought into contact with this photoresist layer and subjected to UV irradiation. After the stamp was removed, the cured photoresist was baked again and the residual layer was removed by CCP-RIE. The detailed fabrication process is described in Section 4.1, Fabrication of photoresist nanohole arrays.

Fabrication of nanotube arrays: an Al_2O_3 layer is uniformly deposited over the photoresist by atomic layer deposition (ALD) (Picosun SUNALE R-150 ALD) at the temperature of 50 °C. Trimethylaluminum (TMA) and deionized water (DI-water) were used as precursors and the thickness of Al_2O_3 was controlled by the number of ALD cycles (142 cycles: 18 nm, 213 cycles: 28 nm). Next, the ring-like array pattern was achieved using inductively coupled plasma reactive ion etching (ICP-RIE) (ULVAC CE300I) with CF_4 and Ar gases (CF_4 40 sccm, Ar 10sccm, process pressure 1.3 Pa) for 60 seconds. Here, the antenna power is set to 500 W with a bias of 100 W. To fabricate NT structures with a high aspect ratio, SF_6 plasma followed by C_4F_8 plasma (Bosch etching process) was applied for deep etching of Si NT structure using a Si deep etcher (Sumitomo Precision Products MUC-21 ASE-SRE). The flow rates of SF_6 and C_4F_8 were both fixed at 35 sccm, the chamber pressure was 0.75 Pa, and the RF power was 100W. The number of Bosch cycles was set to 30 and 60 for adjusting the length of NT arrays. After removing the organic contamination by plasma ashing (>100 °C), the Al_2O_3 mask was removed by immersion in HF (1%) for at least 40 min at room temperature. SEM images of specific process steps were recorded using a Hitachi SU8000 SEM with an acceleration voltage of 10 kV.

The corresponding 75˚-tilted SEM images for etch step are shown in Figure 6.1b. The image of the first step shows photoresist nanohole arrays fabricated on the Si substrate (layer thickness of about 200 nm), with the exposed Si surface in the nanohole. In the next image, the Al_2O_3 spacer layer is uniformly formed on the resist, and the particle contamination on the surface is due to platinum deposition by the ion sputtering system for SEM characterization. The third image shows that the ring-like array pattern was achieved successfully using an anisotropic RIE process with the photoresist completely removed. The RIE process anisotropically removes the horizontal spacer layer, resulting in a remaining spacer sidewall serving as a ring-like etching mask. The reason why the etching depth differs between the outside and inside of the ring is that it takes extra time to etch the resist on the outside of the ring. The fourth image shows the successful fabrication of the Si NT array with an Al_2O_3 mask attached to the tip.

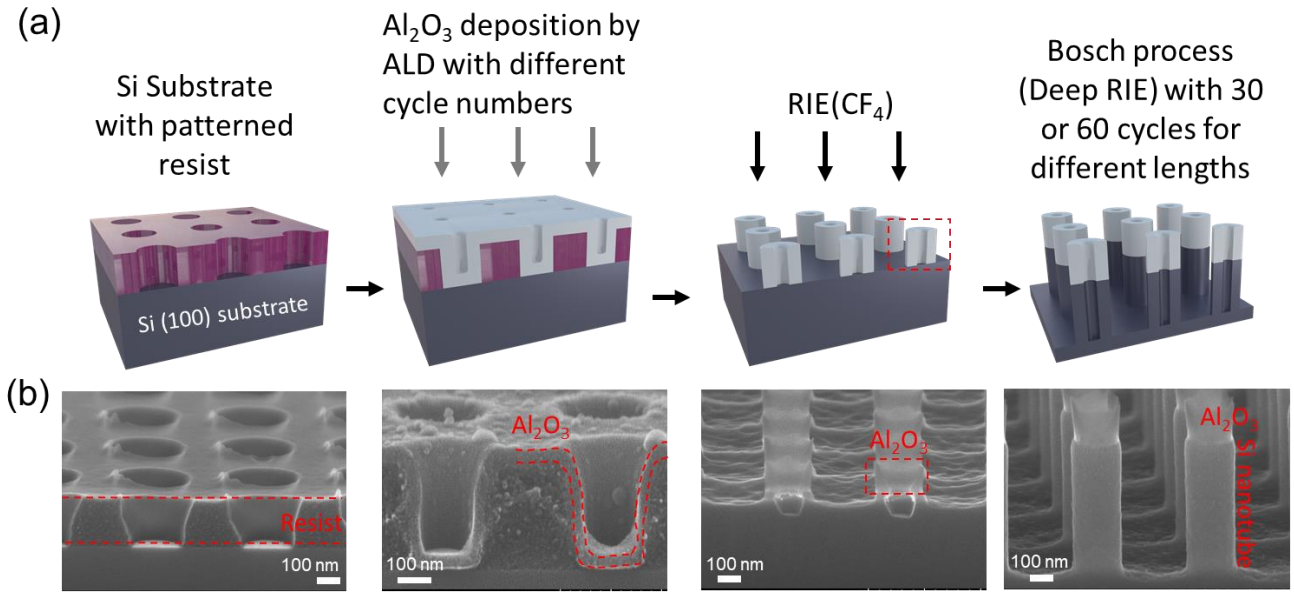

Figure 6.1. (a) Schematic illustration of the procedure for fabricating Si NT arrays using nanoimprint lithography (NIL) with spacer patterning. (b) Corresponding 75˚-tilted SEM images for each process step.

The inner diameter of the Si NT array can be adjusted by varying the thickness of the deposited Al_2O_3 layer. Figure 6.2 shows a schematic illustration of the fabrication of Si NT arrays with different inner diameters. Here, the outer diameter of the NTs should be the same as the diameter of the photoresist nanohole, and the inner diameter can be adjusted by the thickness of the deposited Al_2O_3 layer.

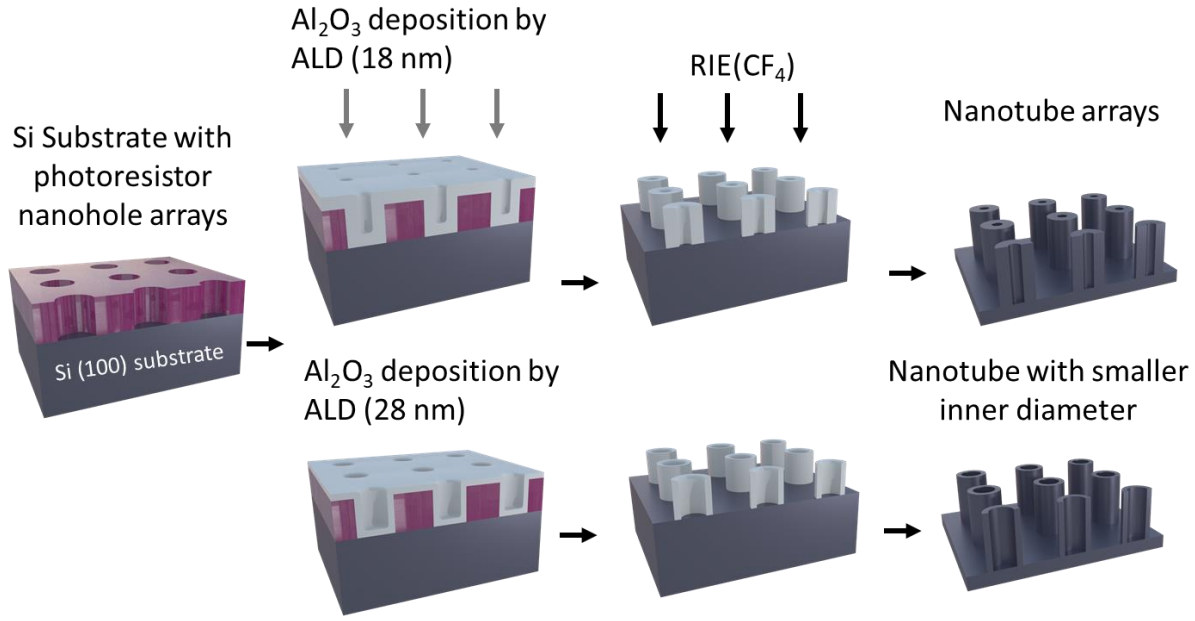

Figure 6.2. Schematic illustration of a procedure for fabricating Si NT arrays with different inner diameters by varying the Al_2O_3 thickness.

6.1.1 Tuning the outer diameter (the 2nd approach)

In order to adjust the outer diameter of the Si NT array, another approach is developed as shown in Figure 6.3. This process can be divided into two parts: the fabrication of Si nano-cylinder arrays and the fabrication of NT arrays.

The nano-cylinder arrays: first, the photoresist nanohole arrays on n-Si(100) wafers were fabricated by NIL introduced earlier. Then, an MgO layer was deposited onto the resist using an electron beam evaporator. The resist was then removed by NMP, acetone, and IPA. Next, SF_6 plasma followed by C_4F_8 plasma (Bosch etching process) was applied for deep etching of Si nano-cylinder structure using a Si deep etcher. The number of Bosch cycles was set to 12 in order to adjust the etching depth to be about 200 nm. Finally, the MgO mask was removed by H_3PO_4 solution, followed by a plasma ashing. The detailed fabrication process is described in Section 4.1, Fabrication of nanowire arrays.

The nanotube arrays: first, an Al_2O_3 layer is uniformly deposited over the nano-cylinder arrays by ALD. Then, the ring-like array pattern was achieved using ICP-RIE with CF_4 and Ar gases. Next, SF_6 plasma followed by C_4F_8 plasma (Bosch etching process) was applied for deep etching

of Si NT structure using a Si deep etcher. The number of Bosch cycles was set to 30 and 60 for adjusting the length of NW arrays. After a plasma ashing, the Al_2O_3 mask was removed by immersion in HF (1%) for at least 20 min at room temperature. The detailed fabrication process is described earlier.

Here, the inner diameter of the NTs should be the same as the diameter of the nano-cylinder, and the outer diameter can be adjusted by the thickness of the deposited Al_2O_3 layer.

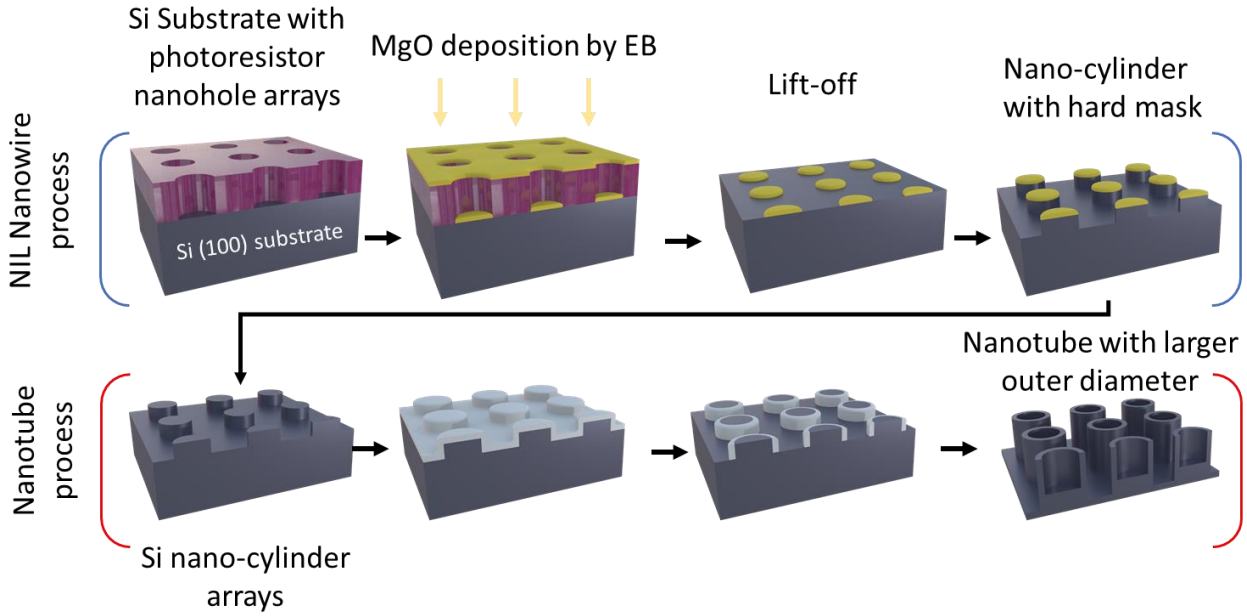

Figure 6.3. Schematic illustration of a procedure for fabricating Si NT arrays with a larger outer diameter using a process starting from Si nano-cylinder arrays.

6.2 Morphology characterization

The morphology of the fabricated Si NT arrays was characterized by a Hitachi SU8000 SEM with an acceleration voltage of 10 kV. Figure 6.4 shows the SEM images of eight different Si NT arrays with two different inner diameters, outer diameters, and lengths. The fabricated NTs present a smooth surface, a non-tapered shape, and a wall thickness of about 10 to 40 nm. The fracture at the top of the NT in Figure 6.4d,f is probably due to the fact that the wall is too thin to withstand the capillary force during drying. The geometry and shape of fabricated Si NT arrays such as height, diameter, and circularity are analyzed using ImageJ (https://imagej.nih.gov/ij/) with cross-sectional and top-view SEM images, and the NT dimensions for each sample are listed in Table 6.1. The height of NT is about 500 nm for 30 Bosch cycles and about 1000 nm for 60 cycles. There was little deformation or fracture of the NTs, indicating that longer lengths can be achieved by increasing the Bosch cycle. The variations of the NT dimensions will be discussed in detail below.

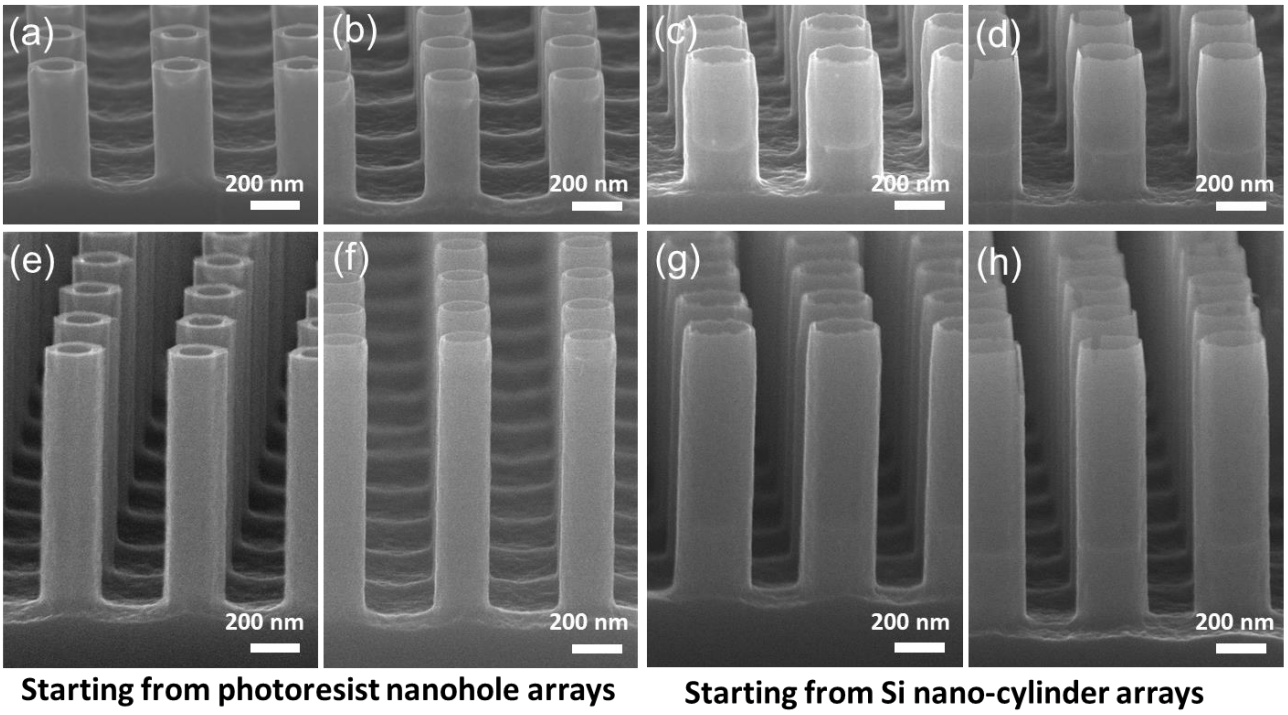

Figure 6.4. 75°-tilted SEM images of Si NT arrays with Bosch process cycle number of (a–d) 30 and (e–h) 60. Si NT arrays fabricated with Al_2O_3 thickness of (a,e,c,g) 28 nm and (b,f,d,h) 18 nm. Si NT arrays fabricated using the process starting from (a,b,e,f) photoresist nanohole arrays and (c,d,g,h) Si nano-cylinder arrays.

Table 6.1. Nanotube dimensions.

Sample	Figure 6.4a	Figure 6.4b	Figure 6.4c	Figure 6.4d
Inner diameter (nm)	131.2 ± 1.1	173.0 ± 0.6	231.8 ± 0.5	243.3 ± 0.8
Outer diameter (nm)	217.1 ± 0.7	229.9 ± 1.7	276.4 ± 0.6	265.4 ± 0.1
Wall thickness (nm)	43.0 ± 0.5	28.4 ± 0.6	22.3 ± 0.2	11.0 ± 0.3
Inner circularity	0.895 ± 0.003	0.882 ± 0.006	0.900 ± 0.005	0.875 ± 0.004
Outer circularity	0.806 ± 0.011	0.885 ± 0.008	0.724 ± 0.011	0.892 ± 0.021
Inner roundness	0.962 ± 0.010	0.943 ± 0.016	0.971 ± 0.015	0.967 ± 0.033
Outer roundness	0.971 ± 0.010	0.915 ± 0.013	0.977 ± 0.006	0.988 ± 0.016
Inner height (nm)	380.5 ± 6.0	460.0 ± 3.5	376.2 ± 1.0	403.3 ± 3.5
Outer height	500.0 ± 4.8	528.0 ± 1.2	540.9 ± 4.3	587.1 ± 2.4

6.2.1 Cross-sectional view

Figure 6.5a–d show the cross-sectional SEM images of the NTs, and it can be observed that the inner and outer heights are different. The NTs fabricated by the approach starting from Si nano-cylinder arrays have a larger ratio of inner to outer height ratio compared to the 1st approach, which is originated from the height of nano-cylinder. It can be seen that there are two regions in the height direction of the NTs in terms of wall thickness and shape (Figure 6.5f–i). These two regions can be assigned to the RIE and Bosch etching processes. Assuming that the Bosch etching depth is the same for all the NTs, the RIE depth is obtained by subtracting the Bosch etching depth from the total depth. The obtained RIE regions correspond well to the wall thickness and shape of each type of NT.

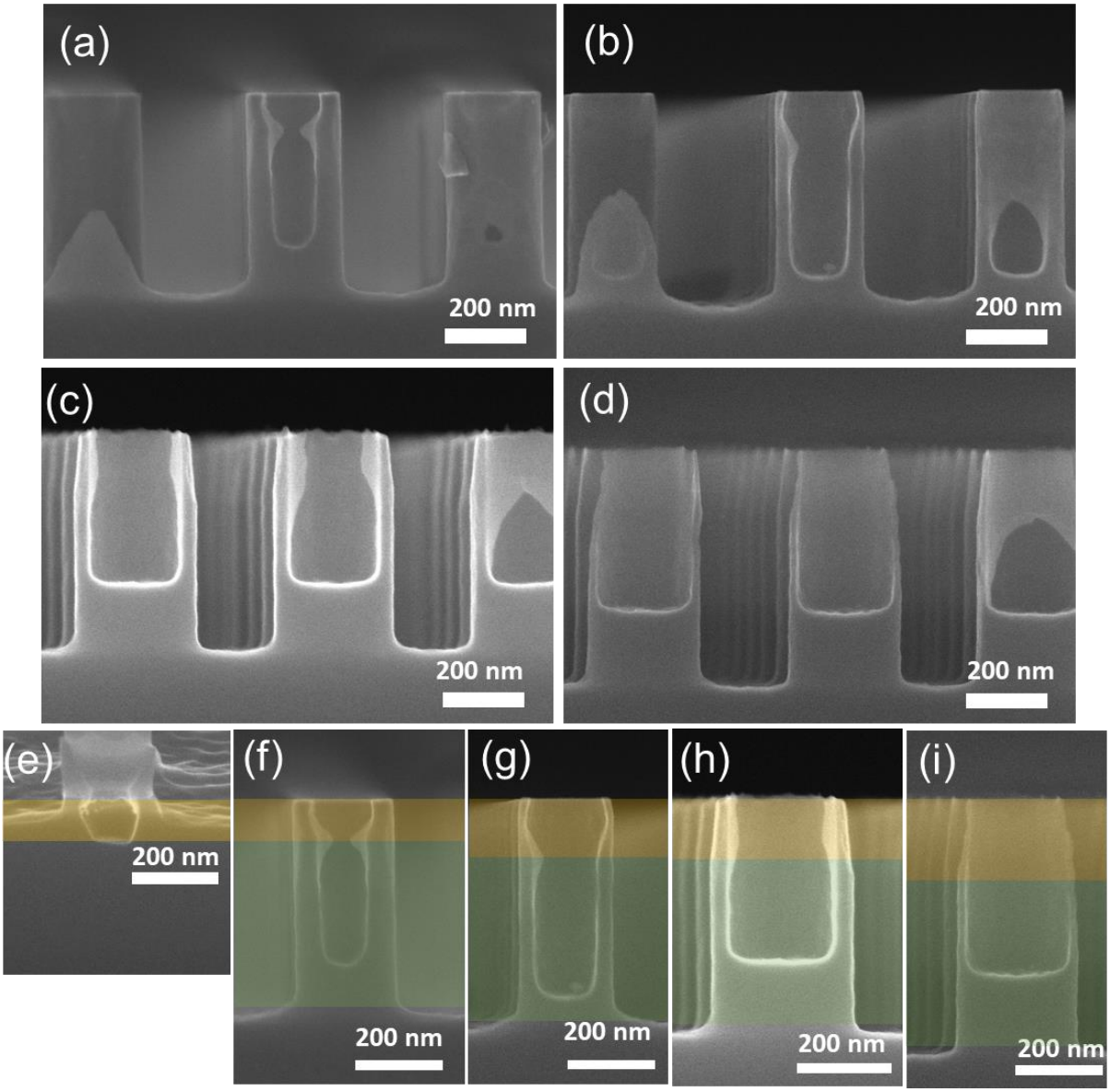

Figure 6.5. Cross-sectional SEM images of Si NT arrays with Bosch process cycle number of 30, Al_2O_3 thickness of (a,c) 28 nm and (b,d) 18 nm, and using the process starting from (a,b) photoresist nanohole arrays and (c,d) Si nano-cylinder arrays. (e) Cross-sectional SEM image of Si NT arrays before Bosch etching process. (f–i) Typical Si NWs of (a–d) overlapped with RIE, and Bosch etching regions, which are represented by yellow, and green colors, respectively.

The difference in RIE-depth between the two approaches can be attributed to the fact that the 1st approach has a photoresist on the substrate, which requires extra time to etch the resist, thus shortening the depth of the RIE region. The difference in RIE-depth between different Al_2O_3 thicknesses can be explained in Figure 6.6. The thicker the Al_2O_3 layer is, the longer it takes to etch, and the deeper the RIE region of NT becomes. The RIE region in the NTs can be reduced or eliminated by optimizing the RIE process conditions such as etching time and power.

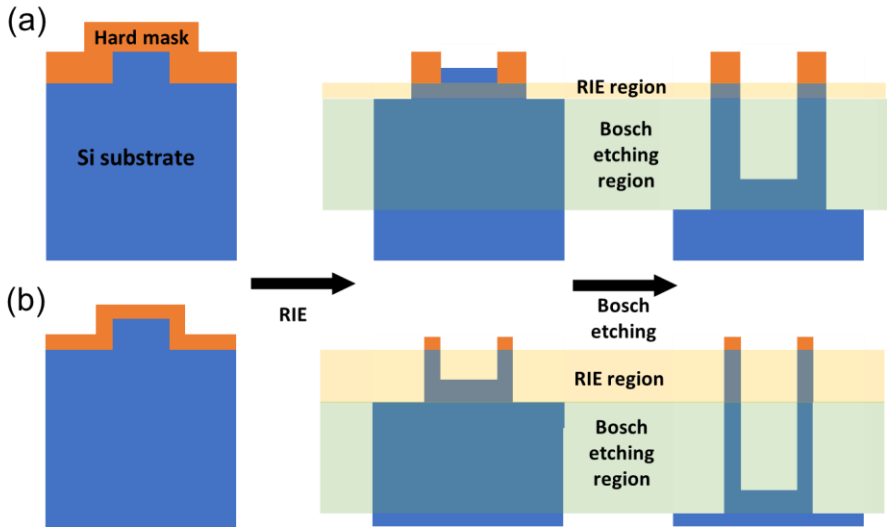

Figure 6.6. Schematic illustration of effect of RIE and Bosch etching process on substrates with different mask thicknesses (approach starting from nano-cylinder arrays).

6.2.2 Shape and wall thickness

ImageJ was used to analyze the top-view SEM images (Figure 6.7) and evaluate the geometry and shape of the NTs. The shape of the NTs viewed from the top surface was evaluated in terms of circularity and roundness, which can be expressed as

$$Circularity = 4\pi \times \frac{[Area]}{[Perimeter]^2} \qquad 6.1$$

$$Roundness = 4 \times \frac{[Area]}{\pi \times [Major\ axis]^2} \qquad 6.2$$

Since the circularity varies with the perimeter of the circle, it can be used to evaluate surface irregularities. In comparison, roundness varies with the major axis of the circle, and can be used to evaluate the aspect ratio or skewness of the circle. The value is equal to one for a perfect circle and decreases with an increase in deformation. The circularity and roundness of the inner and outer ring are evaluated are plotted against the Al_2O_3 thickness in Figure 6.8a,b. Here, we compared the NTs and the Si NW arrays fabricated by NIL. The circularity of the inner ring of the NTs was found to be comparable with the NW for all types, but the circularity of the outer ring using the thick mask was lower than that of the NW. As for the roundness of the NT, it is

almost the same as that of NW within the range of error. These results indicate that the fabricated NTs have a similar aspect ratio to NWs, but the surface irregularity of the outer ring is larger. This surface irregularity can be smoothed by a process involving thermal oxidation and chemical etching [50]. Figure 6.8c shows the wall thickness of NTs derived from the inner and outer ring diameters. The wall thickness increases with increasing of deposited Al_2O_3 thickness, and the increased value corresponds well with the difference of Al_2O_3 thickness. The NWs fabricated by the 1st approach have thicker walls than those fabricated by the 2nd approach. This is probably due to the tapered shape of the photoresist, which causes the mask to tilt (Figure 6.1b).

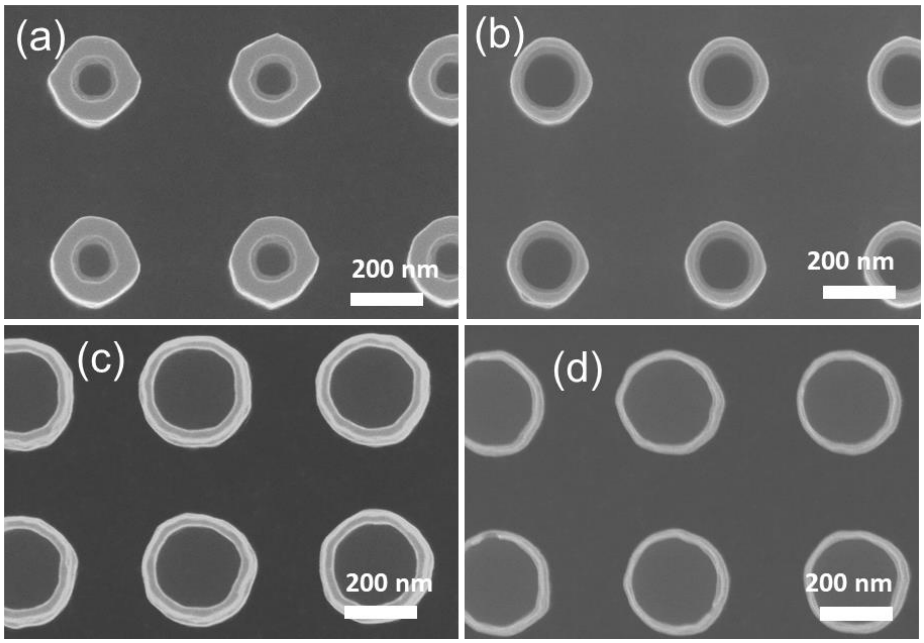

Figure 6.7. Top-view SEM images of Si NT arrays with Bosch process cycle number of 30, Al_2O_3 thickness of (a,c) 28 nm and (b,d) 18 nm, and using the process starting from (a,b) photoresist nanohole arrays and (c,d) Si nano-cylinder arrays.

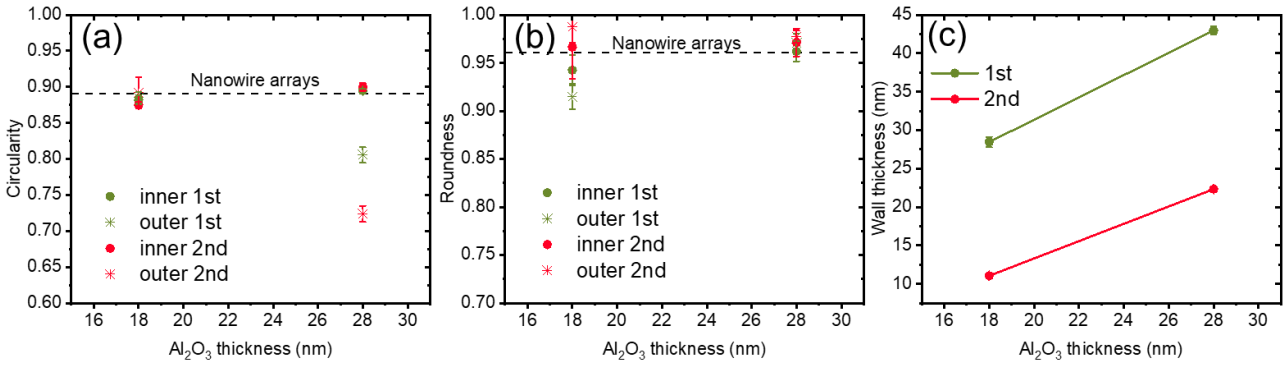

Figure 6.8. (a) Circularity, (b) roundness, and (c) wall thickness estimated from SEM images of Si NT arrays as a function of Al_2O_3 thickness. Here the 1st and 2nd indicate the Si NT arrays using the process starting from photoresist nanohole arrays, and Si nano-cylinder arrays, respectively.

6.3 Evaluation of surface defects by electron spin resonance

Reactive ion etching (RIE) (including Bosch etching) during the semiconductor fabrication can cause surface damage, and induces dangling bond-type defects which may degrade electrical performance. The electron spin resonance (ESR) technique has been used to detect and evaluate the defects in dangling bond-type defects in Si. Dangling bond-type defects in Si are related to a g-value of 2.005 in ESR signal. There are two possible components for this ESR signal: the first is surface defects induced by the RIE process; the second is the P_b centers [148] caused by interfacial defects at the Si/SiO_2 interface. The latter contribution has been reported to be negligible [95]. Here, we use ESR to detect and evaluate the dangling bond-type defects in Si NT arrays and study the dependence of defect density on the geometry of Si NTs.

ESR measurements were performed to detect the defect signals at 4.2 K with magnetic field modulation of 100 kHz and micropower of 1 mW. Figure 6.9b shows the ESR spectra of the NTs with respect to the g value. We can see that there are two components in the ESR signal, one located at g = 2.005 and the other located around g = 2.002. The first one corresponds to surface defects induced by the RIE process, while the second could be attributed to the residual Al_2O_3 mask. In order to separate these two components, the spectra were fitted with derivatives of the Voigt function (Figure 6.10a). The area of the integral of the fitted curve (located at g = 2.005) was used to represent ESR signal intensity, which can be used to evaluate the defects of the sample (Figure 6.10b). After normalized by the surface area of the nanostructures, the results are shown in Figure 6.10c. NT arrays present an overall lower defect density compared with NW arrays. The NT with a thin wall and large diameter shows a relatively higher defect density, which may be due to the fracture of its extremely thin wall (Figure 6.4h). This surface-damaged layer by the RIE process can be removed a process involving thermal oxidation and chemical etching [95].

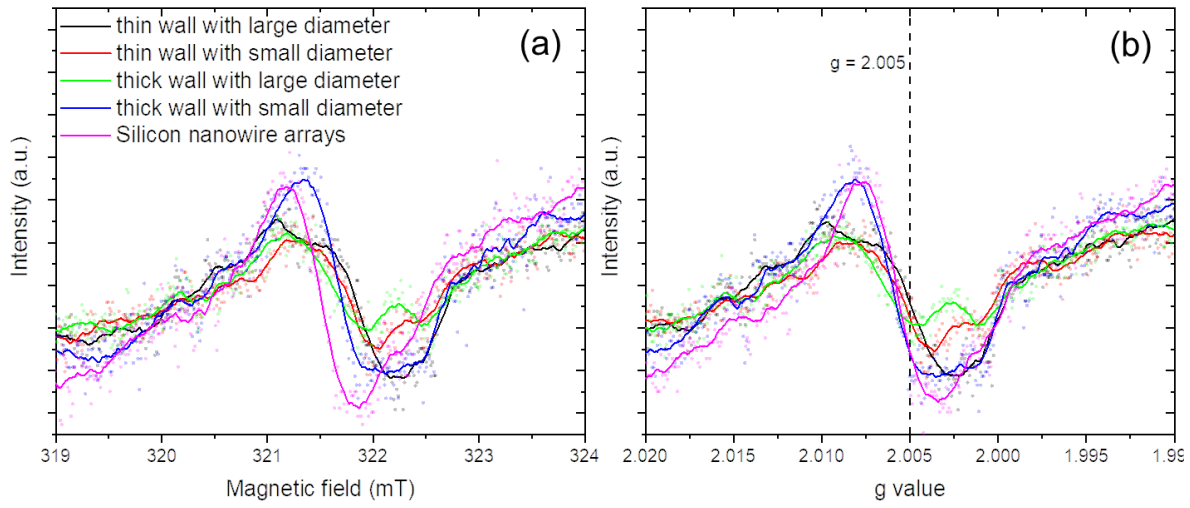

Figure 6.9. ESR spectra measured from the Si NT and NW arrays (number of Bosch process cycles: 60) with respect to (a) magnetic field and (b) g value. The dashed line indicates the g value of 2.005, which is attributed to dangling bond-type defects. Here thin wall, and thick wall present the Si NT arrays using Al_2O_3 thickness of 18 nm, and 28 nm, respectively. Large diameter, and small diameter present the Si NT arrays using process starting from Si nano-cylinder arrays, and photoresist nanohole arrays, respectively.

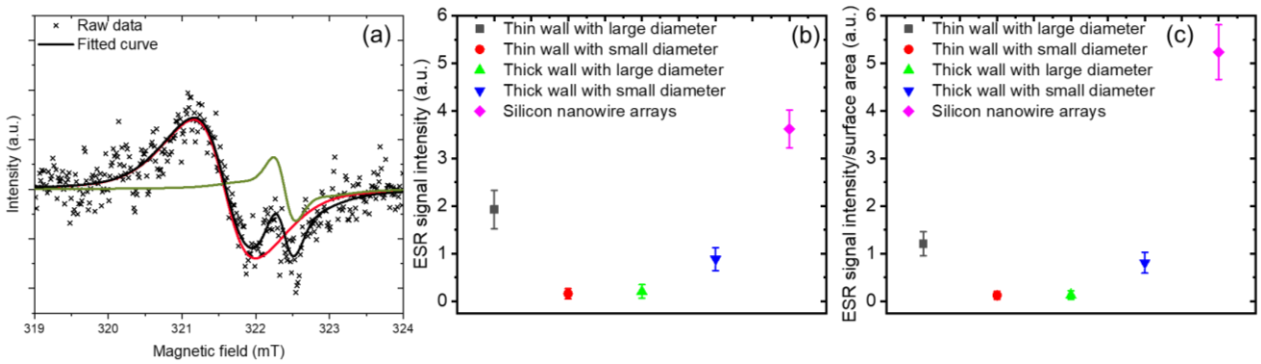

Figure 6.10. (a) ESR spectrum measured from the Si NT arrays (thick wall with large diameter) showing the splitting of signal into two components. The red curve presents the component corresponding to the dangling bond-type defects (g = 2.005). The green component could be attributed to the Al_2O_3 residual. (b) ESR signal intensity calculated from the component of dangling bond-type defects. (c) ESR signal intensity in (b) is divided by the estimated surface area of the nanostructure. The error bar indicates the standard deviation of fitting of the spectrum.

6.4 Reflectance of Si nanotube arrays

Si with subwavelength dimensions has attracted much attention as an antireflective material for improving the light trapping effect of optoelectronic devices. It has been found that NT arrays have lower reflectivity than NW arrays, which improves the efficiency of solar cells [11]. However, the NTs they fabricated have very rough surfaces, and the dependence of reflectance on wall thickness, length, and diameter has not yet been studied. Here, the reflectance of Si NT arrays was measured using UV-vis-NIR spectrophotometers (Jasco V-670), and the spectra are shown in Figure 6.11. Si NT arrays show a reduced reflection compared to Si NW arrays, demonstrating the enhanced light absorption effect of NTs (in Figure 6.11a). Si NT arrays with a larger diameter or a longer length seem to have an overall reduction in reflectance for 300–900 nm. This improvement in antireflective is attributed to the cooperation of various mechanisms, including the refractive index gradient between air and substrate, and coupling with waveguided or localized photonic modes [149], [150].

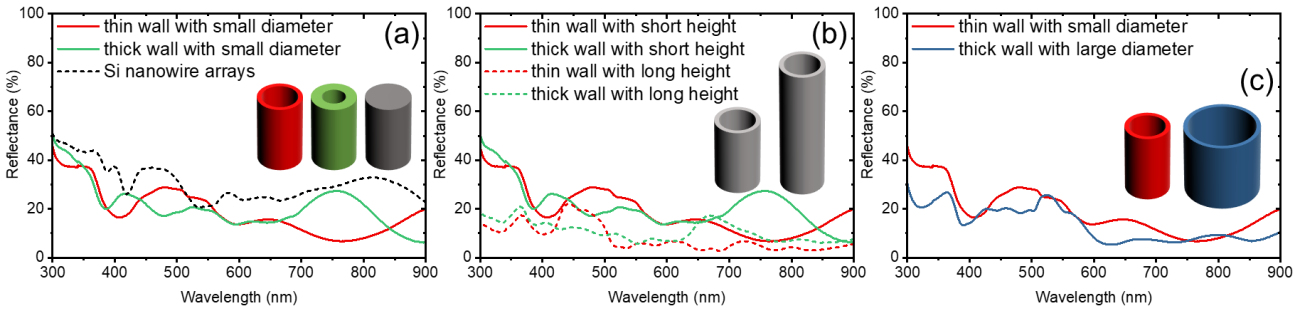

Figure 6.11. Reflectance spectra of Si NT arrays with different (a) wall thicknesses, (b) heights, and (c) diameters. Note that the thin wall with small diameter and thick wall with large diameter have similar wall thickness (approximately equal to 25 nm), thus it is appropriate to compare them in (c). The insets show the illustrations of SiNTs and SiNWs.

6.5 Summary

Si NT arrays with smooth surfaces were successfully fabricated using NIL with spacer patterning. Different lengths (from 500 nm to 1000 nm), and wall thicknesses (from 40 nm to 10 nm) of NTs can be achieved by varying the Bosch process cycles, and Al_2O_3 thickness, respectively. Two different approaches are developed to fabricate Si NT arrays with different inner and outer diameters. The geometry and wall thickness variations along the length of NT are due to the different depths of the RIE region. The top-view ring shape of fabricated NTs has a similar aspect ratio to NWs, but the surface irregularity of the outer ring is larger.

NT arrays present an overall lower defect density compared with NW arrays, and the NT with a thin wall shows a relatively higher defect density.

UV-vis-NIR reflectance results show that Si NT arrays have lower reflectance than Si NW arrays, and the Si NTs with a longer length and larger diameter have a lower reflectance.

Chapter 7

Conclusions

We successfully fabricated the $Ge_{1-x}Sn_x$ NWs with high Sn contents (~5 at.%) using Au–Sn catalysts. The Sn incorporation, crystallinity, and growth direction were understood and controlled. The boron doping of $Ge_{1-x}Sn_x$ NWs was demonstrated.

The growth of $Ge_{1-x}Sn_x$ NWs is closely dependent on the Sn content in the Au–Sn catalyst, and the use of Au–Sn alloy catalysts facilitates the understanding of the growth of $Ge_{1-x}Sn_x$ NWs. The high Sn% catalyst promotes the incorporation of Sn and improves the crystallinity of NWs. The Au–Sn alloy catalyst with high Sn contents also induced twinning defects in the NWs grown. The high Sn% in the catalyst results in very low C_e and high supersaturation ultimately promotes the formation of twins. Growth direction preference was explained by the calculation of surface energy of NWs. NWs grown by high Sn catalysts grow in the ⟨110⟩ direction, whereas NWs grown by low Sn catalysts grow in the ⟨111⟩ direction. Boron-doped $Ge_{1-x}Sn_x$ NWs were successfully grown at 360°C by CVD. Raman scattering analysis showed that the NWs were doped with boron atoms and electrically activated, and the addition of boron does not affect the Sn incorporation in NWs.

Ge NW arrays and Ge/p-Si core–shell NW arrays were fabricated successfully by NIL, and the hole gas accumulation in Ge region is demonstrated.

The lengths of Ge NW arrays can be varied from 500 nm to 2140 nm by adjusting the Bosch process cycles. Different diameters (from 220 nm to 30 nm) can be achieved by chemical etching at room temperature using H_2O_2 solution. A p-Si shell layer was formed on Ge NWs using CVD method. The accumulation of hole gas in the Ge region was demonstrated by Raman scattering analysis, and the hole gas concentration increases with decreasing the core size.

We have developed a simple and low-cost method for fabricating vertically oriented SiNTs and GeNTs by wet etching the ZnO of ZnO/Si(Ge) core–shell NWs. The growth, morphology, crystallinity, and stress were investigated.

The growth rate of the Si shell can be controlled by adjusting the flux of the precursor gas and the growth temperature. The ZnO/Si core–shell NWs were crystallized by thermal annealing and crystallinity can be controlled. The fabricated SiNTs were found to be amorphous and have hexagonal hollow spaces. In the case of GeNT fabrication, the higher the growth temperature, the faster the growth rate and the larger the gain size of the Ge shell, but the rougher the surface. Tensile and compressive stresses were observed in the ZnO core and Ge shell, respectively, which increased with the thickness of the shell. The stress in the shell is released after ZnO core removal.

Si NT arrays with smooth surfaces were successfully fabricated using NIL with spacer patterning. surface defect density and reflectance of NT arrays were studied.

By varying the Bosch process cycle and the thickness of Al_2O_3, NTs of different lengths (500 nm to 1000 nm) and thicknesses (40 nm to 10 nm) can be achieved. Different inner and outer diameters can be achieved by utilizing different approaches. Different depths of the RIE region result in the different cross-sectional geometry of NTs. The fabricated NTs have a similar shape from the top-view compared to NWs in terms of aspect ratio, but a rougher out ring. The defect density in NT arrays is lower than NW arrays. The defect density in thin-walled NTs is relatively higher than other NTs. Si NT arrays have a lower reflectance than the Si NW arrays, and the longer the length and the larger the diameter, the lower the reflectance of Si NTs.

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