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Topical Review

Metal-induced layer exchange of group IV materials

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Abstract

Layer exchange (LE) is an interesting phenomenon in which metal and semiconductor layers exchange during heat treatment. A great deal of effort has been put into research on the mechanism and applications of LE, which has allowed various group IV materials (Si, SiGe, Ge, GeSn and C) to form on arbitrary substrates using appropriate metal catalysts. Depending on the LE material combination and growth conditions, the resulting semiconductor layer exhibits various features: low-temperature crystallization (80 °C–500 °C), grain size control (nm to mm orders), crystal orientation control to (100) or (111) and high impurity doping (>10^{20} cm^{-3}). These features are useful for improving the performance, productivity and versatility of various devices, such as solar cells, transistors, thermoelectric generators and rechargeable batteries. We briefly review the findings and achievements from over 20 years of LE studies, including recent progress on device applications.

Keywords: layer exchange, semiconductor, graphene, low temperature synthesis, flexible devices

(Some figures may appear in colour only in the online journal)

1. Introduction

Group IV materials have been studied and used since the emergence of electronics. In addition to Si, the most common electronic material, there are many other group IV materials with excellent characteristics. Ge has been used in photodetectors and multi-junction solar cells because of its unique optical characteristics [1]. Ge's high carrier mobilities are potentially attractive for high-speed transistors [2], which are gaining attention again with recent advances in device technology [3–5]. SiGe alloy has long been used as a thermoelectric material because of its large Seebeck coefficient and low thermal conductivity [6]. Additionally, tuning the SiGe composition enables us to control physical properties such as bandgap and lattice constant [7]. GeSn alloy has attracted intense interest because it provides direct transition in the near infrared region and theoretically exhibits high carrier mobilities exceeding Ge [8, 9]. Graphitic carbon (C) is used in various devices because of its excellent electrical and thermal conductivities, mechanical strength and electrochemical stability. In addition to the individual attractive features, group IV materials are also environmentally friendly and compatible with widely used Si processes.

From the above features, the thin film formation of group IV materials on insulators such as SiO_2, glass and plastics has been conducted to improve device performance, increase functionality, reduce production cost and expand applications [10, 11]. However, obtaining high-quality crystals on insulating substrates is quite challenging because most of the insulators are amorphous and not resistant to high temperature. Therefore, techniques for synthesizing high quality thin films at low temperatures have been widely studied. Metal-induced crystallization (MIC) lowers the crystallization temperature of amorphous semiconductor thin films and has been well studied for Si [12–14], Ge [15–17] and SiGe [18]. The layer exchange

(LE) phenomenon in MIC was first reported in 1998 by Nast *et al* in the Si-Al system [19]. Since this finding, LE has attracted many researchers interested in the phenomenon itself, the various features changing dramatically with a little conditional modulation and the tremendous potential for device applications. Enormous effort has been devoted to studying the LE mechanism, high-quality crystallization at low temperatures and applications to various materials and devices. In this review, we will briefly summarize the past 20 years of these LE studies.

2. Metal-induced layer exchange

2.1. Mechanism

The LE mechanism has been well studied both experimentally and theoretically using the Si-Al system [20–27]. According to those reports, the LE process can be summarized as shown in figure 1. First, a metal layer and an amorphous semiconductor (including C here) layer, generally ranging from 5 to 500 nm thickness, are sequentially deposited on an arbitrary substrate and heat-treated at a temperature lower than the eutectic point (figure 1(a)). The LE process itself is cost effective because various thin-film-preparation methods can be used, such as sputtering, thermal evaporation and chemical vapor deposition (CVD). Inert gases such as N_2 or Ar are generally used as the heat treatment atmosphere but H_2 [28] or vacuum [29] are also useful. LE occurs even if the order of the layers is inverted [30, 31], which enables formation of the lower electrode in a self-organizing manner [32, 33]. During annealing, semiconductor atoms diffuse from the amorphous layer into the metal layer, mainly through the metal grain boundaries (figure 1(a)). When the semiconductor concentration in metal is supersaturated, the semiconductor nucleates in metal (figure 1(b)). The position and shape of the nucleus will be discussed later. After that, semiconductor atoms dissolving in metal contact the nuclei, which induces semiconductor crystals' lateral growth (figure 1(c)). The lateral growth stresses metal and pushes it to the upper layer (figure 1(c)) in a process called push-up phenomenon. Eventually, crystalline semiconductor forms a bottom layer while metal forms an upper layer (figure 1(d)). Thermodynamically, the driving force of the LE process is the difference in Gibbs free energy between amorphous and crystalline semiconductor [22, 25]. The metastability and high free energy of the amorphous layer cause supersaturation, which leads to nucleation in the metal layer [23, 26]. Therefore, to induce LE, the initial semiconductor layer must be amorphous or at least poorly crystalline [34]. Once LE is completed, LE does not occur again because the resulting semiconductor layer is completely crystalline. When the substrate is crystalline and lattice-matched to the semiconductor layer, epitaxial growth can be induced by tuning the growth conditions [35–37].

LE can be observed in the following ways. By removing the metal after the LE, a crystalline semiconductor film is obtained on the substrate. Generally, the metal layer is removed using wet etching, where the etchant selection is important so as not to damage the semiconductor film. The color of the sample surface (and the back surface when the substrate is transparent) changes according the stage of LE (figure 2(a)) [38]. For most material combinations, LE can be confirmed by the naked eye. The detailed LE process can be observed with a microscope. *In situ* optical micrographs indicate that semiconductor nuclei form, grow laterally and cover the entire surface of the substrate (figure 2(b)) [27, 39, 40]. More specifically, the complete LE is determined using a transmission electron microscope (TEM; figure 2(c)) with an energy dispersive x-ray analysis [41]. Some studies directly observed the *in situ* microscopic cross-section [23, 42] and plane-view showing the push-up phenomenon [43] during LE. Cross-section images using focused-ion-beam microscopy and scanning electron microscopy (SEM) are also useful to observe the LE process [20]. Such confirmations of LE are essential because the success or failure of LE depends on various factors, as mentioned in this paper.

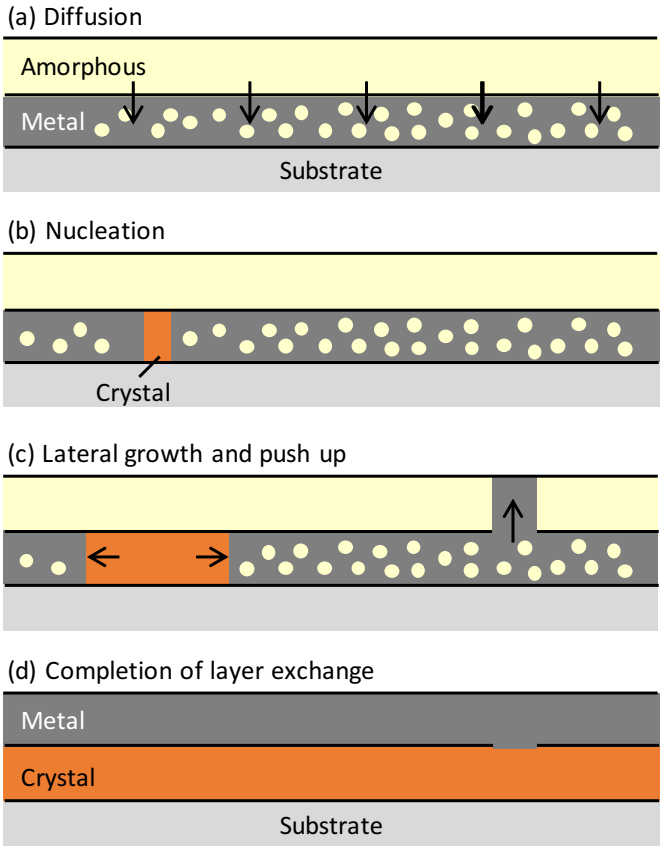

Figure 1. Schematic of the LE process. (a) Diffusion of semiconductor atoms from the amorphous layer into the metal layer. (b) Nucleation of semiconductor in metal. (c) Lateral growth of semiconductor crystals and metal push up. (d) Completion of LE.

2.2. Material combinations

According to the LE mechanism, the basic conditions necessary for LE are: (i) the semiconductor dissolves well in the metal, (ii) the semiconductor and metal do not form

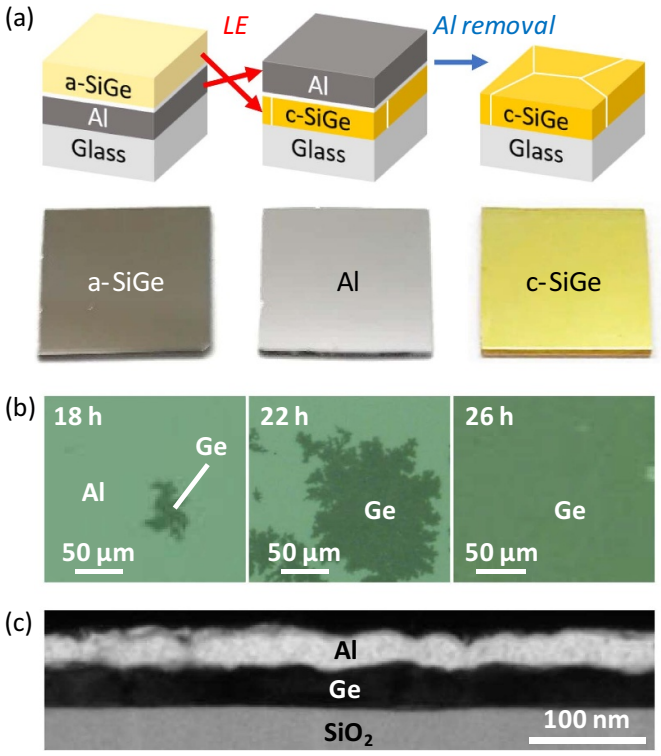

Figure 2. Observation of the LE process. (a) Schematic and photographs of the samples of Al-induced LE of $Si_{0.7}Ge_{0.3}$ corresponding to each stage [38]. (b) *In situ* optical microscopy observation of the Al-induced LE of Ge annealed at 350 °C, through which back surfaces are observed through the transparent SiO_2 substrate [40]. The annealing time is shown in each image. (c) Bright-field TEM cross-section of the sample after the LE between Al and Ge [41].

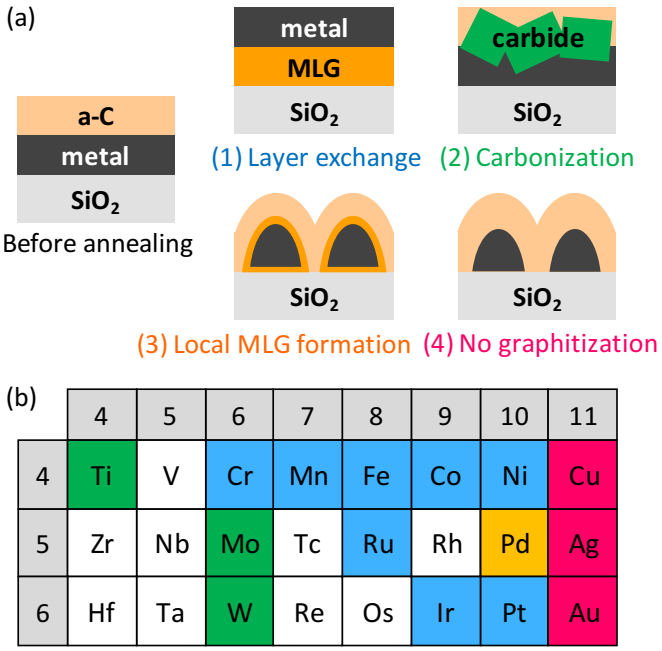

Figure 3. Classification of interactions between transition metals and amorphous C (a-C) [71]. (a) Schematic sample structure showing interactions between metals and a-C classified into four groups. (b) Organization on the periodic table. The elements are colored by the classification of interactions between transition metals and a-C: blue shows group (1) layer exchange, green shows group (2) carbonization, yellow shows group (3) local MLG formation and red shows group (4) no graphitization.

compounds and (iii) the semiconductor diffuses into the metal before the metal diffuses into the semiconductor. Both (i) and (ii) can be determined from the phase diagram [23, 26]. This will be the quickest guide to roughly finding the material combination of LE. Conversely, (iii) is difficult to judge quantitatively because few papers have shown the relationship between amorphous semiconductor and metal diffusion rates. However, the diffusion coefficients of crystalline semiconductors and metals are known in many cases and are helpful [44, 45]. For example, Sn and Ag diffuse into amorphous Ge quickly, which contributes to low-temperature crystallization but does not induce LE, which results in the metal-Ge mixed structure [46, 47]. However, even in such cases, it is possible to control the diffusion rate and achieve LE by inserting an appropriate interlayer between metal and semiconductor [47]. The quality of the metal and amorphous semiconductor layers, which varies with preparation method and conditions, also affects the possibility and various morphology of LE [48–51], which likely reflects the diffusion rate. Oxygen contamination should be avoided because too much oxygen in metals or semiconductors inhibits complete LE [52, 53].

So far, LE has been reported in the following material combinations: Si-Al [19], Si-Ag [54, 55], Si-Au [56, 57], Ge-Al [41, 58], Ge-Ag [47], Ge-Au [59] and Ge-Zn [60]. These metals are also useful for the LE of amorphous SiGe alloy [61–65], where the growth conditions should be optimized according to the SiGe composition [40, 66]. Crystalline semiconductor alloys such as SiGe and GeSn can be also formed by inducing the reaction between each single element [67–69]. Sb also induces LE with Si and Ge, but has a problem in thin film stability. For C, we found that Ni, Co, Fe, Cr, Mn, Ru, Ir and Pt can induce LE and provide multilayer graphene (MLG) (figure 3) [70, 71]. Taking C as an example, it will be also important for LE that C has sufficient solid solubility in the metal and that the metal layer is not aggregated during annealing, in addition to not forming a compound. Fe is an exception: it induces LE while it potentially makes compounds with C [72]. This is presumably because diffusion, solid solution and nucleation occur before compound formation.

2.3. *Characteristics of layer-exchanged thin films*

2.3.1. Film shape. In LE, the initial bottom and top layers serve as 'molds' for the eventual top and bottom layers, respectively and thereby almost determine the film shapes. We define this phenomenon as LE, which differs from the precipitation methods often used for graphene synthesis. As can be inferred from the schematic image in figure 1, when the initial metal and semiconductor film thicknesses are the same, a uniform semiconductor layer is likely achieved after LE. However, in practice, 'holes' and 'islands' (also called hillocks)

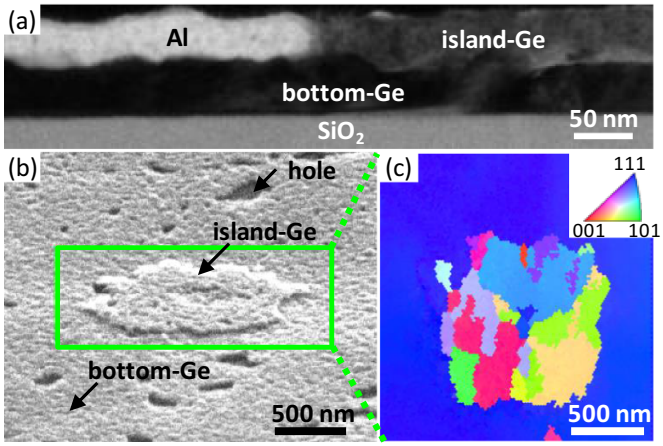

Figure 4. Properties of the island formed by the LE between Al and Ge (each 50 nm thick) at 350 °C. (a) Bright-field TEM cross-section image showing the island of the sample before Al removal [74]. (b) SEM and (c) IPF showing the island of the sample after Al removal [75]. The coloration indicates the crystal orientation (refer to the inset legend).

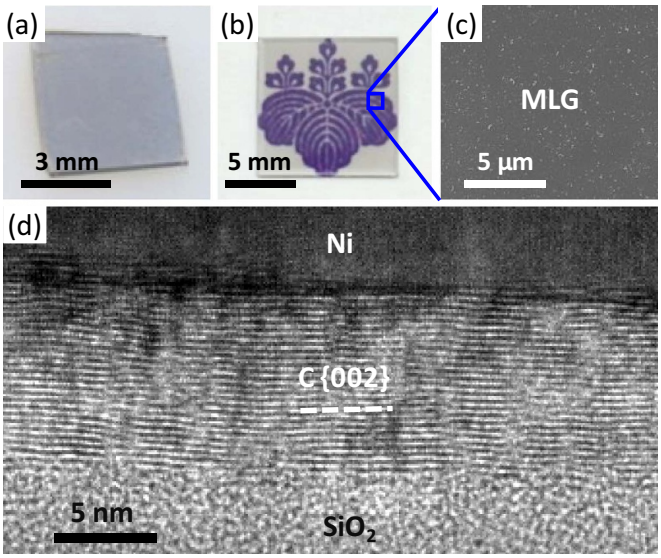

Figure 5. MLG thickness control on a SiO_2 glass substrate using the Ni-induced LE of amorphous C. (a) Photograph of a 50-nm-thick MLG formed at 600 °C [70]. (b) Photograph and (c) SEM image of a 5-nm-thick MLG formed at 800 °C [89]. (d) High-resolution TEM lattice image of a 10-nm-thick MLG formed at 800 °C [89].

form depending on the material combination and growth conditions [20, 21, 73]. Figure 4 shows an example of the Ge-Al system [74, 75]. After LE, the top layer comprises Al and Ge parts (figure 4(a)). The bottom layer is uniformly Ge in this region. However, in some parts, Al remains at the bottom to conserve the Al and Ge volumes, which become holes after Al etching. In fact, the Ge layer clearly has holes and islands after Al removal (figure 4(b)). The Ge island comprises randomly oriented small grains, while the bottom Ge layer is completely (111) oriented (figure 4(c)).

The thickness ratio between the metal and semiconductor layers greatly affects the appearance of the holes and islands [74, 76–78]. When the initial semiconductor layer is thinner than the metal layer, the island area decreases while the hole area increases, which results in poor semiconductor layer coverage on the substrate. Conversely, when the initial semiconductor layer is thicker than the metal layer, the hole area decreases while the island area increases, which results in the poor semiconductor surface crystallinity. Thus, the island and hole are in a trade-off relationship. This aspect also depends on the type and even the thickness of the substrate [79, 80]. This is because the stress applied to the metal and semiconductor layers during LE considerably affect growth morphology [81–84]. The islands can be removed by peeling off with tape [85] or using dry [86] and wet etching techniques [74, 87]. The best way to obtain high-quality semiconductor films with high surface coverage is to remove the islands in the island-rich samples [75]. For applications requiring a rough surface instead of a uniform film, nanostructures can be obtained in a self-organizing manner by stopping the LE growth halfway [88].

In the field of graphene synthesis, LE is a unique method that can uniformly control graphene film thickness over a wide range [89], which is difficult using conventional precipitation methods [90]. Ni-induced LE can selectively produce MLG in a thick layer (figure 5(a)) and a transparent thin layer (figures 5(b) and (c)). The MLG is oriented to the substrate (figure 5(d)), which leads to a high electrical conductivity in the in-plane direction [89]. Therefore, the film thickness can be controlled according to the application, such as transparent electrodes, wiring and anodes for batteries.

2.3.2. Low temperature crystallization. Metal-induced LE lowers the crystallization temperature of amorphous semiconductors by several hundred degrees. This feature enables synthesis of crystalline semiconductor films on integrated circuits, glass and even flexible plastic substrates [91–93]. The effect of lowering the crystallization temperature, i.e. increasing the crystallization rate, strongly depends on the kind of metal catalyst (figure 6). Therefore, the annealing time required for completing LE depends on the material combination in addition to the annealing temperature and thereby has a wide range from minutes to hundreds of hours. Zn remarkably increases both the nucleation rate and lateral growth velocity in Ge and enables crystallization at 80 °C [60]. The lower eutectic point tends lower LE temperature, but does not limit this because the LE temperature is affected by various factors, as described below.

Lowering the crystallization temperature is because of the reduction of activation energies for nucleation and/or lateral growth (figure 6). This is likely caused by the following three effects: (i) the screening effect weakens the atomic bond of amorphous semiconductors [94], (ii) diffusion of semiconductor atoms in a metal and its grain boundaries is generally much faster than self-diffusion in an amorphous semiconductor [44, 45, 95] and (iii) semiconductor nucleation in a metal occurs with lower interfacial energies [96] compared

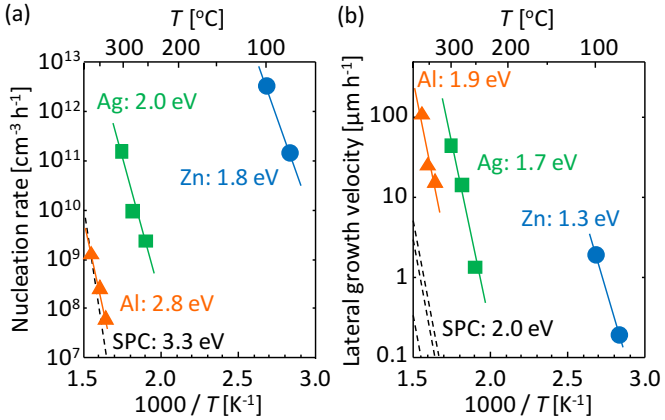

Figure 6. Comparison of the growth rates for LE of Ge using Al [40], Ag [47] and Zn [60]. Arrhenius plots of the (a) nucleation rate and (b) lateral growth velocity, determined by *in situ* optical microscopy observations. T is the growth temperature. Data from SPC are also shown [97, 98]. Values indicate the activation energies obtained from the Arrhenius equation and the slopes of the lines.

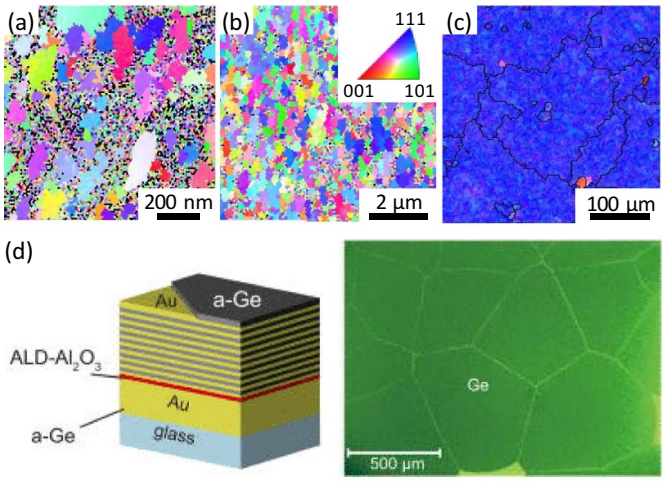

Figure 7. Grain size of the LE-Ge. IPFs for the Ge layers formed by LE using (a) Zn at 80 °C [60], (b) Ag at 250 °C [47] and (c) Al at 350 °C [74] where black solid lines indicate the random grain boundaries. The coloration indicates the crystal orientation (refer to the inset legend in (b)). (d) Au-induced LE using an amorphous-Ge/Au multilayer structure for promoting lateral growth of Ge grains: schematic before LE and the optical micrograph of the resulting Ge layer after LE [99]. Reprinted from [99], with the permission of AIP Publishing.

with solid-phase crystallization (SPC), in which the semiconductor nucleates in the amorphous layer [97, 98]. These effects depend on the metal species, which reflects the deference of the screening effect, diffusion rate and interfacial energies [14, 17, 96]. The crystallization temperature can be also lowered (that is, LE can be facilitated) by: (i) controlling the semiconductor/metal interlayer [58, 100, 101], (ii) tuning the grain size of the metal layer [102–104], (iii) modulating the substrate surface condition [105], (iv) initial semiconductor doping in the metal layer [27, 106, 107], (v) applying eternal voltage during annealing [108] and (vi) introducing defects [109] or impurities [110–112] into the amorphous semiconductor layer.

2.3.3. Grain size control. LE can control the grain size of the resulting semiconductor layer to a wide degree from nm to mm. In LE, the grain size greatly depends on the metal species. Electron backscattering diffraction analysis is a powerful method for assessing net grain size because a domain visible under optical micrographs is divided into a few to thousands of crystal grains. For Ge, Zn provides several tens of nm [60], Ag provides a few μm [47] and Al and Au provide more than 50 μm [59, 74] (figures 7(a)–(c)). A small grain size effectively lowers the thermal conductivity of the thermoelectric thin film [60, 113], while a large grain size effectively reduces grain boundary defects in solar cells [114] or transistors [115]. Common to all metal species, the guideline for increasing grain size is to suppress nucleation, as with SPC without metal catalysts [116, 117]. Lowering the growth temperature [118–123] or preparing an interlayer between semiconductor/metal are effective for this [124–129]. Thin film preparation also contributes to large grain growth because the thinner metal layer requires greater lattice diffusion of semiconductor atoms in addition to grain boundary diffusion, which delays nucleation [96]. The metal grain size, that is the grain boundary density, affects the grain size of the resulting semiconductor layer because it changes the diffusion rate of the semiconductor atoms into the metal [102–104]. Higashi *et al* improved the lateral diffusion rate and induced large grain growth in the Ge-Au system by preparing a thin multilayer structure of Ge and Au (figure 7(d)) [99]. The Ge grain size approached the mm range, which can be called pseudo-single crystals for many thin film devices. This multilayer technique is also useful for the LE in materials other than Ge [130]. In such a system capable of obtaining a large grain size, single crystals can be obtained at arbitrary positions by limiting the area of the initially prepared film [49, 131–133].

2.3.4. Crystal orientation control. Some material combinations in LE can synthesize crystal-orientation-controlled semiconductor films even on amorphous substrates. This is a unique feature of LE and likely originates from the high mobility of semiconductor atoms in metal bringing the growth process closer to equilibrium [134–136]. The crystal orientation is often evaluated by inverse pole figures (IPFs) derived from electron backscattering diffraction analysis. Especially in the Si-Al system, the crystal orientation of Si on amorphous substrates can be selectively controlled to (100) and (111) [137–139]. Therefore, both techniques and mechanisms for controlling the crystal orientation have been well studied in the Si-Al system [25, 100, 140]. The following four parameters influence the crystal orientation: (i) initial thickness of Al (figure 8(a)) [66, 139], (ii) annealing temperature (figure 8(a)) [139, 141], (iii) thickness and material of the interlayer between Si/Al (figure 8(b)) [129, 137, 142] and (iv) substrate (underlying) material and its surface condition (figure 8(c)) [143–147]. In particular, the Al thickness and underlying material have a large influence: thick Al (>100 nm) provides the (100) orientation [148, 149], while thin Al (<100 nm) provides the crystal orientation depending on the underlying material, such as (111) for SiO_2 and (100) for ZnO:Al

(figure 8(c)). With an Al thickness of approximately 100 nm, Si crystal orientation is sensitive to the annealing temperature and interlayer (figures 8(a) and (b)). When the substrate is SiO_2, high annealing temperatures and thin interlayers (fast Si diffusion) induce (100) orientation, while low annealing temperatures and thick interlayers (slow Si diffusion) induce (111) orientation (figures 8(a) and (b)). These behaviors are identical for inverted LE structures in the Si-Al system [139, 150]. This is helpful in considering the mechanism of the orientation control.

Crystal orientation has been well discussed in terms of minimizing the surface free energy of the Si nucleus [151]. In crystalline Si (and Ge), the 111 faces have the lowest surface energy and thus are preferentially formed [152]. The Si 111 face also likely appears on the interfaces with SiO_2 and Al [25, 100]. In the LE process, Si diffuses at the Al grain boundaries and nucleates when reaching a certain volume [24]. When the Al layer is thick or the Si diffusion is fast, triangular (pyramid-shaped) nuclei are heterogeneously formed in contact with the interlayer (figure 8(d)), which was confirmed experimentally [20, 42]. In this case, most of the surface area of the Si nucleus is in contact with Al. Because of the Si/Al interface becoming the 111 faces to minimize the total surface energy of Si nucleus, the Si/interlayer interface becomes the 100 face [25, 148]. Conversely, when the Al layer is thin or the Si diffusion is slow, the Si atoms reach the substrate [25, 125], likely forming a trapezoidal nucleus. In this case, the Si nucleus has an interface area in contact with the substrate and interlayer, which become the 111 faces for lowering the total surface energy of Si (figure 8(d)). Therefore, when the quality of the substrate (and interlayer) changes, the crystal orientation changes according to the interfacial energies. Although the value of each interfacial energy is needed for accurate discussion, this model is consistent with the various experimental results for the Si-Al system.

These four parameters of thickness, annealing temperature, interlayer and substrate likely influence the crystal orientation and grain size for any material combination in LE; however, the situation changes slightly depending on the combination. For the Al-induced LE of Ge, when the Ge layer is thin (<100 nm) and Ge diffusion is slow, the crystal orientation can be controlled to (111) or (100) depending on the underlying layer, as in the case of Si [59, 153, 154]. Conversely, when the Ge layer is thick (>100 nm) and Ge diffusion is fast, the crystal orientation is random [41, 155]. Although the reason remains unclear, the orientation anisotropy of the Ge/Al interfacial energy may be small. In a material with large surface energy anisotropy such as graphene, the resulting film after LE is almost completely oriented under any condition (figure 5(d)) [71, 89].

2.3.5. High impurity doping. MIC generally has a problem with metal contamination in resulting semiconductor layers. Although some techniques use the lateral growth region as a contamination free layer [156–158], these techniques have difficulty in large area formation. In LE, many metal atoms also remain in the islands; however, the metal content in the bottom semiconductor layer is almost limited by the solid solubility of metal in semiconductor [20, 40]. This is also a unique feature of LE. According to this principle, metals with small solid solubility (such as Ag and Au) are expected to provide a semiconductor layer with little metal contamination [54, 93]. Conversely, high impurity doping into a semiconductor layer is also possible by positively using this feature. In the Si-Al system, the resulting Si layer shows p-type conduction [20] because Al works as an acceptor. The higher growth temperature provides higher hole concentration, which likely reflects the increased solid solubility [159, 160]. In the SiGe-Al system, an amount (10^{18}–10^{20} cm^{-3}) of Al is doped in the resulting $Si_{1-x}Ge_x$ (x: 0–1) layer according to the solid solubility limit in each SiGe composition [40, 161] (figure 9(a)). These features enable low-temperature SiGe synthesis with high electrical conductivity (figure 9(b)), which is useful for thermoelectric generators (TEGs) [38, 60] and contact layers for optical devices [162, 163]. Adding an impurity to the initial semiconductor [163–165] or metal [166, 167] layers also can highly dope the impurity into the resulting semiconductor layer in a self-organizing manner during LE. This feature is also effective for forming a semiconductor alloy. In the Ge-Al system, Sn preparation in the initial LE structure results in the crystalline GeSn alloy, though the Sn concentration is equivalent to the solid solubility limit (∼2%) [69]. This behavior is considered to more likely occur as the LE is closer to the equilibrium state. Some papers reported that the hole concentration in the Si layer formed by Al-induced LE, where Al works as an acceptor, can be controlled, that is, not completely restricted with the solid solubility limit [168–170]. These behaviors possibly occur by bringing LE closer to a non-equilibrium state.

3. Device applications of layer exchange

3.1. Solar cells

Solar cells have long been studied as an application of LE because the Si-Al system can produce a large-grained Si layer [171]. The ability to lower the process temperature is also attractive because it allows the use of inexpensive substrates such as glass. The seed layer approach, that is, the epitaxial growth of Si on large-grained p-type Si formed by Al-induced LE, has been studied (figure 10(a)) [162, 172, 173]. In line with this, epitaxial thickening of Si on the seed layer has been performed in various techniques, such as ion-assisted deposition [174, 175], CVD [176–181] and solid-phase epitaxy [182–184]. However, the conversion efficiency remains low (8.5%) compared with other Si thin-film solar cell technologies (figure 10(b)) [171]. There remains a problem in improving the quality of the LE-Si seed layer after Al removal. Fabricating a bottom electrode under LE-Si is also an issue [185, 186]. The inverted LE structure is promising because it provides a self-organized Al bottom electrode and no islands and holes on the Si surface [187]. In addition to the seed layer, the LE-Si was demonstrated to be useful as a field-effect passivation layer [165] and a heterojunction-photodetector material [150].

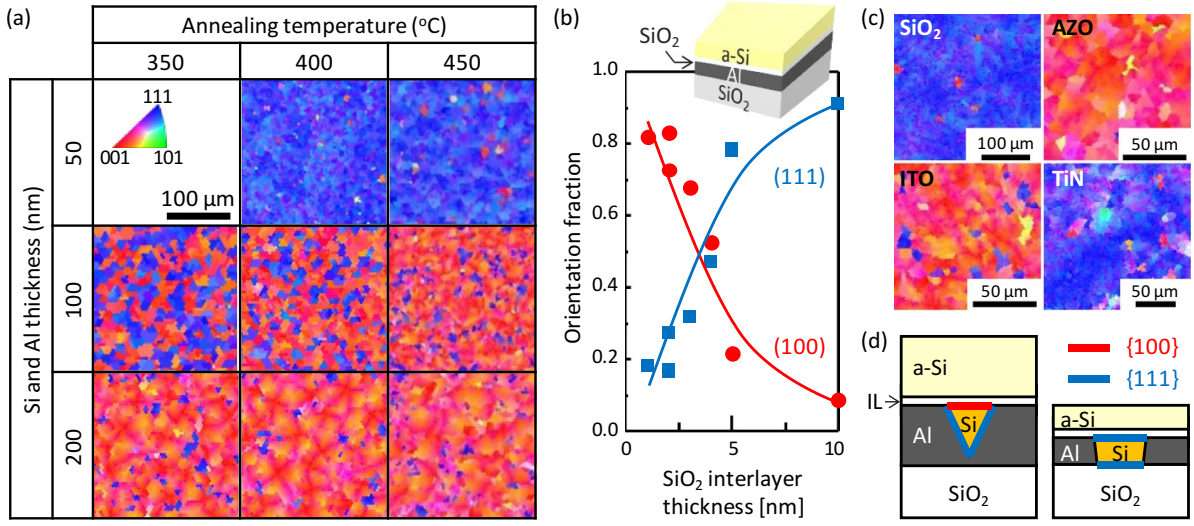

Figure 8. Crystal orientation of Si formed by Al-induced LE. (a) IPFs summarized as a matrix of annealing temperature and Si and Al thickness [139]. (b) Crystal orientation fraction as a function of the SiO_2 interlayer thickness [142]. (c) IPFs of the samples with various underlayers: SiO_2, ZnO:Al (AZO), In_2O_3:SnO_2 (ITO) and TiN [145]. Coloration in IPFs indicates crystal orientation, according to the legend in (a). (d) Schematic of Si nucleation in Al which determines the crystal orientation.

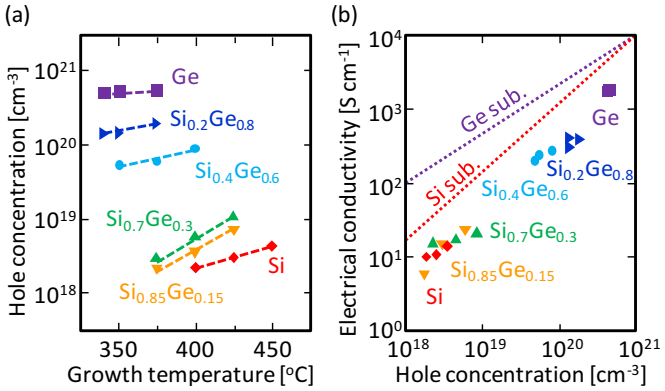

Figure 9. Electrical properties of the $Si_{1-x}Ge_x$ (x: 0, 0.15, 0.3, 0.6, 0.8 and 1) layers formed by Al-induced LE [40]. (a) Hole concentration as a function of growth temperature. (b) Relationship between the electrical conductivity and the hole concentration. The data for single crystal Si and Ge wafers are shown by dotted lines.

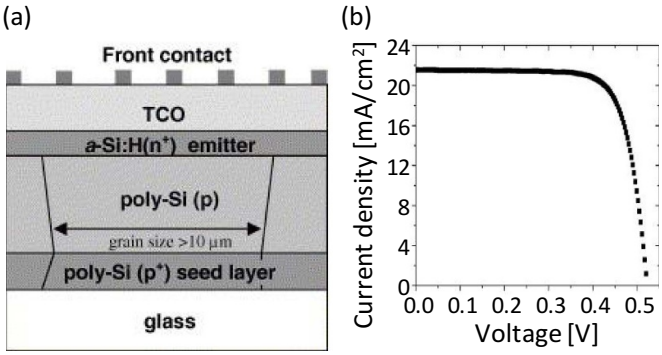

Figure 10. Polycrystalline silicon thin-film solar cells using the Si seed layer formed by Al-induced LE. (a) Schematic of the proposed seed layer approach [162]. (b) Current density—voltage curve of the record Si solar cell using the LE seed layer, featuring an energy conversion efficiency of 8.5%, an open circuit voltage of 522 mV, a short circuit current of 21.6 mA cm^{-2} and a fill factor of 75.8% [171]. (a) Reprinted from [162], Copyright (2004), with permission from Elsevier. (b) Reprinted from [171], Copyright (2013), with permission from Elsevier.

The seed layer approach using the Ge layer formed by Al-induced LE is also attractive. The motivation to replace the bulk Ge substrate, used in multijunction solar cells, with a Ge film on insulating substrates is quite high because the Ge substrate is expensive while Ge can absorb light even in a thin film. The Ge film, grown epitaxially from a large-grained p-type Ge seed layer formed by the Al-induced LE, exhibited a bulk minority carrier lifetime of 5.6 μs, which is close to that of a single-crystal Ge [188]. Ge is also useful as a seed layer for group III–V compound semiconductors because of lattice matching. The GaAs film, grown epitaxially from the Ge seed layer formed by Al-induced LE, became a pseudo-single crystal (grain size >100 μm) with high (111) orientation (figures 11(a)–(c)) [189]. Reflecting the large grain size, the photoresponsivity approached that of a simultaneously formed GaAs film on a single-crystal Ge wafer (figure 11(d)). The internal quantum efficiency reached 90% under a bias voltage of 0.3 V, which is the highest for a GaAs film synthesized on glass [190]. Use of the seed layer approach using the LE-Ge has just begun and is expected to reduce the fabrication cost of high-efficiency solar cells.

3.2. *Thin film transistors*

With the development of crystal growth and transistor technologies for Ge, study on Ge thin film transistors (TFTs) has recently become more active [191, 192]. In line with this, TFTs using the Ge channel layer formed by LE with Au and Ag catalysts have been reported [115, 166]. Because both Au and Ag have a small solid solubility in Ge, little metal contamination in the LE-Ge layer is expected [93]. The Au-induced LE can provide large-grained Ge layers at quite low

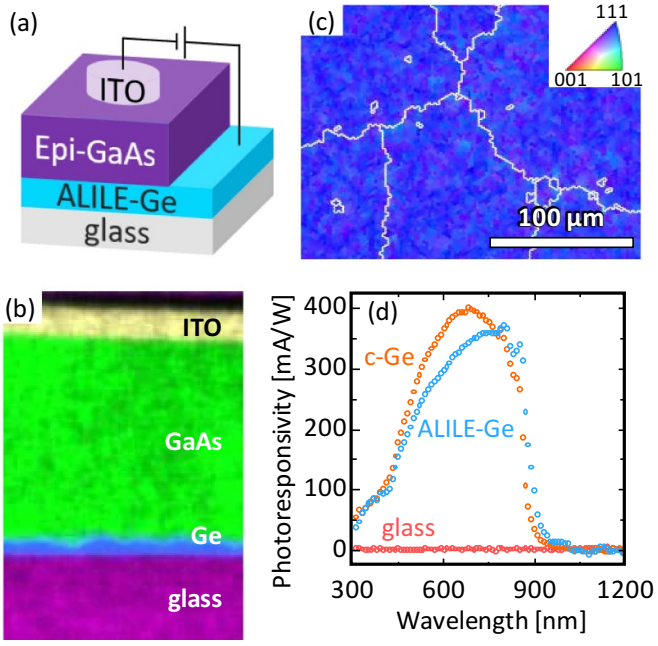

Figure 11. Solar cell application of pseudo-single crystal GaAs film on glass with a Ge seed layer formed by Al-induced LE (ALILE) [189]. (a) Schematic structure. (b) Cross-section elemental mapping obtained by energy dispersive x-ray analysis. (c) IPF of the GaAs film. The white solid lines indicate random grain boundaries; the coloration indicates the crystal orientation (refer to the inset legend). (d) Photoresponse spectra of the GaAs films formed at 520 °C with ALILE-Ge, single-crystal Ge (c-Ge) and glass substrates where the bias voltage is 1.0 V.

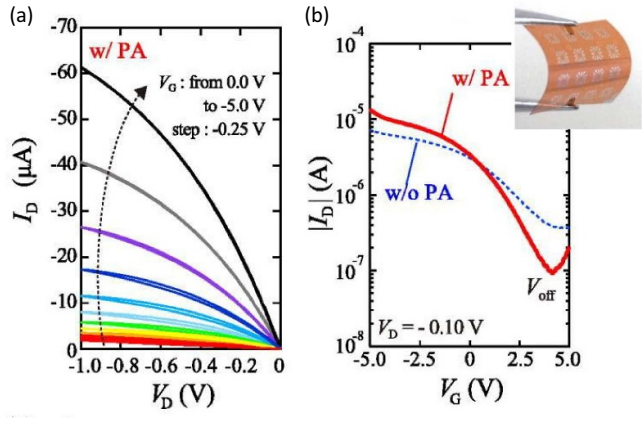

Figure 12. Flexible TFT based on the pseudo-single crystal Ge layer formed on a polyimide substrate using Au-induced LE [194]. (a) I_D-V_D characteristics. (b) I_D-V_G characteristics at a V_D of −0.1 V. The inset shows a photograph of the sample. Reprinted from [194], with the permission of AIP Publishing.

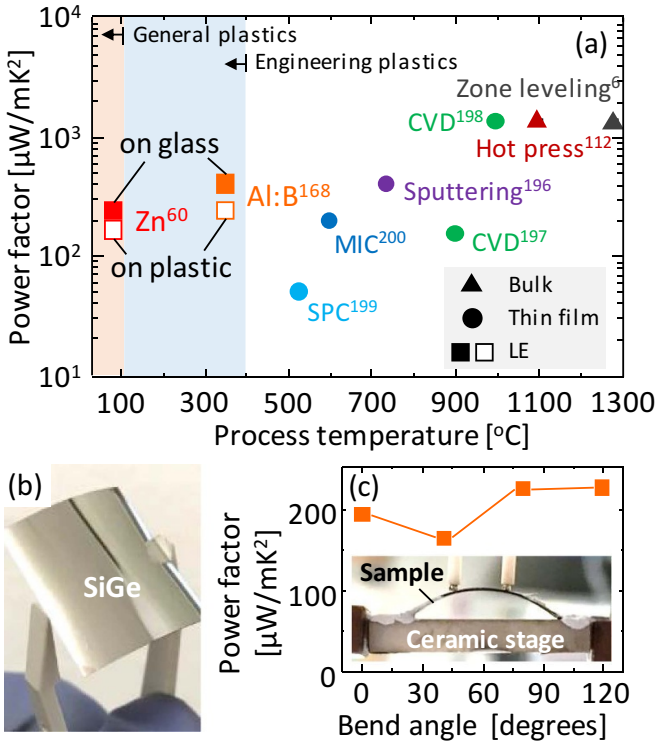

Figure 13. TEG application of LE-SiGe. (a) Comparison of the power factor at room temperature and the process temperature of p-type SiGe. The growth method (metal species) and the reference number are shown near each symbol. (b) Photograph and (c) bend angle dependent power factor of the SiGe sample formed at 350 °C using Al-induced LE [38]. The inset photograph in (c) shows the measurement setup of the sample with a bend angle of 80°.

temperatures. The resulting Ge layer after Au removal exhibits Hall hole mobility of 210 cm^2 Vs^{-1}, which is the highest as semiconductor thin films formed at <300 °C [193]. Transistor operation was demonstrated using the pseudo-single crystal Ge layer formed on glass and even on a plastic substrate (figure 12) [193, 194]. The field-effect mobilities exceeded 70 cm^2 Vs^{-1} on glass and 10 cm^2 Vs^{-1} on a plastic substrate. Although the challenge remains in reducing leakage current, the field-effect mobility is the highest among the p-channel TFTs fabricated at ⩽400 °C on flexible plastic substrates. Suzuki *et al* formed n- and p-type Ge layers at 330 °C using LE with an AgSb and Ag catalyst, respectively [163]. These resulted in both p- and n-channel TFTs, which will configure complementary-metal-oxide-semiconductor devices on flexible substrates.

3.3. Thermoelectric generators

SiGe alloy is the most well-known, reliable and tested thermoelectric material [6]; however, the bulk-SiGe formed by sintering methods is generally expensive, which limits its application. Conversely, a SiGe alloy film can be easily synthesized using sputtering [195], CVD [196, 197], SPC [198] and MIC [199]. To obtain high power factor in SiGe for TEGs, a high temperature process is generally required, mainly for the dopant activation, which is necessary for improving electrical conductivity (figure 13(a)). Conversely, LE can provide SiGe films with high electrical conductivity even at low temperatures by inducing both impurity doping and its activation according to the solid solubility. With this feature, LE using Al or Zn simultaneously achieved a high power factor and a low temperature process in p-type SiGe (figure 13(a)) [38, 60]. Excellent performance on a flexible

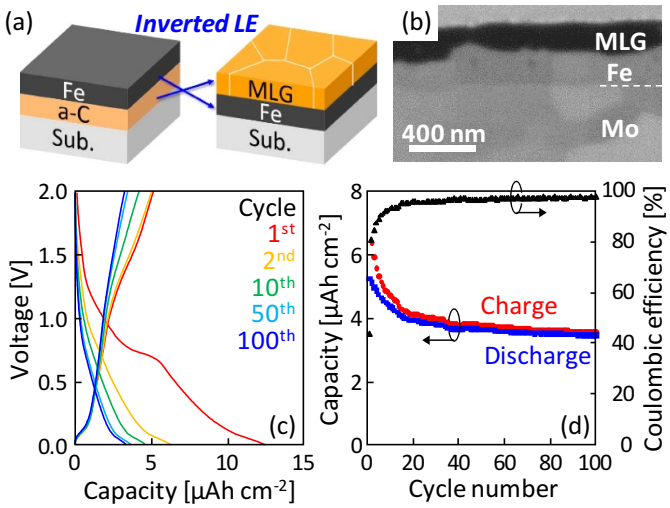

Figure 14. Rechargeable battery anode application of MLG formed by Fe-induced LE [72]. (a) Schematic of the self-organization of anode structure (i.e. MLG on Fe-electrode) using inverted LE. (b) Cross-sectional SEM image of the anode structure formed on a Mo substrate at 600 °C. Li-ion battery anode operation of the MLG: (c) galvanostatic charge/discharge cycles; (d) capacity and coulombic efficiency as a function of cycle number.

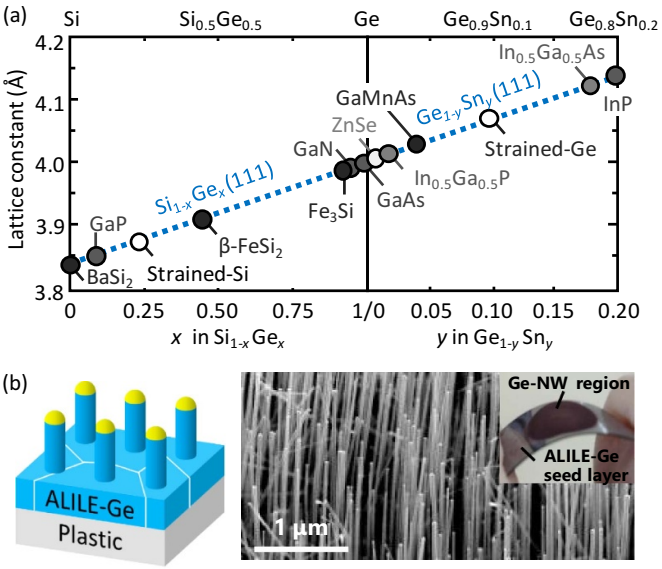

Figure 15. Application of LE to an epitaxial buffer layer. (a) Lattice constant of (111)-oriented $Si_{1-x}Ge_x$ ($0 \leqslant x \leqslant 1$) and $Ge_{1-y}Sn_y$ ($0 \leqslant y \leqslant 0.2$) showing that various materials are lattice matched. Some materials do not correspond to the net lattice constant but can be grown in mesh relation [202, 204]. (b) Vertically aligned Ge nanowires (NWs) on a flexible plastic substrate with a Ge seed layer formed by Al-induced LE (ALILE): schematic, SEM image and photograph [214].

plastic substrate was also demonstrated (figures 13(b) and (c)). A $Si_{0.4}Ge_{0.6}$ layer fabricated on a polyimide substrate using Al:B-induced LE exhibited a power factor of 240 μW mK^{-2}, which is the best recorded for environmentally-friendly inorganic semiconductors formed on flexible plastic substrates [167]. By using Ag or Au as the LE metal and initially doping them with n-type impurities, the conduction type of the SiGe film can be controlled to n-type. Therefore, the LE technique is promising for developing active SiGe films which are useful for highly-reliable flexible TEGs.

3.4. Rechargeable batteries

Research on a thin-film rechargeable battery has progressed remarkably for next-generation batteries suitable for mobile devices or sensors [200]. To achieve this, techniques for forming anode, solid electrolyte and cathode materials on an arbitrary substrate are essential. Graphite, an anode material for general rechargeable batteries, cannot be directly synthesized on most substrates because its synthesis temperature is too high (∼3000 °C). Conversely, the inverted LE allowed low-temperature (⩽600 °C) self-organization of the anode electrode structure, that is, a graphite thin film (MLG) on a current collector metal (figure 14(a)) [72]. To evaluate the anode performance, the same structure was formed on a Mo substrate (figure 14(b)), which exhibited Li-ion batteries' anode operation (figures 14(c) and (d)). Si and Ge are also considered as anode materials because of their high capacity [201]. Qu *et al* formed a nanostructured Si anode with high surface area using LE and demonstrated Li-ion batteries' excellent anode characteristics (1650 mAh g^{-1} after 500 cycles) [88]. Because these group IV materials, which are useful as an anode, can be synthesized on plastic substrates using LE, the findings will increase the potential for developing flexible rechargeable batteries.

3.5. Epitaxial buffer layers

LE allows for controlling of the crystal orientation of semiconductor thin films on amorphous substrates. For example, Al-induced LE provides highly (111)-oriented SiGe with large grains (>50 μm) over the entire composition range [40]. Therefore, the lattice constant is tunable by controlling the SiGe composition. With these features, the semiconductor thin films formed by LE can be used as epitaxial buffer layers for developing various functional materials on different substrates. The (111) plane in SiGe and GeSn are lattice matched with many materials such as compound semiconductors, silicides [202, 203] or nitrides [204] (figure 15(a)). The lattice tunable buffer layer will be also useful for applying strain to Si and Ge to increase the carrier mobilities [205, 206]. In fact, different materials such as GaAs [188, 207], $BaSi_2$ [208, 209], ZnO [150] and GaN [210] were developed on glass using the LE buffer layer. Additionally, aligned nanowires were synthesized on glass [123, 211–213] and even on a flexible plastic substrate [214] using the property that the nanowires grow in a specific orientation (figures 15(b) and (c)). The LE layer is also useful for seeding rapid-melting growth of Ge [215]. Kurosawa *et al* demonstrated single-crystal Ge wires with (100), (111) and (110) hybrid orientations on a Si platform [216]. Therefore, LE has high potential as a technology that can develop and integrate various functional materials on arbitrary substrates.

Table 1. Summary of LE material combinations and their features. T is the growth temperature for LE. GS, orientation, and p are the net grain size, controllable crystal orientation perpendicular to the substrate, and hole concentration of the resulting group IV layer, respectively. Applications show the device applications that have been mainly investigated. References show the representative papers for each combination or application.

Group IV	Metal	T (°C)	GS (μm)	Orientation	p (cm^{-3})	Applications	References
Si	Al	280–550	5–400	111, 100	10^{18}–10^{19}	Solar cells	[19, 162, 171]
Si	Ag	500–800			Intrinsic		[54]
Si	Au	250–400			Intrinsic		[56]
Ge	Al	180–410	1–200	111, 100	$\sim 10^{20}$	Solar cells	[41, 188, 189]
Ge	Ag	250–420	0.1–2	Weak 111		TFTs	[47, 166]
Ge	Au	250–300	1–600	111, Weak 100	10^{17}–10^{18}	TFTs	[59, 193]
Ge	Zn	80–200	0.01–0.2	Random	$\sim 10^{20}$	TEGs	[60]
SiGe	Al	300–450	10–200	111, 100	10^{18}–10^{20}	TEGs	[38, 66]
SiGe	Au	250–300	∼10	Weak 111			[65]
GeSn	Al	300–350	20–60	111, 100			[69]
C	Ni	500–1000	0.1–2	002	10^{19}–10^{20}	Electrodes	[70, 89]
C	Fe	600–1000	∼0.1	002		Batteries	[72]
C	Pt etc	600–1000		002			[71]

4. Summary

We reviewed the LE research to date, from the mechanism to device applications. LE allows various group IV materials (Si, SiGe, Ge, GeSn and C) with various properties to form on arbitrary substrates by selecting the appropriate metal catalysts and growth conditions (table 1). The features obtained using LE and the corresponding device applications are summarized as follows. (i) Low-temperature crystallization (80 °C–500 °C) enables us to use heat-sensitive Si integrated circuits, glass and even flexible plastic as the substrates. (ii) Grain size can be controlled in a wide range: large grains (∼mm) for high-performance thin-film solar cells and transistors; small grains (∼nm) for thermoelectric films with high thermal resistance. (iii) Crystal orientation control is effective for forming epitaxial buffer layers of various functional materials on amorphous substrates. (iv) Impurity concentration control according to the solid solubility is attractive for various devices: high concentration for TEGs and contact layers of optical devices; low concentration for channel layers of TFTs. Thus, by properly selecting material combinations and growth conditions, LE can synthesize the desired film according to the application.

5. Future perspective

Although the history of LE is long, its applications to materials other than the Si-Al system and devices other than solar cells have only just begun. The effects of the crystallinity and doping level on the film and device performance are largely unknown. The related studies should be continued and accelerated in each field. While thin films (<500 nm) are sufficient for the seed layer and TFT channel applications, thick films (>500 nm) are preferred for the TEGs and rechargeable batteries. There is much room for LE research from the perspective of thick film synthesis. Further, there will be various material combinations and device applications other than those introduced in this paper. For example, LE synthesis of compound semiconductors is unprecedented but attractive for flexible electronics with optical elements and power devices. The potential for further development of LE is large.

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