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Energy distribution of Al_2O_3/diamond interface states characterized by high temperature capacitance-voltage method

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ABSTRACT

In our previous work, we demonstrated the world's first inversion-type p-channel diamond metal–oxide–semiconductor field-effect transistor (MOSFET). However, it exhibited low channel mobility due to high interface state density (D_{it}). In this study, the electronic states of Al_2O_3/diamond interfaces above the valence band edge (E_v) were carefully examined by capacitance–voltage (C–V) measurements in a wide frequency range of 1 Hz–10 MHz at 300, 350, and 400 K, providing an accurate characterization of deeper interface state density compared with our previous work (from 10 Hz to 10 kHz at room temperature) within the limitations of the high-low method. We observed humps in C–V curves, which became wider as the temperature increased and the frequency decreased, indicating the presence of interface states at deep energy levels. They can act as Coulomb scattering centers in diamond MOSFETs; thus, their characterization at low frequencies and high temperatures is necessary. The energy distribution of D_{it} was estimated using the high-low method at 400 K, indicating that D_{it} was in the range of $(0.4–1.5) \times 10^{12}$ $cm^{-2}eV^{-1}$ within 0.23–0.76 eV from E_v of diamond. More effective passivation techniques are required to reduce interface states at deep energy levels.

1. Introduction

Diamond has attracted much attention in power electronics due to its superior physical properties, such as a wide bandgap, high carrier mobility, high breakdown field, and high thermal conductivity [1,2]. Numerous studies have been devoted to the development of diamond power metal–oxide–semiconductor field-effect transistors (MOSFETs). Most diamond MOSFETs have been fabricated using H-terminated diamond surfaces with their unique properties of two-dimensional hole gas [3–9]. Recently, Kawarada et al. reported the highest breakdown voltage in lateral H-diamond MOSFETs and the first vertical H-diamond MOSFETs [10,11]. However, H-diamond MOSFETs basically exhibited normally on characteristics. Although a few accumulation-channel MOSFETs have demonstrated normally off properties, controlling the threshold voltage (V_{th}) by choosing the metal work function is difficult [12–15]. MOSFETs with inversion channels are feasible to control electric power owing to their gate voltage control capability, which enables V_{th} control by impurity concentration in the body. In 2016, our group demonstrated the first inversion-type p-channel diamond MOSFET with normally off operation with Al_2O_3 film deposited on O-terminated diamond (111) surface followed by wet annealing [16]. It shows that the wet annealing process, which forms OH-terminated diamond surfaces, is one of the most promising candidates to realize inversion-type diamond MOSFETs. However, the inversion-type p-channel diamond MOSFET suffers from low field-effect mobility (μ_{FE}, ~8 $cm^2V^{-1}s^{-1}$) [16], which is mainly attributed to the existence of high interface state density (D_{it}) on the order of 10^{13} $cm^{-2}eV^{-1}$ near the valence band edge (E_v) of diamond. To realize the diamond power MOSFETs with low on-

Abbreviations: ALD, Atomic layer deposition; HPHT, High-pressure, high-temperature; MPCVD, Microwave plasma chemical vapor deposition.

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resistance, we aim to elucidate the mechanisms of low channel mobility and high D_{it}. However, there are only a few reports involving the characterization of the diamond MOS interfaces [17–22].

For interface characterization in SiC or other wide-gap semiconductor materials, one basic approach is the high-low method, by which the capacitance–voltage (C–V) characteristics at both high and low frequencies are measured and compared. On one hand, the high frequency is expected to be as high as possible so that interface states cannot respond to the measurement frequency and the measured capacitance (C_{hf}) does not include interface-state capacitance (C_{it}). On the other hand, the low frequency should be low enough for measuring the low-frequency capacitance (C_{lf}) to obtain the C–V curves with including the capacitance contribution of interface states as much as possible. The capacitance difference can be attributed to the interface states; thus, D_{it} can be calculated as [23]

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right), \quad (1)$$

where C_{ox} denotes the oxide capacitance and q denotes the elementary charge. However, in the previous interface studies of diamond, most of them did not address the C–V characteristics, or just characterized C–V at a certain frequency or two frequencies [21,24–28]. Thus, D_{it} was not able to be extracted or significant errors would exist in D_{it} evaluation. For example, 10 Hz and 10 kHz were used for low- and high-frequency measurements in a previous study [21]. The C–V curves at frequencies higher than 10 kHz were not obtained. Owing to the narrow frequency range, only the interface states responding to this narrow range were estimated as D_{it}, which may underestimate true D_{it}. Besides, the presence of interface states at deep energy levels towards the midgap may need to be considered for diamond, a wide-gap semiconductor material, because they can act as the Coulomb scattering centers in diamond MOSFETs and degrade the channel mobility. Thus, to detect interface states at deeper energy levels, measurements at lower frequencies and higher temperatures may be required due to their long time constants.

In this work, we report the D_{it} characterization for the diamond MOS interface, especially by focusing on the interface states at deep energy levels, which may have been overlooked in the previous studies. We discuss the appropriate measurement conditions for characterizing the diamond interface by the high-low method, paying attention to the measurement temperature and frequency.

2. Experimental methods

Diamond MOS capacitors were fabricated on a p-type diamond epitaxial layer with a net boron concentration of approximately 1×10^{16} atom/cm^3 and a thickness of 1 μm on a high-pressure, high-temperature (HPHT) synthetic IIb 2.6° off-axis (111) single-crystal diamond substrate with a boron concentration of ~1×10^{20} atom/cm^3 via microwave plasma chemical vapor deposition (MPCVD) equipment. To form an excellent ohmic contact on the backside of diamond, a heavily boron-doped diamond layer with a concentration of ~1×10^{21} atom/cm^3 and a thickness of 50 nm was deposited on the backside of the substrate by MPCVD. Recently, our group has successfully formed atomically flat OH-terminated diamond (111) surfaces without surface degradation by using H-terminated diamond subjected to wet vapor annealing [29]. Therefore, this method was employed here to form the OH-terminated diamond (111) surface. The specific process flow is as follows. After cleaning with sulfuric–peroxide mixture, the diamond sample was exposed to hydrogen plasma in the MPCVD chamber with a pressure of 225 Torr and microwave power of 800 W at 900 °C for 10 min to realize hydrogen termination. Then, the sample was subjected to wet annealing at 500 °C for 60 min in a quartz tube of an electric furnace to realize OH-terminated diamond surface. The wet ambient was prepared by bubbling of N_2 carrier gas through de-ionized water. Next, about 50-nm-thick Al_2O_3 film was grown by atomic layer deposition (ALD) at 300 °C. Finally, Au electrodes were deposited to form gate and backside ohmic contacts. The circular gate electrodes were 200 μm in diameter.

The frequency-dependent C–V characteristics were examined at various temperatures of 300, 350, and 400 K, respectively. High-frequency C–V measurements (1 kHz–10 MHz) were conducted from depletion to accumulation using an Agilent 4294A impedance analyzer with a 42941A impedance probe kit. Low-frequency measurements at 1 Hz were performed from depletion to accumulation using an Agilent ultralow-frequency C–V system, which consists of an Agilent B1500A and an Agilent 33210A function generator.

3. Results and discussion

Fig. 1 shows the C–V characteristics from 1 Hz to 10 MHz at 300 K for the p-type diamond MOS capacitor. First, the accumulation capacitance was clearly observed, and it was found that the leakage current is small enough owing to good insulator quality, which is confirmed with the DC current–voltage (I–V) measurements where the current density is lower than 10^{-9} A/cm^2 at a negative gate bias of −20 V (not shown). With regard to the frequency dispersion, a hump in a C–V curve at 1 Hz was observed, and the magnitude of the hump decreased with increasing frequency. These results can be attributed to the interface states at deep energy levels, which possess long emission time constants and cannot immediately change occupancy in response to the AC gate voltages at high frequencies, thereby leading to frequency dispersion. At high temperatures, the thermal emission of interface states at deep energy levels becomes faster, and even deeper interface states can be detected within the same given frequency range. Therefore, higher measurement temperature is required to

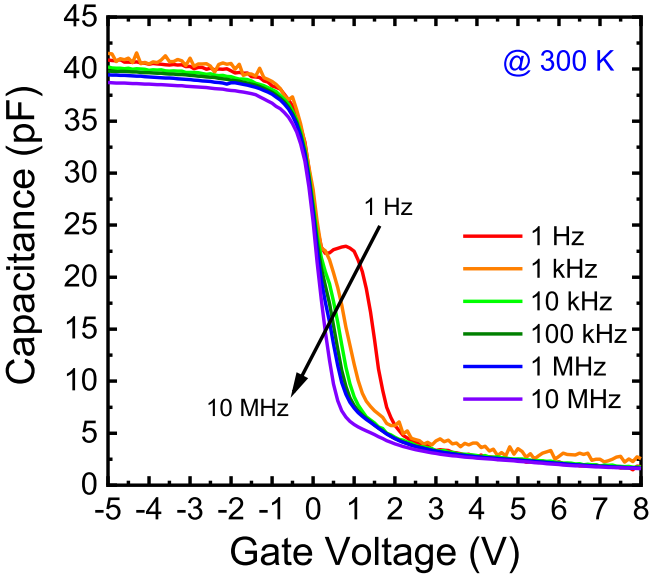

Fig. 1. Frequency dependence of C–V characteristics from 1 Hz to 10 MHz at 300 K. (A colour version of this figure can be viewed online.)

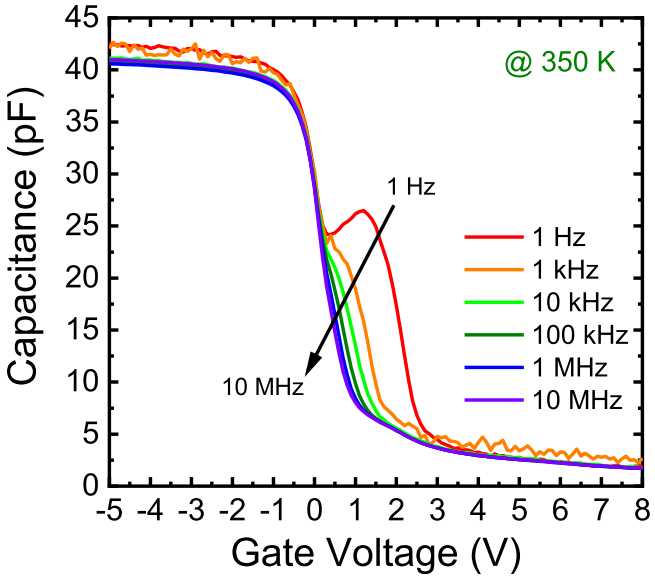

Fig. 2. Frequency dependence of *C*–*V* characteristics from 1 Hz to 10 MHz at 350 K. (A colour version of this figure can be viewed online).

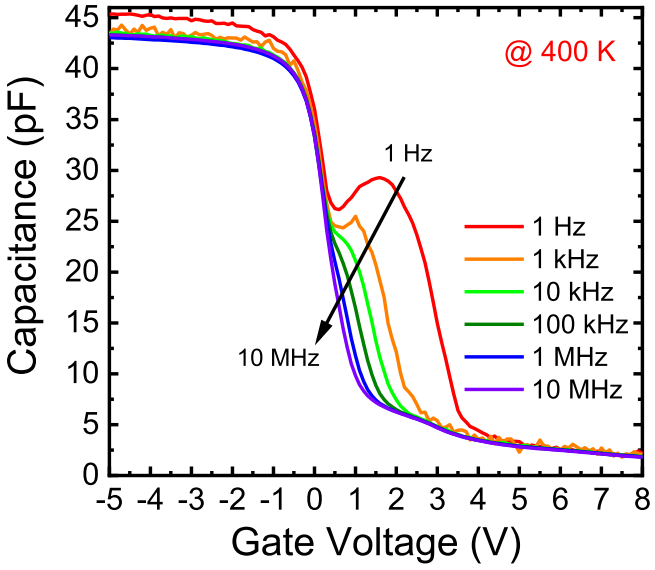

Fig. 3. Frequency dependence of *C*–*V* characteristics from 1 Hz to 10 MHz at 400 K. (A colour version of this figure can be viewed online.)

detect interface states at deep energy levels while maintaining the measurement frequency as low as possible. Figs. 2 and 3 present the high-low frequency *C*–*V* curves at 350 and 400 K. By comparing the three *C*–*V* curves, we deduce that the frequency dispersion of *C*–*V* curves in the depletion region increases as the measurement temperature increases, indicating that interface states at deep energy levels can be detected at 400 K. Therefore, high temperature is necessary to characterize the diamond MOS interface where interface states exist at deep energy levels. Note that the frequency dispersion of the accumulation capacitance may be due to the response of border traps, which is often observed in InGaAs and SiC MOS structures [30,31]. We checked the effect of series resistance on the accumulation capacitance by a standard correction method [32], but the dispersion was unchanged after the correction. The discussion about the dispersion in the accumulation capacitance requires an analysis by the distributed circuit model [30,31], which is beyond the scope of this paper.

To evaluate D_{it} as a function of energy position from E_v of diamond by the high-low method, it is necessary to estimate the detectable energy range within the wide bandgap of diamond at various temperatures. According to the Shockley–Read–Hall (SRH) statistics [33], the hole emission time constant (τ_p) of an interface state to the valence band of a p-type semiconductor can be expressed as

$$\tau_p(E) = \frac{1}{\sigma_p \nu_{th} N_v} \exp\left(\frac{E - E_v}{kT}\right), \quad (2)$$

where σ_p is the capture cross section, ν_{th} the thermal velocity, N_v the effective density of states in the valence band, $E - E_v$ the trap energy level relative to the valence band edge (E_v), k the Boltzmann constant, and T the absolute temperature [34]. The temperature dependence of τ_p versus energy position from E_v is plotted in Fig. 4, assuming a capture cross section on the order of 10^{-17} cm^2, which was determined by AC conductance method and will be published elsewhere. Because the reciprocal of the interface state time constant corresponds to the frequency, the upper and lower dashed lines indicate the minimum and maximum frequencies, and the corresponding detectable energy ranges at different temperatures can be estimated. As the temperature increases, the detectable energy range in the shallow region close to E_v does not substantially change, whereas the relatively deep energy region exhibits stronger temperature dependence. At 400 K and 1 Hz, the detectable energy level is up to around 0.76 eV from E_v, whereas at 300 K and 1 Hz, it reaches around 0.55 eV from E_v, and more importantly, the small frequency dispersion of *C*–*V* curves at 300 K could lead to an error in D_{it} estimation. Therefore, the *C*–*V* data at higher temperatures more accurately reflect the actual interface state density. Note that even though high-temperature measurements are desirable to characterize the diamond MOS interface, the interface properties may be degraded at high temperatures. Thus, in this study, the upper limit of the measurement temperature was chosen at 400 K. Based on the *C*–*V* dispersion from 1 Hz to 10 MHz at 400 K and high-low method, the energy distribution of D_{it} was estimated, as shown in Fig. 5. Note that the surface potential was determined by the Berglund integral, and the integral constant (ψ_{s0}) was determined from the flatband voltage in the *C*–*V* curve at 10 MHz [35]. Besides, the *C*–*V* hysteresis was not observed at each frequency, which assures the feasibility of the high-low method. From the energy dependence of D_{it}, it can be seen that D_{it} increases dramatically from 0.23 to 0.6 eV. As the energy position becomes deeper than 0.6 eV, D_{it} gradually saturates. Despite the detection limit, the decrease in D_{it} in the energy levels deeper than 0.76 eV from E_v, which corresponds to the gate voltage higher than 1.6 V, can be expected from the reduced frequency dispersion of the *C*–*V* characteristics. The estimated trap density was $(0.4–1.5) \times 10^{12}$ cm^{-2}eV^{-1}, which is lower than that of the Al_2O_3/diamond MOS with a value of $(4–9) \times 10^{12}$ cm^{-2}eV^{-1} in which the OH-terminated diamond surface was formed on the O-terminated diamond [21]. Despite the different measurement temperature and frequency ranges, the Al_2O_3/diamond interface quality was improved. As it is known that the surface was roughened during the O-termination formation process by immersing the atomically flat H-terminated diamond in a hot mixture of HNO_3/H_2SO_4 acids and the surface roughness increased by around 0.1 nm [36]. This would deteriorate the subsequent wet annealing process and thus lead to poor OH-terminated diamond surface, which may cause a high density of interface states. When the OH-terminated diamond surface was formed by wet annealing of the H-terminated diamond, surface degradation was not observed [29], resulting in

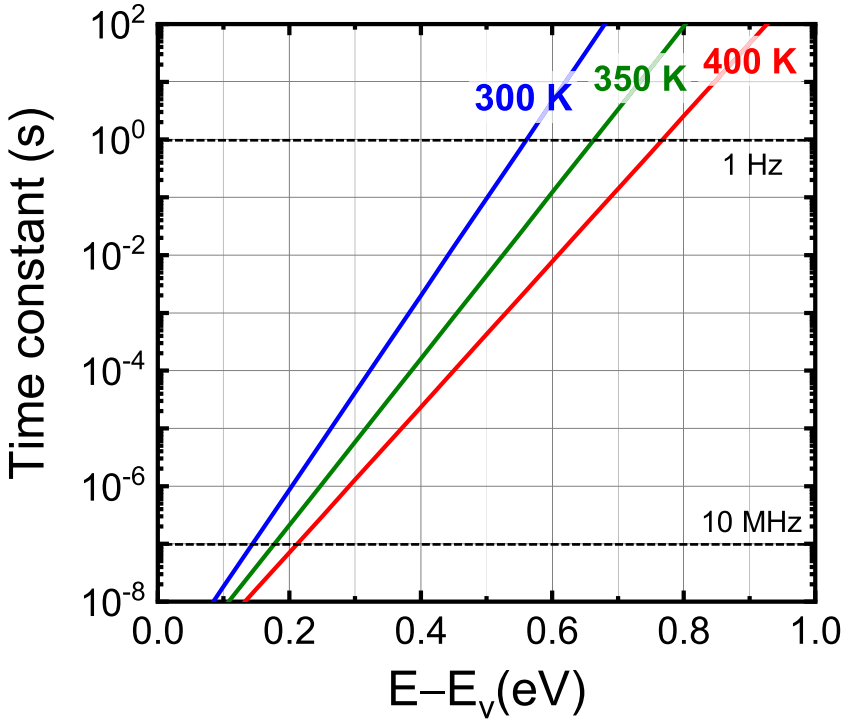

Fig. 4. Emission time constant of holes from an interface state to the valence band edge of diamond at 300, 350, and 400 K. The capture cross section was assumed to be 1×10^{-17} cm^2. Two horizontal lines indicate the upper and lower frequency limits. (A colour version of this figure can be viewed online.)

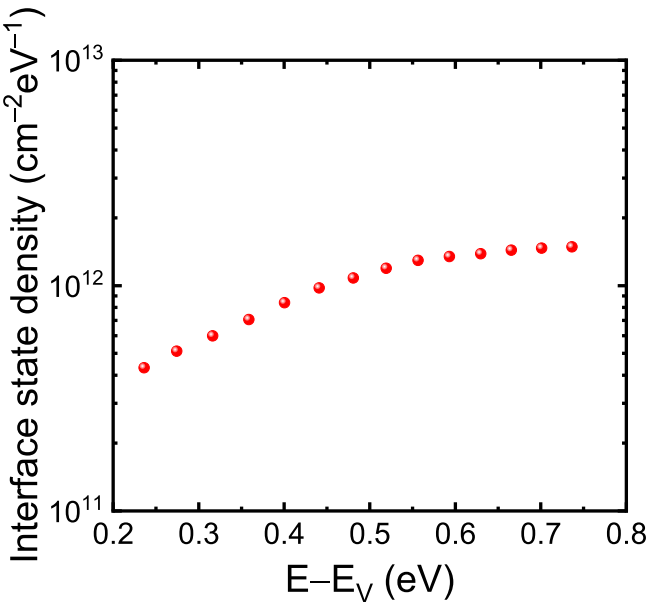

Fig. 5. Energy distribution of interface trap density (D_{it}) for the Al_2O_3/diamond MOS structure estimated by the *C–V* data from 1 Hz to 10 MHz at 400 K. (A colour version of this figure can be viewed online.)

better OH-terminated diamond surface and thus higher interface quality. It should be pointed out that the discussion above focused on the atomically flat diamond surface. However, in this work, we did not employ the atomically flat diamond surface to fabricate MOS capacitors and the surface roughness is in the order of 1–5 nm; thus, the surface roughening caused by the O-termination process would be negligible. Therefore, we thought D_{it} reduction of the OH-terminated diamond surface formed by H-plasma treatment and subsequent wet annealing could not be explained by surface roughness change. Here, we would like to discuss the possible reason. In terms of the O-terminated diamond surface, the origin of surface states is considered as two types of surface oxygen sites; one is bridge site (C–O–C) and the other is on top site (C=O) [37,38]. Also, these two kinds of bonding structures have been observed for O-terminated diamond surface by Fourier transform infrared (FTIR) spectroscopy in our previous work [29]. Due to the existence of C–O–C and C=O, it would be less effective by using subsequent wet annealing to form C–OH termination. Regarding the following ALD process, it can be expected that C–O–C and C=O are difficult to react with $Al(CH_3)_3$ (TMA) and both would remain at the interface and may be responsible for high D_{it} of the OH-terminated diamond MOS formed on O-terminated one. On the other hand, when the OH-termination is formed by H-plasma and subsequent wet annealing, the C–OH bonds were formed [29]. Then during the ALD growth of Al_2O_3, these C–OH bonds can react with TMA to form C–O–Al. However, it is difficult for C–O–C and C=O to react with TMA to form C–O–Al. Thus, there would be more C–O–C and C=O for OH-terminated diamond formed by O-terminated treatment than that formed by H-terminated treatment. Considering that the D_{it} is originated from C–O–C and C=O, we can conclude the D_{it} is lower by using H-terminated diamond followed by wet annealing than that by O-termination and subsequent wet annealing. In measurements, the interface states at deep energy levels can be observed at only very low frequencies and high temperatures; thus, they may have been overlooked in previous studies. When the interface states at deep energy levels are positively charged, they can also act as Coulomb scattering centers in diamond MOSFETs. Therefore, more effective passivation techniques need to be developed to improve the interface quality of the Al_2O_3/diamond interface, considering the interface states at deep energy levels detected in this study. Note that there are always limitations in the high-low *C–V* method due to surface potential

fluctuations [39] and the difficulty of surface potential determination [40]. In addition, the high- and low-frequency curves were separately measured in this study. For more accurate characterizations, simultaneous C–V needs to be used to align the surface potentials for high- and low-frequency curves. The D_{it} estimated in this study is accurate within the limitations of high-low method and not perfectly accurate mainly due to the above problems. More precise characterization requires other characterization techniques, such as the conductance method [41,42].

4. Conclusions

In this study, we discussed the method to evaluate D_{it} at the Al_2O_3/diamond interface using high-quality samples prepared by H-terminated diamond and subsequent wet N_2 annealing. The high-low C–V characteristics from 1 Hz to 10 MHz at various temperatures from 300 to 400 K were examined. We found that interface states exist at deep energy levels, and the energy distribution of the interface states was estimated by the high-low method. The interface quality was improved compared with the previous process where the OH-terminated diamond surface was formed from the O-terminated diamond. More effective passivation techniques are needed to be developed to reduce the interface states at deep energy levels, which would be beneficial for the development of diamond MOSFETs with high channel mobility.

CRediT authorship contribution statement

Xufang Zhang: Conceptualization, Methodology, Formal analysis, Investigation, Data curation, Writing - original draft, Visualization, Funding acquisition. **Tsubasa Matsumoto:** Conceptualization, Formal analysis, Funding acquisition. **Ukyo Sakurai:** Data curation, Formal analysis. **Toshiharu Makino:** Resources. **Masahiko Ogura:** Resources. **Satoshi Yamasaki:** Formal analysis. **Mitsuru Sometani:** Formal analysis. **Dai Okamoto:** Formal analysis. **Hiroshi Yano:** Formal analysis. **Noriyuki Iwamuro:** Formal analysis. **Takao Inokuma:** Resources, Formal analysis. **Norio Tokuda:** Conceptualization, Resources, Supervision, Formal analysis, Writing - review & editing, Funding acquisition, Project administration.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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