Single silicon vacancy-oxygen complex defect and variable retention time phenomenon in dynamic random access memories

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Single silicon vacancy-oxygen complex defect and variable retention time phenomenon in dynamic random access memories

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The variable retention time phenomenon has recently been highlighted as an important issue in dynamic random access memory (DRAM) technology. Based on electrically detected magnetic resonance and simulation studies, we suggest that a single Si vacancy-oxygen complex defect is responsible for this phenomenon, when the defect is embedded in the near surface drain-gate boundary of a DRAM cell. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2213966]

In 1992 Restle *et al.* reported the two-level variable retention time (VRT) phenomenon of dynamic random access memory (DRAM), which was observed universally in 64 Kbit–16 Mbit DRAMs of various manufacturers.[1] We also observed this phenomenon in a 256 Mbit DRAM cell, as shown in Fig. 1(a). The two-level VRT is characterized by two reversible states (deemed "good" and "bad") that exhibit two discrete data retention times (RTs). It was recently demonstrated that the junction leakage current (JLC) of a VRT bit reversibly changes between low and high levels, causing the VRT phenomenon.[2] Similar two-level "telegraph" phenomena were also observed as random telegraph noise in the channel current of a small Si field effect transistor[3] and in the leakage current of an ultrathin SiO_2 film.[4] This noise originates from the interaction between a single defect and the carriers.[3,4] Likewise, the VRT phenomenon is believed to be related to a single "bistable" defect (VRT defect);[1,2] however, its microscopic entity is still unclear. Since the VRT has a drastic impact on a DRAM's performance and reliability,[2,5,6] this is a highly important issue.

In this letter, we suggest that Si vacancy-oxygen (*V*O) complexes are the most likely source of the VRT defect. We detected such complexes in DRAM cells by means of electrically detected magnetic resonance (EDMR). The location, electronic levels, and bistable nature of those complexes are discussed in conjunction with the basic features of the VRT.

First, we found that the characteristic thermal activations of the VRT in old and current DRAMs are similar. Restle *et al.*[1] established that VRT can be described using a bistable energy diagram with two energy barriers, E_g and E_b [Fig. 1(b)]. The average lifetime for a good (bad) state is in proportion to $\exp[E_{g(b)}/kT]$, where k is the Boltzmann constant and T is temperature.[1,2] For our VRT bits, as shown in the Arrhenius plot in Fig. 1(c), E_g and E_b were found to be approximately 1.16 and 1.06 (±0.06) eV, respectively, which are close to Restle's values (E_g=0.90–1.04 eV, E_b =0.84–1.08 eV, and generally $E_g > E_b$). We also found that their activation energies were between 0.7 and 1.4 eV; however, most cases exhibited a barrier of approximately 1 eV and $E_g > E_b$. Therefore, the nature of the VRT defect is apparently unchanged in current DRAMs. This defect must be located in the Si depletion layer since it generates the JLC.

To investigate this defect, we performed EDMR measurements on the JLC in 10 000 DRAM cells with 64 or 512 Mbit technologies (gate length=0.25 and 0.11 μm and junction area$\approx$2500 and 300 μm^2, respectively). The EDMR setup and measurement conditions used here were basically the same as those previously reported.[7,8] Figure 2 shows typical EDMR spectra for the two samples when the reverse bias (V_R) was applied to their *pn* junctions (the n^+-drain to the *p*-well). Two types of defects were observed in the 64 Mbit sample; they were assigned to large *V*O complexes (V_6 or larger) or V_2O and V_2O_2 (V_2O_x) based on a previous detailed study.[7] The 512 Mbit sample clearly exhibited a large *V*O signal, but the V_2O_x signal was unclear due to noise. Nevertheless, we deduced that both types of defects were present in every DRAM, because they were formed by ion implantation in the drain (n^+) region,[7] which is a fundamental process for DRAM technology. The defects possess two or more Si dangling bonds (DBs), which generate electronic levels E_t in the gap; for the V_2O_x type (with two DBs, electron spin S=1), two (+|0) levels lie at E_V (valence band top)+0.3–0.4 eV.[9] These levels are similar to those of the well-known P_b center (DB at $Si-SiO_2$ interface).[9] We thus speculate that E_t exists at similar positions for the large *V*O defects because they also have DBs. Their EDMR signal intensities were sensitive to the gate voltage, indicating that they were located in the near-surface drain region close to the gate.[7] These complexes are the likely source of the VRT defect.

The JLC due to the defect J can be calculated using the well-known Shockley-Read-Hall formula,[10]

$$J = C_n C_p v_{th} n_i / [C_n \exp(-E/kT) + C_p \exp(E/kT)],$$

where $C_{n(p)}$ is the electron (hole) capture cross-section, v_{th} is the carrier thermal velocity [$=(3kT/m^*)^{1/2}$; we used the effective mass ($m^*=0.25m_0$) for Si (Ref. 11)], n_i is the intrinsic carrier concentration of Si, and E is the difference between

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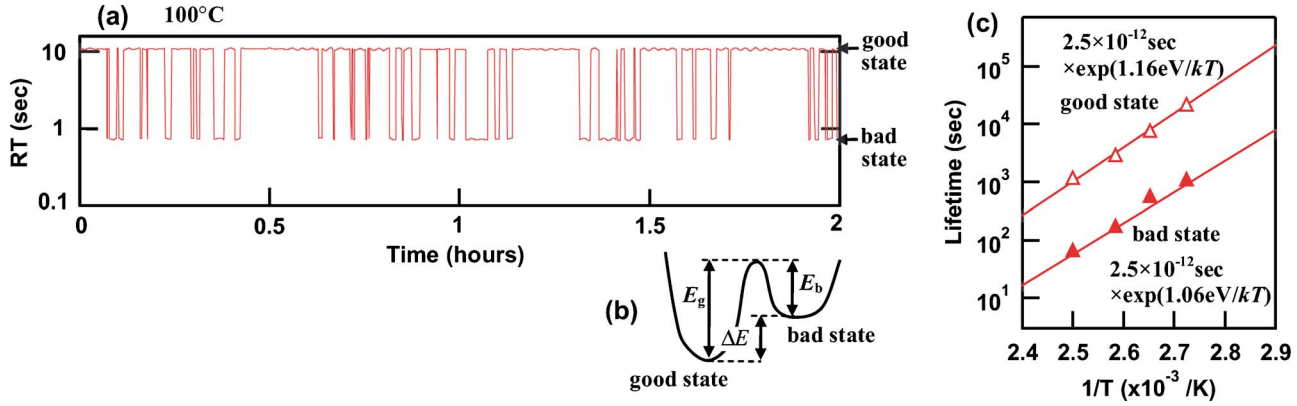

FIG. 1. (Color online) (a) Two-level VRT phenomenon observed in 256 Mbit DRAM cell. (b) Bistable energy diagram for VRT (Ref. 1). (c) Thermal activation of reversible change between good and bad states for 256 Mbit DRAM cell.

the intrinsic Fermi level and the defect level ($=E_i-E_t$). We simulated J vs E_t for a typical defect level,[12] as shown in Fig. 3(a) (the "normal" curve). The good and bad states correspond to energetically lower and higher defect levels, which are separated by $\Delta E(=E_g-E_b\approx0.1$ eV), as assumed in Fig. 1(b). The simulated change in J was $10^{1.3}$, which is comparable to the observed change in RT [see Fig. 1(a)].

However, the simulated JLC from the bad state was 1/100 or less of the actual current level (100 fA or more). This inconsistency can be reasonably accounted for by the presence of a strong electric field (F) in the device. Using a standard numerical simulator, we simulated the electric field distribution in a 256/512 Mbit DRAM cell operating under normal charge retention. As shown in Fig. 3(b), the highest electric field (0.5 MV/cm) was observed at the boundary between the n^+ drain and the gate, which coincides with the region where the VO complexes were embedded. With such a strong F, the $(+|0)$ level of a DB can activate the Poole-Frenkel effect (PF).[13] The trap assisted tunnel (TAT) effect can also work.[11] Using previously reported formulas,[11,13] we calculated the enhancements to the electron emission and trap rates from the $(+|0)$ level,

$$E_{\mathrm{PF}}=(qF/\pi\varepsilon)^{1/2},$$

$$\Gamma_n=\exp(E_{\mathrm{PF}}/kT)+\int_{E_{\mathrm{PF}}/kT}^{(E_{\mathrm{gap}}-E_t)/kT}\times\exp\{z-\alpha z^{3/2}[1-(E_{\mathrm{PF}}/zkT)^{5/3}]\}dz,$$

$$\Gamma_p=1+\int_0^{E_t/kT}\exp\{z-\alpha[(E_{\mathrm{gap}}/kT)^{3/2}-(E_{\mathrm{gap}}/kT-z)^{3/2}]\}dz,$$

$$\alpha=8\pi[2m^*(kT)^3]^{1/2}/3qhF,$$

where E_{PF} is the potential-barrier reduction due to the PF effect, q is the electron charge, F is the applied electric field, ε is the dielectric constant of Si, Γ_n expresses the enhancement for electron emission due to PF (the first term) and TAT (the second term), Γ_p expresses the electron-trap enhancement by TAT, E_{gap} is the band gap of Si, and h is Planck's constant. We estimated that the electron emission from the defect level is enhanced 320 times at 0.5 MV/cm, as shown in Fig. 3(c). Therefore, the previous simulation of J (the normal curve) should be revised to appear like the "with PF+TAT" curve in Fig. 3(a). As a result, we expect the JLC to be over 100 fA for the bad state, which is a reasonable level to account for the VRT.

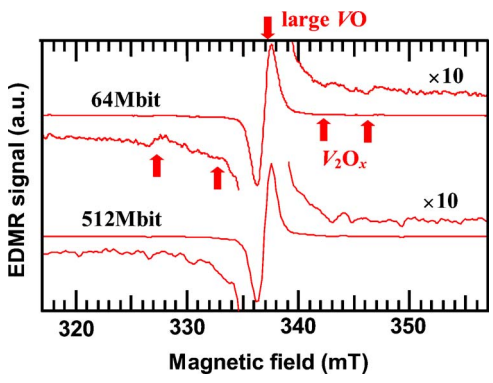

FIG. 2. (Color online) Typical EDMR spectra measured for JLCs of 64 and 512 Mbit samples (80 nA at V_R=9.6 V and 55 nA at V_R=5.9 V, respectively) at room temperature with the magnetic field parallel to [011] axis.

The VRT defect should be bistable with activation energies (E_g and E_b) of approximately 1 eV. We propose here a model of strain-induced bistability for the small VO complexes (V_2O_x). They are formed as rare defects because their EDMR signal intensity was very small. This corresponds to previous findings that VRT bits appear with a small probability.[1,2,5] For the case of V_2O_x under a strong lattice strain, one orientation becomes more stable than the other, as was demonstrated in electron paramagnetic resonance experiments under artificial strain.[14] Using convergent beam electron diffraction, we observed strain of over 100 MPa in the relevant devices.[8] We deduced that the good and bad states correspond to two orientations, like those shown in Fig. 4. The reorientation of V_2O_x is similar to that of divacancy (V_2), with an estimated activation barrier of $\sim$1.4 eV.[14] This barrier is compatible with that observed for the VRT.

The above discussion implies that the impact of the V_2O_x complex on the VRT depends strongly on F and strain (namely, ΔE). This may explain (1) why the VRT exhibits a very wide variation, such that RT is changed by several percent to 1–2 orders of magnitude[1,5] (because the JLC varies in the above range depending on F and ΔE) and (2) why the VRT is affected by the packaging and thermal processes[5,6] (because they change the distribution of strain in a device).

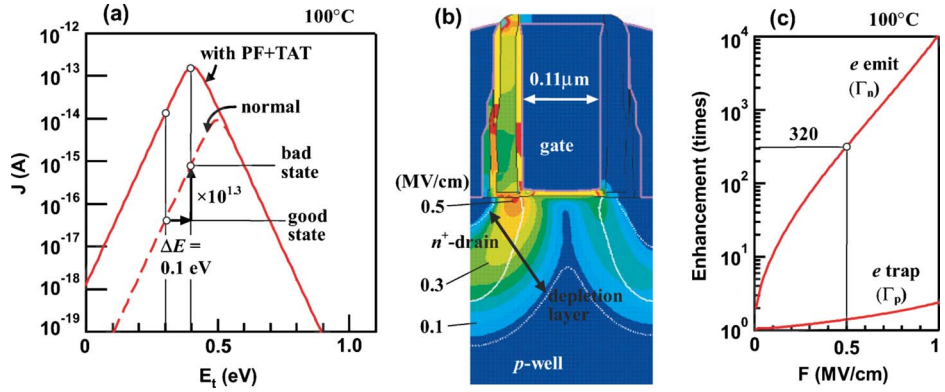

FIG. 3. (Color online) (a) Simulated junction leakage current J from defect level E_t, assuming that electron and hole capture cross-sections (C_n and C_p, respectively, in cm^2) are $C_n=1\times10^{-14}$, $C_p=1\times10^{-15}$ for "normal" curve, $C_n=320\times10^{-14}$, and $C_p=1\times10^{-15}$ for "with PF+TAT" curve. Good (bad) state is set to $E_V+0.3$ (0.4) eV. (b) Simulated two-dimensional electric field distribution in 256/512 Mbit DRAM cell under normal charge retention operation. (c) Enhancement factors for electron emission and trap rates due to Poole-Frenkel effect (PF) and trap assisted tunneling effect (TAT).

The role of the large *V*O complexes on the VRT phenomenon is not clear at present. However, their DBs can interact with hydrogen atoms (H) and potentially cause H-related phenomena. Recent experiments suggested a correlation between H and the RT degradation observed at a relatively low $T(\leqslant 250\,^{\circ}\mathrm{C})$.[6] They also suggested that VRT is correlated with H.[5] The *V*O complexes may be related to these H-related phenomena.

In summary, using EDMR, we observed that the *V*O complexes were present in all the DRAM cells we investigated. Numerical simulation showed that a single bistable *V*O defect located in the near surface gate-drain boundary can behave as a VRT defect.

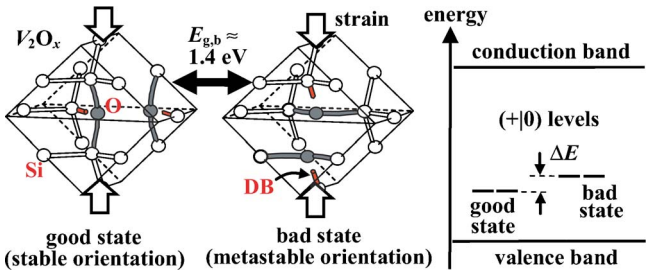

FIG. 4. (Color online) Model for bistable V_2O_x defect under strain: (a) Atomic view and (b) energy-level view.

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