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Experimental and theoretical analyses of gate oxide and junction reliability for 4H-SiC MOSFET under short-circuit operation

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In this study, the experimental evaluation and numerical analysis of the short-circuit capability of the 1200 V SiC MOSFET with a thin gate oxide layer were carried out. Two different failures, including the gate oxide breakdown and the thermal runaway of the device caused by the high gate electric field and elevated lattice temperature, were initially investigated and their critical temperature points for two failure modes were accurately extrapolated by solving the thermal diffusion equation; the obtained results are in good agreement with simulation results. It was confirmed that short-circuit robustness depends not only on thermal properties of the material but also on dimensional parameters of the device and that the heat is the dominant factor that causes device failure during short-circuit transient.

1. Introduction

Owing to the wide band gap and large dielectric constant of silicon carbide material, the SiC device exhibits electrical properties and reliability superior to those of the Si device, such as the thin drift layer, the lower on-state resistance, the extremely high operation temperature, and so on. Therefore, a low conduction loss, as well as a small lattice temperature fluctuation, can be realized when the device is normally switched on. However, the device will be irreversibly damaged after ten microseconds of the occurrence of short-circuit, caused by the on-state of both devices in the upper and lower arms of application circuit. Moreover, the short-circuit withstand time is crucial for the protection circuit; thus, the short-circuit capability of the device must be carefully considered and evaluated.

Several papers about the short-circuit capability were reported and its destructive mechanism was also elaborated for power devices.[1-10] However, the short-circuit capability has not been studied for the SiC device with a relatively thin gate oxide layer.[11-19] In this study, using the thermal diffusion equation, the short-circuit capability of the 1200 V SiC MOSFET with a gate oxide of 40 nm thickness was characterized at room temperature. Two different failures, including the gate oxide breakdown and thermal runaway of the device caused by the high gate electric field and elevated lattice temperature, were initially investigated. Moreover, the maximum surface temperatures of the SiC MOSFET in two failure modes were extrapolated by simulation and mathematical methods.

2. Evaluation of short-circuit capability of tested SiC MOSFET

The short-circuit capability of a SiC MOSFET is evaluated using a test bench as shown in Fig. 1. The used device under test (DUT) is one chip in the package of TO247 with a rated current of 19 A. The energy of the test bench is supplied by a series of capacitors with voltages ranging from 0 to 600 V. The device operation is controlled by a gate driver with voltages of 18 and -5 V to turn-on and turn-off, respectively. Because the effect of gate resistance on the short-circuit capability can be ignored, the gate resistance connected to the gate driver is fixed at 47 Ω.

Figures 2(a) and 2(b) exhibit the drain current and gate voltage waveforms of the 1200 V/19 A SiC MOSFET with a 400 V DC bus, respectively. It is obvious that the drain current increases promptly and the device enters from the linear region to the active region until achieving its saturation current at the initial pulse time. After that, the drain current decreases from 117 to 51.6 A owing to the degradation of the carrier mobility constrained by the elevated lattice temperature. The drain current will become horizontal when the

device tends to fail during short-circuit transient.[20] Similarly to that of the Si IGBT, the tail current of SiC MOSFET appears at the end of transient and remains for four microseconds after turn-off. Moreover, the gate voltage gradually shows a recessive trend when the short-circuit transient is increased.

Generally, the thickness of the gate oxidation layer in both Si and SiC power MOSFETs ranges from 30 to 100 nm.[21] The most prominent oxide degradation mechanism in SiC is the Fowler-Nordheim (FN) tunneling and Poole-Frenkel (PF) emission effect,[22] leading to a leakage current, especially at the high gate electric field and ambient temperature, which can be assessed by time-dependent dielectric breakdown (TDDB) test.[23] It has been also demonstrated that a substantial increase of FN current occurs as the temperature rises up to 523 K, and that the effective barrier height between SiC and oxide decreases to 2.38 eV as the temperature rises up to 573 K.[21,24] Therefore, the high temperature will affect the reliability of gate oxide prominently.

On the basis of the same parameters with the tested SiC MOSFET, Figs. 3(a) and 3(b) show the simulation results about the electric field in gate oxide and lattice temperature profiles at the interface of SiC and oxide (y=0 μm) at four points of short-circuit transient as shown in Fig. 2(a). When the gate voltage increases from 0 to 18 V, the electric field in gate oxide gradually increases to the maximum point, as shown in point A to C in Fig. 3(a). It is evident that the maximum point of the electric field experiences a migration process from the JFET region to the source region. However, there is still a monotonic difference in electric field in the JFET region between points C and D even at the same gate voltage bias. This is because with increasing short-circuit transient, the lattice temperature in the device increases. Thus, more holes are produced and concentrate in the JFET region, which could relieve the electric field in gate oxide at a high lattice temperature. At point D with a high electric field of 4.3 MV/cm and a high lattice temperature of 844 K, as shown in Fig. 3(b), the ruggedness between the gate and the source terminal cannot be ignored. This directly explains the degradation of gate voltage from 18 to 16.3 V, as shown in Fig. 2(b).

The impedances of the three terminals of the failure device between the gate, drain and source (R_{gs}, R_{gd}, and R_{ds}) are measured, to be 2.6, 8.6 M and ∞ Ω, respectively. The results indicate that the gate-source terminal of the device is finally shorted and the irreversible breakdown of gate oxide occurs.[25,26] In addition, the breakdown voltage of the failure device remains to be around 1218 V at a drain leakage current of 0.2 mA, as shown in Fig. 4. This breakdown voltage decreases slightly compared with that of the fresh device because the generation of holes in the top JFET area at high temperatures causes the

electric field centralization at the p-well / n drift junction. Such results suggest that failure does not exist in the drain-source terminal, but in the gate-source terminal.[27] The short-circuit energy during the period of 16 μs is determined to be 12.8 J/cm^2 from equation

$$E_{SC} = \int_0^{t_{SC}} VIdt \ . \quad (1)$$

To further investigate the device reliability during short-circuit transient, the test is performed under harsher conditions. Figures 5(a) and 5(b) show other short-circuit current and gate voltage waveforms at room temperature, with a 600 V DC bus. Different from the former case, the drain current is no longer under gate driver control and eventually thermal runaway occurs when the short-circuit withstand time is prolonged from 5 to 8 μs. The delay time can also be observed after the device switches off as shown in Fig. 5(a). Moreover, the gate voltage gradually decreases from 18 to 15.9 V, which is higher than that of the gate-source terminal breakdown mode. Likewise, the short-circuit energy is derived to be 19.4 J/cm^2 by using Eq. (1).

In addition, Figs. 6(a) and 6(b) reveal the simulation results about the electric field in gate oxide and lattice temperature profiles at the interface of SiC and oxide (y=0 μm) with a 600 V DC bus. Different from the previous case, the variation in electrical field between points C and D is more obvious than that of the device with a 400 V DC bus. This is because the number of holes markedly increases in the top of JFET area as the lattice temperature rises to around 1500 K, as shown in Fig. 6(b). The holes and electrons induced by high temperature in the top JFET and source areas somewhat affect the electric field in the oxide. Moreover, the ultra high lattice temperature not only affects the electric field in the oxide but also increases the intrinsic carrier concentration. Once those two parameters exceed the critical condition of the device, the device will fail, similar to the results in Fig. 5.

After failure, the impedances of the three terminals between the gate, drain and source (R_{gs}, R_{gd}, and R_{ds}) are measured, to be 0.2, 0.6 and 0.6 Ω, respectively. These results indicate that the three terminals are completely damaged at high lattice temperatures owing to the heat generated in the device.

As discussed above, the failure modes with different short-circuit energies can be actually divided into two types. In a relatively low short-circuit energy situation, the gate-source terminal is prone to be shorted owing to the gate oxidation layer degradation caused by FN tunneling and PF emission leakage current effects, while all the three terminals of the device are destroyed by large short-circuit energies.

3. Mathematical analysis of lattice temperature for two failure modes during short-circuit transient

Owing to the absence of the loading component in the short-circuit mode, the drain current, related to the temperature, is only confined by the saturation current. The short-circuit energy, thus, can be expressed by

$$P_{\mathrm{SC}} = J_{\mathrm{sat}} \cdot V \ . \tag{2}$$

Moreover, the thermal diffusion equation, which indicates the dependence of short-circuit withstand time on coordination and time, is a rigorous thermodynamic model that can be used to obtain the rising temperature solution during short-circuit transient. In practice, the direction of thermal diffusion is essentially from the surface of the die to the bottom of the case owing to the presence of a heat sink. Thus, the vertical direction of the device is critical to be considered. The temperature distribution can be simplified and solved as

$$\rho \cdot c \cdot \frac{\partial T_{(z,\, t_{\mathrm{SC}})}}{\partial t} = \nabla^2 (\kappa \cdot T) + \frac{P_{\mathrm{SC}} t_{\mathrm{SC}}}{V_{\mathrm{volume}}} \ , \tag{3}$$

where, c and κ are the heat capability, and thermal conductivity, respectively. V_{volume} is the thermal volume, which includes the parameters of the active area and n drift layer. The basic SiC material parameters are listed in Table I. The temperature distribution solution based on Eq. (3) can be expressed as[29)]

$$T(z, t_{\mathrm{SC}}) = \Delta T e^{-(Z/\sqrt{D_{\mathrm{SiC}} t_{\mathrm{SC}}})} + T_{\mathrm{A}} \ , \tag{4}$$

$$\Delta T = \frac{E_{\mathrm{SC}}}{A V_{\mathrm{volume}} \rho c} \ , \tag{5}$$

where, T_{A} is the case temperature at the initial time of short-circuit transient, ρ is the material density for SiC, and Z is the thickness of the device. The constant A is determined to be the fitting parameter by taking thermal diffusion parameters into account, which are 10.8 and 7.71 for those two failure situations, respectively.[30,31)]

Equations (4) and (5) show that the short-circuit capability of the SiC MOSFET depends not only on thermal properties of the material but also on the dimensional parameters of the device. Increasing the drift layer thickness and the active area can effectively improve the short-circuit capability.

Subsequently, the temperature distribution profile with 300 μm wafer thickness is shown in Fig. 7. It can be seen that the maximum temperature is located at the upper surface with an exponential decay profile. The maximum temperatures are 848 and 1463 K, for

short-circuit withstand times of 16 and 8 μs, with DC bus voltages of 400 and 600 V, respectively. The theoretical analysis results are in good agreement with the simulation results, as shown in Fig. 3(b) and Fig. 6(b), which can accurately extrapolate the critical temperature for two failure modes including the gate oxide breakdown and thermal runaway of the device with different short-circuit energies.

4. Conclusions

In this study, the maximum lattice temperatures for two failure modes based on the short-circuit test for a 1200 V/19 A SiC MOSFET were investigated by experimental and numerical methods. Analytical formulas revealed that short-circuit capability of the SiC MOSFET depends not only on thermal properties of material but also on the dimensional parameters of the device. Moreover, the maximum lattice temperature is the dominant factor that causes device failure.

All the experimental, mathematical, and simulation results show that the SiC MOSFET has a superior thermal reliability and a high quality of short-circuit capability, which make it the best candidate for power application. Consequently, whole analysis models can be used for a bench mark of ruggedness for the SiC MOSFET.

References

1) N. Iwamuro, A. Okamoto, S. Tagami, and H. Motoyama, IEEE Trans. Electron Devices **38,** 303 (1991).
2) S. Clemente, IEEE Trans. Power Electron. **8,** 337 (1993).
3) A. Ammous, B. Allard, and H. Morel, IEEE Trans. Power Electron. **13,** 12 (1998).
4) M. Trivedi and K. Shenai, IEEE Trans. Electron Devices **45,** 313 (1998).
5) A. Benmansour, S. Azzopardi, J. C. Martin, and E. Woirgard, Microelectron. Reliab. **46,** 1778 (2006).
6) S. Lefebvre, Z. Khatir, and F. Saint-Eve, IEEE Trans. Electron Devices **52,** 276 (2005).
7) Z. Khatir, S. Lefebvre, and F. Saint-Eve, Microelectron. Reliab. **47** 422 (2007).
8) J. Yamashita, E. Haruguchi, and H. Hagino, Proc. Int. Symp. Power Semiconductor Devices and ICs, 1994, p. 45.
9) N. Iwamuro, Y. Harada, T. Yamazaki, N. Kumagai, and Y. Seki, IEEE Electron Device Lett. **16,** 399 (1995).
10) F. Hille, F. Umbach, T. Raker, and R. Roth, Proc. Int. Symp. Power Semiconductor Devices and ICs, 2010, p. 33.
11) X. Huang, G. Wang, Y. Li, A. Q. Huang, and B. Jayant Baliga, Applied Power Electronics Conf. Expo, 2013, p. 197.
12) R. Letor and G. C. Aniceto, IEEE Trans. Ind. Appl. **31**, 234 (1995).
13) T. Basler, R. Bhojani, J. Lutz, and R. Jakob, Proc. Int. Symp. Power Semiconductor Devices and ICs, 2013, p. 277.
14) R. S. Chokhawala, J. Catt, and L. Kiraly, IEEE Trans. Ind. Appl. **31,** 256 (1995).
15) C. Abbate, G. Busatto, and F. Iannuzzo, Microelectron. Reliab. **51,** 1767 (2011).
16) N. Boughrara, S. Moumen, S. Lefebvre, Z. Khatir, P. Friedrichs, and J.-C. Faugières, IEEE Electron Device Lett. **30**, 51 (2009).
17) A. Castellazzi, T. Funaki, T. Kimoto, and T. Hikihara, Microelectron. Reliab. **52**, 2414 (2012).
18) J. A. Schrock, W. B. Ray, K. Lawson, A. Bilbao, S. B. Bayne, S. L. Holt, L. Cheng, J. W. Palmour, and C. Scozzie, IEEE Trans. Power Electron. **30**, 2891 (2015).
19) K. Sun, H. Wu, J. Lu, Y. Xing, and L. Huang, IEEE Trans. Power Electron. **29**, 2229 (2014).
20) Z. Wang, X. Shi, L. M. Tolbert, F. Wang, Z. Liang, D. Costinett, and B. J. Blalock, IEEE Trans. Power Electron. **31**, 1555 (2016).
21) R. Singh and A. R. Hefner, Solid-State Electron. **48,** 1717 (2004).

22) M. Sometani, D. Okamoto, S. Harada, H. Ishimori, S. Takasu, T. Hatakeyama, M. Takei, Y. Yonezawa, K. Fukuda, and H. Okumura, J. Appl. Phys. **117**, 024505 (2015).
23) L. C. Yu, G. T. Dunne, K. S. Matocha, K. P. Cheung, J. S. Suehle, and K. Sheng, IEEE Trans. Device Mater. Reliab. **10**, 418 (2010).
24) A. K. Agarwal, S. Seshadri, and L. B. Rowland, IEEE Electron Device Lett. **18**, 592 (1997).
25) T.-T. Nguyen, A. Ahmed, T. Thang, and J.-H. Park, IEEE Trans. Power Electron. **30**, 2445 (2015).
26) Y.-C. Yeo, T.-J. King, and C. Hu, IEEE Trans. Electron Devices **50**, 1027 (2003).
27) A. Agarwal, H. Fatima, S. Haney, and S.-H. Ryu, IEEE Electron Device Lett. **28**, 587 (2007).
28) H. Yano, N. Kanafuji, A. Osawa, T. Hatayama, and T. Fuyuki, IEEE Trans. Electron Devices **62**, 324 (2015).
29) B. J. Baliga, *Fundamentals of power semiconductor devices* (Springer, New York, 2008), p. 960.
30) T. Shoji, A. Soeno, H. Toguchi, S. Aoi, Y. Watanabe, and H. Tadano, Jpn. J. Appl. Phys. **54**, 04DP03 (2015).
31) T. Shoji, J. Saito, and M. Ishiko, Denki Gakkai Ronbunshi. C **130**, 939 (2010) [in Japanese].

Figure Captions

Fig. 1. (Color online) Schematic of short-circuit test for tested SiC MOSFET.

Fig. 2. (Color online) (a) Experimental results of the time dependence of drain current waveforms with maximum short-circuit withstand time of 16 μs and 400 V DC bus. (b) Experimental results of degradation of gate voltage with maximum short-circuit withstand time of 16 μs and 400 V DC bus.

Fig. 3. (Color online) (a) Simulation results of electric field profile in gate oxide during four points of short-circuit transient for SiC MOSFET with gate oxide of 40 nm, maximum short-circuit withstand time of 16 μs, and 400 V DC bus. (b) Simulation results of lattice temperature profile during four points of short-circuit transient for SiC MOSFET at y=0 μm.

Fig. 4. (Color online) Experimental results of breakdown voltage between gate oxide failure device and fresh device.

Fig. 5. (Color online) (a) Experimental results of the time dependence of drain current waveforms with maximum short-circuit withstand time of 8 μs, and 600 V DC bus. (b) Experimental results of degradation of gate voltage with maximum short-circuit withstand time of 16 μs and 600 V DC bus.

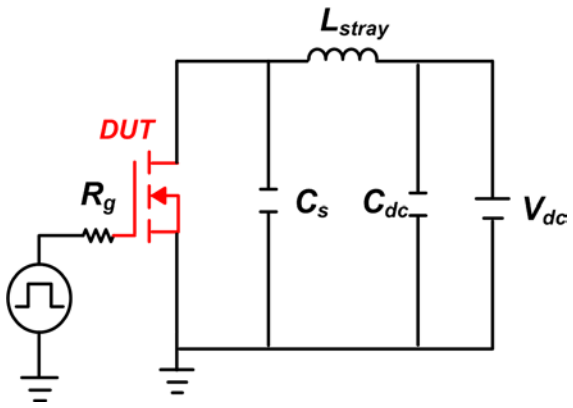
Fig. 6. (Color online) (a) Simulation results of electric field profile in gate oxide during four points of short-circuit transient for SiC MOSFET with gate oxide of 40 nm, maximum short-circuit withstand time of 8 μs and 600 V DC bus. (b) Simulation results of lattice temperature profile during four points of short-circuit transient for SiC MOSFET at y=0 μm.

Fig. 7. (Color online) Calculation of the temperature distribution profile for different test conditions.

Table I. Thermal characteristics of SiC.[30)]

Thermal capacity c	0.67 $J \cdot g^{-1} \cdot K^{-1}$
Thermal conductivity κ	4.5 $W \cdot cm^{-1} \cdot K^{-1}$
Density of SiC materiral ρ	3.21 g/cm^3
Thermal diffusivity D	2.21 cm^2/s

Fig.1. (Color Online)



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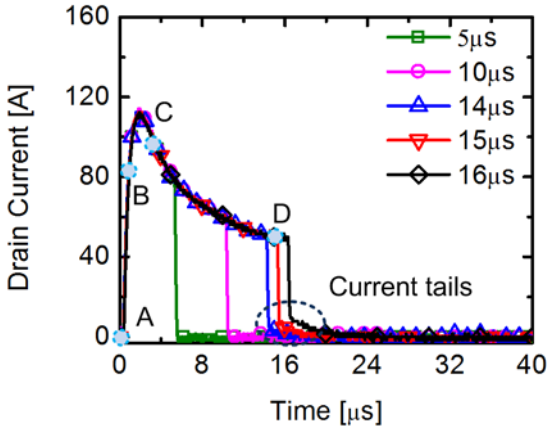

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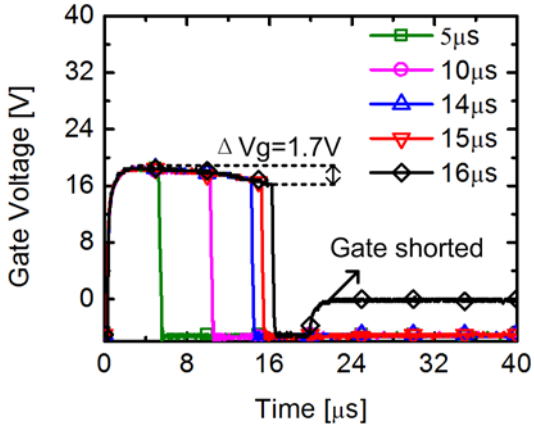

(b)

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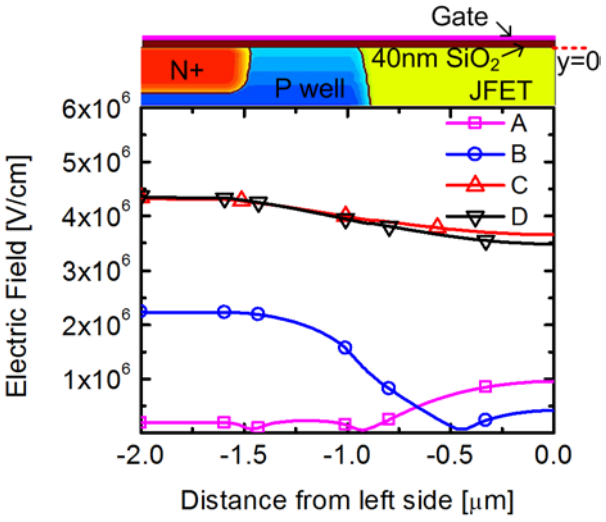

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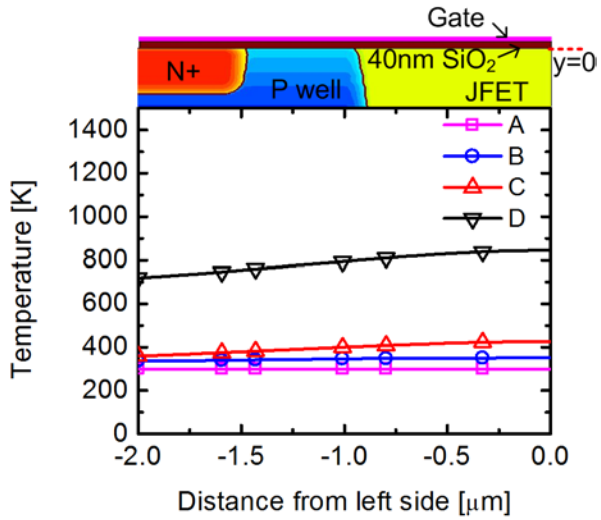

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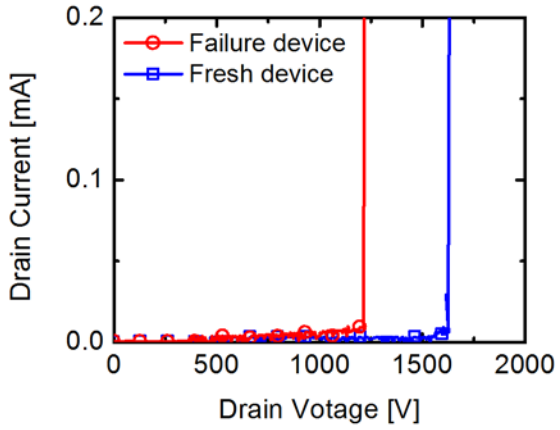

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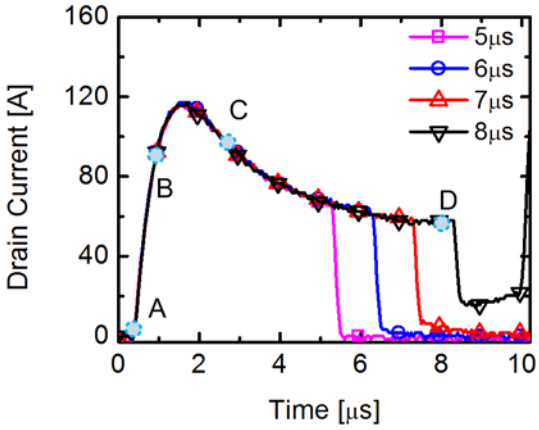
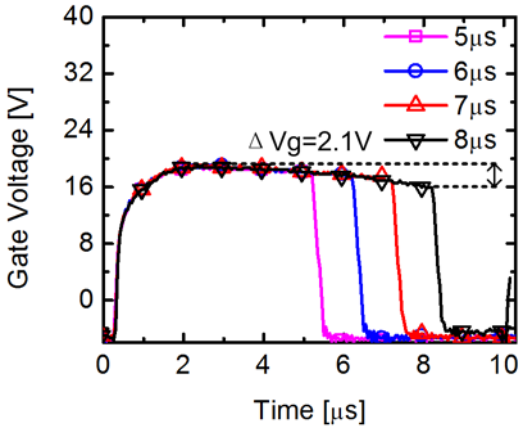


(a)



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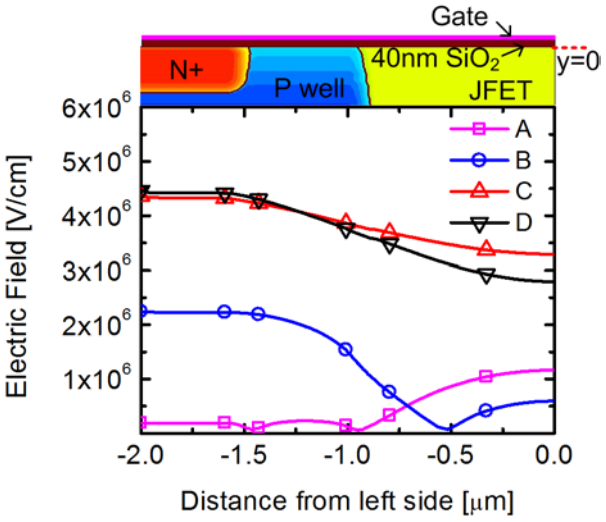

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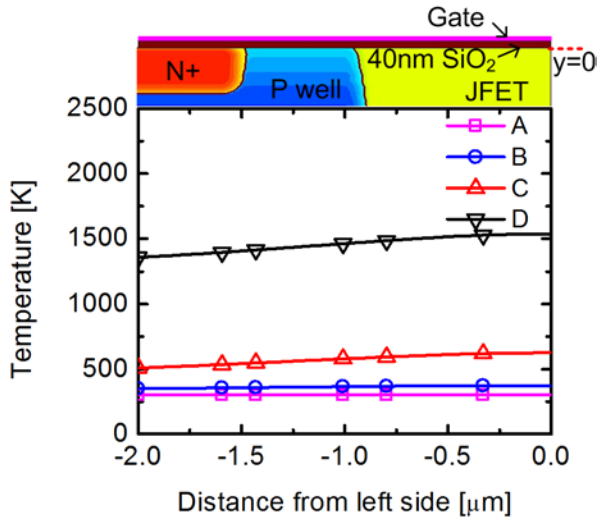

(b)

Fig.7. (Color Online)