Time-dependent dielectric breakdown (TDDB) distribution in n-MOSFET with HfSiON gate dielectrics under DC and AC stressing

Time-dependent Dielectric Breakdown (TDDB) Distribution in n-MOSFET with HfSiON Gate Dielectrics under DC and AC Stressing

[1, 3] Izumi Hirano, [1] Yasushi Nakasaki, [2] Shigeto Fukatsu, [2] Masakazu Goto, [2] Koji Nagatomo,

[2] Seiji Inumiya, [2] Katsuyuki Sekine and [1] Yuichiro Mitani and [3] Kikuo Yamabe

[1] Corporate Research & Development Center, Toshiba Corporation

[2] Semiconductor and Storage Products Company, Toshiba Corporation

8 Shinsugita-cho, Isogo-ku Yokohama 235-8522, Japan

[3] University of Tsukuba, 1-1-1 Tennodai, Tsukuba, Ibaraki 305-8572,Japan

Phone: +81-45-770-5990 Fax: +81-45-770-4113 E-mail: izumi3.hirano@toshiba.co.jp

Abstract

This paper discusses time-dependent dielectric breakdown (TDDB) in n-FETs with HfSiON gate stacks under various stress conditions. It was found that the slope of Weibull distribution of T_{bd}, Weibull β, changes with stress conditions, namely, DC stress, unipolar AC stress and bipolar AC stresses. On the other hand, the time evolution component of stress-induced leakage current (SILC) was not changed by these stresses. These experimental results indicate that the modulation of electron trapping/de-trapping and hole trapping/de-trapping by stress condition changes the defect size in high-k gate dielectrics. Therefore, the control of injected carrier and the characteristics of trapping can provide the steep Weibull distribution of T_{bd}, leading to long-term reliability in scaled CMOS devices with high-k gate stacks.

Introduction

Downscaling of metal-oxide-semiconductor field-effect transistor (MOSFET) requires the implementation of a high-k dielectric with a metal gate stack to reduce power consumption.[1] Hf-based dielectrics have emerged as among the most promising high-k gate dielectric materials for alternative dielectrics, in view of their relatively high permittivity and high thermodynamic stability on Si.[2-4] In addition to the many integration challenges arising from the introduction of deposited oxides as a replacement for thermally grown SiO_2, new reliability concerns have emerged.

Time-dependent dielectric breakdown (TDDB) is one of the most serious concerns regarding the practical use of high-k gate stacks and its mechanism has been widely discussed.[5-18] In particular, the statistical distribution of TDDB is important from the viewpoint of determining device lifetime. This is because the ULSI consists of over one billion transistors and the device reliability cannot be decided only by average characteristics. In general, the lifetimes of gate oxide reliability at ppm-order cumulative failure are predicted from the extrapolation of experimental results, which are measured under accelerated conditions (i.e. at higher temperature and stress voltage than actual operating conditions).

Wide distribution of T_{bd} (i.e. small Weibull β) is a serious concern from the viewpoint of device reliability, including yield. Therefore, not only the average T_{bd} but also its distribution should be considered with a view to improving the dielectric breakdown characteristics of high-k gate dielectrics. Furthermore, not only the lifetime under DC stress but also that under AC stress is important in practical use.

It was reported recently that the shape parameter of Weibull plot, β, of time to breakdown (T_{bd}) of high-k was smaller than that of SiO_2 with similar physical thickness.[19, 20] In addition, the dependence of TDDB characteristics and the slope of Weibull distribution on bias polarity

has also been reported.[21] Furthermore, it is reported that the Weibull β of T_{bd} strongly depends on gate electrode materials for metal gate/HfSiON stacks.[22, 23]

In the present work, the n-MOSFET TDDB distributions for HfSiON gate dielectrics under both DC and AC stresses were studied. It was found that the distribution of T_{bd} under bipolar AC stress becomes steeper than that under DC stress. On the other hand, the averages of T_{bd} and SILC characteristics were almost the same under DC stress and bipolar AC stress. From these experimental results, it is proposed that the ratio of injected carrier components, that is, the ratio of injected hole to electron in high-k, can change the defect size, leading to modulation of the Weibull distribution.

EXPERIMENT

A flow diagram of MOSFET fabrication and the cross-section of the MOSFET used in this study are shown in Figure 1. HfSiO films were directly deposited on Si(100) substrates treated with diluted HF by metal-organic chemical vapor deposition (MOCVD). Post-deposition annealing (PDA) was carried out in O_2 ambient at $600^{o}C$ for 240 sec for interface engineering. Plasma nitridation was used for nitrogen incorporation in the HfSiO films and post-nitridation annealing (PNA) was carried out in $O_2/N_2 = 0.1\%$ ambient at 1000 ^{o}C for 10 sec. Hf concentration was about 50% (Hf/(Hf+Si)) and nitrogen concentration was about 20 atom %. Typical areas of the devices were 10^{-7} cm^2. TDDB measurements were performed for n^{+}poly-Si/n-FETs and carrier separation measurements were carried out for both n^{+}poly-Si/n-FETs and n^{+}polySi/p-FETs. From transmission electron microscope(TEM) image, physical thickness of HfSiON gate dielectrics is around 4 nm and SiO_2 interface layer is around 1 nm. Effective oxide thickness (EOT) of around 1.5 nm is obtained by Cg-Vg measurement.

TDDB measurements were performed at $125^{o}C$ under DC stress and AC stress. 63%

T_{bd} and its distribution was obtained from the data with at least 25 samples. Figure 2 shows the stress conditions of DC stress, unipolar AC stress and bipolar AC stresses. Table 1 shows the parameters: cycle stress time, $T1$ for inversion stress time, $T2$ for accumulation or zero-voltage stress time, and stress voltage, $Vgst_1$ for inversion stress and $Vgst_2$ for accumulation stress.

The electron and hole currents under each stress were investigated by using the carrier separation measurement, as shown in Figure 3. The carrier separation results of n$^+$poly-Si/n-FET under positive bias and n$^+$poly-Si/p-FET under negative bias correspond to inversion and accumulation condition for n$^+$poly-Si/n-FET, respectively.

In order to study the defect generation phenomena, stress-induced leakage current (SILC) under each stress was also examined. Figure 4 shows the SILC measurement flow. First initial Cg-Vg measurement and initial Ig-Vg measurement is carried out. Then DC or AC stress is applied and after that stressed Cg-Vg measurement and stressed IV measurement is carried out. From initial and stressed Cg-Vg measurement, flat-band voltage shift (ΔVfb) by applied stresses is obtained. SILC is estimated as ΔIg = Ig at Vg-Vfb=1V - Ig$_{initial}$ at Vg-Vfb=1V. Here, the influence of charge trap on Vg shift is removed by rectifying monitor voltage of SILC by Vfb. Delay time after stress is around 2 sec because Cg-Vg measurement is performed between applied stress and SILC measurement. In this Cg-Vg and Ig-Vg measurement, Vg sweeps from -1 to 1. As a result, Vfb and SILC recover during negative bias. [24] SILC is partially relaxed for each stress condition.

RESULTS AND DISCUSSION

TDDB characteristics under DC and AC stresses

Figure 5 shows the typical time evolutions of gate leakage current (Ig) in n-MOSFETs under

DC stress, unipolar AC stress 1 and bipolar AC stress 1. Ig was measured at stress voltage. In Figure 5 (a), the horizontal axis shows the total time of stressing, including time of zero-voltage stress in unipolar stress or negative stress in bipolar stress. In Figure 5 (b), the horizontal axis shows the sum of stress time under application of positive stress. We determined the time at which current begins to increase as time to breakdown, T_{bd}, as indicated by arrow in Figure 5 (b), which corresponds to $Ig(t_{n+1})/Ig(t_n) > 1.03$ as a definition of breakdown. Using this criterion of breakdown, the good area scaling of Weibull distribution was observed, indicating that this criterion is a reasonable detection of first breakdown. In general, first breakdown is considered to result from a weak localized conductive path between the gate electrode and the substrate. This conductive path is formed by connecting the defects generated in dielectrics [25-27]. Based on this model, the statistics of soft breakdown can be described by Weibull distribution.

Figure 6 (a) and (b) show the Weibull plots of T_{bd} under DC stress, unipolar AC stress and bipolar AC stresses. Here, T_{bd} is the cumulative time of the positive Vg only. The Weibull function has an excellent fit to the experimental data for each stress. Table 2 shows the stress condition and 63% Tbd and Weibull β. Weibull β was estimated by fitting of T_{bd} for longer than 10 seconds in Figure 6. Since the first 10 seconds of stress for each stress condition is the same condition, the difference of T_{bd} within 10 seconds for each stress did not originate from different stress conditions. The values of Weibull β under unipolar AC stress were around 1 and almost the same value under DC stress. On the other hand, the values of β under bipolar stresses were larger than those under both DC and unipolar stress. Moreover, Weibull β under bipolar AC stress 3 shows the largest value, followed by that under bipolar AC stress 2 and that under bipolar AC stress 1; Weibull β increases with longer $T2$ of bipolar stress. 63% T_{bd} under DC stress and unipolar AC stresses are almost the same. On the other hand, T_{bd} distribution under bipolar AC stress is steeper than that under DC stress, although 63% T_{bd}

were almost the same under DC stress and bipolar stresses.

SILC characteristics under DC and AC stresses

To investigate the defect generation characteristics, we measured the stress-induced leakage current (SILC). To correct the shift of the flat-band voltage, both capacitance-voltage (Cg-Vg) and current-voltage (Ig-Vg) measurements were performed before and after stresses as shown in Fig. 4. SILC is related to the defect generated and has been explained in terms of trap-assisted tunneling mechanisms. Therefore, the time evolution of SILC has been used to monitor the degradation of dielectrics.

Figure 7 (a) shows the shift of Cg-Vg curves by trap generation under DC stress and Figure 7 (b) shows the change of the low field Jg - (Vg -*Vfb*) due to SILC under DC stress. In this case, positive shift of Cg-Vg curve by electron trap generation was observed. This electron trap may be hardly de-trapped by Cg-Vg measurement. Similar behaviors were observed under unipolar AC stress and bipolar AC stress. In order to eliminate the modulation of electric field under trapped electron due to applied stress, we use the *Vfb* by Cg-Vg measurement. Monitor voltage of SILC was Vg-Vfb=1V as indicated by dotted line in Fig.7 (b). From the results of Fig.7, the time evolution of SILC as shown in Fig.8 was estimated.

Figure 8 shows the time evolution of SILC under DC stress, unipolar AC stress 2 and bipolar AC stress 3. SILC can be described by power-law dependence as SILC $= A \cdot t^{\alpha}$. Here, almost the same value of α, around 0.6, was obtained for each stress, even though the β showed very different values.

The origin of different Weibull β due to stress conditions

We discuss the origin of correlation between Weibull β and stress conditions. In order to separate the electron current and hole current under each stress, we performed the carrier separation measurement. Figure 9 shows the carrier separation results of n[+]poly-Si/n-FET under positive bias and n[+]poly-Si/p-FET under negative bias, corresponding to inversion and accumulation condition, respectively, in n[+]poly-Si/n-FET. Under $Vgst_1$, as shown in Fig. 9 (a), the electron current (J_g) was about three orders of magnitude higher than hole current (J_{sub}). These electrons are injected from inversion layer to poly-Si gate electrode. Injected electrons immediately cause impact ionization and, consequently, create electron-hole pairs. Generated holes tunnel back into the oxide. These hole current are observed as J_{sub}. [28] In addition, electrons are tunneling from the valence band to the gate. While electrons are tunneling from the valence band to the gate, they create holes that are collected by the p-type substrate. These holes were also observed as J_{sub}. [29]

Leakage current under $Vgst_2$ of n[+]poly-Si/n-FET corresponds to that of n[+]poly-Si/p-FET under $Vgst_2$ - ΔVfb (ΔVfb = Vfb(n[+]poly-Si/n-FET) - Vfb(n[+]poly-Si/p-FET)). The hole current (J_{sd}) was about an order of magnitude higher than electron current (J_{sub}) under $Vgst_2$ - ΔVfb of n[+]poly-Si/p-FET. Therefore, holes are intentionally injected from accumulation layer to gate electrode by applying the accumulation stress, $Vgst_2$, as shown in Fig. 9 (b). If the stress time of $Vgst_1$ is constant, the larger J_{hole} / $J_{electron}$ can be realized by applying the longer stress time of $Vgst_2$. Here, we have confirmed that the devices are not degraded by the voltage of $Vgst_2$ because the $Vgst_2$ is small enough. From these results, we calculated the total ratio of injected holes to injected electrons for each stress condition as (J_{hole} / $J_{electron}$)$_{total}$ = (J_{hole} / $J_{electron}$)$_{vgst1}$ + (J_{hole} / $J_{electron}$)$_{vgst2}$.

Figure 10 shows the correlation between β and (J_{hole} / $J_{electron}$)$_{total}$ under each stress condition. Strong correlation was observed, that is, Weibull β monotonically increases with (J_{hole} / $J_{electron}$)$_{total}$. Since the Weibull β under DC stress and unipolar stresses were almost the same

as shown in Figure 5, the injected carriers under *Vgst2* rather than relaxation of charges between pulses strongly influence Weibull distribution of T_{bd} in HfSiON. The carrier ratio controlled by bias polarity must dominate the Weibull β. On the other hand, it has been reported that the relaxation of charges under AC stress influences TDDB behavior. [30] In this study, it was found that the relaxation of charges and trapped holes can both influence TDDB.

We discuss the model for the modulation of β due to the ratio of injected carriers and discharging of carriers. Here, we account for the Weibull distribution of T_{bd} by using the percolation model.

The percolation model has been reported recently and the slope of Weibull distribution was explained by using this model. Based on this model, a simpler model, namely, a cell-based model, has been proposed. [31] In this model, it is assumed that the gate oxide is divided into cubic cells of volume (a_0^3) and one cell changes to be conductive with a probability. The breakdown can take place when all the cells in one column are conductive. Here, A_{ox} is the gate oxide area, a_0 is a conductive cell size, and t_{ox} is the oxide thickness. In this cubic lattice, we can distinguish $N = A_{ox}/a_0^2$ column of area (a_0^2) and thickness (t_{ox}), with each column being subdivided in $n = t_{ox}/a_o$ cell. If λ is the probability of each cell being conductive, the probability that all the cells in one column are conductive is λ^n. The breakdown can occur when one of its columns is fully conductive. Therefore, the device failure cumulative distribution is given by $1 - F_{BD}(\lambda) = (1-\lambda^n)^N$, where F_{BD} is the cumulative breakdown distribution. If the breakdown is triggered, $\lambda << 1$ is satisfied. In this case, $\ln(1-\lambda^n)$ can approximate $-\lambda^n$. Under these assumptions, Weibull distribution (W_{BD}) becomes

$$W_{BD} = \ln\left(-N \ln(1-\lambda^n)\right)$$

$$= \ln(N) + n\ln(\lambda) \qquad (1)$$

Since $N = A_{ox}/a_o^2$ and $n = t_{ox}/a_o$, the breakdown distribution can be written as follows:

$$\ln[-\ln(1-F)] = \ln\left(\frac{A_{ox}}{a_0^2}\right) + \frac{t_{ox}}{a_0}\ln(\lambda(t)) \qquad (2)$$

Here, SILC is related to the generated defect and has been explained in terms of trap-assisted tunneling mechanisms. [32-34] Therefore, λ(t) is given by a well-known power law, as shown in eq.(3), and can be estimated by stress-induced leakage current (SILC).

$$\lambda(t) = \xi \cdot t^{\alpha} \propto SILC = A \cdot t^{\alpha} \qquad (3)$$

From eq.(1) and eq.(2), the Weibull β is described by eq.(4)

$$Weibull\beta = \alpha \cdot \frac{t_{ox}}{a_0} \qquad (4)$$

Therefore, under the constant oxide thickness, large β implies either large α or small a_0.

The result of Fig. 8 indicates that the change of β under different stress condition does not come from the change of α. Figure 11 shows the estimated a_0 by using values of α, Weibull β and t_{ox} obtained experimentally under each stress condition. These a_0 seem to decrease with increase of J_{hole} / $J_{electron}$ for different stress conditions. These results indicate that the ratio of injected carriers changes the defect size generated in HfSiON.

Figure 12 shows the schematic illustrations of the percolation model under high (J_{hole} / $J_{electron}$)$_{total}$ condition and low (J_{hole} / $J_{electron}$)$_{total}$ condition, corresponding to DC stress and bipolar stress. In the percolation model, breakdown occurs when the generated defects connect in the direction of thickness. From our experimental results shown above, when the J_{hole} / $J_{electron}$ is high, corresponding to bipolar AC stress, the generated defect size (a_0) is small and large amounts of generated defects bring on the breakdown. When the (J_{hole} / $J_{electron}$)$_{total}$ is low, corresponding to DC stress, the generated defect size (a_o) is large and the small amounts of generated defects bring on the breakdown. On the other hand, almost similar 63% T_{bd} and similar SILC under DC stress, unpolar AC stresses and bipolar AC stresses were observed as shown in Table 2 and Fig.8. One of the possible defect generation mechanisms is

as follows. In this study, estimated SILC (ΔIg/Ig) was reflected the defect size because generation of a large defect causes the large increase of Ig. As result, low generation rate of a large defect and high generation rate of a small defect causes almost the same SILC. Under DC stress or unipolar AC stress, large defect is generated at a low-rate. Under bipolar AC stress, small defect is generated at a high-rate. It can explain that the Weibull distribution changes with stress sequence regardless of almost the same T_{bd} and the same SILC. Although more experiments and calculations are still required, we infer the mechanism for the modulation of generated defect size as follows.

From the first-principle calculations,[35] it was reported that the capture of two holes by oxygen vacancy (Vo) causes the structural relaxation in HfSiO. We think that this structural relaxation corresponds to defect generation in the percolation model.

It was also reported that the electron capturing by Vo promotes formation of an additional Vo (2nd Vo adjacent to the 1st Vo site) around the Hf atom at the site. On the other hand, hole injections cannot promote further Vo formation at the same site. [35]

From these calculations, we suppose the schematic models of the defect generation that is modulated by discharge of carriers and the balance of carriers as shown in Fig. 13. Under inversion stress, each Vo captures electron initially and forms Vo^{2-}. When the accumulation stresses were applied, which correspond to bipolar AC stress, electrons de-trapped from Vo^{2-} and return to Vo, resulting in prevention of Vo condensation. Each Vo will capture holes under further accumulation stress, resulting in structural relaxation at Vo alone. Each Vo may be regarded as a defect, corresponding to the small defect in the percolation model. In this case, additional Vo generation cannot be promoted and the sphere of structural relaxation is small.

In the case of DC stress, each Vo will capture electrons and forms Vo^{2-} under inversion stress. As a result, further Vo formation is promoted, that is, condensation of Vo. In each condensed Vo region, subsequent hole injection will bring about the structural relaxation in each large

region, corresponding to the large defect in the percolation model.

CONCLUSION

This paper discussed the TDDB characteristics of HfSiON under various stress conditions. It was found that the stress conditions modulate Weibull β. For example, the β under bipolar stress is larger than that under DC and unipolar AC stress. From these results, it was found that the discharge of electrons and injected carrier ratio $(J_{hole} / J_{electron})_{total}$ strongly influences Weibull distribution of T_{bd} in HfSiON. These results suggest that the characteristics of trapped and de-trapped carriers modulate the defect size in high-k gate dielectrics, leading to change of the β.

It can be concluded that control of electron trapping/de-trapping and hole trapping/de-trapping can provide steep Weibull distribution of T_{bd}, leading to long-term reliability in scaled CMOS devices with high-k gate stacks.

References

1) G. D. Wilk, R.M. Wallace, and J. M. Anthony: Appl. Phys. Rev. 89 (2001) 5243.

2) M. Koyama, A. Kaneko, T. Ino, M. Koike, Y. Kamata, R. Iijima, Y. Kamimuta, A. Takashima, M. Suzuki, C. Hongo, S. Inumiya, M. Takayanagi, and A. Nishiyama: IEDM Tech. Dig., 2002, p.849.

3) A. L. P. Rontondaro, M. R. Visikay, J. J. Chambers, A. Shanware, R. Khamankar, H. Bu, R. T. Laaksonen, L. Tsung, M. Douglas, R. Kuan, M. J. Bevan, T. Grider, J. McPherson, and L. Colombo : Symp. VLSI Technology, Dig. Tech. Pap., 2002,p.148.

4) S. Inumiya, K. Sekine, S. Niwa, A. Kaneko, M. Sato, T. Watanabe, H. Fukui, Y. Kamata, M. Koyama, A. Nishiyama, M. Takayanagi, K. Eguchi, and Y. Tsunashima: Symp. VLSI Technology, Dig. Tech. Pap., 2003,p.17.

5) K. Okada, H. Ota, A. Hirano, A. Ogawa, T. Nabatame, and A. Toriumi: IEEE Int. Reliability Physics Symp., 2008, p. 661.

6) K. Okada, W. Mizubayashi, N. Yasuda, H. Satake, H. Ota, M. Kadoshima, K. Tominaga, A. Ogawa, K. Iwamoto, T. Horikawa, T. Nabatame, and A. Toriumi: IEDM Tech. Dig., 2004, p. 721.

7) K. Okada, T. Horikawa, H. Satake, H. Ota, A. Ogawa, T. Nabatame, and A. Toriumi: IEEE Int. Reliability Physics Symp., 2006, p. 189.

8) J. McPherson, J.-Y. Kim, A. Shanware, and H. Mogul. Appl. Phys. Lett. **82** (2003) 2121.

9) J. W. McPherson, J.-Y. Kim, A. Shanware, H. Mogul, and J. Rodriguez: IEEE Trans. Electron Devices **50** (2003) 1771.

10) A. Shanware, J. McPherson, M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, H. Bu, M. J. Bevan, R. Khamankar, and L. Colombo: IEDM Tech. Dig., 2001, p. 137.

11) T. Yamaguchi, I. Hirano, R. Iijima, K. Sekine, M. Takayanagi, K. Eguchi, Y. Mitani, and N. Fukushima: IEEE Int. Reliability Physics Symp., 2005, p. 67.

12) M. Rafik, G. Ribes, D. Roy, and G. Ghibaudo: IEEE Int. Reliability Physics Symp., 2007, p. 44.

13) G. Ribes, M. Denais, S. Bruyere, D. Roy, F. Monsieur, V. Huard, C. Parthasarthy, M. Muller, T. Skotnicki, and G. Ghibaudo: Proc. 35th ESSDERC, 2005, p. 435.

14) M. Sato, K. Yamabe, K. Shiraishi, S. Miyazaki, K. Yamada, R. Hasunuma, T. Aoyama, Y. Nara, and Y. Ohji: IEEE Int. Reliability Physics Symp., 2008, p. 335.

15) W. Luo, T. Yuan, Y. Kuo, J. Lu, J. Yan, and W. Kuo: Appl. Phys. Lett. **89** (2006) 072901.

16) B. H. Lee, H. Byoung, C. Y. Kang, P. Kirsch, D. Heh, C. D. Young, H. Park, Y. J.

Hongbae, G. Bersuker, S. Krishnan, R. Choi, and H.-D. Lee: Appl. Phys. Lett. **91** (2007) 243514.

17) T. Nigam, A. Kerber, and P. Peumans: Int. Reliability Physics Symp., 2009, p. 523.

18) K. Torii, H. Kitajima, T. Arikado, K. Shiraishi, S. Miyazaki, K. Yamabe, M. Boero, T. Chikyow, and K. Yamada: IEDM Tech. Dig., 2004, p. 129.

19) Y. H. Kim, K. Onishi, C. S. Kang, H-J. Cho, R. Choi, S. Kishnan, M. S. Akbar, and J. C. Lee: IEEE Electron Device Lett. **24** [1] (2003) 40.

20) T. Kauerauf, R. Degraeve, E. Cartier, C. Soens and G. Groeseneken: IEEE Electron Device Lett. **23** [4] (2002) 215.

21) W. Y. Loh, B. J. Cho, M. S. Joo, M. F. Li, D. SH, Chan, S. Mathew, amd D-L. Kwong : IEDM Tech. Dig., 2003 p.927.

22) I. Hirano, Y. Nakasaki, S. Fukatsu, M. Goto, K. Nagatomo, S. Inumiya, K. Sekine, and Y. Mitani: Int. Reliability Physics Symp., 2009 p. 355.

23) R. Hasunuma, T. Naito, C. Tamura, A. Uedono, K. Shiraishi, N. Umezawa, T. Chikyow, S. Inumiya, M. Sato, Y. Tamura, H. Watanabe, Y. Nara, Y. Ohji, S. Miyazaki, K. Yamada, and K. Yamabe: ECS Trans. **11** [4] (2007) 3.

24) E. Cartier and A. Kerber: IEEE Int. Reliability Physics Symp., 2009, p.486

25) R. Degraeve, B. Govoreanu, B. Kaczer, J. van Haudt, and G. Groeseneken: Int. Reliability Physics Symp., 2005, p.360

26) J. H. Stathis: J.Appl.Phys.**86** (1999) 5757.

27) J. H. Stathis: Microelectron Eng, **36** (1997) 325.

28) K. F. Schuegraf and C. Hu: IEEE Trans. Electron Devices **41** [5] (1994) 761

29) B. Eitan and A. Kolodny: Appl. Phys. Lett **43**(1983) 106

30) A. Kerber, A. Varshenker, D. Lipp, T.Nigam and E. Cartier: IEEE Int. Reliability Physics Symp., 2010 p.369

31) J. Suñé : IEEE Electron Device Lett., **22** [6] (2001) 296.

32) R. Moazzami and C. Hu: IEDM Tech. Dig., 1992, p. 139.

33) S. Takagi, N. Yasuda, and A. Toriumi: IEEE Trans. Electron Devices **46** (1999) 335.

34) D. J. Dimaria and E. Cartier: J. Appl. Phys. **78** (1995) 3883.

35) Y. Nakasaki, I. Hirano K. Kato and Y. Mitani: Microelectron. Eng.,**86** (2009) 1901.

Figure captions

Figure 1. Flow diagram of MOSFET fabrication and the cross-section of the MOSFET used in this study

Figure 2. Stress conditions of DC stress, AC unipolar stress and AC bipolar stresses.

Figure 3. Schematics of carrier separation measurement of (a) n⁺poly-Si/n-FET and (b) n⁺poly-Si/p-FET.

Figure 4. Measurement flow of SILC.

Figure 5. Typical time evolutions of gate current(I_g)) under DC stress, unipolar AC stress and bipolar AC stress. (a) the horizontal axis shows the total time of stressing, including time of zero-voltage stress in unipolar stress or negative stress in bipolar stress. (b) the horizontal axis shows the sum of stress time under application of positive stress.

Figure 6. Weibull plots of T_{bd} under DC stress, unipolar stress and bipolar stresses. The large values of β were obtained under bipolar stress, although 63% T_{bd} is almost the same value.

Figure 7. (a) Cg-Vg curve before and after applied DC stresses. (b) Ig-Vg characteristics before and after applied DC stresses.

Figure 8. Typical time evolutions of SILC under DC stress, unipolar AC stress 2 and bipolar AC stress 3.

Figure 9. Carrier separation results of n^+poly-Si/n-FET and n^+poly-Si/p-FET under inversion conditions. (a) and (b) show the schematic image of carriers under $Vgst_1$ and $Vgst_2$, respectively.

Figure 10. Correlation between Weibull β of T_{bd} and $(J_{hole}/J_{electron})_{total}$ under DC, unipolar and bipolar AC stresses.

Figure 11. Correlation between a_o and $(J_{hole}/J_{electron})_{total}$ under each stress.

Figure 12. Schematic illustrations of percolation model under (a) bipolar AC stress (high $J_{hole}/J_{electron}$ condition) and (b) DC stress (low $J_{hole}/J_{electron}$ stress condition).

Figure 13. Microscopic images of generated defect size under (a) bipolar AC stress condition and (b) DC stress condition.

Table 1. Parameters of cycle stress time, $T1$ for inversion stress time, $T2$ for accumulation or zero-voltage stress time, and stress voltage, $Vgst_1$ for inversion stress and $Vgst_2$ for accumulation stress.

Table 2. The results of 63% T_{bd} and Weibull β for different stress condition.

Figure 1

● Isolation

● DHF Cleaning

● HfSiO deposition

● Post-deposition annealing

● Plasma Nitridation

● Post-Nitridation annealing

● Poly-Si deposition

● Ion implantation
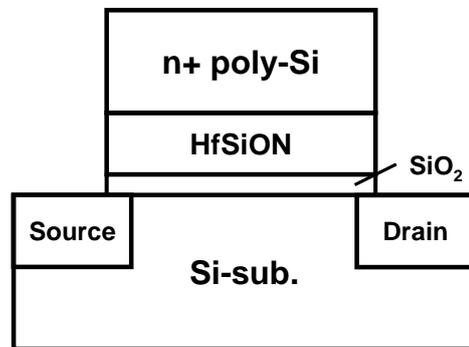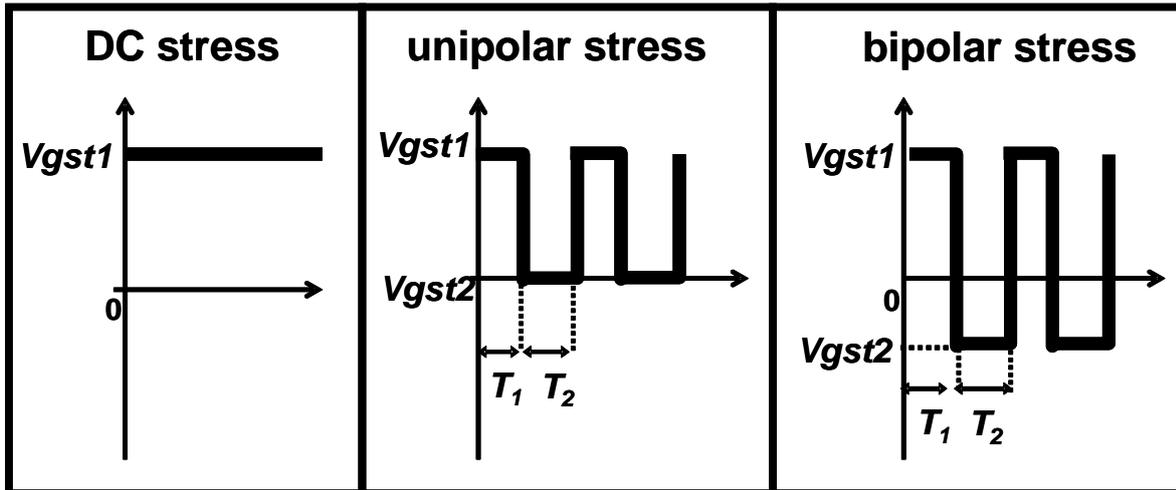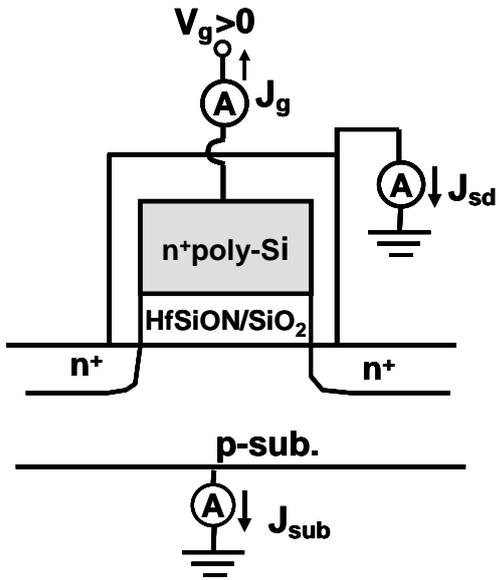
● Activation annealing

Conventional CMOS process

| n+ poly-Si |
| HfSiON |

SiO$_2$

| Source | | Drain |
| | Si-sub. | |

Figure 2

DC stress	unipolar stress	bipolar stress
Vgst1	*Vgst1* *Vgst2* T_1 T_2	*Vgst1* 0 *Vgst2* T_1 T_2

Table 1

DC stress	Unipolar AC stress 1	Unipolar AC stress 2
$Vgst1 = 2.5V$	$Vgst1 = 2.5V$ $Vgst2 = 0V$ $T_1 = 10$ s $T_2 = 10$ s	$Vgst1 = 2.5V$ $Vgst2 = 0V$ $T_1 = 10$ s $T_2 = 1000$ s

Bipolar AC stress 1	Bipolar AC stress 2	Bipolar AC stress 3
$Vgst1 = 2.5V$ $Vgst2 = -1V$ $T_1 = 10$ s $T_2 = 10$ s	$Vgst1 = 2.5V$ $Vgst2 = -1V$ $T_1 = 10$ s $T_2 = 100$ s	$Vgst1 = 2.5V$ $Vgst2 = -1V$ $T_1 = 10$ s $T_2 = 1000$ s

Figure 3

(a)

$V_g > 0$

(A) J_g

(A) J_{sd}

n⁺poly-Si

HfSiON/SiO$_2$

n⁺   n⁺

p-sub.

(A) J_{sub}

(b)

$V_g < 0$

(A) J_g

(A) J_{sd}

n⁺poly-Si

HfSiON/SiO$_2$

p⁺   p⁺

n-sub.

(A) J_{sub}
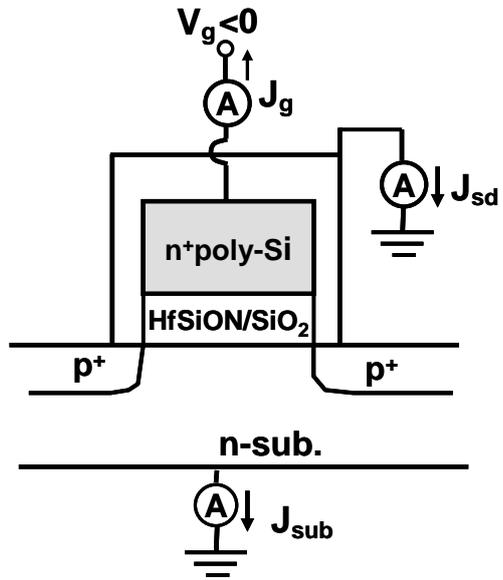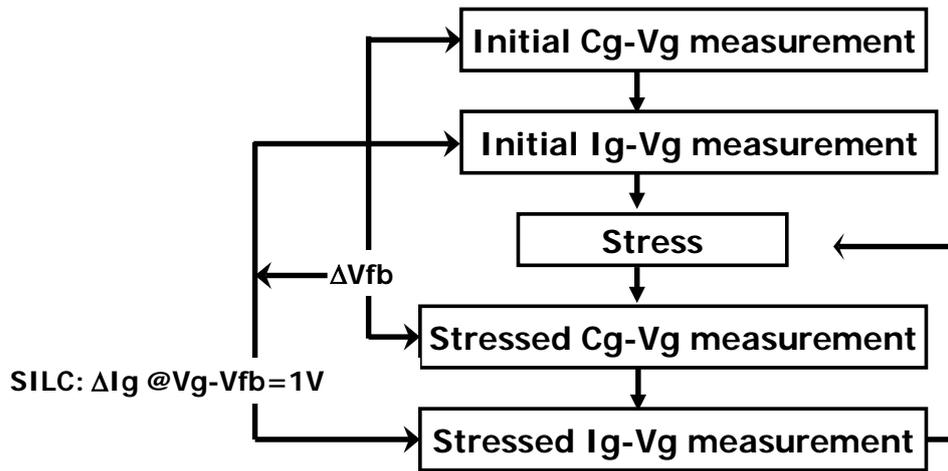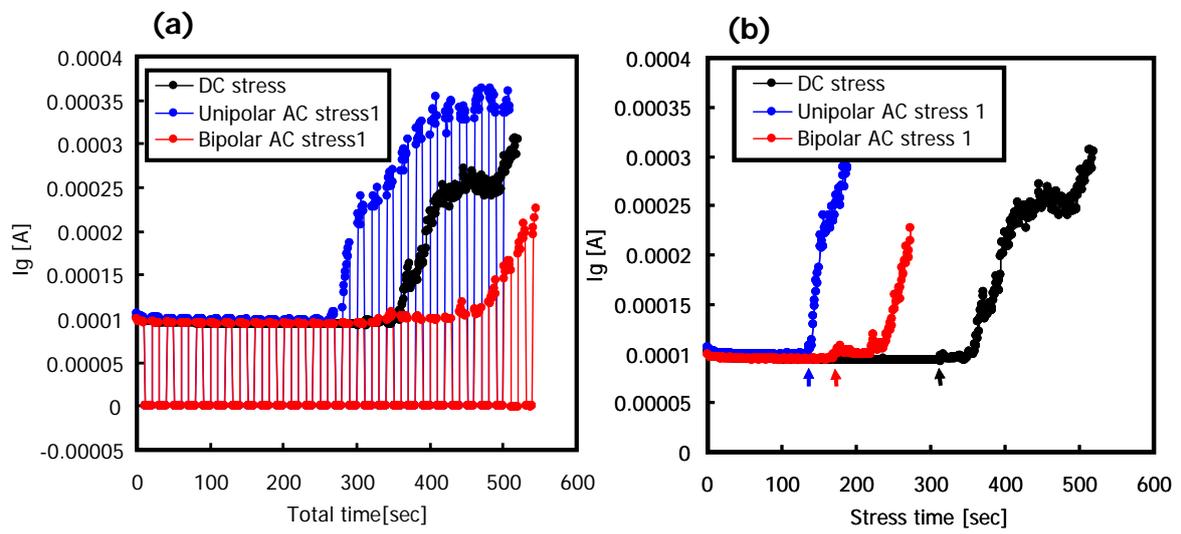
Figure 4

Figure 5

Figure 6
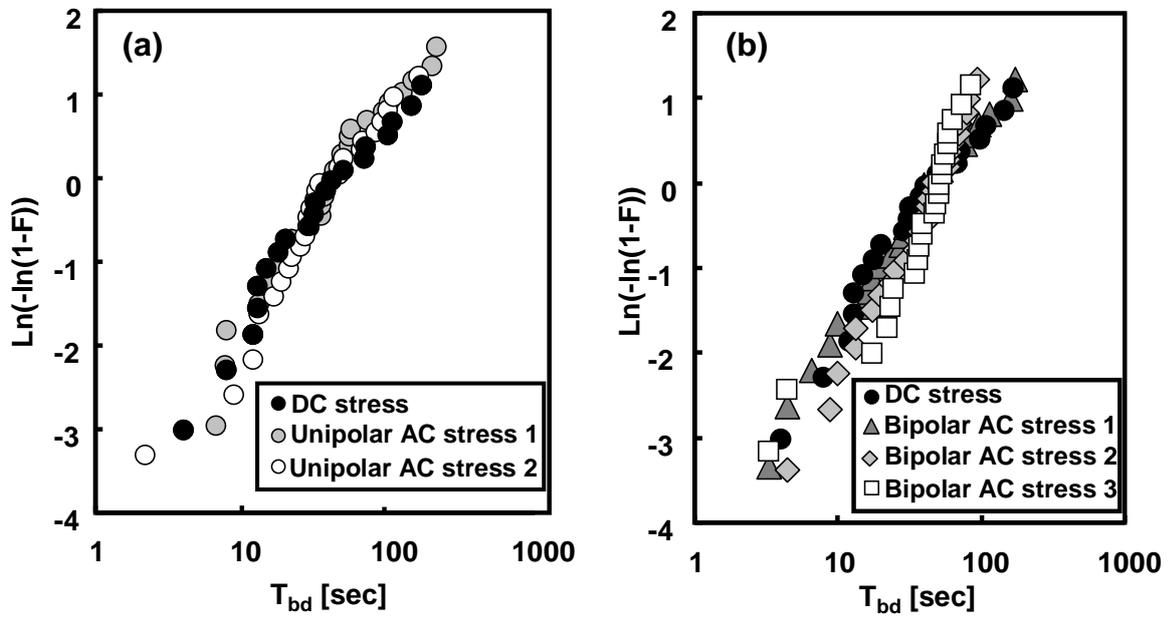
Table 2

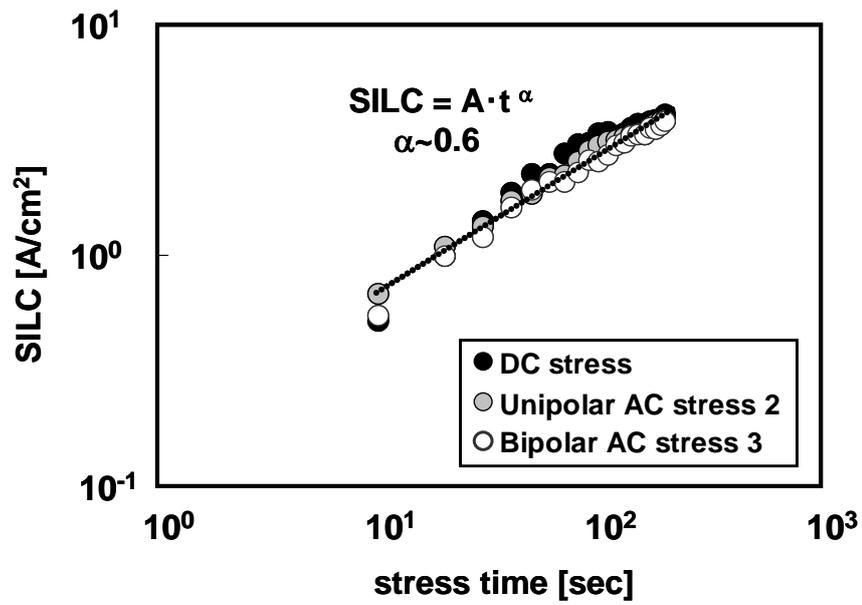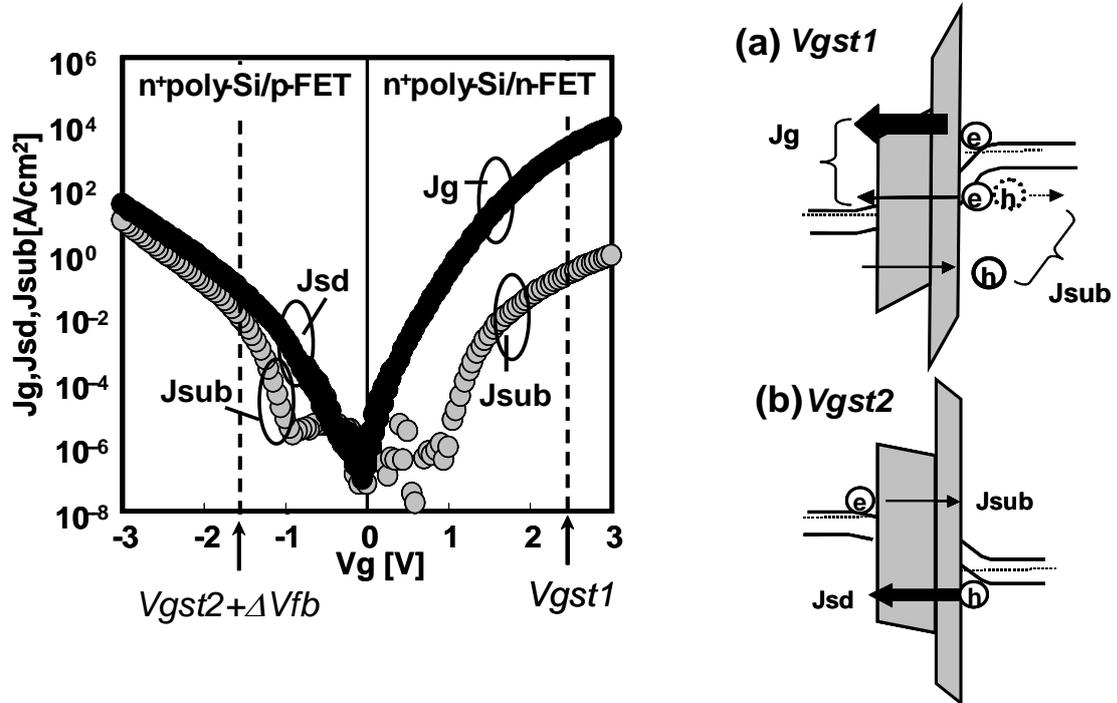| Stress type	stress condition				experimental data	
	Vgst1	*Vgst2*	*T1*	*T2*	63% T_{bd}	Weibull β
DC	2.5 V	n/a	n/a	n/a	52 s	1.0 ±0.1
Unipolar AC stress 1	2.5 V	0 V	10 s	10 s	46 s	1.1 ±0.1
Unipolar AC stress 2	2.5 V	0 V	10 s	1000 s	45 s	1.2 ±0.1
Bipolar AC stress 1	2.5 V	-1 V	10 s	10 s	50 s	1.1 ±0.1
Bipolar AC stress 2	2.5 V	-1 V	10 s	100 s	48 s	1.6 ±0.1
Bipolar AC stress 3	2.5 V	-1 V	10 s	1000 s	50 s	2.1 ±0.1

Figure 7
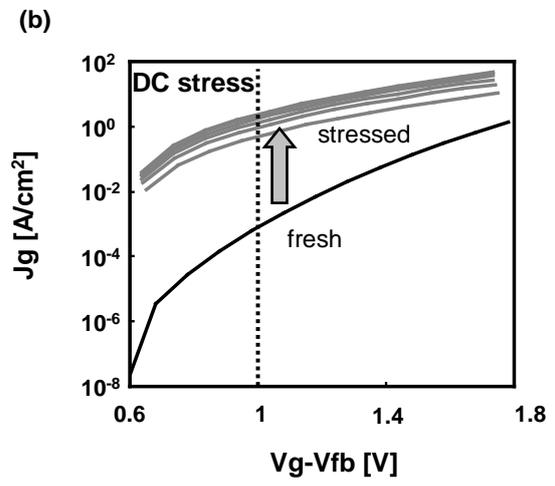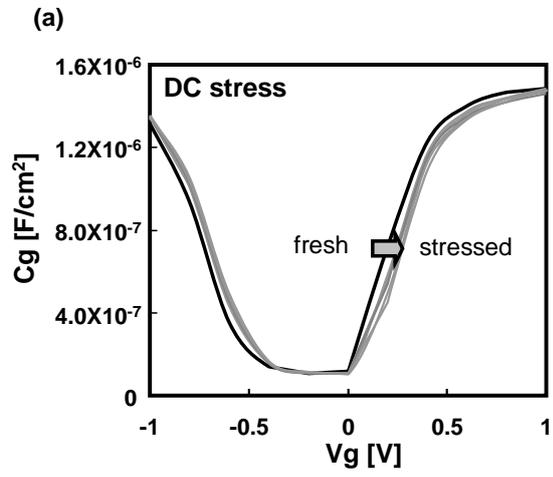
Figure 8

Figure 9

Figure 10

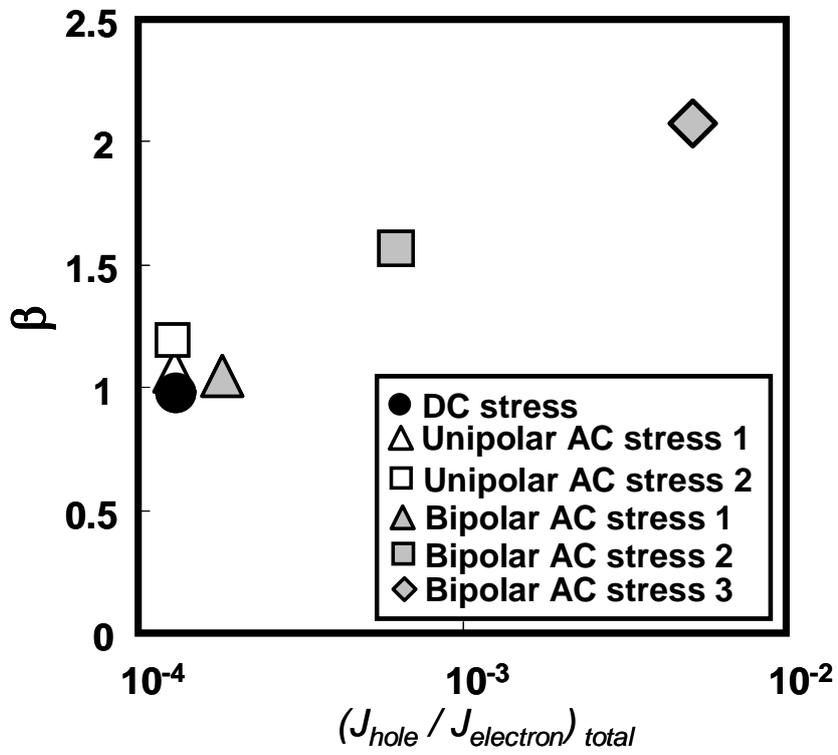# Figure 11

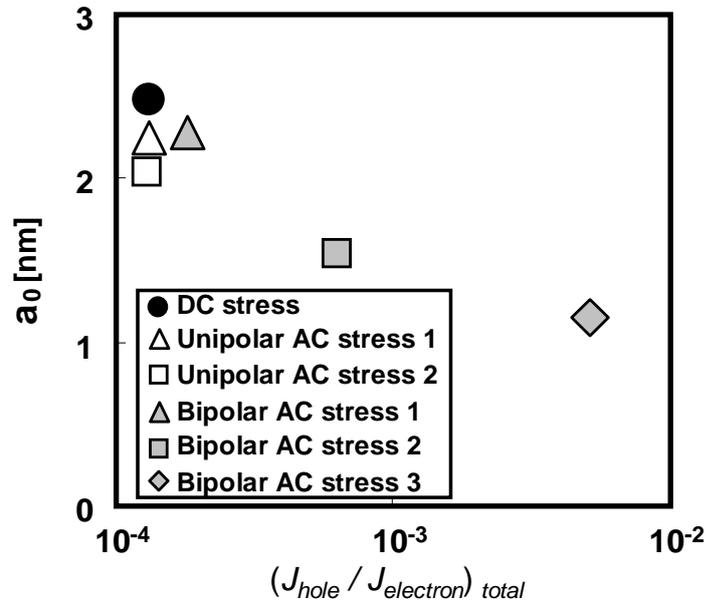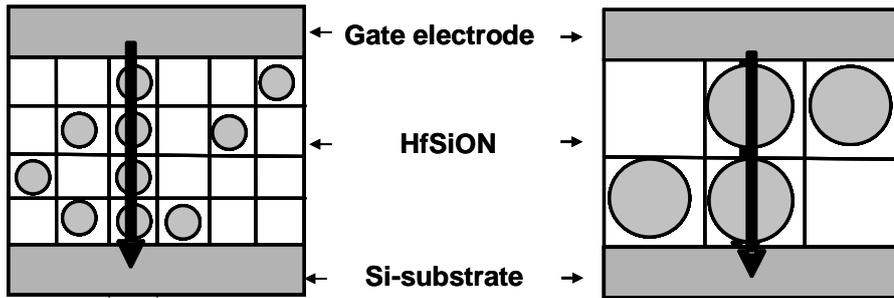# Figure 12

bipolar AC stress
(high $J_{hole}/J_{electron}$ condition)

DC stress
(low $J_{hole}/J_{electron}$ condition)

Gate electrode

HfSiON

Si-substrate

⬤ : generated defect

Figure 13

a) Accumulation stress (bipolar AC stress)

Capture hole to Vos

Inversion stress

Discharge electrons from Vo

2+

structural relaxation at Vo alone

Capture electrons to Vo

b) Inversion stress (DC stress)

condensation of Vo

Capture hole to Vos

structural relaxation at Vo in large condensed Vo's