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Structural advantages of rectangular-like channel cross-section on electrical characteristics of silicon nanowire field-effect transistors

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Abstract

We have experimentally demonstrated structural advantages due to rounded corners of rectangular-like cross-section of silicon nanowire (SiNW) field-effect transistors (FETs) on on-current (I_{ON}), inversion charge density normalized by a peripheral length of channel cross-section (Q_{inv}) and effective carrier mobility (μ_{eff}). The I_{ON} was evaluated at the overdrive voltage (V_{OV}) of 1.0 V, which is the difference between gate voltage (V_g) and the threshold voltage (V_{th}), and at the drain voltage of 1.0 V. The SiNW nFETs have revealed high I_{ON} of 1600 μA/μm of the channel width (w_{NW}) of 19 nm and height (h_{NW}) of 12 nm with the gate length (L_g) of 65 nm. We have separated the amount of on-current per wire at V_{OV} = 1.0 V to a corner component and a flat surface component, and the contribution of the corners was nearly 60 % of the total I_{ON} of the SiNW nFET with L_g of 65 nm. Higher Q_{inv} at V_{OV} = 1.0 V evaluated by advanced split-CV method was obtained with narrower SiNW FET, and it has been revealed the amount of inversion charge near corners occupied 50 % of all the amount of inversion charge of the SiNW FET (w_{NW} = 19 nm and h_{NW} = 12 nm). We also obtained high μ_{eff} of the SiNW FETs compared with that of SOI planar nFETs. The μ_{eff} at the corners of SiNW FET has been calculated with the separated amount of inversion charge and drain conductance. Higher μ_{eff} around corners is obtained than the original μ_{eff} of the SiNW nFETs. The higher μ_{eff} and the large fractions of I_{ON} and Q_{inv} around the corners indicate that the rounded corners of rectangular-like cross-sections play important roles on the enhancement of the electrical performance of the SiNW nFETs.

Key words: silicon on insulator, silicon nanowire, rectangular-like cross-section, on-current, split-CV, inversion charge density, effective carrier mobility.

1. Introduction

Aggressive scaling of the planar metal-oxide-semiconductor field-effect transistors (MOSFET) has encountered difficulties with suppression of the short channel effects (SCE), which induces an increase in off-state leakage current (I_{OFF}) to degrade the on-current/off-current ratio (I_{ON}/I_{OFF}). A solution to suppress the SCE is an introduction of three-dimensional channel FETs for enhancement of the electrostatic controllability of the channel. Silicon nanowire (SiNW) FETs have the most effective channel controllability and nearly ideal off-characteristics have been experimentally demonstrated [1]. I_{ON} enhancement of the SiNW FET has also been reported [2]. Higher I_{ON} with lower I_{OFF} is advantageous for realization of a low power supply voltage device and thus a low power consumption device application. The I_{ON} is mainly attributed to the inversion charge density (Q_{inv}) and effective carrier mobility (μ_{eff}) of the SiNW channel. The μ_{eff} of SiNW FET has been investigated in many institutes [3-5] and mainly focused on the surface orientations of the SiNW channel. We focused on structural effects of the SiNW channel on the electrical performance of SiNW FETs. In this work we fabricated the SiNW FETs with rectangular-like channel cross-section and planar SOI FETs on (100) SOI wafer simultaneously and electrically characterized, especially the I_{ON}, μ_{eff} and Q_{inv}. We intensively analyzed structural advantages of rectangular cross-section SiNW FET. Experimental results suggested that corners in the rectangular cross-section played important roles on the enhancement of the electrical performances of the SiNW nFETs.

2. Device fabrication process

A (100)-oriented silicon-on-insulator (SOI) wafer was used as a starting material with the SOI layer and the buried oxide (BOX) layer thickness of 75 and 50 nm, respectively. The mesa-type Si fin with embedded source and drain (S/D) pad region with a silicon nitride hard mask of 50 nm formed by the low-pressure chemical vapor deposition on an oxide pad layer of 7 nm atop was oxidized in dry oxygen ambient at 1000 ^{o}C for 1 hour to form narrow SiNW channel. The silicon nitride layer prevents the oxidation and the resultant reduction of the SOI layer thickness of S/D region to avoid an unexpected increase in parasitic series resistance (R_{SD}). The sacrificial oxide was partially stripped by wet etching process and silicon nitride sidewalls were formed by deposition and etch-back process. The residual oxide was completely stripped, and the SiO_2 gate oxide with a thickness (T_{ox}) of 3 nm and a non-doped poly-silicon film of 75 nm was deposited, which resulted in a trigate-like gate semi-around structure [6]. After gate ion implantation process (phosphorus for nFETs and boron for pFETs), silicon dioxide hard mask deposited by chemical-vapor deposition with tetraethoxysiliane (TEOS) of 30 nm was formed. Dry ArF lithography process and dry etching

process with TEOS hard mask was used to form gate electrode. After the poly-Si gate electrode formation, the 1st spacer formation and the ion implantation were performed (arsenic (15 keV) for the SiNW nFET with the channel width w_{NW} of 9 nm, and phosphorus (5 keV) for the SiNW nFETs with w_{NW} of 19, 28, and 39 nm and the planar SOI nFETs, and boron (4 keV) for pFETs) at the dose of 1×10^{15} cm^{-2}. The 2nd spacer formation and the deep S/D ion implantation were performed (arsenic (20 keV) for the SiNW nFET with the channel width w_{NW} of 9 nm, and phosphorus (5 keV) for the SiNW nFETs with w_{NW} of 19, 28, and 39 nm and the planar SOI nFETs, and boron (4 keV) for pFETs) at the dose of 5×10^{15} cm^{-2}. After a spike rapid thermal annealing process for an activation of the implanted dopants, a self-align nickel silicidation process was performed. An excessive silicidation of SiNW channel was not observed due to optimized process conditions [7, 8]. Post metallization dielectric with the thickness of 470 nm was deposited and finally the wafer was sintered in forming gas ambience. The schematic process flow is shown in **figure 1**. A review scanning electron microscope (SEM) image of the SiNW FETs with the gate length L_g of 65 nm and cross-sectional transmission electron microscope (TEM) images of SiNW channels are shown in **figure 2**. As the SiNW channel was formed by thermal oxidation in high-temperature, the corners have rounded shape [9]. The radius of corners (W_c) of sample A and B is 4 nm, whereas 6.5 nm of sample C based on the TEM images. The channel height (h_{NW}) and width (w_{NW}) in cross-section are summarized in the inset in the **figure 2**.

3. Results

3.1 Dc-characteristics of SiNW FETs

Typical output and transfer characteristics of the SiNW FETs (w_{NW}=19 nm and h_{NW}=12 nm) with the L_g of 65 nm and the T_{ox} of 3 nm are shown in **figure 3**. A well-behaved transistor operation was confirmed for the both SiNW nFETs and pFETs. The on-current per wire of the SiNW nFET (w_{NW}=19 nm and h_{NW}=12 nm) was as high as 60 μA, whereas 22μA of the SiNW pFETs of the same size was obtained. Although the SiNW FETs have corners in the rectangular-like cross-sectional shape, no kink was observed in the transfer characteristics, which might be due to low-doped SiNW channel [10]. Large on-off current ratio (I_{on}/I_{off}) of $>10^6$ with the drain induced barrier lowering (DIBL) and the subthreshold swing (S.S.) of 62 mV/V and 70 mV/dec., for the SiNW nFETs have been obtained. We can observe saturation region clearly in output characteristics of nFETs, which suggests low R_{SD}. Sufficiently low S. S. indicates that interfacial state density (D_{it}) of SiNW FET with rectangular-like cross-section is negligible.

3.2 On-current of SiNW FETs

On-currents normalized by a peripheral length, which is a total length of top and side channels of SiNW cross-section, (I_{ON}) of SiNW nFETs with the gate length from 500 to 65 nm were measured

and summarized in the **figure 4(a)**. The on-current per wire was extracted at the overdrive voltage V_{OV} =1.0 V, which is a difference of a gate voltage (V_g) and a threshold voltage (V_{th}), and drain voltage $|V_d|$=1.0 V. As the w_{NW} increases on-current per wire was also increased. After normalization of on-current per wire by the peripheral length of channel, the largest I_{ON} of the narrowest SiNW nFET (w_{NW}=19 nm and h_{NW}=12 nm) was obtained. Among these, SiNW nFETs (w_{NW}=19 nm and h_{NW}=12 nm) showed excellent high I_{ON} of 1600 μA/μm. The I_{ON} of SiNW pFETs with the gate length from 500 to 65 nm are also shown in **figure 4(b)**. The structural advantages of SiNW nFETs on the I_{ON} drivability is summarized in **figure 5**. Higher I_{ON} was obtained with smaller w_{NW} in each gate length and exceeds the I_{ON} of planar SOI nFETs, which suggests that the smaller w_{NW} is advantageous to I_{ON} drivability between the w_{NW} of 19 and 39 nm.

I_{ON}/I_{OFF} characteristics of SiNW nFETs are shown in **figure 6**. The I_{OFF} was defined as the drain current normalized by the peripheral length of SiNW channel at the V_g-V_{th} of -0.3 V and drain voltage (V_d) of 1.0 V. The SiNW nFET with narrower w_{NW} demonstrates superior I_{ON}/I_{OFF} characteristics, especially significantly improved I_{ON}/I_{OFF} in short L_g region due to electrostatic controllability of the narrow SiNW channel.

Parasitic series resistance of source/drain (R_{SD}) of SiNW FETs tends to become larger than that of planar devices [11], which degrade the I_{ON}. The R_{SD} of SiNW FETs was evaluated applying a Chern's channel-resistance method (CRM) [12] to the SiNW FETs with the three different mask gate length (L_{mask}) of 550, 450, and 350 nm. We plotted the total resistance (R_{tot}) at the effective gate length of each device. Then, we fitted a straight line to R_{tot} of the SiNW FETs with different gate length using least square method. Finally we obtained R_{SD} at the intercept of the y-axis. Extracted R_{SD} was summarized in **figure 7**. The R_{SD} of nFETs correspond to only 10 % of the total resistance (R_{tot}) for the SiNW nFET with the L_g of 65 nm, owing to the process optimization for S/D formation. It is worth noting that arsenic implantation instead of phosphorus results in about 10 times higher R_{SD}, presumably due to the damages in the S/D region as well a the difference in the Ni silicide formation [13, 14]. On the other hand, the R_{SD} of pFETs are much higher than that of nFETs. One reason of relatively low I_{ON} compared with that of the SiNW nFETs in the previous section is the large R_{SD} of the SiNW pFETs. A difference of the L_{mask} and actual gate length (ΔL) of SiNW pFETs obtained during the analysis using CRM was larger than ΔL of the SiNW nFETs. We speculate the difference of ΔL between the SiNW nFETs and the SiNW pFETs might suggest the difference of the dopant diffusion process into the SiNW channel between phosphorus and boron. The redistribution of boron during Ni silicidation process was also reported [15] and more process optimization is necessary for the SiNW pFETs.

3.3 On-current separation into a corner component and a flat surface component

In the previous section, the structural advantages of w_{NW} on the I_{ON} of the SiNW FET was

investigated. The advantages could be explained by the effects of corners in the rectangular-like cross-section. In this section, we attempt to separate on-current of corner component (I_{corner}) and on-current along flat surface (I_{flat}) of the SiNW nFETs for the determination of contributions of the corners in **figure 8**. The on-current along flat surface I_{flat} and the on-current of the corner component I_{corner} were calculated as follows. First we subtracted the on-current per wire of the SiNW FET with smaller w_{NW} from an on-current per wire of the SiNW FET with larger w_{NW}. Then we normalized the difference of the on-current per wire with the difference of w_{NW} between each SiNW FET. We obtained the normalized on-current along flat surface of (*i*) 1069, (*ii*) 932, and (*iii*) 994 μA/μm using the SiNW nFET with w_{NW} of (*i*) 19 and 28 nm, (ii) 28 and 39 nm, and (*iii*) 19 and 39 nm. The averaged normalized on-current along flat surface was 998 μA/μm. Next, we calculated the on-current along flat surface I_{flat}. We assumed that the normalized on-current of side-surface is the same as that of the top-surface. The peripheral length of upper corners were measured based on cross-sectional TEM images and the rest of the peripheral length was that of the flat surface as mentioned in section 2. We multiplied the normalized on-current of the flat surface by the peripheral length of the flat surface and obtained the on-current along flat surface I_{flat}. The rest is the on current of corner component I_{corner}. Separated I_{corner} and I_{flat} is summarized in **figure 9** and about 60 % of the I_{ON} of the SiNW FET (w_{NW}=19 nm and h_{NW}=12 nm) was attributed to the corners.

3.4 Inversion charge of SiNW FETs at the on-state

Inversion charge density (Q_{inv}) and effective carrier mobility (μ_{eff}) was experimentally extracted by advanced split-CV technique [16] applied to multi-channel SiNW FETs with a number of 64 wires to facilitate the measurement accuracy. The amount of inversion charge (Q) of SiNW channel was calculated as

$$Q = \int \left(C_{gc1} - C_{gc2} \right) dV$$

, where C_{gc1} is the gate-to-channel capacitance (C_{gc}) of multi-channel SiNW (MSiNW) FET with larger L_{mask} and C_{gc2} is the C_{gc} of the MSiNW FET with smaller L_{mask}. The inversion charge density Q_{inv} at V_g-V_{th}=1.0 V for nFETs and Q_{inv} at V_g-V_{th}=-1.0 V for pFETs were obtained, which is shown in **figure 10 (a)**. As the cross-sectional dimension increased, the amount of inversion charge increased. After normalization by unit channel area, largest Q_{inv} was achieved with the SiNW FETs with the smallest w_{NW}. The increase of inversion charge density was observed for both p-type and n-type SiNW FETs, which is shown in **figure 10 (b)**. The solid line in **figure 10 (b)** is calculated Q_{inv} on assumptions below.

For an investigation of contributions of corners to the total amount of inversion charge, the amount of inversion charge was separated to the component of corners and that of flat surface. It was assumed that (*i*) inversion charge density of the flat surface is the same as that of planar SOI FETs

and that (*ii*) the peripheral length of upper corners was measured with cross-sectional TEM image as in the section 3.3. The amount of inversion charge at the corner (Q_{corner}) and the amount of inversion charge along flat surface (Q_{flat}) are shown in **figure 11**. As the w_{NW} decrease fraction of the amount of inversion charge around corners increase. The solid line in **figure 10 (b)** was the calculated inversion charge density Q_{inv} on the assumptions as follows: (*i*) the inversion charge at the corners was 4.9×10^{-15} C with the W_c of 4 nm, which was the average of the corner component of inversion charge shown in **figure 11** (*ii*) the Q_{inv} of flat surface is the same as that of SOI planar nFETs. The Q_{inv} of the sample C is out of the line, which suggests the W_c of sample C is larger than 4 nm, which agrees with the W_c obtained by the cross-sectional TEM image in **figure 2 (b)**.

3.5 Effective carrier mobility evaluation of the SiNW FETs

The μ_{eff} of SiNW FETs was obtained using the advanced split-CV method [16] and results were calculated using the equations

$$\mu_{eff} = \frac{\Delta L^2 \cdot \Delta g_d}{Q}$$

where ΔL is the difference of mask gate length (L_{mask}) between two transistors used for measurement. Δg_d is the difference of the drain conductance, which is written as

$$\frac{1}{\Delta g_d} = \frac{1}{g_{d1}} - \frac{1}{g_{d2}}.$$

, where g_{d1} is the drain conductance of the SiNW FET with larger L_g and g_{d2} is the drain conductance of the smaller L_g. The results are shown in **figure 12**. Higher μ_{eff} of SiNW nFET than planar SOI nFETs were obtained from the middle-field to the high-field region, which is one reason of the high I_{ON} of SiNW nFETs. The higher μ_{eff} of SiNW nFETs than that of planar SOI nFETs suggests higher μ_{eff} could be obtained around corners. For an extraction of μ_{eff} at the corners and that along the flat surface of the channel, g_d was also separated to the corner component and that along flat surface on the same assumption as in the extraction process of the inversion charge at the corners and that of the flat surface. Finally μ_{eff} at V_g-V_{th} = 1.0 V around corners and along the flat surface of channel were calculated, which are shown in **figure 13**. The μ_{eff} around corners saturates as the w_{WN} increase toward 28 nm. Higher μ_{eff} at corners of nFETs than that of flat surface were obtained.

The μ_{eff} of pFETs were also extracted using the advanced split-CV method and shown in **figure 12 (b)**. μ_{eff} of the SiNW FETs were comparable with that of planar SOI pFETs and shows a little degradation of μ_{eff} as w_{NW} decrease.

4. Discussion

We obtained large I_{ON} of the SiNW nFETs due to the increase in the Q_{inv}, the enhancement of μ_{eff} and the reduced R_{SD}. Although the increase in the Q_{inv} is observed for both nFETs and pFETs, the enhancement effect in the μ_{eff} was observed only for nFETs. The comparable μ_{eff} of SiNW pFETs with that of planar SOI pFETs is one reason of relatively low I_{ON} of the pFETs. The extracted μ_{eff} around the corners of the SiNW nFETs are enormously large, which coincides with the experimental results of [17]. The channel surface orientation of corners is composed of various surface crystal orientations, which seems to degrade the surface carrier mobility of the corners [18]. However, the carrier mobility around corners obtained in this work is very large and even surpasses (100)-surface universal mobility [19]. The enhanced μ_{eff} around the corners might be due to volume inversion around corners. Our two-dimensional device simulation using almost the same structure as that in this work (w_{NW}=19 nm, h_{NW}=12 nm and w_{NW}=28 nm, h_{NW}=12 nm) resulted in 2.5 times as high inversion charge density around the corners, the peak density of which is 5.3×10^{19} cm^{-3}, as that along flat surface at the on-state. The high inversion charge density supports the existence of volume inversion around the corners. The μ_{eff} enhancement due to the volume inversion has been reported [20, 21]. The effective carrier mobility μ_{eff} of nearly 550 cm^2/Vs was obtained in the double gate mode at inversion carrier density of 10^{12} cm^{-2} for [20]. The extracted μ_{eff} of corners with the w_{NW} of 19 nm is comparable with the reported experimental results. The discussion above indicates that μ_{eff} in SiNW channel is not only governed by channel surface orientation, but especially structural advantage of corners of rectangular cross-sectional shape. On the other hand, corner enhancement of μ_{eff} for the SiNW pFETs seem not to exist.

As a large amount of inversion charge and superior effective electron mobility was obtained around corners of rectangular cross-section, one might expect that larger I_{ON} can be obtained with smaller w_{NW} of SiNW nFETs as an extrapolation in **figure 5** toward lower w_{NW}. However we can observe that μ_{eff} at the corners of SiNW FET degrades as the w_{WN} decrease in **figure 13**. This result suggests that μ_{eff} degrades as the distance between each corner decreases, which is equal to a decrease of w_{NW}. Therefore we speculate that the I_{ON} of the SiNW nFET does not monotonically increase as the w_{NW} decrease. Optimized dimensions of cross-section should be studied for an enhancement of the I_{ON} with structural advantages of the SiNW nFET with the rectangular-like cross-section. We speculate an optimized cross-sectional dimension is near w_{WN}=19 nm and h_{NW}=12 nm due to comparable Q_{inv} at V_g-V_{th}=1.0 V and higher μ_{eff} compared with those of the SiNW nFET with w_{NW} =9 nm and h_{NW}=10 nm.

5. Conclusion

We have investigated the structural advantage of rectangular cross-section on electrical performances, especially the I_{ON}, Q_{inv} and μ_{eff} of the SiNW nFETs. It is confirmed that the corners in rectangular-like cross-section play important roles on the achievement of the I_{on} as high as

1600 μA/μm of the SiNW nFET (w_{NW}=19 nm and h_{NW}=12 nm) thanks to the increase of the Q_{inv} and the significant enhancement of the μ_{eff} around corners. This result suggests that current conduction is not only governed by channel surface orientation but by cross-sectional shape of channel. For pFETs, the increase of the Q_{inv} has been observed. However the enhancement of μ_{eff} is not observed. By narrowing the SiNW channels, μ_{eff} of corners tend to degrade, although the μ_{eff} of the corners of narrower SiNW FET was higher than that of flat surface. Therefore we speculate that the structural advantage by the reduction of the w_{NW} is not monotonic.

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Figure captions

Figure 1. A schematic process flow of the gate semi-around SiNW FETs. The gate semi-around SiNW FET was fabricated with conventional CMOS process facilities.

Figure 2. (a) A review SEM image and (b) cross-sectional TEM images of the SiNW channels and the cross-sectional dimensions. A cross-section of planar SOI FETs is also shown.

Figure 3. (a) The transfer and (b) output characteristics of the SiNW FETs (w_{NW}=19 nm and h_{NW}=12 nm).

Figure 4. The I_{ON} dependence on gate length (L_g) and channel width (w_{NW}) of the SiNW FETs and planar SOI FETs.

Figure 5. Structural advantages of the SiNW nFETs with rectangular-like cross-section over planar SOI nFETs, which increase as the w_{NW} decrease.

Figure 6. I_{ON}/I_{OFF} characteristics of the SiNW nFETs (w_{NW}=19, 28, and 39 nm, h_{NW}=12 nm) with the gate length from 65 to 500 nm.

Figure 7. Total resistance (R_{tot}) of SiNW nFETs and pFETs with the different L_g. Intercepts on y-axis are extracted R_{SD}.

Figure 8. Assumptions for calculation and extraction of I_{ON}, Q_{inv}, and μ_{eff} of the fraction of corners and those of flat surface. W_c is assumed to be 4 nm considering cross-sectional TEM images in figure 2(b).

Figure 9. Extracted on-current of the corner component and the flat surface component of the SiNW nFETs with the L_g of 65 nm.

Figure 10. (a) The amount of inversion charge and (b) the inversion charge density of the SiNW FETs and planar SOI FETs (solid for pFETs and open for nFETs). The solid line in (b) is calculated on the assumptions: (*i*) the amount of inversion charge at the rounded corners is 4.9×10^{-15} C with the radius (W_c) of 4 nm (*ii*) the inversion charge density along flat surface is 9.7×10^{-21} C/cm^2.

Figure 11. The amount of inversion charge at the corners (Q_{corner}) and along the flat surface (Q_{flat}) of the SiNW nFETs with the channel width w_{NW} of 9, 19, and 28 nm.

Figure 12. Effective carrier mobility of the multi-channel SiNW (a) nFETs and (b) pFETs in this work extracted using the advanced split-CV method [16].

Figure 13. Separated μ_{eff} of corners and that of flat surface of the SiNW nFETs (w_{NW}=9, 19 and 28 nm).

Figure 1.

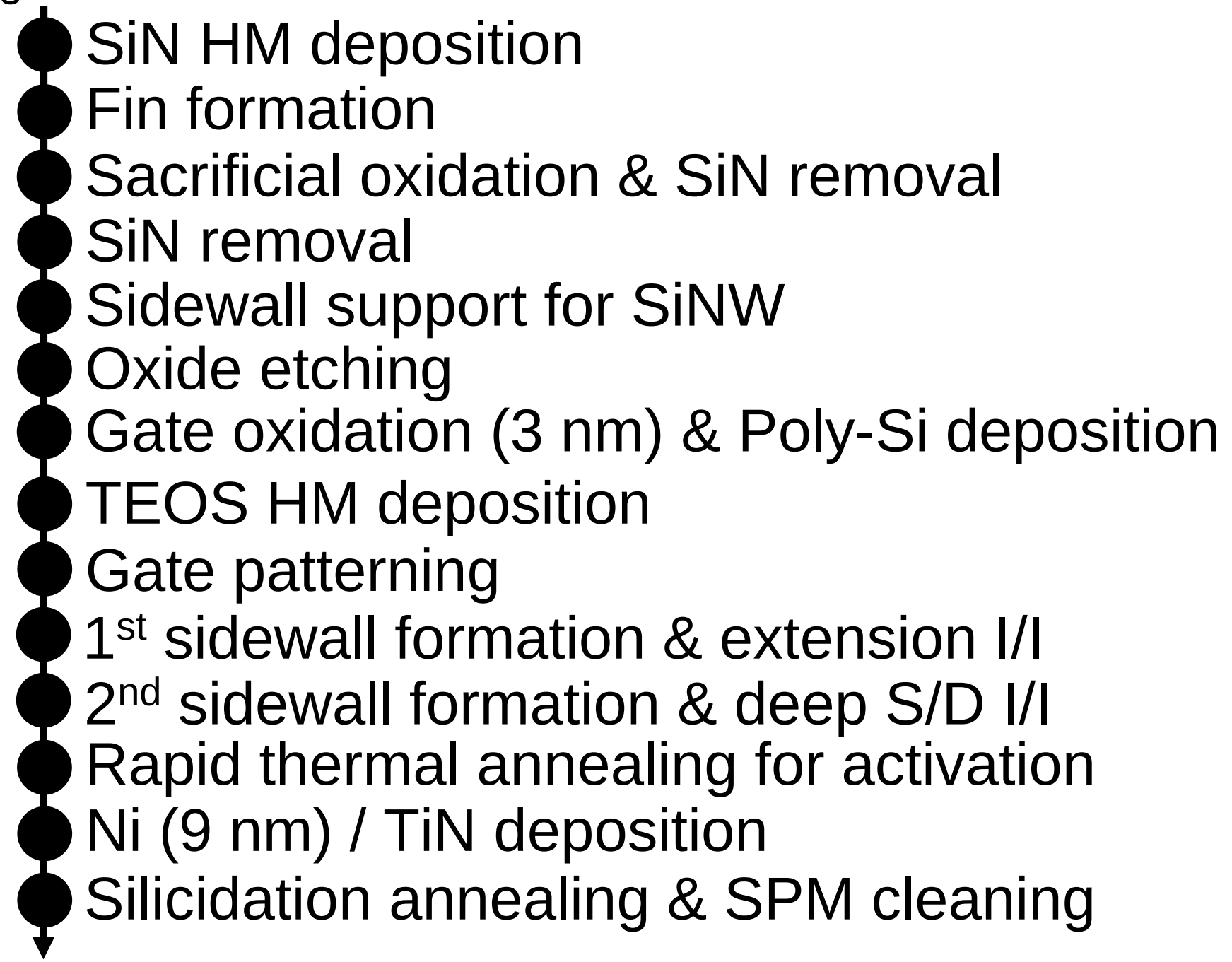
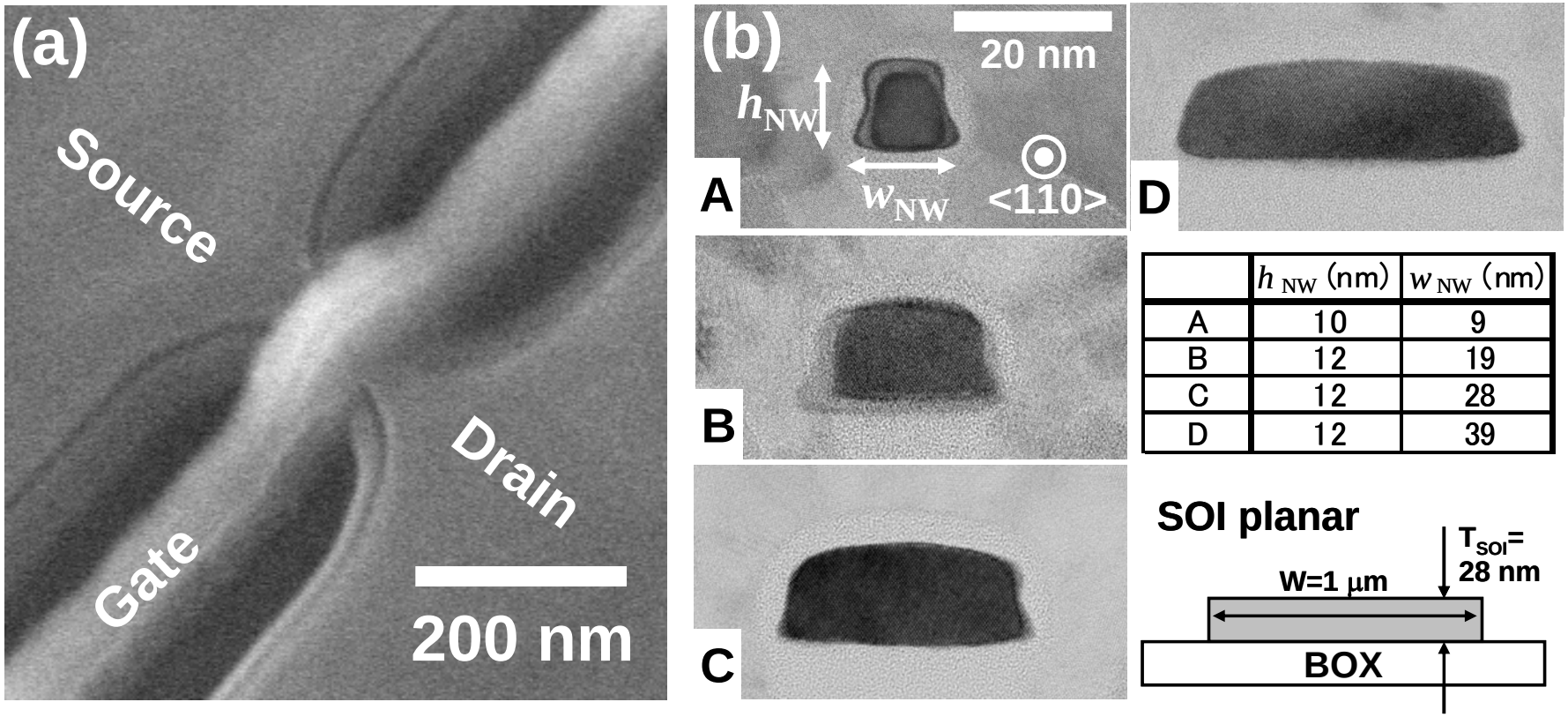

SiN HM deposition
Fin formation
Sacrificial oxidation & SiN removal
SiN removal
Sidewall support for SiNW
Oxide etching
Gate oxidation (3 nm) & Poly-Si deposition
TEOS HM deposition
Gate patterning
1st sidewall formation & extension I/I
2nd sidewall formation & deep S/D I/I
Rapid thermal annealing for activation
Ni (9 nm) / TiN deposition
Silicidation annealing & SPM cleaning

Figure 2.



	h_{NW} (nm)	w_{NW} (nm)
A	10	9
B	12	19
C	12	28
D	12	39

Figure 3.

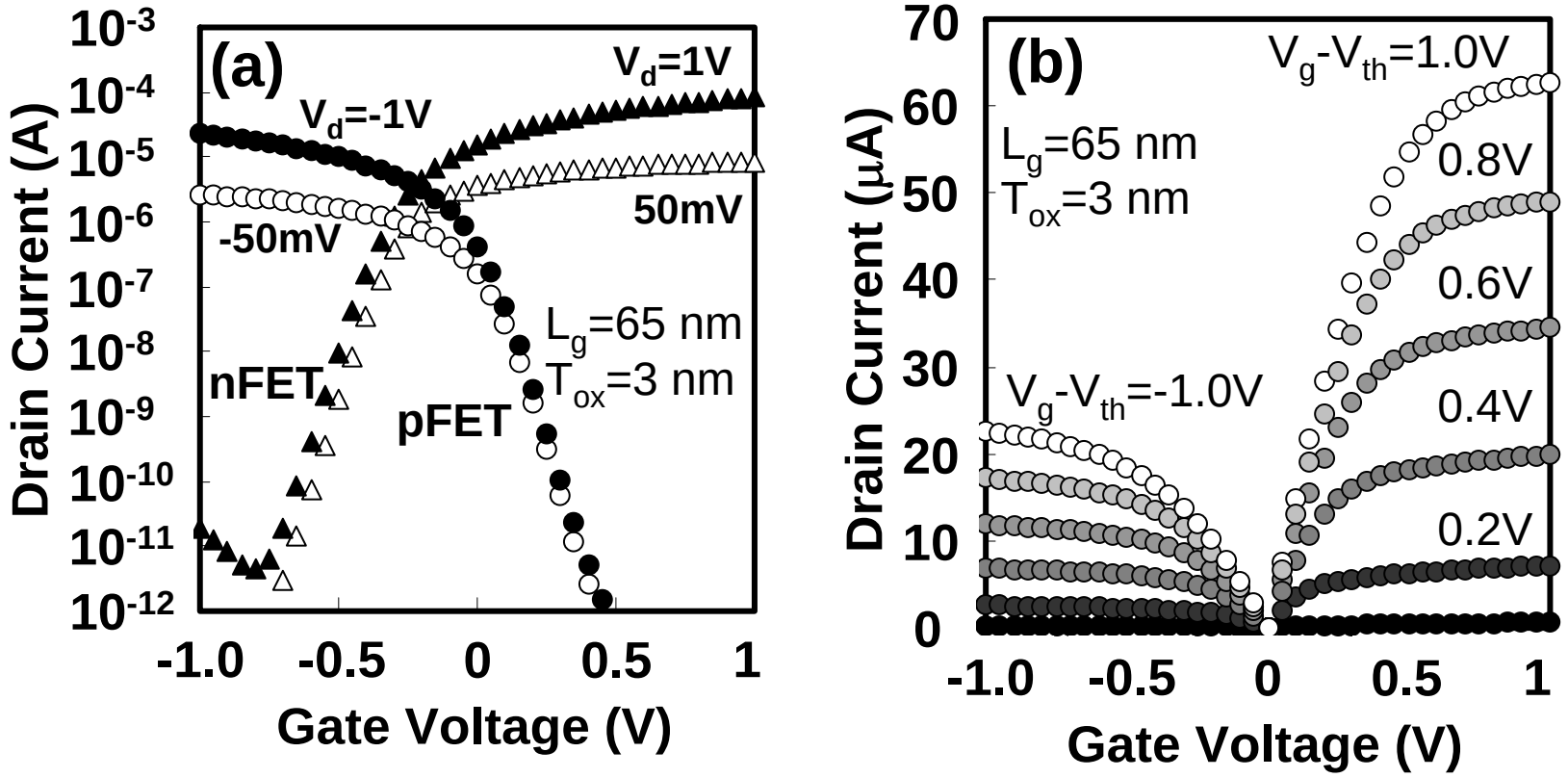

(a)
V_d=1V
V_d=-1V
50mV
-50mV
L_g=65 nm
T_{ox}=3 nm
nFET
pFET
Drain Current (A)
Gate Voltage (V)
(b)
V_g-V_{th}=1.0V
0.8V
0.6V
0.4V
0.2V
V_g-V_{th}=-1.0V
L_g=65 nm
T_{ox}=3 nm
Drain Current (μA)
Gate Voltage (V)

Figure 4.

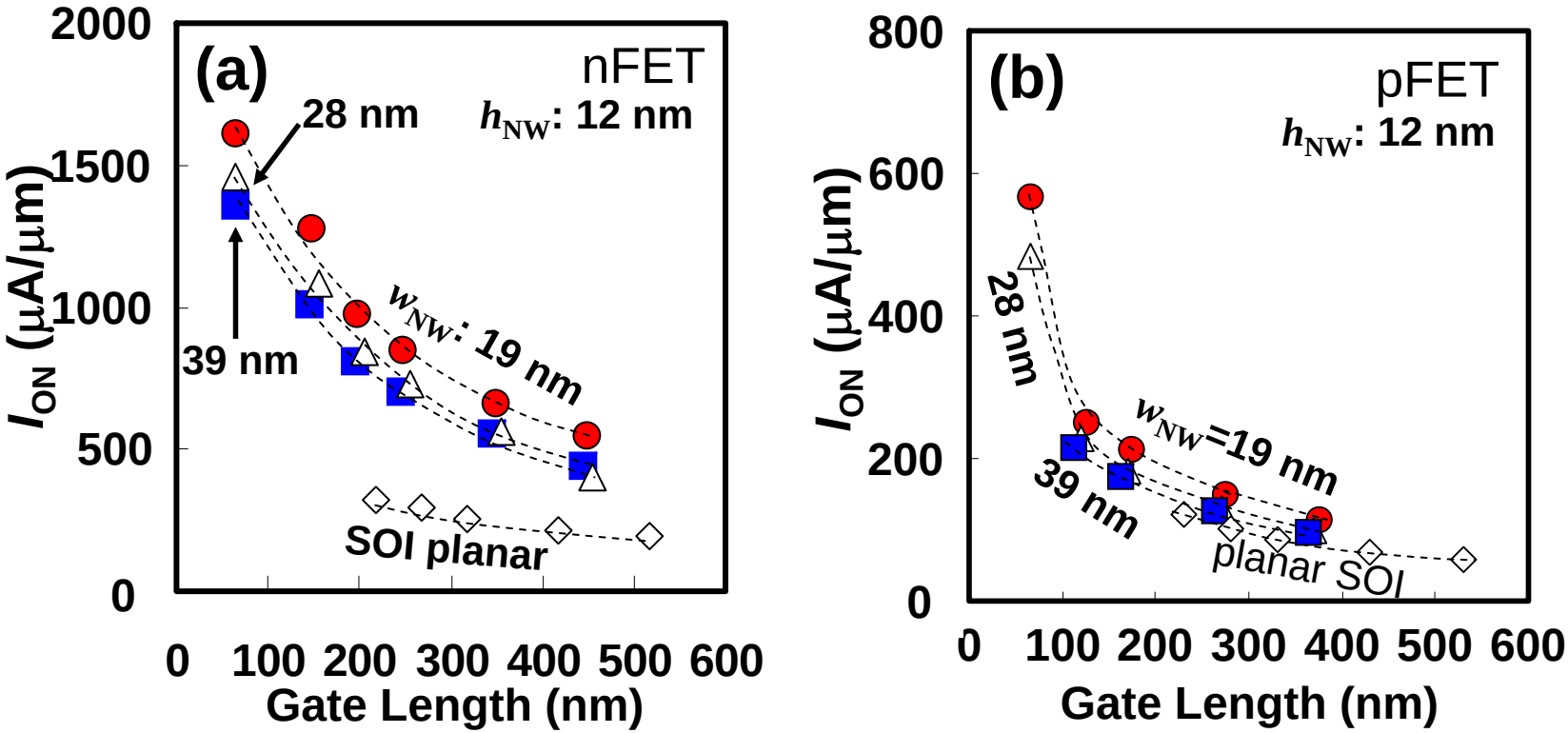

(a)
nFET
h_{NW}: 12 nm
28 nm
39 nm
w_{NW}: 19 nm
SOI planar
I_{ON} (μA/μm)
Gate Length (nm)
0
500
1000
1500
2000
0 100 200 300 400 500 600
(b)
pFET
h_{NW}: 12 nm
28 nm
39 nm
w_{NW}=19 nm
planar SOI
I_{ON} (μA/μm)
Gate Length (nm)
0
200
400
600
800
0 100 200 300 400 500 600

Figure 5.

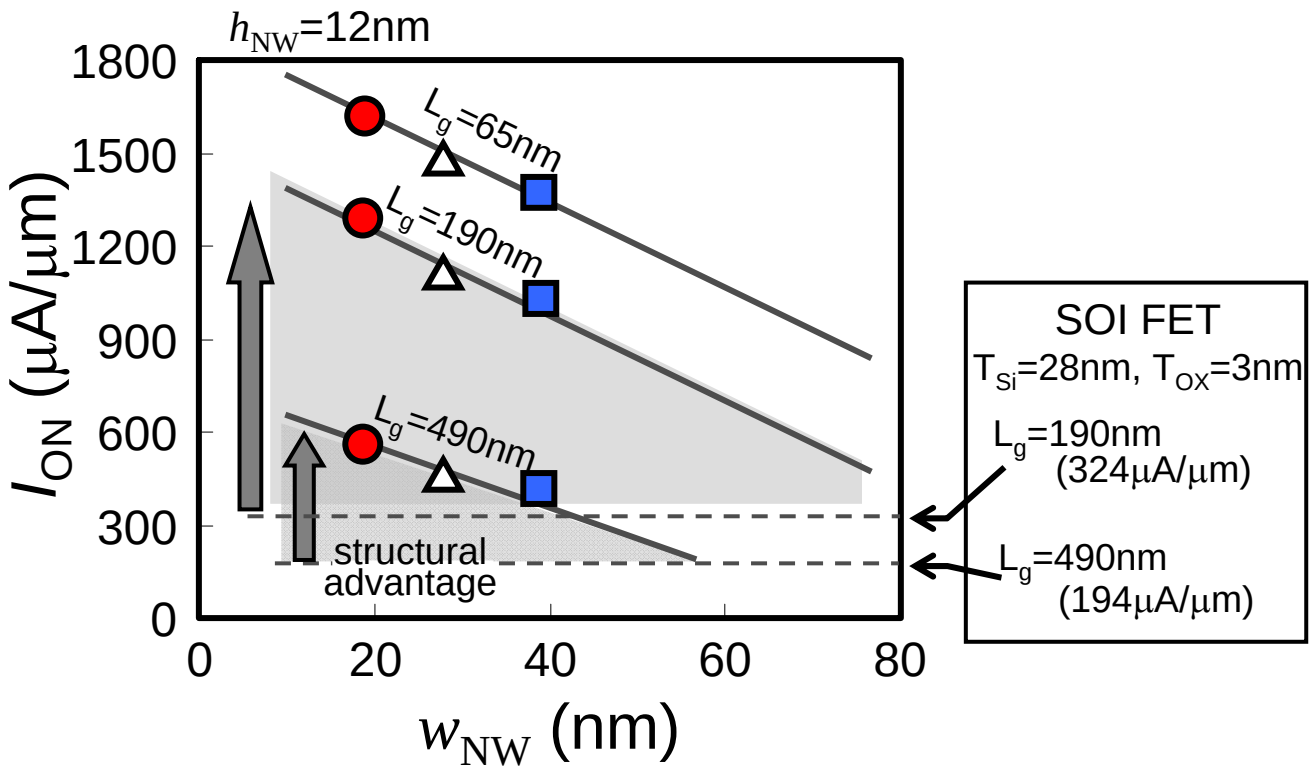

h_{NW}=12nm
1800
1500
1200
900
600
300
0
I_{ON} (μA/μm)
0
20
40
60
80
w_{NW} (nm)
L_g=65nm
L_g=190nm
L_g=490nm
structural advantage
SOI FET
T_{Si}=28nm, T_{OX}=3nm
L_g=190nm (324μA/μm)
L_g=490nm (194μA/μm)

Figure 6.

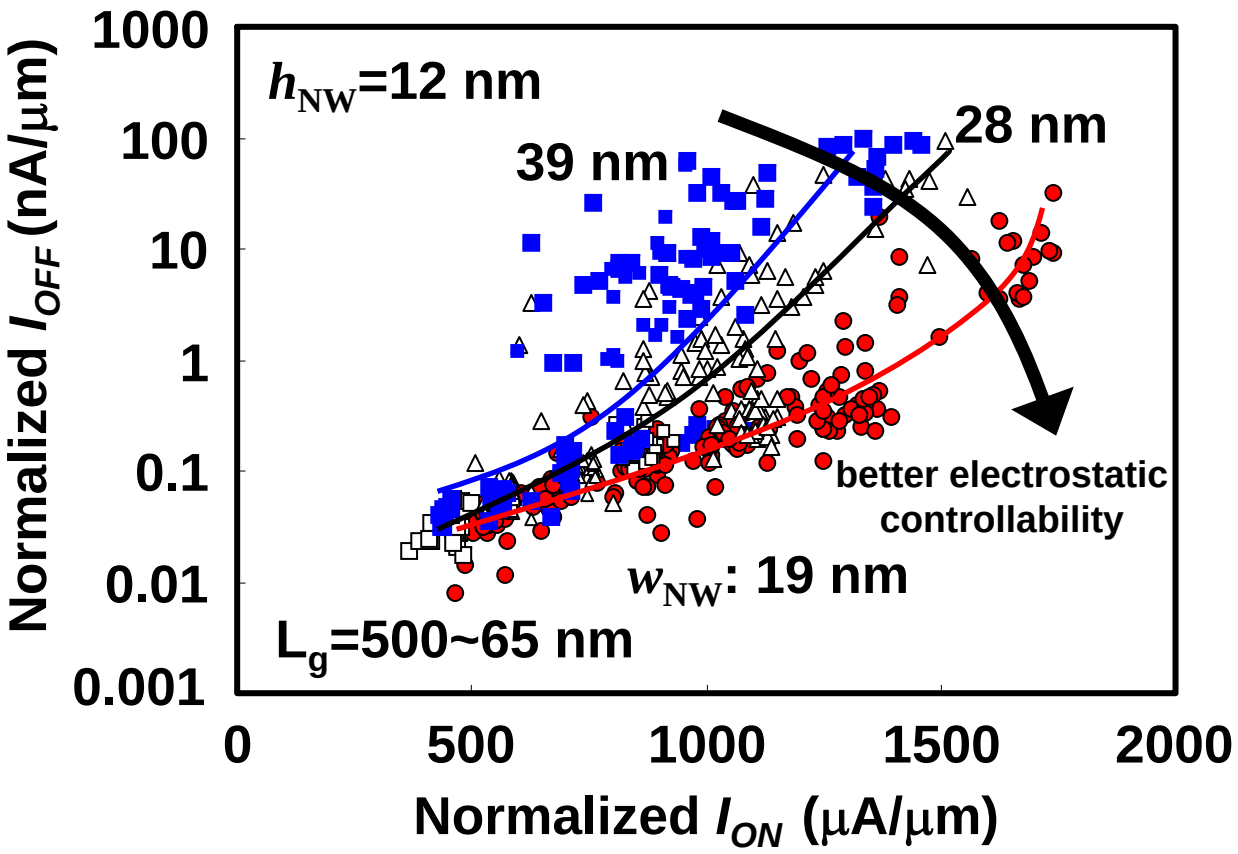

1000
100
10
1
0.1
0.01
0.001
Normalized I_{OFF} (nA/μm)
h_{NW}=12 nm
39 nm
28 nm
better electrostatic controllability
w_{NW}: 19 nm
L_g=500~65 nm
0
500
1000
1500
2000
Normalized I_{ON} (μA/μm)

Figure 7.

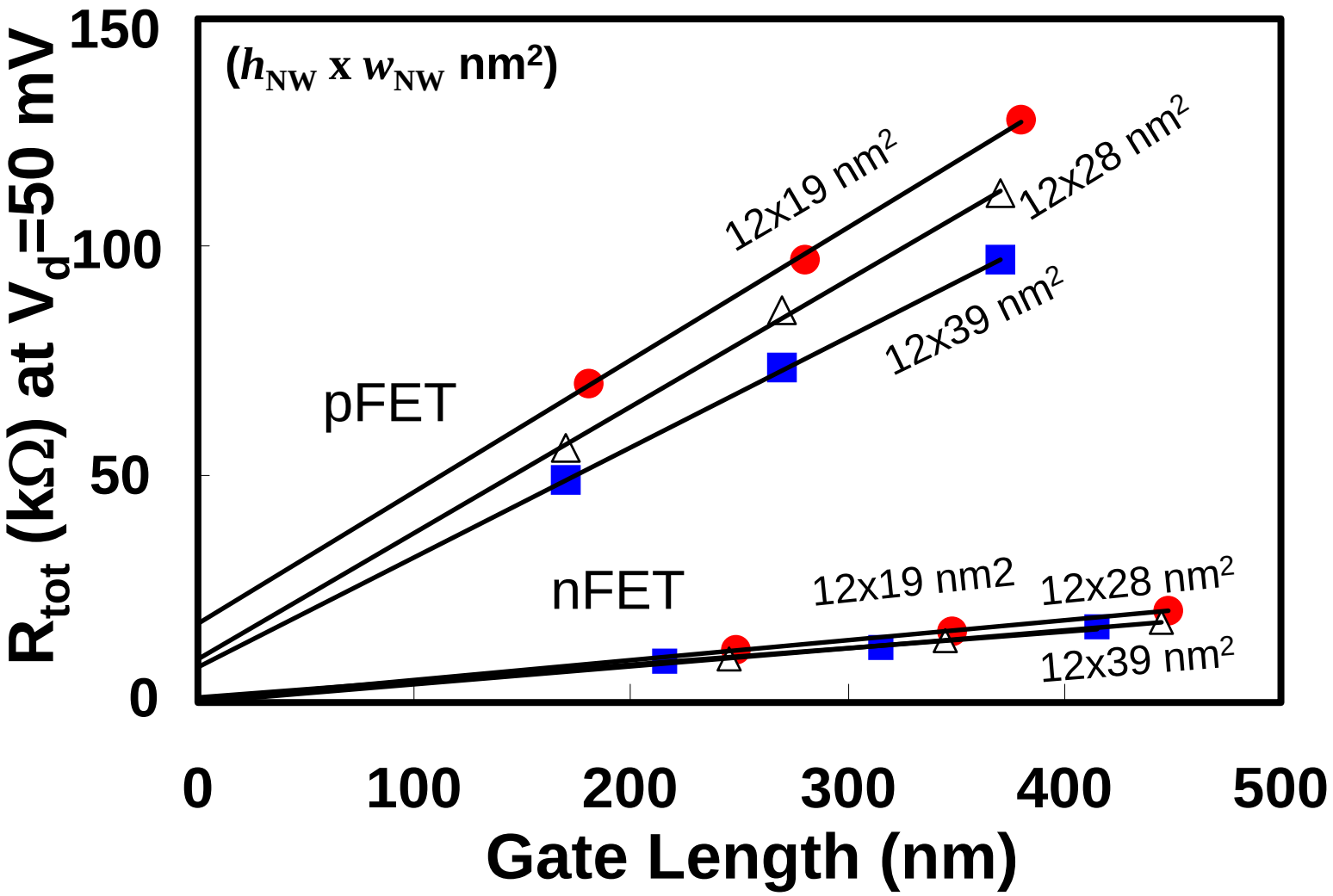

(h_{NW} x w_{NW} nm²)
12x19 nm²
12x28 nm²
12x39 nm²
pFET
nFET
12x19 nm2
12x28 nm²
12x39 nm²
R_{tot} (kΩ) at V_d=50 mV
150
100
50
0
0
100
200
300
400
500
Gate Length (nm)

Figure 8.

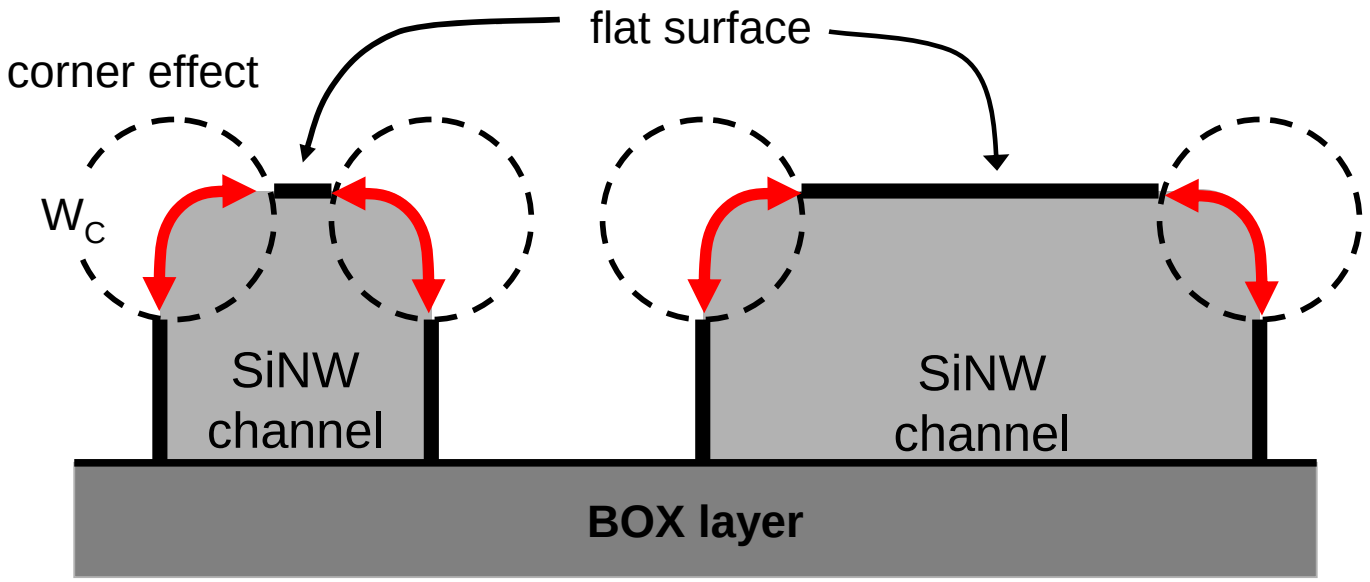

flat surface
corner effect
W_C
SiNW channel
SiNW channel
BOX layer

Figure 9.

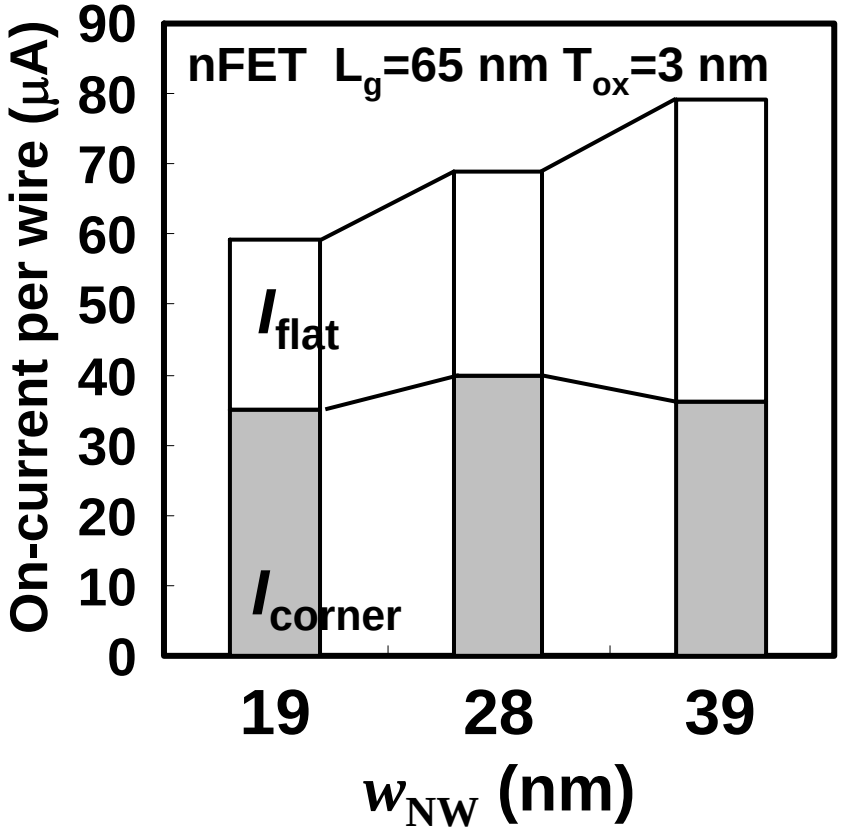

nFET L_g=65 nm T_{ox}=3 nm
On-current per wire (μA)
90
80
70
60
50
40
30
20
10
0
I_{flat}
I_{corner}
19
28
39
w_{NW} (nm)

Figure 10.

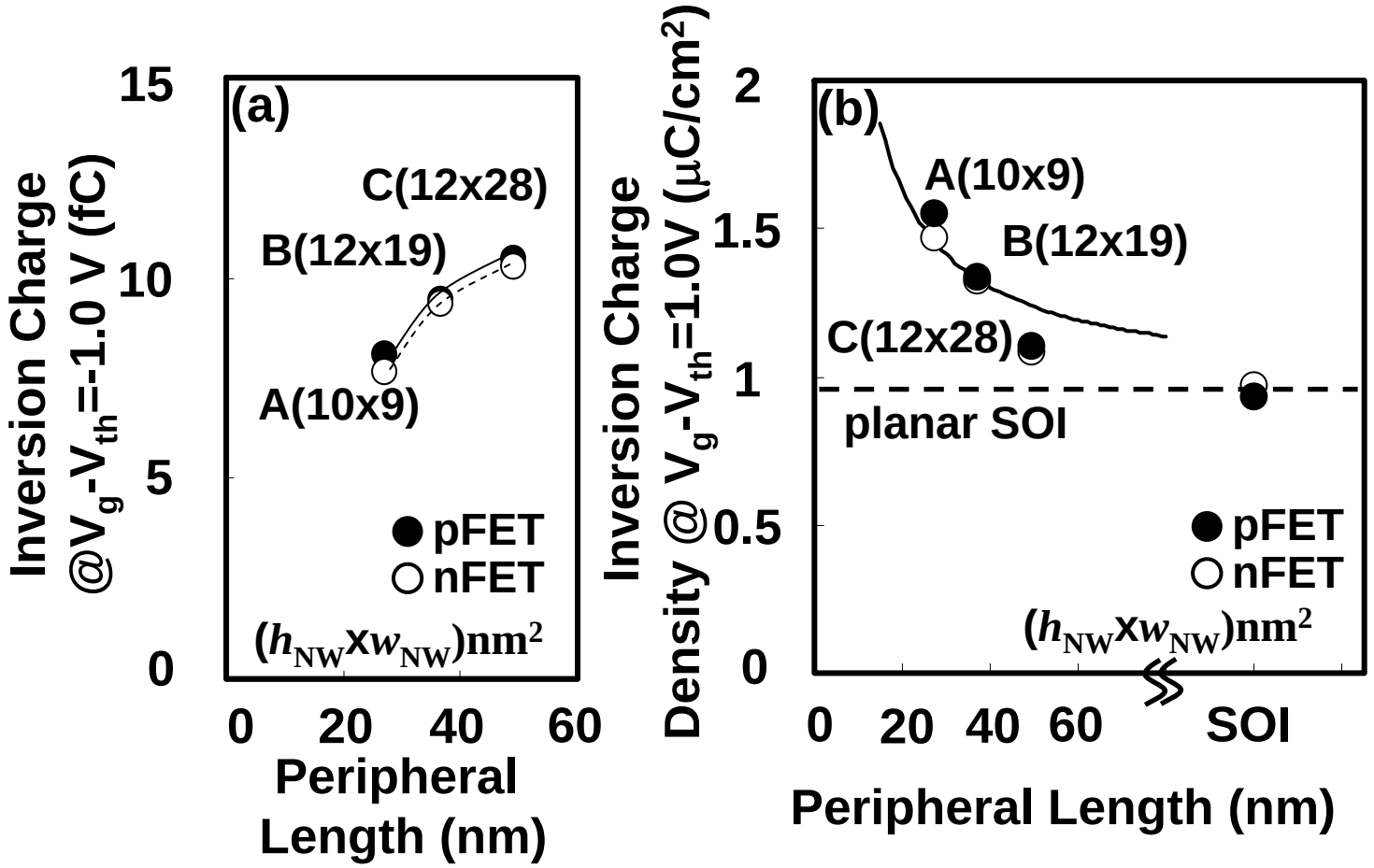

(a)
C(12x28)
B(12x19)
A(10x9)
pFET
nFET
(h_{NW}xw_{NW})nm^2
Inversion Charge
@V_g-V_{th}=-1.0 V (fC)
15
10
5
0
0
20
40
60
Peripheral
Length (nm)
(b)
A(10x9)
B(12x19)
C(12x28)
planar SOI
pFET
nFET
(h_{NW}xw_{NW})nm^2
Inversion Charge
Density @ V_g-V_{th}=1.0V (μC/cm^2)
2
1.5
1
0.5
0
0
20
40
60
SOI
Peripheral Length (nm)

Figure 11.

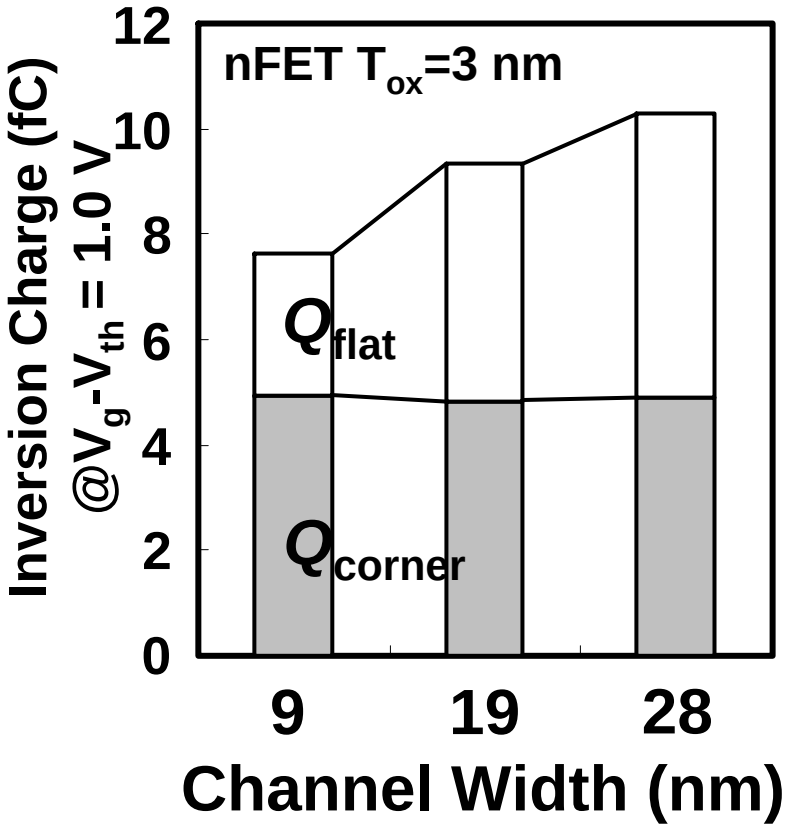

nFET T_{ox}=3 nm
Inversion Charge (fC)
@V_g-V_{th} = 1.0 V
12
10
8
6
4
2
0
Q_{flat}
Q_{corner}
9
19
28
Channel Width (nm)

Figure 12(a).

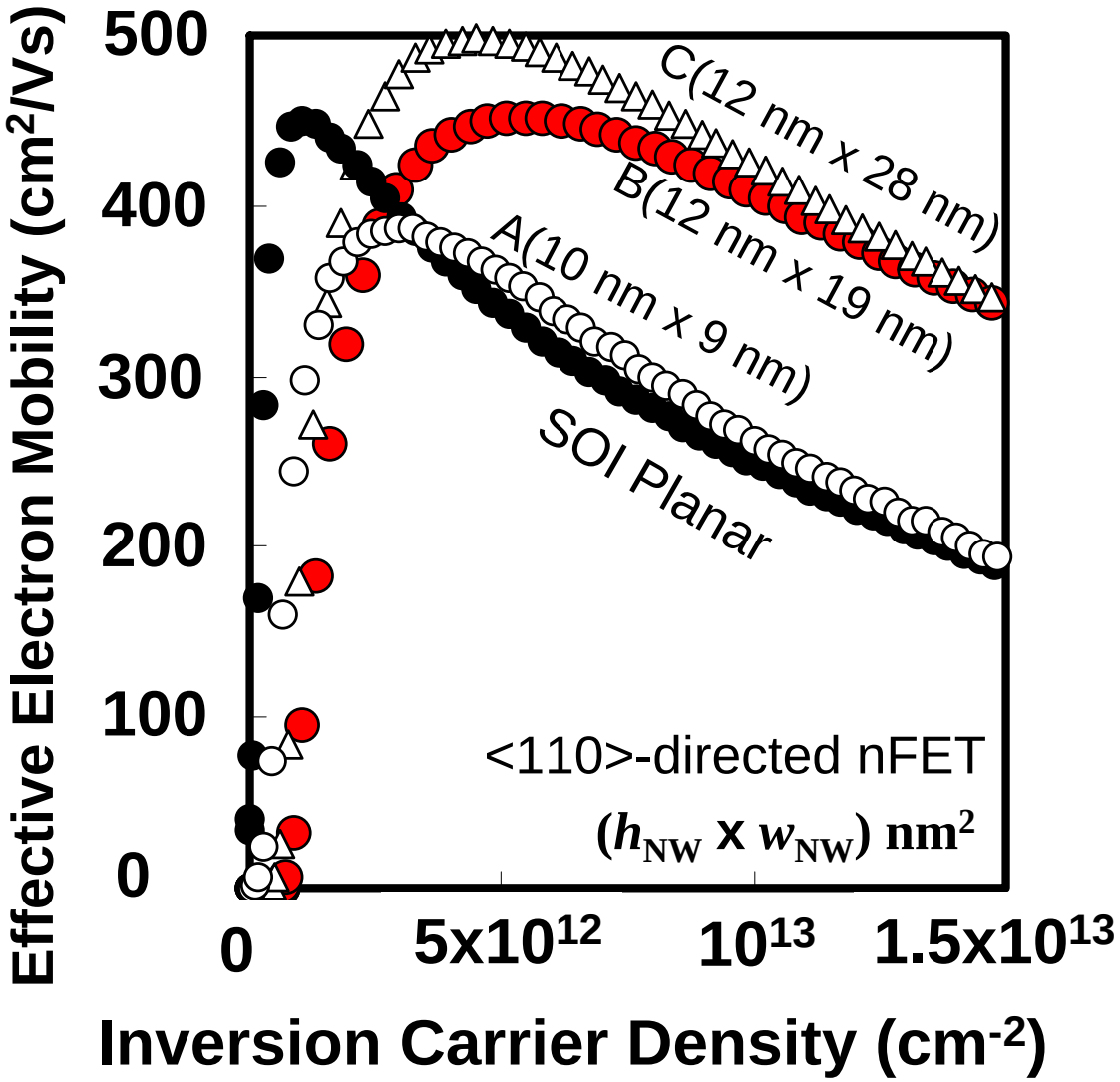

Effective Electron Mobility (cm²/Vs)
500
400
300
200
100
0
0
5x10¹²
10¹³
1.5x10¹³
Inversion Carrier Density (cm⁻²)
C(12 nm x 28 nm)
B(12 nm x 19 nm)
A(10 nm x 9 nm)
SOI Planar
<110>-directed nFET
(h_NW x w_NW) nm²

Figure 12(b).

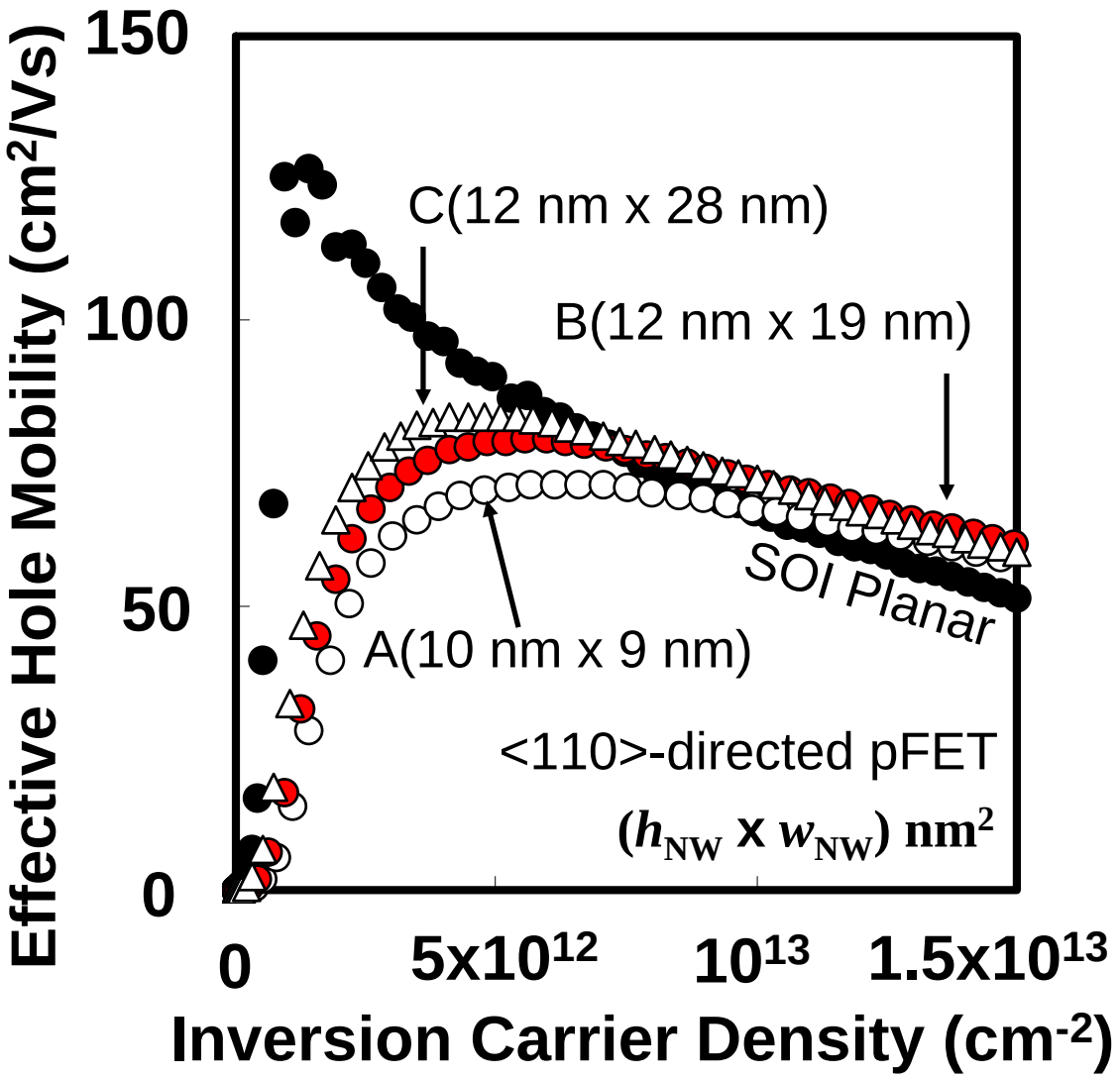
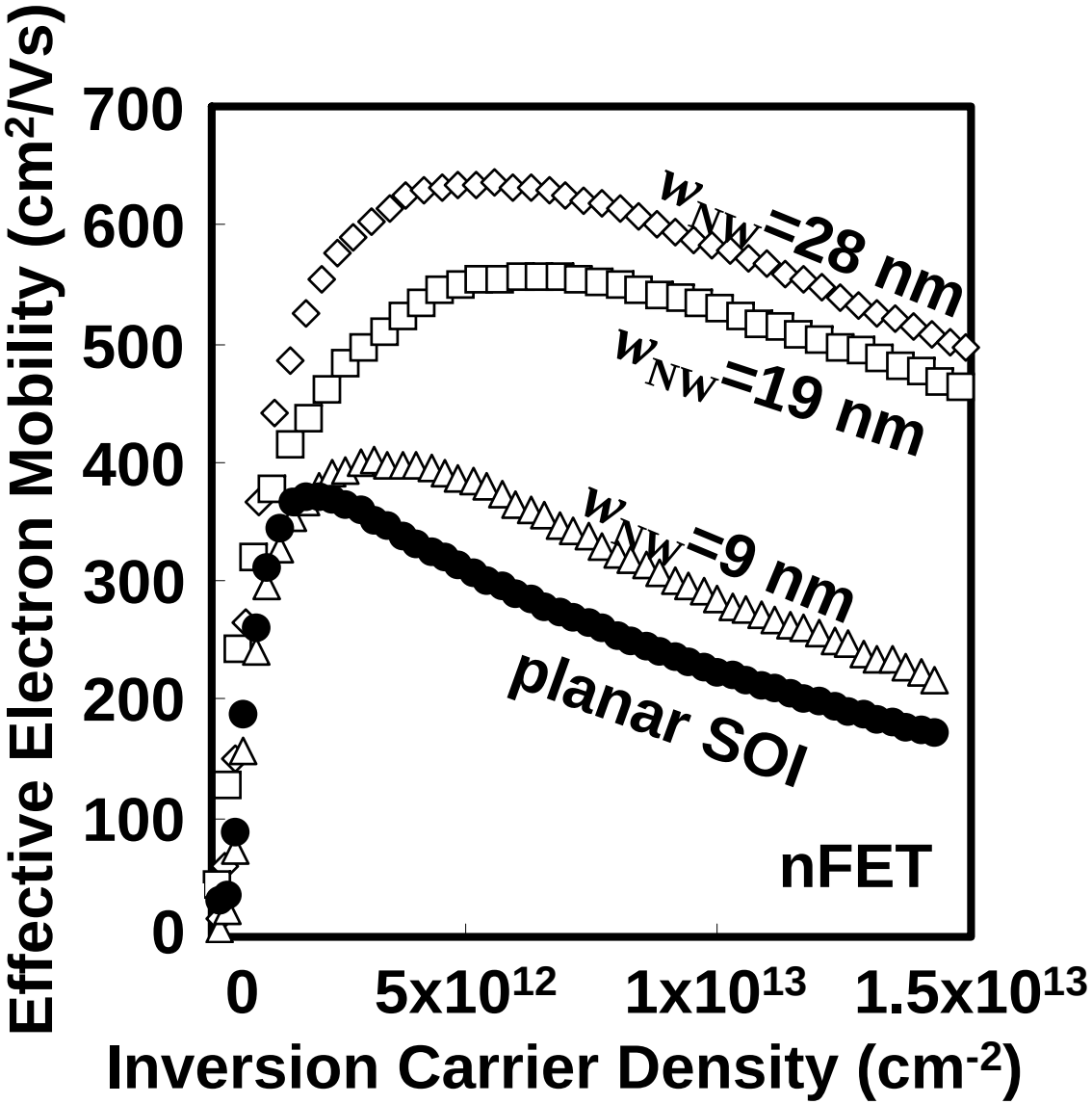

150
100
50
0
Effective Hole Mobility (cm²/Vs)
C(12 nm x 28 nm)
B(12 nm x 19 nm)
SOI Planar
A(10 nm x 9 nm)
<110>-directed pFET
(h_NW x w_NW) nm²
0
5x10¹²
10¹³
1.5x10¹³
Inversion Carrier Density (cm⁻²)

Figure 13.


Effective Electron Mobility (cm²/Vs)
700
600
500
400
300
200
100
0
0
5x10¹²
1x10¹³
1.5x10¹³
Inversion Carrier Density (cm⁻²)
w_NW=28 nm
w_NW=19 nm
w_NW=9 nm
planar SOI
nFET