Applied Physics Letters

Polycrystalline thin-film transistors fabricated on high-mobility solid-phase-crystallized Ge on glass

Cite as: Appl. Phys. Lett. **114**, 212107 (2019); https://doi.org/10.1063/1.5093952
Submitted: 26 February 2019 . Accepted: 12 May 2019 . Published Online: 31 May 2019

K. Moto, K. Yamamoto, T. Imajo, T. Suemasu, H. Nakashima, and K. Toko

Applied Physics Letters ARTICLE scitation.org/journal/apl

Polycrystalline thin-film transistors fabricated on high-mobility solid-phase-crystallized Ge on glass

Cite as: Appl. Phys. Lett. **114**, 212107 (2019); doi: 10.1063/1.5093952
Submitted: 26 February 2019 · Accepted: 12 May 2019 ·
Published Online: 31 May 2019

K. Moto,[1,2] K. Yamamoto,[3,a)] T. Imajo,[1] T. Suemasu,[1] H. Nakashima,[4] and K. Toko[1,5,a)]

AFFILIATIONS

[1]Institute of Applied Physics, University of Tsukuba, 1-1-1 Tennodai, Tsukuba, Ibaraki 305-8573, Japan
[2]JSPS Research Fellow, 8 Ichiban-cho, Chiyoda-ku, Tokyo 102-8472, Japan
[3]Interdisciplinary Graduate School of Engineering Science, Kyushu University, Kasuga, Fukuoka 816-8580, Japan
[4]Global Innovation Center, Kyushu University, Kasuga, Fukuoka 816-8580, Japan
[5]PRESTO, Japan Science and Technology Agency, 4-1-8 Honcho, Kawaguchi, Saitama 332-0012, Japan

[a)]**Authors to whom correspondence should be addressed:** yamamoto.keisuke.380@m.kyushu-u.ac.jp **and** toko@bk.tsukuba.ac.jp

ABSTRACT

Low-temperature formation of Ge thin-film transistors (TFTs) on insulators has been widely investigated to improve the performance of Si large-scale integrated circuits and mobile terminals. Here, we studied the relationship between the electrical properties of polycrystalline Ge and its TFT performance using high-mobility Ge formed on glass using our recently developed solid-phase crystallization technique. The field-effect mobility μ_{FE} and on/off currents of the accumulation-mode TFTs directly reflected the Hall hole mobility μ_{Hall}, hole concentration, and film thickness of Ge. By thinning the 100-nm thick Ge layer with a large grain size (3.7 μm), we achieved a high μ_{Hall} (190 cm^2/Vs) in a 55-nm thick film that was almost thin enough to fully deplete the channel. The TFT using this Ge layer exhibited both high μ_{FE} (170 cm^2/Vs) and on/off current ratios ($\sim 10^2$). This is the highest μ_{FE} among low-temperature ($<500\,^{\circ}C$) polycrystalline Ge TFTs without minimizing the channel region ($<1\,\mu$m).

Ge has attracted attention as the most promising candidate for post-Si materials because it has a higher carrier mobility than Si and is compatible with the conventional Si process. Ge metal-oxide-semiconductor field-effect transistor (MOSFET) mobilities have exceeded those of Si-MOSFETs because of the development of device technologies including gate stacks.[1–6] However, leakage current in bulk Ge is inevitable because of the narrow bandgap (0.66 eV). Ge-on-insulator (GOI) technology is the most promising solution. High quality GOI structures have been obtained by mechanical transfer,[7–9] oxidation-induced condensation,[5,10] rapid-melting growth,[11–14] and lamp annealing.[15,16] The GOI structure formed by these methods effectively suppresses the leakage current and improves the device performance of Ge-MOSFETs. These results demonstrate the potential of Ge transistors; however, their application is limited because these methods require a single-crystal wafer or high temperature process ($>500\,^{\circ}C$).

Research on low-temperature synthesis of polycrystalline Ge (poly-Ge) thin films on insulators has been conducted for decades. This enables monolithic integration of high-performance Ge thin-film transistors (TFTs) into Si-large-scale integrated circuits (LSIs) and flat panel displays. Ge-TFTs have been established using poly-Ge formed by solid-phase crystallization (SPC),[17–20] laser annealing,[21] seed layer technique,[22] and metal-induced crystallization.[23–27] Poly-Ge generally has a high hole concentration p because of defect-induced acceptors and low Hall effect hole mobility μ_{Hall} due to grain boundary scattering.[18,28] Although the miniaturization of the channel region ($<1\,\mu$m) and the multigate structure have successfully reduced the leakage current and improved MOSFET mobility, the crystallinity of poly-Ge is insufficient to overcome the performance of Ge-TFTs over Si-MOSFETs. To improve the performance of Ge-TFTs, it is essential not only to enhance the crystallinity of poly-Ge but also to comprehensively study the relationship between its electrical properties and TFT characteristics.

SPC progresses in two steps: nucleation and subsequent lateral growth. Because the grain size is determined by the balance between the nucleation frequency and the lateral growth rate, there is a possibility of enlarging the grain size by devising growth conditions.[18] We recently found that the densification of the amorphous Ge (a-Ge) precursor significantly enlarged the grain size of poly-Ge due to lateral

growth promotion in SPC.[29] Moreover, the precursor densification reduced the trap-state density (4.4×10^{11} cm^{-2}) and energy barrier height (6.4 meV) of the grain boundary, resulting in a μ_{Hall} of 340 cm^2/Vs.[29] Additionally, μ_{Hall} was updated to 620 cm^2/Vs by thickening a-Ge, postannealing at 500 °C, and inserting GeO_2 underlayer.[30,31] This μ_{Hall} is the highest ever recorded for a thin film directly grown on an insulator at temperatures below 900 °C. In the present study, we fabricate poly-Ge TFTs using SPC-Ge and discuss the relationship between the film properties (thickness, μ_{Hall}, and p) and TFT characteristics (field-effect mobility: μ_{FE} and on/off currents). We demonstrate the highest μ_{FE} among low-temperature (<500 °C) poly-Ge TFTs without minimizing the channel region.

The a-Ge layers were deposited on SiO_2 glass substrates using the Knudsen cell of a molecular beam deposition system (base pressure: 5×10^{-7} Pa). The initial film thickness of the a-Ge layer, t_i, ranged from 25 to 200 nm. The Ge layers were densified by heating the substrate at 125 °C during deposition.[29] The samples were then loaded into a conventional tube furnace in an N_2 atmosphere and annealed at 450 °C for 5 h to induce SPC. Figures 1(a)–1(e) show the crystal orientation maps obtained by electron backscattering diffraction (EBSD). The EBSD images indicate that the grain size dramatically varies with t_i, while the crystal orientation is almost random for all t_i. Figure 1(f) shows that the highest grain size is obtained at t_i = 100 nm. This behavior likely reflects the balance of the precursor density and the stress in the Ge film. The heating deposition densifies the precursor at $t_i > 50$ nm, while the precursor density remains low at $t_i \leq 50$ nm.[29,30] For $t_i > 50$ nm where the precursor is densified, the grain size increases due to the lateral growth promotion. Conversely, in SPC, heterogeneous nucleation occurs at the film surface or substrate interface. The thin films have stress due to the difference in thermal expansion coefficients with the substrates, which retard the nucleation.[32] The thicker film makes the surface stress more relaxed and then makes surface nucleation more likely to occur, resulting in a smaller grain size. Reflecting the balance, the grain size is maximized at t_i = 100 nm. We used Hall effect measurements to evaluate the electrical properties of the SPC-Ge layers. All samples showed p-type conduction because the defects in Ge provide shallow acceptor levels that generate holes at room temperature.[28] Therefore, larger grain sizes, that is, fewer grain boundaries, provide lower p, as shown in Figs. 1(f) and 1(g). Figure 1(g) also shows that μ_{Hall} peaks at t_i = 200 nm, whereas the grain size peaks at t_i = 100 nm. This behavior is likely attributed to the carrier scattering near the Ge/SiO_2 interface.[30] Because the interface scattering is weaker for the thicker film, t_i = 200 nm exhibits higher μ_{Hall} than t_i = 100 nm.

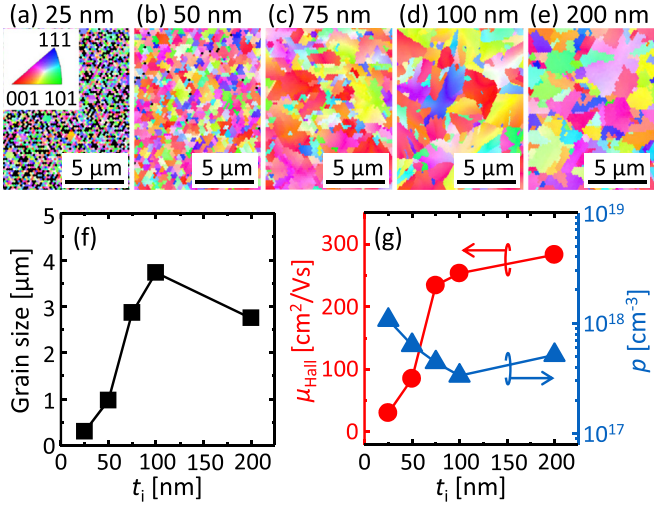

FIG. 1. Initial film thickness t_i dependence of the grain size and electrical properties of the SPC-Ge layers. (a)–(e) EBSD images with various t_i values (25, 50, 75, 100, and 200 nm). The colors indicate the crystal orientation, according to the inserted color key. (f) Average grain size determined by EBSD analyses. (g) Hall hole mobility μ_{Hall} and hole concentration p obtained by the Hall effect measurement with the van der Pauw method as a function of t_i.

We fabricated accumulation-mode metal source/drain (S/D) p-channel TFTs using SPC-Ge with different t_i values (Fig. 1). Figure 2 shows the process and structure. First, SPC-Ge on glass was isolated into a 55- × 155-μm^2 rectangle using a diluted H_2O_2 solution.[2] Then, sacrificial oxidation was performed by electron cyclotron resonance (ECR) plasma oxidation forming GeO_2 (1 nm thick). After removing the sacrificial oxide by wet treatment, photoresist was coated and patterned into S/D shape rectangles on both sides of the isolated Ge island. Pt and TiN (each 10 nm thick) as metal S/Ds were sequentially deposited using radio-frequency magnetron sputtering and patterned by removal of photoresist. Postmetallization annealing (PMA) was performed at 400 °C for 30 min in N_2 to form PtGe/Ge contacts. The PtGe/Ge contacts have a low hole barrier height and are suitable for accumulation-mode p-channel Ge-TFTs.[33] We used Al/SiO_2/Al_2O_3/SiO_2/GeO_2 for the gate stack. GeO_2 (3 nm thick) was formed by ECR plasma oxidation at 130 °C and protected with an SiO_2 film (2 nm thick). Al_2O_3 (20 nm thick) was then deposited using atomic layer

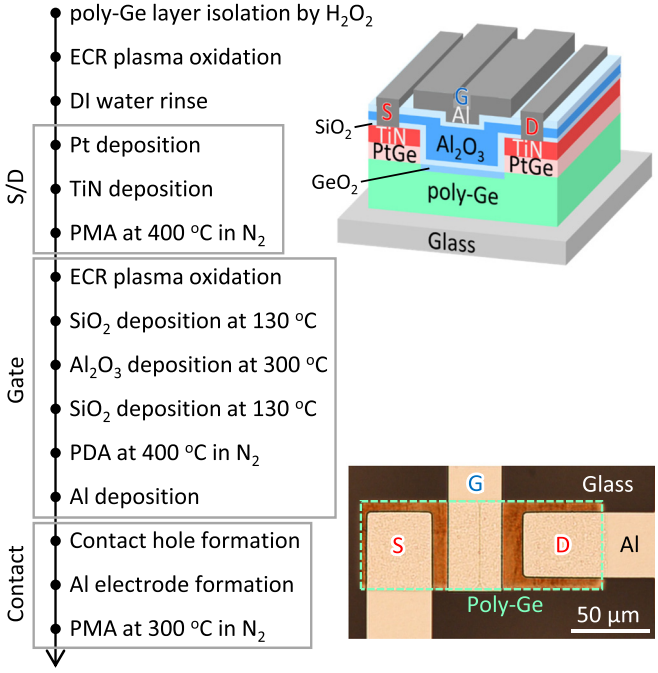

FIG. 2. Fabrication process flow (left) and schematic and an optical micrograph (right) of the p-channel SPC-Ge TFTs.

deposition at 300 °C. This Al_2O_3 film electrically isolates the sidewall of metal S/D and the gate electrode. To protect Al_2O_3 during gate electrode patterning, SiO_2 (5 nm thick) was deposited by ECR plasma sputtering at 130 °C. Subsequently, postdeposition annealing (PDA) was performed at 400 °C for 30 min in N_2. As a gate electrode, Al (200 nm thick) was deposited using vacuum evaporation and patterned by wet etching. A contact hole was opened and an Al electrode (100 nm thick) was deposited using vacuum evaporation and patterned by a lift-off process. Finally, contact annealing was performed at 300 °C for 30 min in N_2. The channel width and length (W/L) were 55 and 5–15 μm, respectively (Fig. 2). Here, all processes including SPC were conducted below 450 °C.

We estimated μ_{FE} of the TFTs using the following equation:

$$\mu_{FE} = g_m \frac{L}{W} \frac{1}{C_{ox} V_D}, \quad (1)$$

where transconductance g_m was obtained from the drain current (I_D)-gate voltage (V_G) characteristics. The gate oxide capacitance C_{ox}, determined from the capacitance-voltage characteristics of the MOS capacitor with the same gate stack fabricated on the bulk Ge substrate, was 0.20 μF/cm^2 corresponding to the equivalent oxide thickness of 17.7 nm. The drain voltage V_D was fixed at −0.1 V. Figures 3(a)–3(d) show that the I_D–V_G and μ_{FE} characteristics vary significantly with t_i. Figure 3(e) shows on current I_{on}, off current I_{off}, and on/off current ratio I_{on}/I_{off} estimated from the I_D–V_G characteristics. I_{on} increases with increasing t_i, which reflects μ_{Hall} [Fig. 1(g)] and exhibits high values ($>10^{-4}$ A) at $t_i \geq 100$ nm. I_{off} is determined by the relationship between t_i and the maximum depletion layer width d_{max}, which can be estimated from p. For example, the d_{max} of Ge when $p = 3 \times 10^{17}$ cm^{-3} is approximately 54 nm, assuming that the dielectric constant and intrinsic carrier concentration of Ge are 16 and 2.4×10^{13} cm^{-3} at room temperature,[6] respectively. From the relationship between d_{max} and t_i, we found that the lower t_i provides the higher occupation of the depletion layer in the whole SPC-Ge layer, which decreases I_{off} [Fig. 3(e)]. Reflecting I_{on} and I_{off}, I_{on}/I_{off} reaches the maximum at $t_i = 50$ nm. Figure 3(f) shows that μ_{FE} is consistent with the trend of μ_{Hall} reflecting the properties of SPC-Ge, while μ_{FE} is much lower than μ_{Hall}. This is likely because not only carrier scattering at the MOS interface but also large I_{off} causes underestimation of g_m and μ_{FE}. To overcome this problem, a-Ge layer compatible with high μ_{Hall} (corresponding high I_{on}) and a thin film (corresponding low I_{off}) is desirable.

Considering the aspect ratio of the grain size and film thickness for $t_i \geq 50$ nm, the grain size is constant in the depth direction for each t_i. The influence of the carrier scattering near the Ge/SiO_2 interface should be identical at the same thickness. Therefore, for achieving high μ_{Hall} with a thin film, we thinned the $t_i = 100$ nm sample, which has the largest grain size [Fig. 1(f)], using chemical-mechanical polishing (CMP). Figure 4(a) shows that p is constant in the depth direction. According to d_{max} estimated from p, full depletion in SPC-Ge is obtained when the thinned film thickness t_{CMP} is below 55 nm. Conversely, μ_{Hall} decreases significantly for $t_{CMP} < 50$ nm [Fig. 4(b)], likely reflecting carrier scattering at the Ge/SiO_2 interface.[15,30] Therefore, we determined that $t_{CMP} = 55$ nm is almost optimal for achieving both high μ_{FE} and I_{on}/I_{off}. The $t_{CMP} = 55$ nm sample showed a smooth surface [Fig. 4(b), root mean square value: 1.3 nm], and the same grain size as before CMP. This sample was processed into TFTs by the procedure shown in Fig. 2. Figure 4(c) shows the

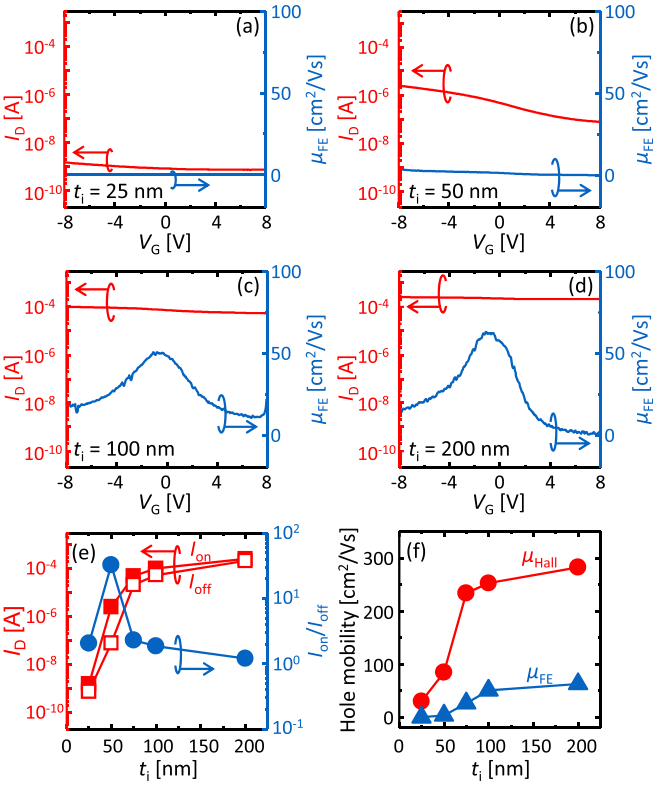

FIG. 3. Electrical properties of p-channel SPC-Ge TFTs with various initial film thickness t_i values, where channel length $L = 10$ μm. (a)–(d) I_D-V_G and field-effect mobility μ_{FE} characteristics at $V_D = -0.1$ V. (e) On current I_{on}, off current I_{off}, and on/off current ratio I_{on}/I_{off} and (f) μ_{FE} and Hall effect mobility μ_{Hall} as a function of t_i.

typical p-channel transistor operation, i.e., I_D increases with increasing V_G. Figure 4(d) shows high I_{on}/I_{off} (10^2) and μ_{FE} (170 cm^2/Vs) because of both the high I_{on} due to the high μ_{Hall} and low I_{off} due to the thin thickness (55 nm) in SPC-Ge. The current TFT performance is the highest among simple poly-Ge TFTs formed on glass and will be further improved by nanofabrication processes such as miniaturization of the channel region and multigate structure. For TFTs fabricated on polycrystalline semiconductors, their variability is also important. Specifically, it is more sensitive in the case of devices with a channel length comparable to the grain size like this study. The cumulative distribution of measured μ_{FE}s for different channel lengths (5, 10, and 15 μm) in the same substrate is shown in Fig. 4(e). The experimental data show a clear increase in variability as the channel length decreases, which is in good agreement with the trends reported in Ref. 34 from both the theoretical and experimental viewpoints. Device variability will also be improved by device design optimization for the corresponding grain size.

In conclusion, we studied the relationship between film properties (thickness, μ_{Hall}, and p) and TFT characteristics (μ_{FE} and I_{on}/I_{off}) using high-mobility poly-Ge layers formed on glass by SPC. Thicker t_i enabled higher μ_{FE} because of higher μ_{Hall}, while it enabled larger I_{off}, which led to poor I_{on}/I_{off}. These results indicated that both high μ_{Hall} and thin t_i are essential to achieve both high μ_{FE} and I_{on}/I_{off}. By thinning a 100-nm thick Ge layer with a large grain size (3.7 μm), we achieved a high μ_{Hall} (190 cm^2/Vs) at a thin film (55 nm) that is almost

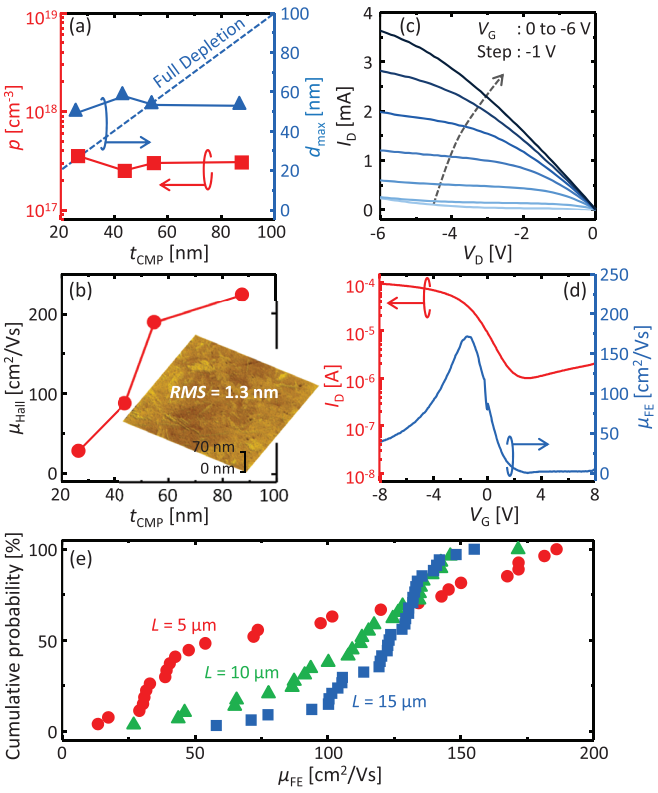

FIG. 4. (a) and (b) "In-depth" profiles of electrical properties for SPC-Ge layers for initial film thickness $t_i = 100$ nm. (a) Hole concentration p and maximum depletion layer width d_{max} estimated from p as a function of film thickness t_{CMP} thinned by using CMP. The dotted line shows the line when the Ge layer is fully depleted. (b) Hall hole mobility μ_{Hall} as a function of t_{CMP}. The inset in (b) shows the atomic force micrograph of SPC-Ge thinned to $t_{CMP} = 55$ nm with a scan region of $10 \times 10\ \mu m^2$. (c) I_D-V_D characteristics and (d) I_D-V_G characteristics and field-effect mobility μ_{FE} at $V_D = -0.1$ V for the SPC-Ge TFT thinned to $t_{CMP} = 55$ nm, where channel length $L = 10\ \mu m$. (e) Cumulative distribution of μ_{FE} with different L values.

thin enough to fully deplete the channel. The TFT using this Ge layer exhibited high μ_{FE} (170 cm^2/Vs) and I_{on}/I_{off} (10^2). The μ_{FE} value is the highest among low-temperature (<500 °C) polycrystalline Ge TFTs without minimizing the channel region (<1 μm). The findings in the present study will contribute to the development of high-performance poly-Ge-TFTs that exceed Si-MOSFETs and lead to advanced three-dimensional LSIs and multifunctional mobile terminals.

This work was financially supported by a Grant-in-Aid for JSPS Research Fellows (No. 17J00544), the Murata Science Foundation, and JST PRESTO (No. JPMJPR17R7). The authors are grateful to Dr. T. Sakurai (University of Tsukuba) for assistance with the Hall effect measurements. EBSD measurements were conducted at the International Center for Young Scientists at NIMS.

REFERENCES

[1]A. Nayfeh, C. O. Chui, T. Yonehara, and K. C. Saraswat, IEEE Electron Device Lett. **26**, 311 (2005).
[2]D. P. Brunco, B. De Jaeger, G. Eneman, J. Mitard, G. Hellings, A. Satta, V. Terzieva, L. Souriau, F. E. Leys, G. Pourtois, M. Houssa, G. Winderickx, E. Vrancken, S. Sioncke, K. Opsomer, G. Nicholas, M. Caymax, A. Stesmans, J. Van Steenbergen, P. W. Mertens, M. Meuris, and M. M. Heyns, J. Electrochem. Soc. **155**, H552 (2008).
[3]R. Pillarisetty, Nature **479**, 324 (2011).
[4]K. Yamamoto, T. Sada, D. Wang, and H. Nakashima, Appl. Phys. Lett. **103**, 122106 (2013).
[5]S. Takagi, R. Zhang, J. Suh, S.-H. Kim, M. Yokoyama, K. Nishi, and M. Takenaka, Jpn. J. Appl. Phys. Part 1 **54**, 06FA01 (2015).
[6]A. Toriumi and T. Nishimura, Jpn. J. Appl. Phys. Part 1 **57**, 010101 (2018).
[7]G. Taraschi, A. J. Pitera, and E. A. Fitzgerald, Solid-State Electron. **48**, 1297 (2004).
[8]Y. Moriyama, K. Ikeda, Y. Kamimuta, M. Oda, T. Irisawa, Y. Nakamura, A. Sakai, and T. Tezuka, Solid-State Electron. **83**, 42 (2013).
[9]K. Yu, F. Yang, H. Cong, L. Zhou, Q. Liu, L. Zhang, B. Cheng, C. Xue, Y. Zuo, and C. Li, J. Alloys Compd. **750**, 182 (2018).
[10]T. Maeda, K. Ikeda, S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. Takagi, Thin Solid Films **508**, 346 (2006).
[11]J. Feng, G. Thareja, M. Kobayashi, S. Chen, A. Poon, Y. Bai, P. B. Griffin, S. S. Wong, Y. Nishi, and J. D. Plummer, IEEE Electron Device Lett. **29**, 805 (2008).
[12]S. Hu, P. W. Leu, A. F. Marshall, and P. C. McIntyre, Nat. Nanotechnol. **4**, 649 (2009).
[13]K. Toko, Y. Ohta, T. Tanaka, T. Sadoh, and M. Miyao, Appl. Phys. Lett. **99**, 032103 (2011).
[14]T. Hosoi, Y. Suzuki, T. Shimura, and H. Watanabe, Appl. Phys. Lett. **105**, 173502 (2014).
[15]K. Usuda, Y. Kamata, Y. Kamimuta, T. Mori, M. Koike, and T. Tezuka, Appl. Phys. Express **7**, 056501 (2014).
[16]Y. Kamata, M. Koike, E. Kurosawa, M. Kurosawa, H. Ota, O. Nakatsuka, S. Zaima, and T. Tezuka, Appl. Phys. Express **7**, 121302 (2014).
[17]T. Sadoh, H. Kamizuru, A. Kenjo, and M. Miyao, Appl. Phys. Lett. **89**, 192114 (2006).
[18]K. Toko, I. Nakao, T. Sadoh, T. Noguchi, and M. Miyao, Solid-State Electron. **53**, 1159 (2009).
[19]A. Hara, Y. Nishimura, and H. Ohsawa, Jpn. J. Appl. Phys. Part 1 **56**, 03BB01 (2017).
[20]S. Kabuyanagi, T. Nishimura, K. Nagashio, and A. Toriumi, Thin Solid Films **557**, 334 (2014).
[21]H. A. Kasirajan, W.-H. Huang, M.-H. Kao, H.-H. Wang, J.-M. Shieh, F.-M. Pan, and C.-H. Shen, Appl. Phys. Express **11**, 101305 (2018).
[22]M. Asadirad, Y. Gao, P. Dutta, S. Shervin, S. Sun, S. Ravipati, S. H. Kim, Y. Yao, K. H. Lee, A. P. Litvinchuk, V. Selvamanickam, and J.-H. Ryou, Adv. Electron. Mater. **2**, 1600041 (2016).
[23]B. Hekmatshoar, S. Mohajerzadeh, D. Shahrjerdi, and M. D. Robertson, Appl. Phys. Lett. **85**, 1054 (2004).
[24]K. Toko, R. Numata, N. Oya, N. Fukata, N. Usami, and T. Suemasu, Appl. Phys. Lett. **104**, 22106 (2014).
[25]K. Kasahara, Y. Nagatomi, K. Yamamoto, H. Higashi, M. Nakano, S. Yamada, D. Wang, H. Nakashima, and K. Hamaya, Appl. Phys. Lett. **107**, 142102 (2015).
[26]T. Suzuki, B. M. Joseph, M. Fukai, M. Kamiko, and K. Kyuno, Appl. Phys. Express **10**, 095502 (2017).
[27]H. Higashi, K. Kudo, K. Yamamoto, S. Yamada, T. Kanashima, I. Tsunoda, H. Nakashima, and K. Hamaya, J. Appl. Phys. **123**, 215704 (2018).
[28]H. Haesslein, R. Sielemann, and C. Zistl, Phys. Rev. Lett. **80**, 2626 (1998).
[29]K. Toko, R. Yoshimine, K. Moto, and T. Suemasu, Sci. Rep. **7**, 16981 (2017).
[30]R. Yoshimine, K. Moto, T. Suemasu, and K. Toko, Appl. Phys. Express **11**, 031302 (2018).
[31]T. Imajo, K. Moto, R. Yoshimine, T. Suemasu, and K. Toko, Appl. Phys. Express **12**, 015508 (2019).
[32]Y. Kimura, M. Kishi, and T. Katoda, J. Appl. Phys. **86**, 2278 (1999).
[33]A. Dimoulas, A. Toriumi, and S. E. Mohney, MRS Bull. **34**, 522 (2009).
[34]A. W. Wang and K. C. Saraswat, IEEE Trans. Electron Devices **47**, 1035 (2000).