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Citation: AIP Advances **8**, 085305 (2018); doi: 10.1063/1.5034048
View online: https://doi.org/10.1063/1.5034048
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Insight into enhanced field-effect mobility of 4H-SiC MOSFET with Ba incorporation studied by Hall effect measurements

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(Received 9 April 2018; accepted 27 July 2018; published online 7 August 2018)

Improved performance in 4H-SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) by incorporating Ba into insulator/SiC interfaces was investigated by using a combination of the Hall effect and split capacitance-voltage measurements. It was found that a moderate annealing temperature causes negligible metal-enhanced oxidation, which is rather beneficial for increments in field-effect mobility (μ_{FE}) of the FETs together with suppressed surface roughness of the gate oxides. The combined method revealed that, while severe μ_{FE} degradation in SiC-MOSFETs is caused by a reduction of effective mobile carriers due to carrier trapping at the SiO_2/SiC interfaces, Ba incorporation into the interface significantly increases mobile carrier density with greater impact than the widely-used nitrided interfaces. © *2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).*
https://doi.org/10.1063/1.5034048

Silicon carbide (SiC) is a wide bandgap semiconductor that has great potential in power device applications.[1] In addition to the superior physical properties of SiC, such as a very high breakdown field and good thermal conductivity over conventional Si, silicon dioxide (SiO_2) as a gate insulator in metal-oxide-semiconductor field-effect transistors (MOSFETs) can be grown by thermal oxidation of SiC substrates. However, the field-effect mobility (μ_{FE}) that determines the on-resistance of SiC-MOSFETs is still far below expectations.[2] This is due to the poor quality of thermally-grown SiO_2/SiC interfaces with a significant amount of electrical defects,[3,4] which leads to carrier trapping and scattering in the inversion channels of FETs. Although SiC-MOSFETs with a conventional thermal oxide exhibit low μ_{FE} values, typically less than 10 cm^2/Vs,[2] the incorporation of particular elements, i.e., hydrogen,[5] nitrogen,[6–8] and phosphorous[9] atoms, has been proven to passivate interface defects. Among these elements, nitrogen is known to provide reproducible μ_{FE} enhancement with minor drawbacks. Consequently, interface nitridation with high-temperature annealing in a nitric oxide (NO) ambience is widely used for fabricating state-of-the-art commercial SiC-MOSFETs. However, the resulting peak mobility of around 35 cm^2/Vs is insufficient,[8] so further improvement is indispensable for the development of next-generation SiC-MOSFETs.

The impacts of incorporating alkali metal and alkaline earth metal atoms into the SiO_2/SiC interfaces on mobility enhancement have been previously discussed. As with Si oxidation,[10–13] these elements are also known to have catalytic effects in thermal oxidation of SiC surfaces called metal-enhance oxidation (MEO).[14–21] The MEO phenomenon is beneficial for reducing oxidation temperatures and time, especially for SiC-MOS fabrication. However, the use of alkali metals, such

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as sodium and potassium, is unacceptable for practical applications owing to an ion drift (mobile charges) in the gate stacks causing severe bias-temperature instability (BTI) of MOSFETs. Recently, Lichtenwalner *et al.* demonstrated high mobility SiC-MOSFETs by incorporating barium (Ba) into the SiO_2/SiC interface,[17] in which the BTI due to the ion drift was remarkably suppressed thanks to the strong chemical bonding of Ba atoms to form a stable silicate phase. In the pioneering research, a few monolayer thick Ba films (ranging from 0.6 to 0.8 nm) were formed beneath the SiO_2 cap dielectrics, then oxidation annealing (MEO) in an O_2/N_2 gas mixture was conducted at 900 or 950°C. A subsequent study also reported the effect of stress relaxation near the Ba-passivated SiO_2/SiC interface on improved electrical properties.[18]

In spite of the promising aspects of SiC-MOSFETs with Ba-incorporated interfacial layers, very few cases of Ba-MEO have been reported so far. Previous research was done with limited conditions (Ba thickness ranging from 0.6 to 0.8 nm and MEO at 900 or 950°C).[17] Moreover, regarding mobility enhancement mechanisms, there has been no systematic report other than the strain analysis mentioned above. Despite some drawbacks of Ba-MEO relating to surface morphology and leakage current as described later, we think that understanding of mobility enhancement mechanisms provides a helpful clue to solve the long-standing problem of degraded field-effect mobility in SiC-MOSFETs. In the current study, we therefore explored optimal Ba-MEO conditions for further improvement of the SiC-MOS interface in the first step. Then, mechanisms of Ba-induced μ_{FE} increment were investigated by discriminating free (mobile) and trapped carriers from the total charge in the inversion channel by means of a combination of the Hall effect and split capacitance-voltage (C-V) measurements of SiC-MOSFETs.

In our previous study, a 0.5-nm-thick metallic Ba layer was directly deposited on a 4H-SiC(0001) substrate using a Knudsen effusion cell at room substrate temperature, followed by capping with the chemical vapor deposition (CVD) grown SiO_2 film. Then, MEO at 950°C was conducted in oxygen ambience.[19,20] We observed a reduction of interface state density (D_{it}) for the Ba-incorporated SiC-MOS capacitors after the prolonged MEO over four hours, but it was found that significant surface roughness leading to harmful electric field concentration in the gate dielectric was induced even on the CVD-grown SiO_2 surface with the MEO. Therefore, we reconsidered the oxidation temperature to improve surface morphology. Figure 1 shows the changes in the surface roughness and additive oxide growth depending on the MEO temperature. In this experiment, since MEO proved to occur with just a tiny amount of Ba atoms with an areal density on the order of 10^{14} cm^{-2},[19] a minimal Ba layer (0.1 nm thick) was directly deposited on the wet-cleaned 4H-SiC(0001) substrate with an n-type epilayer (N_d: 1×10^{16} cm^{-3}) purposed for improving surface morphology. The sample was covered with a 35-nm-thick SiO_2 capping layer with a plasma-enhanced CVD using

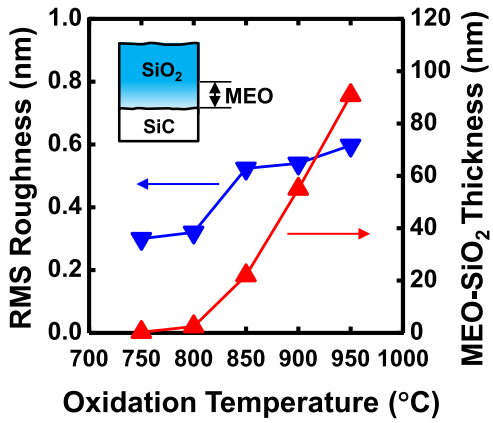


FIG. 1. Oxidation temperature dependence of additive SiO_2 growth and surface morphology induced by Ba-MEO. CVD-SiO_2(35 nm)/Ba(0.1 nm)/SiC stacked structures were annealed in O_2 ambience at various temperatures for 4 h. The additive oxide growth was estimated by subtracting initial thickness of CVD-SiO_2 (35 nm) from the measured value. The changes in the RMS roughness value (blue symbols) and additive oxide growth (red symbols) caused by Ba-MEO were plotted as a function of MEO temperature.

tetraethyl orthosilicate (TEOS) and oxygen (O_2) mixtures as reactant gases, followed by oxidation (Ba-MEO) at various temperatures in pure O_2 ambience for four hours. The resulting surface morphology (root mean square (RMS) roughness value) and thickness of the newly formed SiO_2 by Ba-MEO were evaluated by using atomic force microscopy (AFM) and spectroscopic ellipsometry (SE). As shown in Fig. 1, enhanced SiC oxidation by incorporating Ba was clearly observed at temperatures above 850°C (red symbols). It should be noted that, compared with our previous result with the 0.5-nm-thick Ba interfacial layer (RMS = 1.97 nm),[20] the RMS roughness values were significantly reduced to less than 0.6 nm by minimizing the amount of Ba atoms for MEO, indicating an impact with a reduction of the excess Ba atoms in an improved gate oxide surface morphology. In addition, the RMS values of the CVD-grown SiO_2 films remained almost constant at around 0.3 nm for the MEO temperatures below 850°C, which is a reasonable trend because additive Ba-MEO was negligible, probably a few monolayers in thickness, at this temperature range.

The electrical properties of these Ba-incorporated SiO_2/SiC interfaces were investigated by conventional C-V measurements. After performing Ba-MEO at various temperatures ranging from 750 to 900°C, Al gate electrodes and back contacts were formed by vacuum evaporation to fabricate SiC-MOS capacitors. Some samples were subjected to the post MEO annealing (POA) in pure N_2 ambience at 950°C for 30 min prior to electrode formation to improve the quality of the CVD-SiO_2 film and/or Ba-incorporated SiO_2/SiC interface. Figure 2 represents typical C-V characteristics of the SiC-MOS capacitors with and without POA in N_2 ambience. Bidirectional C-V curves were taken with 1 MHz measurement frequency, in which gate voltage was swept from depletion (-10 V) to accumulation (+10 V), and vice versa at room temperature. For both cases (MEO at 750 and 850°C), maximum accumulation capacitance coincides with the physical thickness of the gate oxides estimated by SE analysis. Moreover, whereas clockwise C-V hysteresis was observed before the POA (open symbols), hysteresis-free C-V curves were achieved with the POA regardless of the MEO temperature (closed symbols), indicating a reduction of the slow traps within the bulk portion of the CVD-SiO_2 films.[22] The D_{it} values of the SiC-MOS capacitors were evaluated using a high-low method and the change in D_{it} distribution depending on the MEO temperature is summarized in Fig. 3. It's clear that a reduced D_{it} was achieved with the Ba-MEO technique compared to results for the reference dry oxide (see black symbols). More interestingly, the lower D_{it} values were obtained with the lower MEO temperatures. This finding implies that additive thick oxide growth caused by Ba-MEO is not crucial to the improvement of interface quality in SiC-MOS devices. Actually, our supplementary experiments also revealed that the D_{it} distribution is dependent not severely on the MEO time, but on the oxidation temperature (data not shown). Therefore, considering the morphology and uniformity of the SiO_2 gate oxides, we concluded that Ba-MEO with a sub-monolayer of Ba atoms (0.1 nm thick) and low MEO temperature (around 750°C) are plausible conditions for fabricating advanced SiC-MOSFETs.

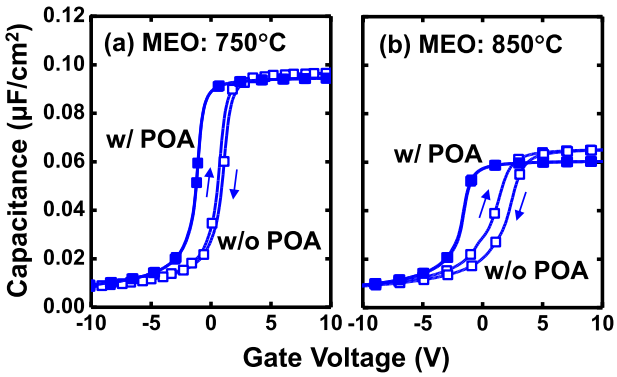


FIG. 2. Typical bidirectional C-V characteristics of Ba-incorporated SiC-MOS capacitors fabricated by MEO with a 0.1-nm-thick Ba interfacial layer at (a) 750°C and (b) 850°C for 4 h. Results with and without POA in N_2 ambience are indicated by the filled and open symbols, respectively.

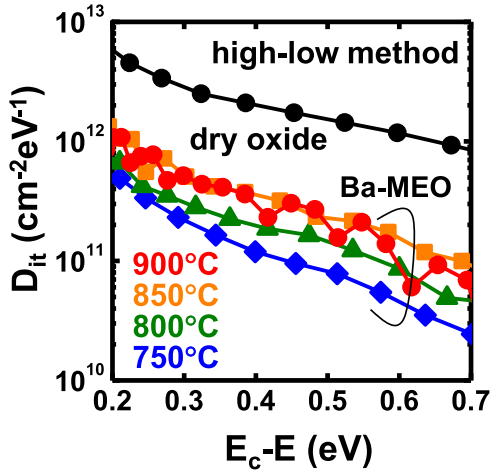


FIG. 3. Change in the energy distribution of D_{it} for Ba-incorporated SiC-MOS capacitors depending on the MEO temperature. Ba-MEO was conducted at various temperatures ranging from 750 to 900°C for 4 h. D_{it} values were estimated using a high-low method. All SiO_2/SiC structures received POA prior to electrode deposition. D_{it} distribution taken from the reference device with a thermal oxide (dry oxide) grown at 1150°C [20] was also shown.

Figure 4 represents the basic performance of Ba-incorporated SiC-MOSFETs fabricated with MEO at 750 or 900°C, followed by POA at 950°C for 30 min. Here, the MEO time was shortened to 1 hour for reducing variation in the gate oxide thickness especially for MEO at 900°C. The results for the reference device with a pure SiO_2 gate dielectric grown by dry oxidation at 1300°C are also shown. To compare transistor performance with various gate oxides having different capacitance equivalent thickness (CET), drain current (I_d) was normalized by the gate oxide capacitance (C_{ox}). As shown in Fig. 4(a), we confirmed there was a significant impact of Ba incorporation into the SiO_2/SiC interface on the I_d enhancement in SiC-MOSFETs. Figure 4(b) shows μ_{FE} of these SiC-MOSFETs with and without Ba as determined from the transfer characteristics. The peak mobility of the SiC-MOSFET fabricated by Ba-MEO at 750°C was estimated to be 62 cm^2/Vs, which is higher than those for other devices in Fig. 4 and the nitrided interface formed by high-temperature NO annealing.[8] These results again indicate an importance in the existence of Ba atoms at the SiO_2/SiC interface rather than the additive thick oxide growth by MEO.

Recently, one of the authors, Hatakeyama, *et al.* discussed mechanisms of μ_{FE} degradation in SiC-MOSFETs on the basis of Hall effect measurements combined with the common FET characterizations, in which they discriminated free carriers that contributed to the actual I_d from the inversion charge accumulated at the interface.[8] The inversion charge, i.e. total charge density (n_{total}) was characterized by an established split C-V method.[23] The free carrier density (n_{free}) at the interface depending on the applied gate voltage (V_g) was determined on the basis of Hall effect measurements

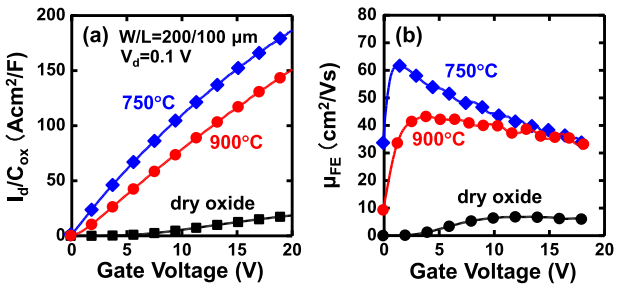


FIG. 4. Basic performance of Ba-incorporated SiC-MOSFETs fabricated with MEO at 750 or 900°C for 1 h: (a) I_d-V_g characteristics normalized by C_{ox}, and (b) μ_{FE} extracted from the transfer characteristics. Results from a reference thermal oxide (dry oxide) formed at 1300°C without Ba incorporation are also shown. The gate width and length of the devices (W/L) and drain voltage for I_d-V_g measurements are indicated.

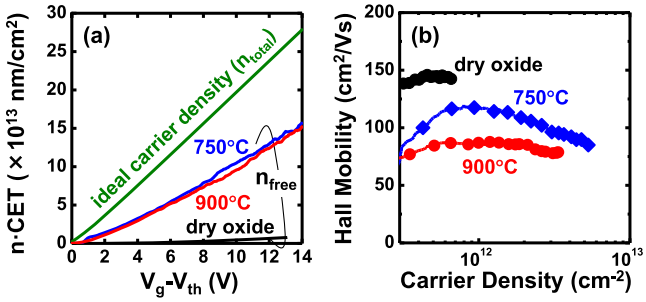


FIG. 5. Analysis of μ_{FE} enhancement factors in Ba-incorporated SiC-MOSFETs: (a) relationship between the n_{total} and n_{free}, respectively, extracted from the split C-V and Hall effect measurements plotted as a function of the gate voltage (V_g-V_{th}). Here, the carrier density (n) was normalized by CET, (b) the μ_{Hall} plotted as a function of carrier density accumulated in the inversion channel. Ba-MEO temperatures and results from the reference device with the pure thermal oxide (dry oxide) are indicated in each figure.

using the van der Pauw technique. Consequently, the V_g-dependent trapped carrier density (n_{trap}) was extracted by subtracting n_{free} from n_{total} for each device. Moreover, Hall effect measurements provided net mobility for the free carriers, which is Hall mobility (μ_{Hall}) in the inversion channel. We applied this combination method to quantitatively analyze the impact of incorporating Ba into the SiO_2/SiC interface by assuming a Hall scattering factor of unity. The split C-V measurements were conducted at 10 Hz using the ultra-low-frequency measurement system to extract the gate-channel capacitance. The p-well region was grounded, DC bias was applied to the gate electrode, and then an AC signal with an oscillation level of 20 mV was input to the source and drain regions. Figure 5(a) shows both n_{free} and n_{total} for the SiC-MOSFETs with and without Ba incorporation, in which the charge densities (vertical axis) were normalized by CET to compare the carrier density ratio (n_{free}/n_{total}) of the devices with different gate oxide thickness. Since the normalized n_{total} values estimated from the split C-V method were mostly identical for the Ba-incorporated SiC-MOSFETs, they were represented by a single trend line labeled as "ideal carrier density" in Fig. 5. As previously reported,[8] only three percent of the ideal carriers counted as mobile carriers in the case of the reference thermal oxide (black line in Fig. 5(a)). It should be noted that the free carrier ratio significantly increased to 55% with Ba-incorporation into the SiO_2/SiC interfaces and that MEO conditions had little or no influence on the carrier ratio in the temperature range. Considering that the free carrier ratio extracted by the same procedure for the nitrided SiO_2/SiC interface under the optimized conditions was still about 30%,[8] the impact of incorporating Ba was more pronounced in terms of the generation of mobile carriers in SiC-MOS structures. As shown in Fig. 5(b), the μ_{Hall} of the reference pure oxide was severely degraded as compared with the reported bulk mobility of 4H-SiC.[8] This indicates that, even for the mobile free carriers, their transport at the SiO_2/SiC interface was significantly disturbed by intrinsic electrical defects at the interface. The μ_{Hall} was found to further deteriorate with Ba incorporation relative to the reference pure oxide, which suggesting carrier scattering due to Ba-related defects at the interface. However, the μ_{Hall} degradation was suppressed with Ba-MEO at 750°C. This accounts for the higher I_d and μ_{FE} achieved with Ba-MEO at the lower annealing temperature shown in Fig. 4(b). From these findings, we concluded that performance improvement in Ba-incorporated SiC-MOSFETs was mostly due to a significant increase in the free carrier density that overcomes slight mobility degradation (μ_{Hall}). Regarding the physical origins for the anomalous carrier trapping at the SiO_2/SiC interface and for both carrier generation and scattering due to the Ba incorporation, we have no plausible model so far. However, since the obtained μ_{Hall} values shown in Fig. 5(b) were still below expectations from the SiC bulk property as mentioned above, there might be room for further improvement in SiC-MOSFETs by means of Ba incorporation and additive combination techniques to increase inversion carrier mobility.

In summary, we investigated the impacts of incorporating Ba into SiO_2/SiC interfaces on the performance of MOSFETs. Physical and electrical characterizations demonstrated that a sub-monolayer of Ba atoms and a moderate MEO temperature, together with high-temperature POA, are beneficial in Ba-MEO for improving SiC-MOS devices in terms of gate oxide morphology and interface

quality. We also found that, while most of the inversion carriers were trapped by electrical defects at the thermally-grown SiO_2/SiC interface, Ba incorporation significantly increased mobile free carriers that directly affect device performance. As a result, the high free carrier ratio up to 55% and increased μ_{FE} about 62 cm^2/Vs over the conventional nitrided interface were achieved by using the Ba-MEO technique.

This work was partly supported by the Council for Science, Technology, and Innovation (CSTI), Cross-ministerial Strategic Innovation Promotion Program (SIP), "Next-generation power electronics" (funding agency: NEDO).

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