Reduction in interface defect density in p-BaSi$_2$/n-Si heterojunction solar cells by a modified pretreatment of the Si substrate

Yudai Yamashita, Suguru Yachi, Ryota Takabe, Takuma Sato, Miftahullatif Emha Bayu, Kaoru Toko, and Takashi Suemasu*

Institute of Applied Physics, University of Tsukuba, Tsukuba, Ibaraki 305-8573, Japan

We have investigated defects that occurred at the interface of p-BaSi$_2$/n-Si heterojunction solar cells that were fabricated by molecular beam epitaxy. X-ray diffraction measurements indicated that BaSi$_2$ (*a*-axis-oriented) was subjected to in-plane compressive strain, which relaxed when the thickness of the p-BaSi$_2$ layer exceeded 50 nm. Additionally, transmission electron microscopy revealed defects in the Si layer near steps that were present on the Si(111) substrate. Deep level transient spectroscopy revealed two different electron traps in the n-Si layer that were located at 0.33 eV (E1) and 0.19 eV (E2) below the conduction band edge. The densities of E1 and E2 levels in the region close to the heterointerface were approximately 10^{14} cm^{-3}. The density of these electron traps decreased below the limits of detection following Si pretreatment to remove the oxide layers from the n-Si substrate, which involved heating the substrate to 800 °C for 30 min under ultrahigh vacuum while depositing a layer of Si (1 nm). The remaining traps in the n-Si layer were hole traps located at 0.65 eV (H1) and 0.38 eV (H2) above the valence band edge. Their densities were as low as 10^{10} cm^{-3}. Following pretreatment, the current versus voltage characteristics of the p-BaSi$_2$/n-Si solar cells under AM1.5 illumination were reproducible with conversion efficiencies beyond 5% when using a p-BaSi$_2$ layer thickness of 100 nm. The origin of the H2 level is discussed.

1. Introduction

Crystalline Si solar cells have exceeded the conversion efficiency (η) of 26% [1], which is approaching the theoretical efficiency limit [2]. Therefore, alternative solar cell materials are being examined, including III-V semiconductors, chalcopyrites, CdTe, and perovskites [3-7]. Tandem-structure solar cells composed of III-V semiconductors have achieved $\eta > 40\%$ [8]. However, these solar cells are based on expensive materials and so there has been renewed interest in high-efficiency solar cells using inexpensive Si substrates. $BaSi_2$ is a semiconductor material that shows great promise for use in solar cells [9] as it has a suitable band gap ($E_g = 1.3$ eV), large optical absorption coefficients that exceed those of chalcopyrites [10-13], and a large minority carrier lifetime (~10 μs) [14-16], which leads to a minority carrier diffusion length ($L = 10$ μm) that is larger than the grain size of $BaSi_2$ [17]. A η beyond 25% is expected for a 2-μm-thick $BaSi_2$ homojunction solar cell [18]. We have shown that the minority carrier lifetime can be reproducibly increased from 0.1 to 10 μs by covering with an amorphous Si (a-Si) passivation layer [16]. Using this surface passivation technique, we have achieved a η of 9.9% in p-$BaSi_2$/n-Si heterojunction solar cells [19]. Other types of solar cells such as $BaSi_2$ nanowires and $BaSi_2$/perovskite stacked layers have also been proposed [20-22].

$BaSi_2$ can be grown epitaxially on a Si(111) substrate [23,24]. $BaSi_2$(100) is a better match for Si(111) with $BaSi_2$[001]//Si[1-10], with a small lattice mismatch of only 1.1%. Thus, a Si-based tandem structure solar cell containing $BaSi_2$ would be a good candidate. The control of defects in both p-$BaSi_2$/n-Si heterojunction and $BaSi_2$ homojunction solar cells is extremely important. Regarding the epitaxial growth of another semiconducting silicide named β-$FeSi_2$ on a Si(111) substrate, Liu *et al*. demonstrated the reduction in the level of the Fe diffusion into the Si substrate by using the template layer [25] and achieved the operation of β-$FeSi_2$ photodiodes [26]. Diffused Fe atoms in Si are known to form deep levels of energy and they work as efficient traps for minority carriers [27,28]. However, there are no reports on the defects that occur at the $BaSi_2$/Si(111) interface. We have found that defect formation around the

heterointerface depends significantly on the method used for removing the oxide layers on the Si substrate surface. We also discuss the oxide removal method on the performance of p-BaSi$_2$/n-Si solar cells.

2. Experimental methods

p-BaSi$_2$/n-Si heterojunction solar cells were fabricated by growing B-doped p-BaSi$_2$ layers epitaxially on a Czochralski (CZ) n-Si(111) substrate (resistivity $\rho = 1–4$ Ωcm) with an area of 2×2 cm^2. The BaSi$_2$ layers were grown using an ion-pumped molecular beam epitaxy (MBE) system that was equipped with an electron beam evaporation source for Si and with standard Knudsen cells for Ba and B. Although BaSi$_2$ epitaxial layers (*a*-axis-oriented) have three epitaxial variants that are located 120° from each other around the surface normal [24], the grain boundaries (GBs) between the variants do not act as recombination centers [13,25,26]. The fabrication process involved the initial cleaning of the Si(111) substrates followed by the formation of a protective surface oxide layer according to standard RCA procedures. The substrates were then heated to 900 °C for 30 min in an ultrahigh-vacuum (UHV) chamber to remove the protective oxide layer on the surface. This process is called thermal cleaning (TC). We modified this TC process for this work as described later. Next, we prepared a 3-nm-thick BaSi$_2$ template layer by depositing Ba on an n-Si(111) substrate at 500 °C by reactive deposition epitaxy (RDE) [29]. This layer acted as seed crystals for subsequent layers. Next, Ba, Si, and B were deposited simultaneously at 600 °C by MBE to form B-doped p-BaSi$_2$ epitaxial layers that were 10–300 nm thick. The Ba deposition rate (R_{Ba}) was 1 nm/min during RDE, while the Si deposition rate (R_{Si}) and R_{Ba} were 0.9 and 2.3 nm/min during MBE, respectively. R_{Ba} and R_{Si} were controlled using an electron impact emission spectroscopy (EIES) feedback system. The hole concentration was fixed at $p = 2.0 \times 10^{18}$ cm^{-3} [30], and the electron concentration of the Si substrate was $n = 2 \times 10^{15}$ cm^{-3} at room temperature. Finally, a 3-nm-thick a-Si layer was

deposited *in situ* on the surface at 180 °C [31]. The a-Si layer prevents the oxidation of the BaSi$_2$ surface and does not hinder carrier transport across the a-Si/BaSi$_2$ interface [32]. Indium-tin-oxide (ITO) electrodes with a diameter of 1 mm and a thickness of 80 nm were fabricated on the surface by sputtering and Al electrodes were placed on the back side.

The crystal quality of the samples was characterized by atomic force microscopy (AFM), reflection high-energy electron diffraction (RHEED), and X-ray diffraction (XRD) with a Cu Kα radiation source. Out-of-plane (θ-2θ) and in-plane (φ-$2\theta_\chi$) XRD measurements were taken to determine the lattice constants using the Nelson-Riley equation [33]. Solar cell performance was evaluated using a mask with a 1-mm-diameter hole under AM 1.5 conditions at 25 °C. Photoresponse and reflectance spectra were evaluated using a lock-in technique with a xenon lamp and a single monochromator with a focal length of 25 cm (Bunko Keiki SM-1700A and RU-60N). The light intensity was calibrated using a pyroelectric sensor (Melles Griot 13PEM001/J). Deep-level transient spectroscopy (DLTS) measurements were used to investigate the defect levels and densities in the n-Si layer. Transmission electron microscopy (TEM) revealed defects that were present in the Si layer near the Si surface steps, and their densities depended on the resistivity (ρ) of the n-Si substrate used.

In this work, we modified the TC process and performed the following additional experiments. To investigate the influence of TC, the p-BaSi$_2$ thickness was fixed at 100 nm. Surface oxide layers that were present following RCA were etched away using 5% HF solution for 30 s, followed by TC under UHV at 650, 750, and 800 °C for 30 min. We also performed TC at 800 °C under UHV for 30 min with a simultaneous deposition of a 1-nm-thick Si layer. Sample preparation details are summarized in Table I.

3. Results and discussion

3.1 Solar cell parameters

Out-of-plane θ-2θ XRD patterns of p-BaSi$_2$ layers with thicknesses (d) ranging from 10 to 300

nm (samples A–G) are shown in Fig. 1. All samples exhibited (100)-oriented diffraction peaks, including $BaSi_2$(200), (400), and (600). Together with RHEED streaky patterns, these results indicated that p-$BaSi_2$ layers (a-axis-oriented) had grown epitaxially on the Si(111) substrate. Both the out-of-plane and in-plane lattice constants were calculated from the peak positions in the θ-2θ and φ-$2\theta_\chi$ XRD spectra, respectively. Measurement errors were minimized by using the Nelson-Riley equation for the calculation [33]. As an example, the $BaSi_2$(200), (400), and (600) peaks in each sample were used to calculate the lattice constants for the a-axis. The strain ($\Delta a/a$) as a function of $BaSi_2$ film thickness, normalized using a in sample G, is shown in Fig. 2. Similarly, strains $\Delta b/b$ and $\Delta c/c$ were deduced using (010) and (001)-oriented diffractions, respectively. When the $BaSi_2$ layer was thin, it was under compressive strain in the in-plane direction, while it was under tensile strain in the direction normal to the surface. As d increased, the strain gradually decreased. A lattice mismatch between $BaSi_2$ and Si, which was determined to be 1.1% along the b-axis and 0.1% along the c-axis [23], may have caused these strains. It is thought that misfit dislocations are generated around a heterointerface.

Current density versus voltage (J-V) plots of samples A–G under AM1.5 illumination are shown in Fig. 3. To accurately determine the series resistance (R_S), diode ideality factor (γ), and reverse saturation current density (J_0) of a diode, we adopted a technique described by Sites and Mauk [34]. Using the photodiode equation, the relationship between R_S and γ can be given as

$$\frac{dV}{dJ} = SR_S + \frac{\gamma k_B T}{q}\left[\frac{1-(SR_{SH})^{-1}dV/dJ}{J+J_{SC}-(SR_{SH})^{-1}V}\right], \tag{1}$$

where T is the absolute temperature, q is the elemental charge, k_B is the Boltzmann constant, S is the area of the electrode, R_{SH} is the shunt resistance, and J_{SC} is the photocurrent density. Using a plot of Eq. (1), we can directly deduce γ from the slope and R_S from the intercept. The solar cell parameters of highest-efficiency cells are summarized in Table II.

External quantum efficiency (EQE) spectra are shown in Fig. 4. η increased with d, reached a maximum of 9.9% at $d = 20$ nm, and then decreased. The reduction in η for samples with $d > 20$ nm was primarily attributed to the reductions in J_{sc} and FF. Notably, EQE

decreased significantly in the short wavelength region as d increased, which indicated that the photogenerated carriers in the p-BaSi$_2$ layer could no longer effectively diffuse to the n-Si layer before recombination because of the relatively high hole concentration ($p = 2.0 \times 10^{18}$ cm^{-3}), leading to the reduction in J_{sc}. There is another possibility that an increased number of defects in BaSi$_2$ due to lattice relaxation caused the reduction in EQE. The reduction in FF was caused by the decrease in R_{SH}. These results, together with the increase in J_0 with d, suggested the degradation of the pn heterointerface.

3.2 DLTS measurement

DLTS is a powerful method for the investigation of defect densities and their energy levels [35]. Hence, defect states near the heterointerface of sample F were characterized by DLTS. In a BaSi$_2$ pn homojunction diode, we plan to form a p-BaSi$_2$ layer first on a Si substrate, where the thickness of p-BaSi$_2$ with a high hole concentration ($p > 10^{18}$ cm^{-3}) is not likely to exceed 100 nm. Hence, we chose sample F to determine the type of defect generated on the Si side when the layer thickness reaches 100 nm.

A schematic representation of the DLTS measurement is shown in Fig. 5(a). All voltages were applied to p-BaSi$_2$ with respect to n-Si. A forward filling pulse voltage (V_p) disturbs the steady-state reverse-bias condition, causing the electric field in the depletion region to decrease. This causes the defect levels to be recharged. When the voltage returns to its steady state, the defect levels begin to discharge by emitting trapped carriers via thermal emission, and the resultant time evolution of the capacitance change $S(T)$ is measured for various rate windows. The DLTS method allows the immediate determination of whether the detected defects act as minority-carrier traps or majority-carrier traps from the sign of the DLTS signals (positive sign indicates the presence of minority-carrier traps, and negative sign indicates the existence of majority-carrier traps).

Both majority- and minority-carrier traps can be observed in a pn junction diode by applying a forward filling pulse, because the forward pulse injects minority carriers into the

depletion region. The large difference between the carrier concentrations of the p-BaSi$_2$ and n-Si layers caused the depletion region to spread to the n-Si layer. In this study, the distribution of defects in the n-Si layer as a function of depth was investigated by changing the depletion layer width. This was achieved by setting the reverse-biased voltage (V_R) to −1 or −0.01 V, which gave a depletion layer width of approximately 870 or 320 nm, respectively. V_p was fixed at 0 or 0.5 V, and the pulse width (t_{pw}) was set to 50 ms. Two downward facing peaks were observed at approximately 120 and 150 K marked by arrows, Fig. 5(b) when V_R = −1 V, which indicated the presence of majority-carrier (electron) trap levels (E1 and E2). Arrhenius plots of these traps are shown in Fig. 6. The trap levels were calculated to be 0.19 eV (E2) and 0.33 eV (E1) from the conduction band edge, and the defect densities were calculated to be 6.3×10^{12} cm^{-3} and 2.2×10^{13} cm^{-3}, respectively. $S(T)$ increased significantly when V_R was decreased from −1 to −0.01 V, as shown in Fig. 5(b), meaning that there were more defects in the region close to the interface. As the large peak observed at ~120 K was composed of multiple peaks, it was difficult to accurately identify the peak position. However, we can say that there were significantly higher defect levels in the vicinity of the interface than in the bulk of the n-Si layer. From the peak value of $S(T)$, the defect density near the interface was estimated to be approximately 10^{14} cm^{-3}. Defects in the vicinity of the interface may act as recombination centers for the photogenerated carriers and hence have deleterious effects on solar cell performance. These defects are thought to originate from the diffusion of Ba atoms from the BaSi$_2$ or misfit dislocations. The detection limit is determined by the donor concentration within the Si substrate during the DLTS measurement. Therefore, we cannot exclude the possibility that other majority-carrier traps and/or minority-carrier traps with a density less than 10^{13} cm^{-3} are present on the n-Si side of sample F.
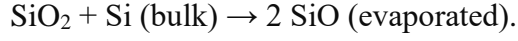
To investigate what occurs near the p-BaSi$_2$/n-Si interface, cross-sectional TEM was performed on samples G and H, as shown in Figs. 7(a) and 7(a'), respectively. Sample G had a resistivity between 1 and 4 Ωcm, while the resistivity of sample H was < 0.01 Ωcm. The lines

that can be observed running normal to the interface in the $BaSi_2$ layer are GBs. The $BaSi_2$ epitaxial layer (*a*-axis-oriented) contained three epitaxial variants around the surface normal, located 120° from each other. As these GBs do not act as recombination centers [16,25,26], we focused on the strain contrast in the n-Si layer of sample H [Fig. 7(a')]. The strain contrast observed in sample H [Fig. 7(b')] was not observed in sample G [Figs. 7(a) and 7(b)]. A magnified view of a position where the strain contrast was observed in sample H is shown in Fig. 7(b'). Such a strain contrast indicates the presence of various disorders or defects. We found that the strain contrast stems from a step with a height of approximately 1−2 nm in the Si layer near the $BaSi_2$/Si interface. AFM topographic views (2×2 μm^2) and cross-sectional profiles (along white lines) for the Si substrates used in samples G and H after TC are shown in Figs. 7(c) and 7(c'), respectively. Although both samples exhibited the stepped Si surface, the height of the steps differed significantly, which was attributed to step bunching on the Si surface. Step bunching occurs to a far greater extent when the temperature of a low-ρ Si(111) substrate is decreased from higher values across the surface transition temperature (~830 °C) at a lower rate (< 0.5 °C/s), where the RHEED pattern changes from a 1×1 structure to a 7×7 structure [36]. To prevent step bunching, we decreased the temperature during TC from 900 to 800 °C.
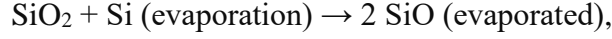
3.3 Effect of modified TC

TC is required to remove the protective oxide layer formed during RCA. To prevent surface recombination, we heated the substrates to 800 °C, which is lower than the 1×1 to 7×7 transition temperature of 830 °C. It becomes more difficult to remove the protective oxide layer at lower temperatures. Hence, the surface oxide layer was initially etched using a 5% HF solution for 30 s, followed by TC under UHV at 650, 750, and 800 °C for 30 min for samples I−K, respectively. Sample L underwent TC at 800 °C under UHV for 30 min, in addition to the simultaneous deposition of a 1-nm-thick Si layer.

The protective oxide layer in samples A−H was removed from the Si substrate according to the following reaction:

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$$SiO_2 + Si \text{ (bulk)} \rightarrow 2 \text{ SiO (evaporated)}.$$

In contrast, when a Si layer was deposited during TC using a molecular beam, the following reaction occurred:

$$SiO_2 + Si \text{ (evaporation)} \rightarrow 2 \text{ SiO (evaporated)},$$

and thus the use of Si (bulk) was suppressed. Furthermore, the reaction temperature decreased by 30–40 degrees so long as the SiO_2 thickness is approximately less than 2.5 nm [37]. The oxide layer thickness following the RCA process was determined to be 2.34 nm using X-ray reflectivity. The thickness of the Si layer required to remove the oxide layer was calculated to be approximately 1 nm. Therefore, we deposited a Si layer (1 nm) at 800 °C and maintained the temperature for 40 min.

Topographic AFM images of the Si substrates (2×2 μm^2) after each pretreatment (samples I–L) are shown in Fig. 8. The distinct stepped structures such as those observed in samples G and H were not observed in these samples, indicating that step bunching was suppressed. The *J-V* characteristics of samples I–L under AM1.5 illumination are shown in Fig. 9, while detailed solar cell parameters are given in Table II. The V_{OC} and/or J_{sc} of samples I–K changed significantly depending on the position of the ITO electrode in a 2×2 cm^2 area. However, this was not the case for sample L. The Si substrates in samples I–K were exposed to air after the removal of the oxide layers following treatment with the HF solution. It is plausible that the fluctuations observed in the solar cell characteristics were caused by air contaminants. Conversely, any variations in the solar cell performance of sample L were very small and the reproducibility was high. Additionally, J_0 (1.41×10^{-6} mA/cm^2) was significantly smaller than those of the other samples, indicating a high-quality interface with reduced defect densities. On the basis of these results, the TC process used for sample L gave the best interface.

To investigate the effects of the TC process used for sample L, DLTS measurements were performed and compared with those of sample F, as shown in Fig. 10. The large DLTS signal around 120 K observed for sample F was not observed for sample L, implying that the

defect density decreased markedly by approximately 100-fold or more. The detection limit is determined by the donor concentration within the Si substrate during the DLTS measurement.

To evaluate the other defects in detail, we fabricated p-BaSi$_2$/n-Si heterojunction solar cells using a high-ρ float-zone n-Si(111) substrate with an impurity concentration of approximately 10^{11} cm^{-3}. During the DLTS measurement, V_p was set at 0.5 V, the pulse width was 50 ms, and V_R was varied from -3 to -0.054 V. The DLTS spectra obtained under these conditions are shown in Fig. 11(a). Two upward facing peaks caused by minority-carrier (hole) trap levels (H1 and H2) were observed at approximately 270 and 170 K, respectively. The majority-carrier trap observed in sample F was not detected in sample M. Arrhenius plots of these traps are shown in Fig. 11(b). The hole trap levels were calculated to be approximately 0.38 (H2) and 0.65 eV (H1) from the valence band edge. As the DLTS signal near 170 K decreased as $\left|V_R\right|$ decreased, the defect density also decreased when approaching the p-BaSi$_2$/n-Si interface. The defect density of H2 decreased from 2.5×10^{10} cm^{-3} at a distance of 62 μm from the interface to 3.7×10^9 cm^{-3} at a distance of 1 μm. On the other hand, the defect density of H1 did not depend markedly on the distance from the interface, indicating that the trap level H1 originates from intrinsic defects in the substrate. It was calculated to be approximately 7×10^9 cm^{-3}. The total hole trap density was approximately 1×10^{10} cm^{-3}. Therefore, we concluded that the TC process used for samples L and M was very effective at suppressing the defects within n-Si and around the heterointerface even though the BaSi$_2$ layers were relaxed and hence the misfit dislocations were present at the heterointerface. The relaxation of the BaSi$_2$ lattice of sample M was confirmed by XRD. In our next study, defects in the BaSi$_2$ layers will be investigated by DLTS. Finally, we investigated whether the hole trap level H2 was caused by point or extensive defects such as dislocations. This involved varying the t_{pw} of V_p from 0.01 to 800 ms, and measuring the $S(T)$ signals at 174 K, as shown in Fig. 11(c). $S(T)$ increased sharply as the pulse width increased from 1 to 10 ms, which is known to be caused by the presence of point defects [38].

4. Conclusions

We fabricated p-BaSi$_2$/n-Si heterojunction solar cells to understand and suppress the interface defect density in the n-Si layer by modifying the TC process. When TC was performed at 900 °C for 30 min under UHV, DLTS measurements revealed that two electron trap levels were located in the n-Si layer at 0.33 eV (E1) and 0.19 eV (E2) below the conduction band edge, and their densities were approximately 10^{14} cm^{-3} in the region close to the heterointerface. The density of these electron traps decreased below the limits of detection when the temperature used during TC was decreased from 900 to 800 °C, with the simultaneous deposition of a 1-nm-thick Si layer. Hole trap levels located at 0.65 eV (H1) and 0.38 eV (H2) above the valence band edge appeared instead, but their densities were as low as 10^{10} cm^{-3} even though the misfit dislocations caused by the relaxation of the BaSi$_2$ lattice were at the heterointerface. With this method, the *J-V* characteristics of the p-BaSi$_2$(100 nm)/n-Si heterojunction solar cells under AM1.5 illumination were reproducible with conversion efficiencies beyond 5%.

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Table I. Sample preparation details. RCA was performed on all Si substrates. The resistivity of the n-Si substrate, the HF etching duration, the substrate temperature during TC (T_{TC}), the deposited Si thickness (d_{Si}) during TC, and the thickness of p-BaSi$_2$(d) are tabulated.

Sample	ρ of n-Si(111) (Ωcm)	HF etching duration (s)	T_{TC} (°C)	d_{Si} during TC (nm)	d (nm)
A	1–4	–	900	–	10
B	1–4	–	900	–	15
C	1–4	–	900	–	20
D	1–4	–	900	–	30
E	1–4	–	900	–	50
F	1–4	–	900	–	100
G	1–4	–	900	–	300
H	< 0.01	–	900	–	400
I	1–4	30	650	0	100
J	1–4	30	750	0	100
K	1–4	30	800	0	100
L	1–4	–	800	1	100
M	> 1000	–	800	1	100

Table II. Solar cell parameters of the cells with the highest efficiency in samples A–G and I–L. The thickness of the p-BaSi$_2$ layer (d), short-circuit current density (J_{SC}), open-circuit voltage (V_{OC}), fill factor (FF), conversion efficiency (η), series resistance (R_S), shunt resistance (R_{SH}), diode ideality factor (γ), and reverse saturation current density (J_0) are all tabulated.

Sample	d (nm)	J_{SC} (mA/cm^2)	V_{OC} (V)	FF	η (%)	R_S (Ω)	R_{SH} (kΩ)	γ	J_0 (mA/cm^2)
A	10	28.9	0.09	0.29	0.7	154	2.90	1.63	9.65
B	15	31.4	0.26	0.34	2.7	202	2.11	1.93	2.89×10^{-1}
C	20	35.8	0.47	0.60	9.9	163	17.71	1.11	1.39×10^{-5}
D	30	32.3	0.45	0.60	8.7	159	13.52	1.38	3.55×10^{-4}
E	50	29.8	0.45	0.51	7.0	314	11.39	1.31	9.12×10^{-4}
F	100	20.5	0.43	0.52	4.6	230	10.79	1.55	3.55×10^{-4}
G	300	13.8	0.43	0.36	2.2	202	6.98	1.81	1.85×10^{-3}
I	100	23.2	0.43	0.52	5.1	129	7.56	1.44	5.80×10^{-4}
J	100	23.2	0.26	0.54	3.3	174	173.88	1.93	2.18×10^{-1}
K	100	28.1	0.41	0.57	6.7	137	14.54	1.23	1.09×10^{-4}
L	100	24.4	0.45	0.48	5.3	207	8.59	1.04	1.41×10^{-6}

Figure captions

Fig. 1. θ-2θ XRD and RHEED patterns observed along Si[11$\bar{2}$] for samples A−G. The BaSi$_2$ thickness (d) was varied from 10 to 300 nm.

Fig. 2. Normalized strain ($\Delta a/a$, $\Delta b/b$, and $\Delta c/c$) as a function of d for samples A−G.

Fig. 3. *J-V* curves under AM1.5 illumination for samples A−G, p-BaSi$_2$/n-Si solar cells with various $d_{p\text{-BaSi2}}$ values ranging from 10 to 300 nm.

Fig. 4. *EQE* spectra of p-BaSi$_2$/n-Si solar cells with various d values.

Fig. 5. (a) Principle of DLTS method and (b) DLTS spectra of a p-BaSi$_2$/n-Si solar cell (sample F) obtained at V_R = −0.01 and −1 V. The pulse width was 50 ms, and the rate window was 4−128 ms. V_p was 0.5 V for V_R = −1 V, while V_p was 0 V for V_R = −0.01 V.

Fig. 6. Arrhenius plots for electron trap levels (E1 and E2) obtained at V_R = −1 V for sample F.

Fig. 7. (a) and (a') Cross-sectional TEM images and (b) and (b') magnified views of (a) and (a'). In (b'), a magnified view of the white circle area is inserted. (c) and (c') Topographic AFM views (2×2 μm^2) and cross-sectional profiles (along white lines) of the Si substrate surfaces of samples G and H taken after TC. The root-mean-square roughness values are presented.

Fig. 8. Topographic AFM views (2×2 μm^2) of the Si substrate surface taken after TC for samples (a) I, (b) J, (c) K, and (d) L. The root-mean-square roughness values are presented.

Fig. 9. *J-V* curves under AM1.5 illumination for samples (a) I, (b) J, (c) K, and (d) L. The p-BaSi$_2$(100 nm)/n-Si solar cells that had their Si substrates treated differently are shown in Table I.

Fig. 10. (a) Principle of DLTS method and (b) DLTS spectra of samples F and L obtained at V_R = −0.01 V. V_p was 0.5 V, the pulse width was 50 ms, and the rate window was 4−128 ms.

Fig. 11. (a) DLTS spectra of sample M as V_R was varied from −3 to −0.054 V. V_p was 0.5 V, the pulse width was 50 ms, and the rate window was 4−128 ms. (b) Arrhenius plots for hole trap levels (H1 and H2) obtained at different V_R values. (c) DLTS spectra obtained at different pulse widths from 0.01 to 800 ms and the dependence of the DLTS signal $S(T)$ on pulse width of V_p, measured at 174 K.
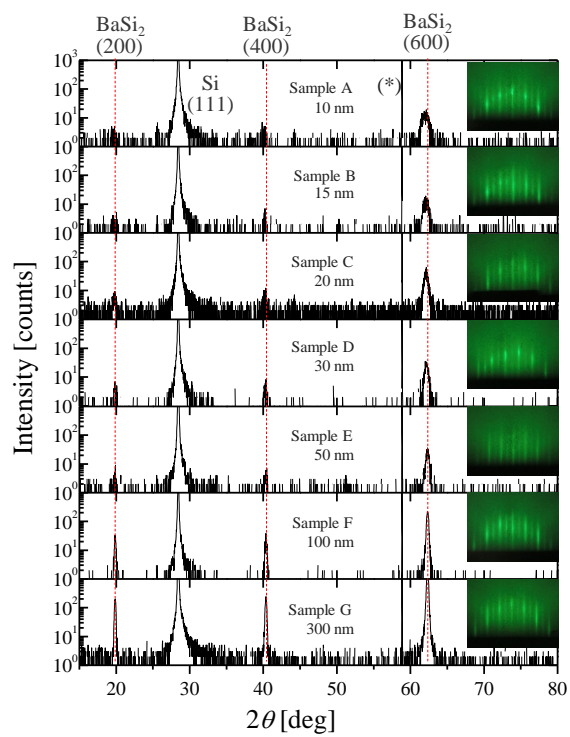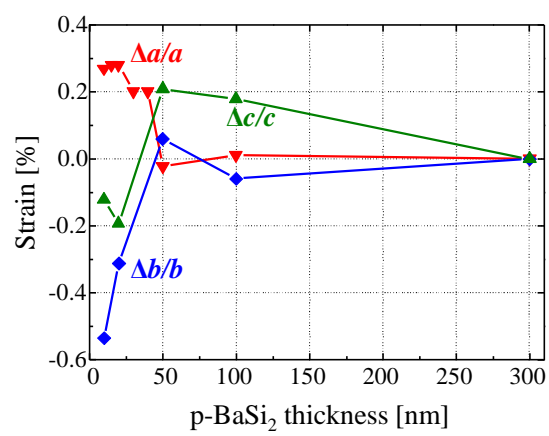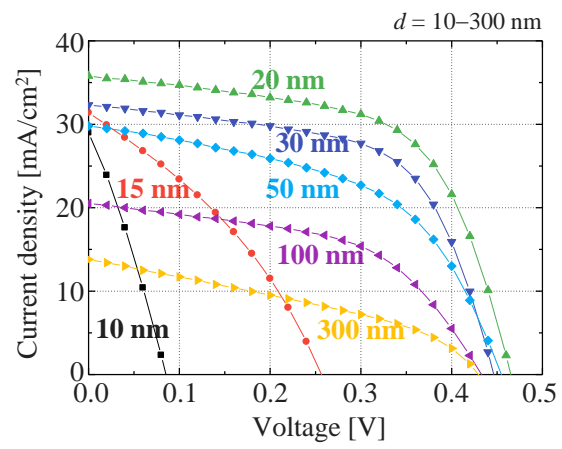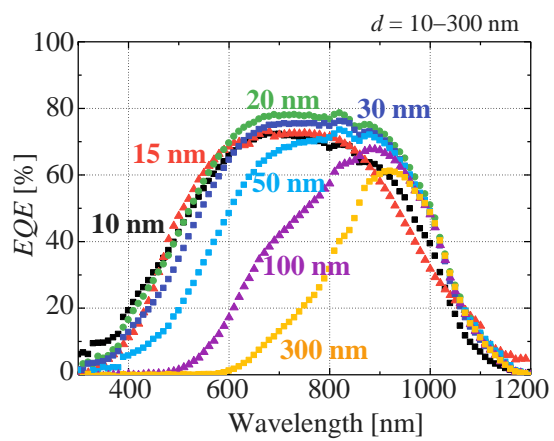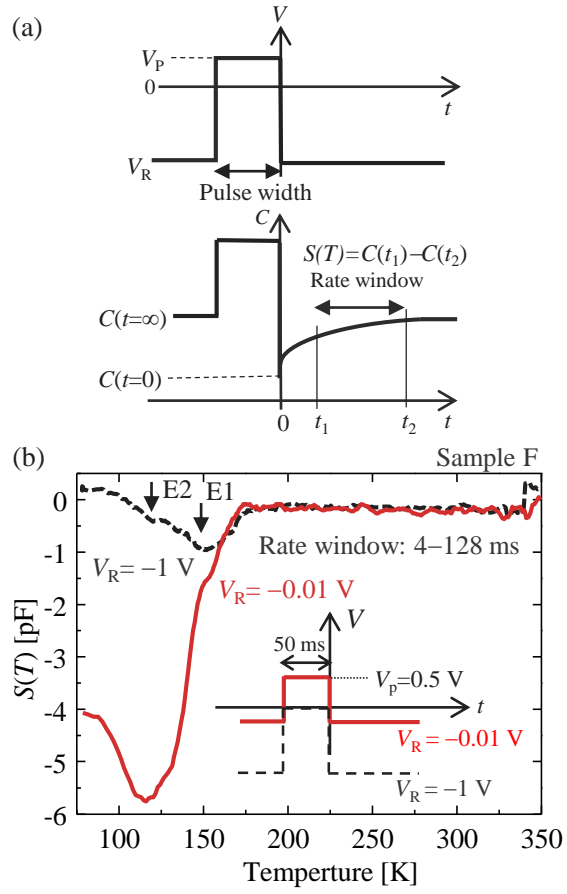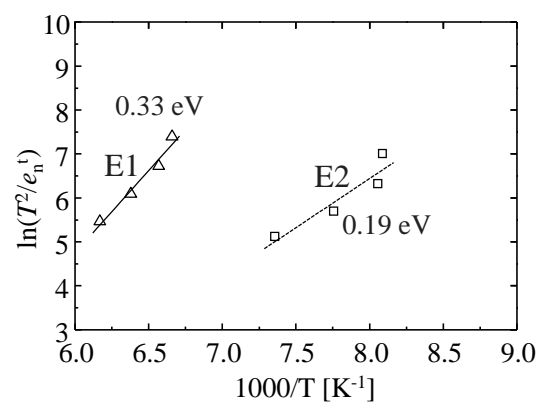
Fig. 1

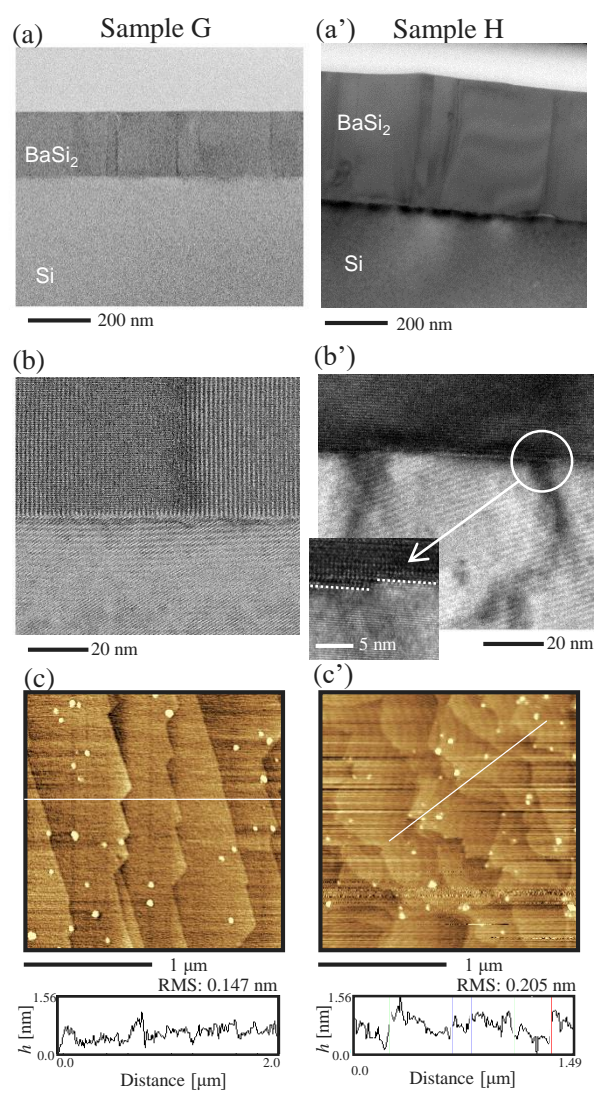Fig. 2

Fig. 3

Fig. 4

Fig. 5

Fig. 6

(a) Sample G   (a') Sample H

BaSi$_2$ BaSi$_2$

Si   Si

200 nm   200 nm

(b)   (b')

20 nm   5 nm   20 nm

(c)   (c')

1 μm   1 μm
RMS: 0.147 nm   RMS: 0.205 nm

Distance [μm]   Distance [μm]

Fig. 7

(a) Sample I

(b) Sample J

1 μm
RMS: 0.113 nm

1 μm
RMS: 0.315 nm

h [nm]

1.56

0.0

0.0

2.0

Distance [μm]

h [nm]

1.56

0.0

0.0

2.0

Distance [μm]

(c) Sample K

(d) Sample L

1 μm
RMS: 0.265 nm

1 μm
RMS: 0.198 nm

h [nm]

1.56

0.0

0.0

2.0

Distance [μm]

h [nm]

1.56

0.0

0.0

2.0

Distance [μm]

Fig. 8

Fig. 9

Fig. 10

(a) Sample M

Rate window: 4–128 ms

−3 V
−1 V
−0.5 V
−0.054 V

$S(T)$ [pF]

Temperture [K]

50 ms
V_p=0.5 V
V_R
V
t

H2   H1

(b)

$\ln(T^2/e_n^t)$

0.65 eV   0.38 eV

H1   H2

−3 V ○ ●
−1 V □ ■
−0.5 V ◇ ◆
−0.054 V △ ▲

1000/T [K⁻¹]

(c)

$S(T)$ [pF]

800 ms
50 ms
10 ms
1 ms
0.01 ms

Temperture [K]

$S(T)$ [pF]

H2

174 K

Pulse width [ms]

Fig. 11