Extraction of additional interfacial states of silicon nanowire field-effect transistors

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Interfacial states of silicon nanowire field-effect transistors with rectangular-like cross-sections (wire height of 10 nm and widths of 9 and 18 nm) have been evaluated from the transfer characteristics in the subthreshold region measured at cryogenic temperatures, where kinks in the drain current becomes prominent. It is found that the kinks can be well-explained assuming local interfacial states near the conduction band (E_c). The main extracted local states have been shown to exist at 10 and 31 meV below E_c with the densities of 1.3×10^{13} cm^{-2}/eV and 5.4×10^{12} cm^{-2}/eV, respectively. By comparing two field-effect transistors with different wire widths, the former states can be assigned to the states located at the corner and the side surface of the wire, and the latter to the top and the bottom surfaces. © *2011 American Institute of Physics*. [doi:10.1063/1.3598402]

Silicon nanowire (SiNW) metal-oxide-semiconductor field-effect transistor (MOSFET) is a promising candidate of future complementary MOS devices for further scaling. To improve the short channel effect immunity with SiNW FETs, the cross-sectional dimensions of SiNW channel should be designed to be small.[1] As a result, curved surfaces near corners of rectangular-like SiNW cross-sections might be the dominant surface for the conduction as the cross-sectional dimensions decrease.[2] In this case, curved surfaces with various surface orientations might be more prominent with smaller cross-sectional dimensions to modify the interfacial state density (D_{it}) distribution energetically and physically different from that of planar-type FETs.[3] As the interfacial states are related to reliability issues of gate oxide of MOSFET,[4] it is important to characterize the interfacial states. In this letter, we report the interfacial state density distribution of SiNW *n*FETs.

SiNW *n*FETs with a semigate-around structure[4] were fabricated on silicon-on-insulator (SOI) wafers. The detailed fabrication process is reported in Refs. 2 and 5. Cross-sectional scanning transmission electron microscope images of the SiNW channels are shown in Figs. 1(a) and 1(b). SiNW *n*FETs with rectangular-like cross-sections with channel widths (w_{NW}) of 9 and 18 nm were examined in this letter. The SiNW *n*FETs had the same channel height (h_{NW}) of 10 nm. Planar-type SOI *n*FET with SOI layer thickness of 28 nm was also evaluated. Effective gate lengths (L_g) of the SiNW *n*FETs with w_{NW} of 9 and 18 nm, and planar-type SOI *n*FET were 415 nm, 458 nm, and 577 nm, respectively, which were extracted by Chern's channel resistance method.[6]

Interfacial state density distribution was evaluated using transfer characteristics and subthreshold slope (*SS*) of the SiNW *n*FETs (Refs. 7 and 8) at a drain bias voltage of 50 mV. The transfer characteristics were measured at temperatures from 290 down to 43 K. *SS* is expressed as[9]

$$SS = \ln 10 \times \frac{kT}{q}\left[1 + \frac{C_d + C_{it}(\phi_s)}{C_{ox}}\right], \quad (1)$$

where k is the Boltzmann constant, T is the measurement temperature, q is the elementary charge, C_{ox} is the oxide capacitance, C_d is the depletion capacitance, and C_{it} (φ_s) is the interfacial state capacitance that is a function of the surface potential φ_s. C_{it} (φ_s) is a first order partial derivative of interface trap charge density (Q_{it}). The minimum *SS* values

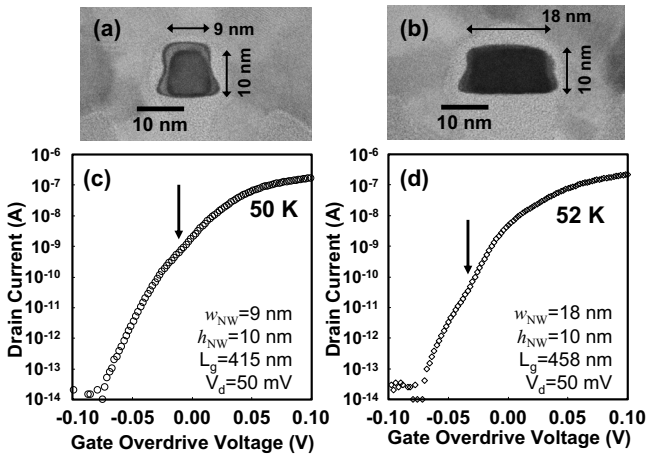

FIG. 1. Cross-sectional scanning transmission electron micrographs of the channels of SiNW FET with (a) w_{NW} of 9 nm and h_{NW} of 10 nm and (b) w_{NW} of 18 nm and h_{NW} of 10 nm. Transfer characteristics of SiNW *n*FETs with (c) w_{NW} of 9 nm and h_{NW} of 10 nm and (d) w_{NW} of 18 nm and h_{NW} of 10 nm are also shown. Kinks are indicated by arrows.

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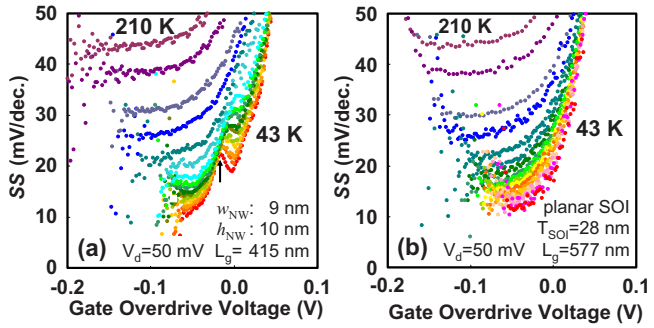

FIG. 2. (Color online) Subthreshold slopes of (a) SiNW *n*FETs with w_{NW} of 9 nm, and (b) planar-type SOI *n*FET as a function of the gate overdrive voltages measured at temperatures from 43 to 210 K.

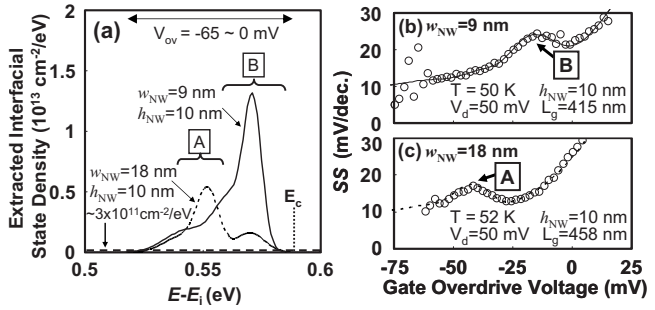

FIG. 3. (a) Interfacial state density of the SiNW *n*FETs with w_{NW} of 9 nm (solid line) and 18 nm (dotted line) as a function of the energy levels in the band gap of the SiNW channels. Dashed line indicates constant interfacial state density in all energy levels. Subthreshold slopes of the SiNW *n*FETs with w_{NW} of (b) 9 nm and (c) 18 nm obtained by experiments (open circle) and calculations (solid and dotted lines).

at each temperature of SiNW *n*FETs with w_{NW} of 9 and 18 nm showed linear relationship on measurement temperatures from 86 to 290 K in Eq. (1) with a slope of 2.0×10^{-4} V/K and 2.1×10^{-4} V/K, which corresponds to constant D_{it} of 2.9×10^{11} cm^{-2}/eV and 2.7×10^{11} cm^{-2}/eV, respectively. Moreover, at the measurement temperatures below 74 K, kinks in transfer characteristics become predominant as shown in Figs. 1(c) and 1(d). Note that this feature was not observed for the planar-type SOI *n*FET (not shown). *SS* of SiNW *n*FET with w_{NW} of 9 nm and planar SOI *n*FET were shown in Fig. 2. Based on Eq. (1), the kinks in the subthreshold slopes of the SiNW FET in Fig. 2(a) can be attributed to the increase in C_{it} (φ_s), which indicate localized interfacial states in the forbidden band gap of the SiNW channel. Therefore, a slight increase in the V_g may fill the local D_{it} with electrons (Q_{it}) to weaken the control of φ_s, which causes the kink in the subthreshold slope. The kink appeared at higher gate overdrive voltage (V_{ov}) as the measurement temperature increased. This is because larger increase in gate voltage is necessary to increase φ_s in strong inversion condition than in depletion and weak inversion conditions.

To extract the energy distribution of the interfacial states D_{it} (E), subthreshold slopes were calculated assuming an arbitrary D_{it} profile and compared with the obtained experimental data. A compact MOSFET model, Hiroshima-university STARC IGFET Model,[10,11] was used for *SS* calculation. Interfacial state density distribution was expressed as a sum of the Gaussian functions in Eq. (2);

$$D_{it}(E) = D_{it,\mathrm{peak}} \exp\left(\frac{E - E_{it}}{2\sigma^2}\right) \tag{2}$$

$$Q_{it}(\phi_s) = q\int D_{it}(E)F(E,T,\phi_s)dE, \tag{3}$$

where E is the energy level in the silicon band gap, F (E,T,φ_s) is the Fermi–Dirac distribution function, $D_{it,peak}$ is the maximum of the interfacial state density distribution, σ is the variance of the Gaussian function, E_{it} is the center of localized interfacial state distribution. C_{ox} was extracted by split-CV method applied to a multichannel SiNW *n*FETs, so that 1.64 μF/cm^2 and 1.28 μF/cm^2 were extracted for 9×10 nm^2 and 18×10 nm^2 SiNW *n*FETs, respectively. The extracted D_{it} (E) is shown in Fig. 3(a). One can observe two distinct peaks in the profile; a component *A* with a peak interfacial state density of 1.3×10^{13} cm^{-2}/eV below 10 meV of E_c, and a component *B* with a peak interfacial state density of 5.4×10^{12} cm^{-2}/eV below 31 meV of E_c. The constant D_{it} obtained from the minimum *SS* measured at temperatures from 86 to 290 K are also shown in Fig. 3(a). These values are relatively small compared with the extracted D_{it}. The calculated *SS* explains well the measured *SS* as shown in Figs. 3(b) and 3(c). A schematic band diagram for probing of the additional D_{it} (E) is shown in Fig. 4(a). While decreasing w_{NW} from 18 to 9 nm, the component *B* increased. On the other hand, the component *A* was larger with larger channel width. These results suggest that the component *B* is related to D_{it} along the side surfaces including the upper and lower corners, and that the component *A* is related to D_{it} at the top surface as well as the bottom BOX-nanowire interface as shown in Fig. 4(b), in which the coupling effect on the fully depleted SiNW *n*FET was considered.[12] Note that no kink was observed with planar SOI *n*FET as shown in Fig. 2(b), indicating the specific D_{it} distribution at the side surfaces or at the corners that have curved surface of the SiNW channel. There might be a concern that the surface potential fluctuation affected subthreshold slopes of MOSFET,[13] which might introduce an error in the extracted D_{it} distribution. Another concern might be that the components *A* and *B* affected mutually because of the coupling effects.[12]

It has been reported using the electron spin resonance that the trivalent silicon defect at silicon and silicon dioxide interface, which is called P_b center, is the origin of the interfacial states.[14,15] Energy-resolved deep level transient spectroscopy is another evaluation method of interfacial states.[16] Two kinds of P_b center, P_{b0} and P_{b1} have been proposed, and

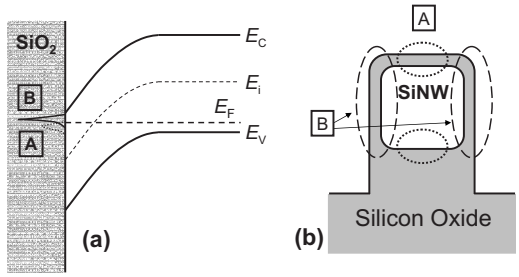

FIG. 4. (a) A schematic band diagram for probing of the localized interfacial states with components *A* and *B*. (b) A schematic illustration for the relationship between the components of the additional interfacial states and the locations.

the energy levels of P_b centers have been investigated by many authors. However, the peak energy levels of the interfacial state density distribution in Fig. 3(a) are not consistent with the peak energy levels of P_{b0} and P_{b1} on (100),[16–20,23] (110),[21,23] and (111)-oriented[16,17,21–23] silicon/silicon dioxide interfaces. These facts indicate that the interfacial states of the SiNW *n*FETs are physically different from those P_{b0} and P_{b1} on (100), (110), and (111)-oriented surfaces.

It has also been reported that stress was induced around the corners of the SiNW channel during gate thermal oxidation processes because of the volume expansion of silicon dioxide.[24,25] Ngai and White[26] reported that the energy level of the interfacial defect changed as the distance between silicon atoms changed. One possible explanation to the interfacial states near the conduction band edge of the SiNW channel is that energy levels of the interfacial states (P_b centers) split due to the distortion of the bond distances induced by the stress around corners during the thermal oxidation process.

Another possible reason might be the additional energy states due to the interstitial silicon atoms[27] in the channel, as interstitial silicon atoms can be injected from the oxidation front into silicon beam structure during the thermal oxidation process.[28] The model suggests that interstitial silicon atoms near the oxide/channel interface injected by sacrificial oxidation and following gate oxidation processes, which generated energy states near conduction band edge that evaluated in this letter.

In summary, we reported the existence of the additional interfacial states of SiNW *n*FETs with rectangular-like cross-sections (wire height of 10 nm and wire width of 9 and 18 nm) from the transfer characteristics in the subthreshold region measured at cryogenic temperatures, where kinks in the drain current becomes prominent. It is found that the kinks can be well-explained assuming local interfacial states near the E_c. The main extracted local states have been shown to exist at 10 and 31 meV below the E_c with the densities of 1.3×10^{13} cm^{-2}/eV and 5.4×10^{12} cm^{-2}/eV, respectively. By comparing two FETs with different wire widths, the former states can be assigned to the states located at the corner and the side surface of the wire, and the latter to the top and the bottom surfaces.

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