Ballistic/Quasi-Ballistic Transport in Nanoscale Transistor

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Abstract

The current voltage characteristics of the silicon ballistic MOSFETs are introduced and discussed. They are derived by considering the current capacity through the bottleneck point in the channel, and they provide a simple measure of the performance limit. The performance of experimental nanoscale bulk MOSFETs are compared with the ideal ballistic limit. It was shown that the performance degradation due to carrier scattering amounts to several to several tens percent in recent nanoscale MOSFETs. Quasi-ballistic transport in MOSFETs was also analyzed by a simple approach based on the transmission viewpoint. Channel-length reduction was found to yield consistent improvement of the ballisticity. Considerable performance degradation, however, was still found to persist even in 10-nm MOSFETs. The role of each carrier scattering mechanism is analyzed. It is shown that elastic scattering degrades the performance, but the inelastic energy relaxation improves the performance of the MOSFET.

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Keywords: Ballistic MOS; Quasi-Ballistic MOS; Nanoscale MOS

1. Introduction

In line with the device-scaling trend, deca-nanometer MOSFETs are already on real LSIs and further downsizing to the nanoscale dimension will likely be achieved within the near future. Since the mean free path of a carrier in the device is estimated to be in the 10-nm range, the probability of a carrier encountering scattering events within the channel rapidly diminishes as downsizing is intensified. The transport of a carrier in the device is closely related to the relative dimension of the device to the mean free path of the carrier, as illustrated in Fig. 1. When the device size L is sufficiently larger than the mean free path λ, the carrier flow is controlled by the diffusive transport and is well-characterized by the conventional mobility theory. In contrast, if L is sufficiently smaller than λ and the scattering probability in the channel is negligibly small, it is the ballistic transport and the device current is completely controlled by the carrier injection from source into the channel. The nanoscale transistors recently fabricated and investigated are in the range where L is comparable to λ, and are characterized by the quasi-ballistic transport. Carriers encounter a limited amount of scattering from source and drain. The mobility theory no longer describes the transport on the one hand, and the presence of scattering distinguishes their behavior from ideal ballistic characteristics. A better approach to these devices is first establishing the ballistic characteristics and then introducing a limited number of scattering events in the carrier transport.

This paper introduces the theory of ballistic MOSFET, and discusses some aspects of the physics of ballistic and quasi-ballistic transport as well as comparison to experimental devices. In section 2, the theory and characteristics of the silicon ballistic MOSFET are introduced. Section3 is devoted to a discussion of physics of the quasi-ballistic transport in MOSFETs. Section 4 provides a summary.

2. Ballistic MOSFETs

Analysis of ballistic transistors[1-4] is not intended to allow for accurate prediction of actual device characteristics. A ballistic transistor is an ideal device that can never be achieved. However, it is ranked as the scaling limit of MOSFETs, and the device characteristics are comparatively easily estimated. The merits of studying the characteristics are threefold. We can discuss the performance limit of MOSFETs by

means of a simple theory. Actual devices, carefully fabricated so as to approach the limit, show performance close to the ideal limit. Therefore, the second merit is that by comparing the observed characteristics of a fabricated device to the ideal ones, one can determine how close the contemporary technology is to reaching the ideal limit. And the final merit is that one can obtain insight into the precise mechanism of the nanoscale device operation.

2.1 Current voltage characteristics

The *I-V* characteristics of a ballistic transistor are derived by Landauer's formula[5]. According to the hypothesis, the source and the drain are assumed to be ideal reservoirs, respectively injecting sufficient carriers into the channel, and backscattering no carriers into the channel. No backscattering within the channel is assumed. The potential profile in the channel generally has a maximum point near or at the source edge of the channel. The maximum constitutes the bottleneck of current flow through the channel. Therefore, the carriers injected from the source populate only within the positive velocity states at the bottleneck point, and constitute the current flow from source to drain. A similar contribution from the drain is also considered. The net current density of the device is given by the carrier flux injected from source to channel minus the flux injected from drain to channel, as we obtain[1,2],

$$I_D = \frac{\sqrt{2}q(kT)^{3/2}}{\pi^2\hbar^2}\sum_{valley}\sum_{n}\sqrt{m_y}\left[F_{1/2}\left(\frac{\phi_{FS}-E_n}{kT}\right)-F_{1/2}\left(\frac{\phi_{FS}-E_n-qV_D}{kT}\right)\right], \quad (1)$$

The carrier charge Q at the bottleneck is

$$|Q| = C(V_G - V_t) = \frac{qkT}{2\pi\hbar^2}\sum_{valley}\sum_{n}\sqrt{m_x m_y}\,\ln\left\{\left[1+\exp\left(\frac{\phi_{FS}-E_n}{kT}\right)\right]\left[1+\exp\left(\frac{\phi_{FS}-E_n-qV_D}{kT}\right)\right]\right\} \quad (2).$$

Here, E_n is the n-th quantum energy level of the inversion layer at the bottleneck, and ϕ_{FS} is the Fermi potential of the source. $F_{1/2}(x)$ is the Fermi Dirac integral of the 1/2 order (Sommerfeld's definition[6]). The summation is over the six silicon valleys and also over the quantum level n in each valley. First, ϕ_{FS} is evaluated by Eq. (2), and the substitution of the value in Eq. (1) then provides the current density I_D. Note

that the device current is independent of the channel length. The current in Eq. (1) is a difference of two terms; the positive term representing the current flowing from source to drain, and the negative term that depends on V_D and represents the flow from drain to source. As V_D increases, the magnitude of the negative component diminishes to eventually become negligible, leading to current saturation. The short channel effect is not explicitly considered. But the drain-induced barrier lowering (DIBL) is implicitly considered by renormalizing the threshold voltage V_t in accordance with the V_t lowering of the actual device.

2.2 Performance limit of MOSFETs

The FET current in the ballistic limit implies the high performance limit of the device in a given structure because the carrier velocity degradation due to scattering is neglected [7]. Figure 2 shows the current density given by Eqs. (1) and (2), and shows the performance limit of MOSFETs as a function of the inversion carrier density. The curve denoted by MSM corresponds to results where multiple subbands of the inversion layer are considered. EOSA stands for the effective one-subband approximation where only the lowest subband is considered, and presents an overestimation. The FET current is a complicated function of various parameters, but the performance limit is reduced to a single curve when described by the inversion carrier density.

The current is factorized into a product of the carrier density, which is primarily controlled by the MOS capacitance, and of the carrier velocity, which is yielded by the transport of carriers. The ballistic conduction free of scattering influences the carrier velocity, and the velocity is directly coupled to the performance limit. In current saturation of a ballistic MOSFET, all carriers injected from the source over the bottleneck potential are running toward the drain. There is no backward flow at the bottleneck. The mean velocity of carriers at the bottleneck point is called the injection velocity, and is hereafter designated by v_{inj}. The value is independent of the drain voltage if the DIBL is neglected, and represents the magnitude of ballistic current in the channel. In actuality, the saturated current is expressed for large V_D as

$$I_{D\,sat} = WC_{ox}(V_G - V_t)v_{inj} \qquad (3)$$

In a weak inversion, v_{inj} is approximately constant and has a value of 1.2×10^7cm/s. This corresponds to the

thermal velocity of the inversion electron and increases as the temperature is raised. In a strong inversion, v_{inj} increases as the carrier density increases due to the carrier degeneracy. As the carrier density is increased, the Pauli principle forces carriers to populate higher energy levels and the increase in kinetic energy leads to an increase in the mean velocity. Notice that the injection velocity is close to the saturation velocity, ~10^7cm/s.

2.3 Comparison with experimental devices

In experimental devices, what performance level can be achieved compared to the ballistic limit? In 1988, IBM for the first time disclosed the *I-V* characteristics of a sub-100 nm MOSFET[8]. The sample was carefully fabricated and measured so as to attain the best possible performance. Figure. 3 shows a comparison of the data, measured at 77K, with the ballistic MOSFET characteristics [8,9]. Good agreement was obtained for the low-gate bias region, and the agreement is also satisfactory in the high-gate bias region when the drain bias is large. The experimental values are reproduced without depending on the mobility. It is rather surprising that such a simple theory shows good agreement despite the complicated structure of the experimental sample.

For comparison of the experimental performance to the ideal performance of the ballistic limit, it is convenient to use the following index *b* that represents the ballisticity of the experimental device.

$$b = I_{D sat exp} / I_{D sat bal} \qquad (4)$$

As for nanoscale devices, some bulk examples fabricated with the sophisticated technology and measured at room temperature are shown in Table 1. The index of ballisticity *b* is distributed between 0.2 and 0.7, well below the ballistic limit [10-13]. Notice that the smaller device shows a worse value of index *b*.

One can find another ballistic nanoscale transistor in carbon nanotube FETs[14].

3. Quasi-Ballistic MOSFETs

The presence of a small number of scatterings basically characterizes the device operation in quasi-ballistic transport and distinguishes it from that in the ballistic transport. An analysis of the

quasi-ballistic MOSFET based on the reflection-transmission probabilities of scattering is performed[15], and a novel viewpoint on mutually competing roles of the elastic scattering and the energy relaxation(ER) due to optical phonon emission(OPE) is proposed. The present approach is less accurate but simpler than the complicated Monte Carlo simulation, and provides a clear-cut and cogent view on the physics of transport. Figure 4 illustrates some characteristic aspects of transport in nanoscale silicon MOSFETs. (1) Carriers are injected from source to channel with the kinetic energy of the order of thermal energy *kT*. (2) Carriers suffer elastic and inelastic scatterings in the course from source to drain. Some are back-scattered and some transmitted. (3) Some suffer ER primarily due to optical phonon emission /absorption. At room temperature, the emission probability is far larger than the absorption probability. The dominant process is the energy loss, and those that have lost a few multiples of *kT* by OPE (63meV for silicon) have little chance to recover the energy to return to the source, and are eventually absorbed into the drain. (4) The steady state current I_D [16] which consists of the flux injected to channel minus the back-scattered flux to source, as well as the ballisticity *b* are given as,

$$I_D = WC_{ox}(V_G - V_t)v_{inj}\left(\frac{1-R}{1+R}\right) \qquad (5)$$

$$b = \left(\frac{1-R}{1+R}\right) \qquad (6)$$

where v_{inj} is the carrier injection velocity from source to channel, and *R* is the backscattering coefficient at the bottleneck point. Here, the mean velocity of the backscattered flux is also assumed to be equal to v_{inj} at the bottleneck for simplicity[2]. We examine the transport of carrier flux at the fixed energy level above the potential maximum at bottleneck by thermal energy *kT* and evaluate the value of *R*. Suppose that an infinitesimal region around a point in the channel shows the one-dimensional transmission coefficient *t* and the reflection coefficient *r* for elastic scattering of carriers(Fig. 5). The residual (1-*t*-*r*), which is not zero if carriers suffer ER primarily due to OPE, gives the ER probability. We can construct a four terminal expression for a thin slab region connecting the incoming and outgoing fluxes *F1* and *F2* on the source side of the region, and those fluxes *F4* and *F3* on the drain side. We call the connecting matrix the R-T matrix. Successively multiplying all R-T matrices of the component slab region in the cannel, we obtain the R-T

matrix connecting the carrier flux from the source and that from the drain. The values of *t* and *r* at each point in the channel are computed from the elastic scattering probability and the OPE probability, respectively given in terms of the energy-dependent mean free path λ and the μ at that point. As for the elastic scattering mechanism, the impurity scattering, the phonon scattering, and the interface roughness scattering are considered at room temperature[17-19]. Actually, the MOSFET region is divided into three parts: the region close to the bottleneck, the residual part within the channel, and the drain region itself, and representative values of λ and μ in each region are allocated. By considering the drain as an independent region, the carrier feedback from scatterings within the drain can be taken into account. The back-scattering coefficient *R* is obtained as the back-scattered flux from channel to source for the unity injected flux from source to channel. Other transport coefficients are similarly obtained. Figure 6 is an obtained result showing the channel length *L* dependence of transport in the nanoscale MOSFET. In addition to *R* and *b*, *Te* shows how large a portion of the injected flux from the source reaches the drain without ER, and *Rb* shows how large a portion of the injected flux rebounds from the drain to the channel due to scattering inside the drain. As the channel length gets shorter, *R* decreases and *b* increases, but even at *L*=5 nm, *b* is still around 0.75. The accomplishment of ballistic transport at room temperature seems difficult due to elastic backscattering close to the source edge. For longer *L*, the *Te* value is small, showing that most carriers are subject to ER inside the channel. But at a short channel of *L*~10nm, *Te* is large indicating that most carriers survive ER and reach the drain. The figure suggests a comparatively low *R* even if *L* is increased. This is because the backscattering efficiency is dependent on tradeoff between the elastic scattering and the ER in the region near the source edge in the channel. In the back part of a long channel, ER prevails suppressing the back-transfer of carriers, as the curve of *Te* implies. The value of *Rb* increases up to 10% of the originally injected carrier in ultra-short channel devices. This result suggests that the increase in *Te* in short channel devices causes an increase in the rebounding flux from the drain. If *L* is short and the ballistic transport prevails in the channel, most of the rebounding flux reaches the source. This process may constitute a serious degradation mechanism of ballistic transport in ultra-short channel MOSFETs.

Our analysis distinguishes the elastic backscattering and ER due to OPE. We can analyze each role of these processes in quasi-ballistic transport. First, we examine the case where the value of mean free path λ

due to elastic scattering is uniformly varied from 5 nm to 100 nm, while the probability of ER by OPE is kept constant at a set of values in Fig. 6. The λ-dependence of *R* and *b* is depicted in Fig. 7(a). As λ is reduced, the backscattering coefficient *R* increases and ballisticity *b* is decreased, as is expected. Next, we examine the case where the probability of elastic scattering is kept constant at the values in Fig. 6, and the uniform value of the mean free path μ is varied. Similar characteristics are depicted in Fig. 7(b). In this case, *R* decreases and *b* increases when μ is reduced. The channel length is 20 nm in each case. It is evident that the elastic backscattering degrades the transport efficiency, and that the ER due to OPE improves the transport efficiency on the contrary. The curve of "energy relaxation rate" in the figure indicates how large a portion out of the original injected flux is subject to ER within the channel. It shows strong dependence on the value of μ.

4. Summary

The *I-V* characteristics of a ballistic silicon MOSFET are introduced. These characteristics indicate the high performance limit of the device. A comparison between the real nanoscale MOSFET performance and the ideal ballistic limit is discussed. Characteristics of the quasi-ballistic MOSFET are discussed by a simple analysis based on the transmission viewpoint. It is shown that the elastic scattering degrades the device performance, but that the inelastic ER improves it by increasing the carrier transmission.

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Figure Captions

Fig. 1. Carrier transport in MOSFETs depends on relative dimension of the device size and the mean free path.

Fig. 2. The saturated current of the ballistic MOSFET showing the high performance limit of the silicon MOSFET at room temperature.

Fig. 3. The experimental bulk *n*MOSFET (70 nm MOSFET at 77 K by Sai-Halasz et al. [8]) characteristics are compared with the ideal ballistic MOSFET characteristics.

Fig. 4. Schematics of the potential profile and the carrier scatterings within the MOSFET

Fig. 5. R-T matrix formalism of the transport based on the reflection-transmission viewpoint

Fig. 6. Transport characteristics of nanoscale MOSFETs as a function of channel length.

Fig. 7. Variation of ballistic transport when the mean free path of each scattering mechanism is separately altered. (a) The elastic mean free path λ is altered, while the probability of ER is kept constant. (b) The mean free path μ for ER due to OPE is altered, while the elastic scattering probability is kept constant.

Table 1. Index of ballisticity for fabricated bulk devices.

Author	Wakabayashi [10]	Timp [11]	Chau [12]	Yu[13]
IEDM Year	00	99	00	01
L (nm)	24	40	30	15
I_D/W (mA/μm)	0.796	1.3	0.514	0.615
Tox (nm) (EOT)	2.5	1.3	1.9 μF/cm	0.8
b	0.45	0.69	0.42	0.24

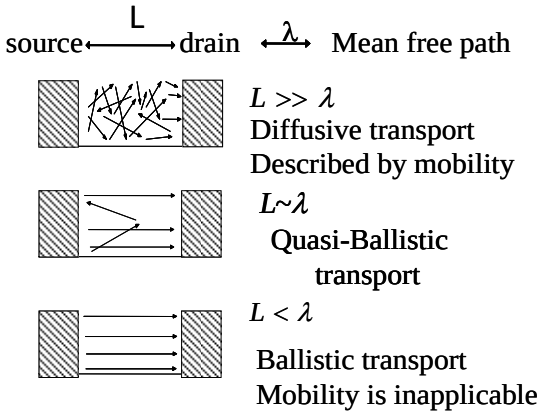
L
source
drain
λ
Mean free path
L >> λ
Diffusive transport
Described by mobility
L~λ
Quasi-Ballistic
transport
L < λ
Ballistic transport
Mobility is inapplicable

Fig. 1.

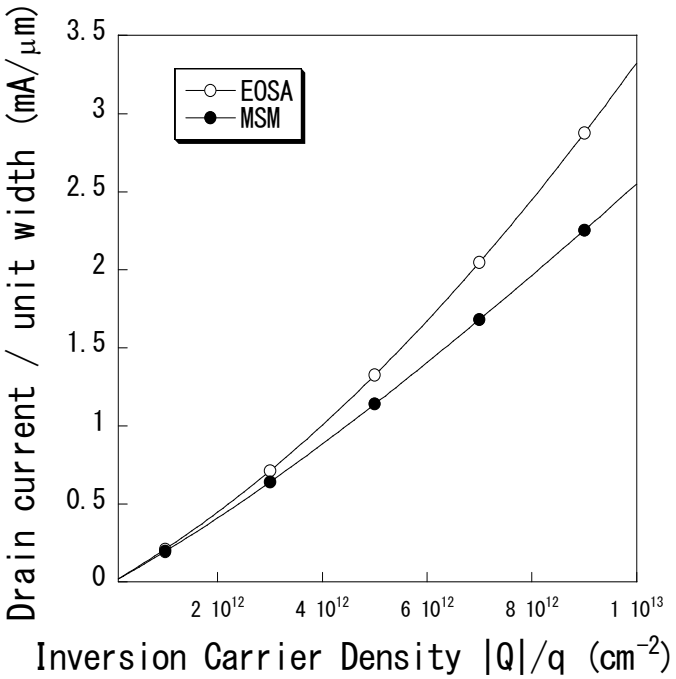
Drain current / unit width (mA/μm)
3.5
3
2.5
2
1.5
1
0.5
0
EOSA
MSM
2 10^12
4 10^12
6 10^12
8 10^12
1 10^13
Inversion Carrier Density |Q|/q (cm^-2)

Fig. 2

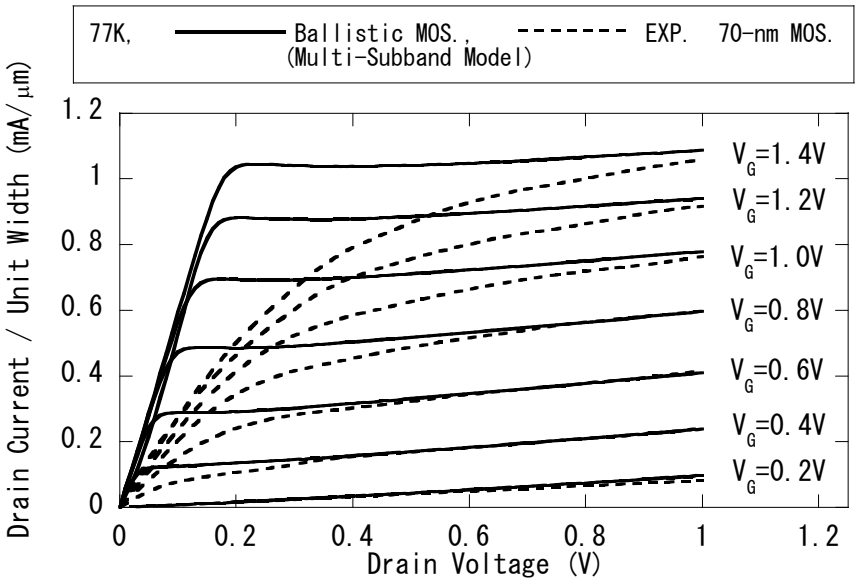
77K,
Ballistic MOS.,
(Multi-Subband Model)
EXP. 70-nm MOS.
Drain Current / Unit Width (mA/μm)
Drain Voltage (V)
V_G=1.4V
V_G=1.2V
V_G=1.0V
V_G=0.8V
V_G=0.6V
V_G=0.4V
V_G=0.2V
0
0.2
0.4
0.6
0.8
1
1.2

Fig. 3

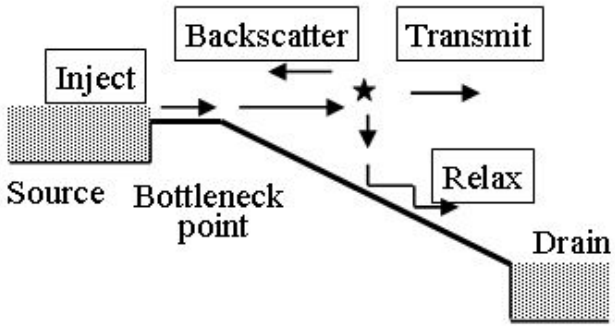
Backscatter
Transmit
Inject
Relax
Source
Bottleneck
point
Drain

Fig. 4

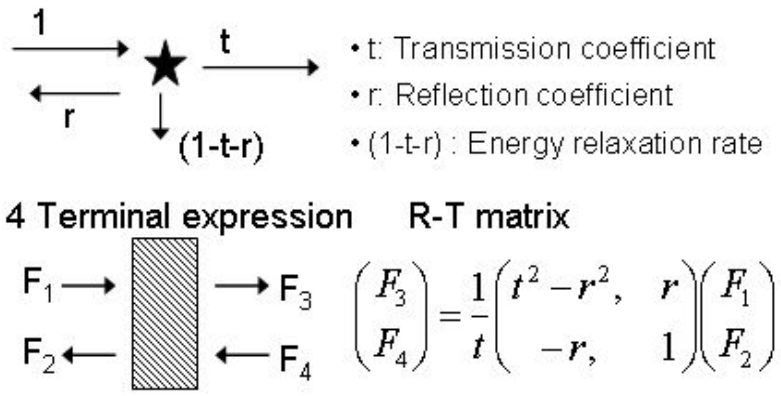
1
t
r
(1-t-r)
• t: Transmission coefficient
• r: Reflection coefficient
• (1-t-r) : Energy relaxation rate
4 Terminal expression
R-T matrix
F1
F2
F3
F4
$\begin{pmatrix} F_3 \\ F_4 \end{pmatrix} = \frac{1}{t}\begin{pmatrix} t^2 - r^2, & r \\ -r, & 1 \end{pmatrix}\begin{pmatrix} F_1 \\ F_2 \end{pmatrix}$

Fig. 5

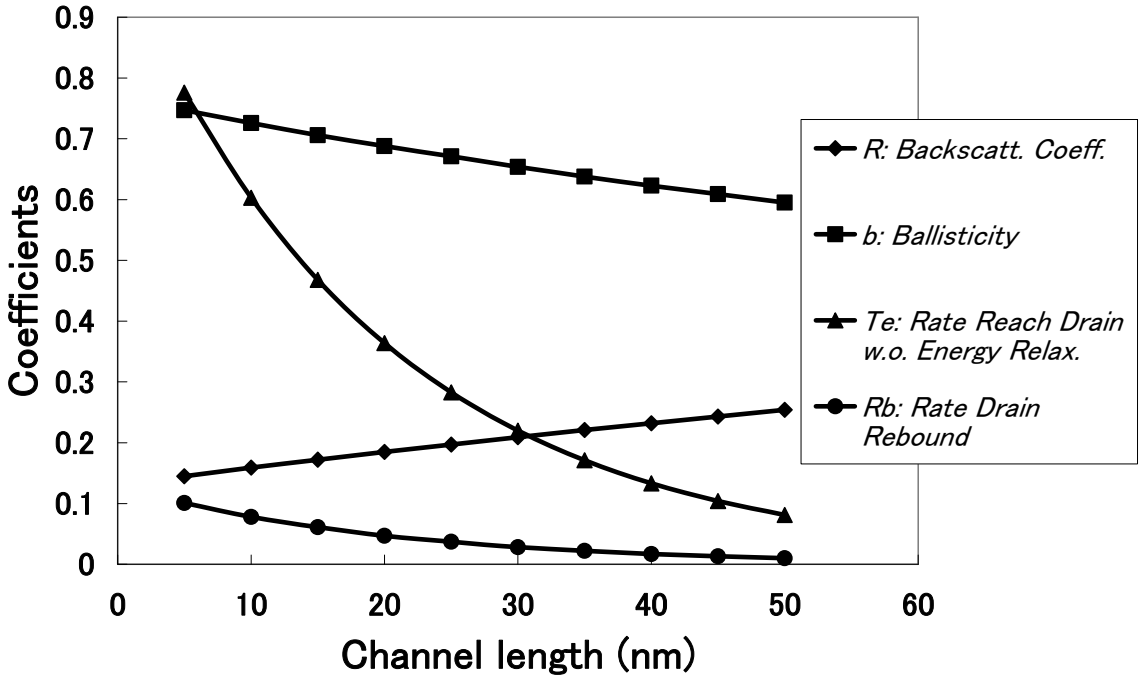
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Coefficients
0
10
20
30
40
50
60
Channel length (nm)
R: Backscatt. Coeff.
b: Ballisticity
Te: Rate Reach Drain w.o. Energy Relax.
Rb: Rate Drain Rebound

Fig. 6

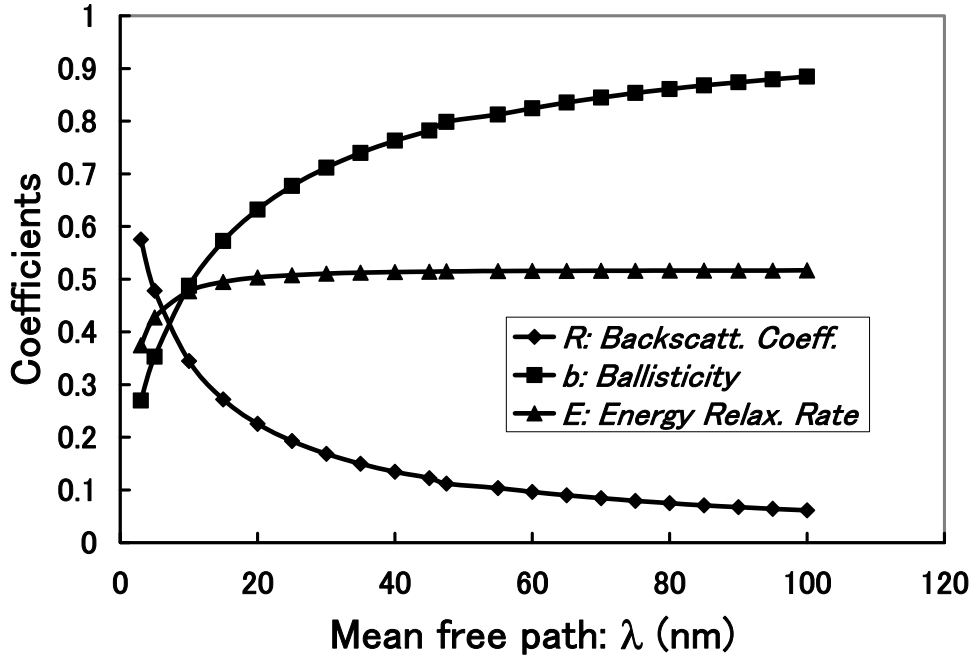
Coefficients
Mean free path: λ (nm)
R: Backscatt. Coeff.
b: Ballisticity
E: Energy Relax. Rate
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
20
40
60
80
100
120

Fig. 7(a)

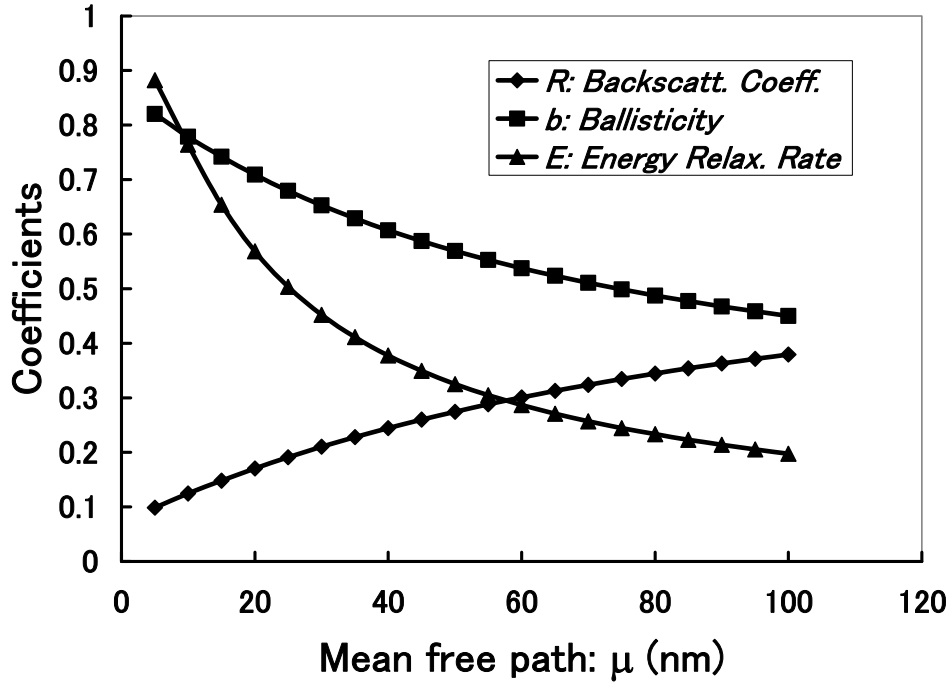
R: Backscatt. Coeff.
b: Ballisticity
E: Energy Relax. Rate
Coefficients
Mean free path: μ (nm)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
20
40
60
80
100
120

Fig. 7(b)